5-Port Gigabit Ethernet Switch with Embedded Memory

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Features

- 5-port Gigabit Ethernet switch integrating MACs, packet buffer memory and switching engine with RGMII/GMII/MII interface
- RGMII support REV 1.3 with 3.3V IO
- Full Duplex 1000 Mbit/s.
- Full and Half Duplex 10/100 Mbit/s
- Supports auto-sensing or manual selection for speed and duplex capability with an embedded MPU
- Store-and-forward operation support
- Performs full wire-speed switching with Head of Line (HOL) blocking prevention
- Supports up to 8 Port-based VLAN Groups
- Supports broadcast storm filtering.
- Quality-of-Service provisioning on 802.1P tag and port-pairs with two priority queues
- By-port Egress/Ingress bandwidth (rate) control
- Embedded 128K Byte SRAM for packet buffer
- Supports packet length up to 1522 bytes
- Supports 9K/12K byte JUBMO packet
- Integrated two-way Address-Lookup engine and table for 4K MAC addresses
- Programmable aging mechanism for the two-way 4K MAC addresses table
- Two hashing schemes: direct and XOR mode.
- Support ingress port security mode, incoming packets with unknown source MAC address could be dropped
- Egress/Ingress Port Mirroring for Sniffer function.
- Flow control
  - Full-duplex IEEE 802.3x flow control
  - Half-duplex back pressure flow control
  - Optional smart flow control for mix-speed connection
- Supports port-based trunking for high-bandwidth links
- Provides 5 GPIO ports
- Provides EEPROM interface for auto-configuration
- System clock input is one 25MHz Crystal and one 125MHz from PHY GCLK output
- 1.8 and 3.3V operations
- 3.3 I/Os and packaged in 272-pin BGA

Product Description

The AX88655AB is an 5-port 10/100/1000 Mbps Ethernet switch with, GMII/RGMII or MII Interface. The switch controller provides network system manufacturers the ideal platform for building smart and cost-effective backbone switches for small to medium sized businesses.

The AX88655AB 5-port 10/100/100 BASE-T single chip switch controllers combine the benefits of network simplicity, flexibility and high integration. Its highly integrated feature set enables network system manufacturers to build smart switches for the fast-growing small to medium business market segment.

Benefits of AX88655AB Switches are below.

- Simplicity
  Provides a smart, simple and low maintenance plug-and-play network interconnect system for small to medium size businesses
- Flexibility
  Highly scalable configuration allows system manufacturers to enable or disable a range of features to best meet their target price point.
- Integration
  Highly integrated design drives down overall switch manufacturing costs.

Target Applications

- ✓ 5-port Gigabit Layer 2 Switches for workgroup
- ✓ High-port count Layer 2 switches with trunking
- ✓ High performance solution of Ethernet backbone

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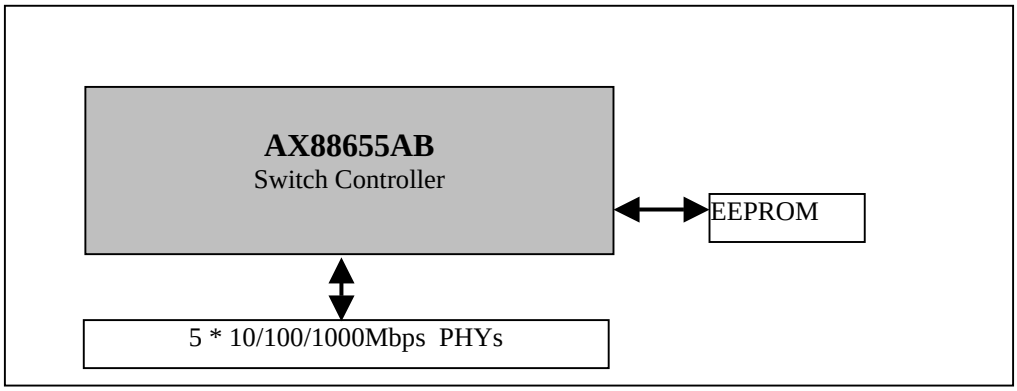
First Released Date: 11/07/2002

System Block Diagram



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FIGURES

1.0 AX88655AB Overview

1.1 General Description

The AX88655AB Gigabit switch controller supports eight 10/100/1000 Mbps ports in wire-speed operation. The AX88655AB Gigabit switch controller provides eight 10/100/1000 Ethernet ports with RGMII/GMII/MII interface. For each ports, the AX88655AB supports GMII/RGMII (802.3ab, 1000BASE-T) interface with full-duplex operation at Gigabit speed, full- or half-duplex operation at 10/100 Mbps speed (using 802.3/u, 10/100BASE-T) and polls the status of PHYs with an embedded MPU.

The device supports 4K internal MAC addresses which are shared by all ports with an embedded SRAM. The learning/routing engine is implemented with a two-way hash/linear algorithm to reduce possibility of routing collision.

Basically the AX88655AB supports non-blocking wire speed forwarding rate and no Head-of-Line (HOL) blocking issue. The AX88655AB provides two flow-control mechanisms to avoid loss of data: an optional jamming based backpressure flow control in the half-duplex operation and IEEE 802.3x in the full-duplex mode.

To support Quality of Service (QoS), each output port has two priority queues and their assignment can be based on the 802.1p priority field or Port-Pair setting. Each output port retrieves the frames from the shared buffer based on queuing and sends them to the transmitting (Tx) FIFO.

1.2 AX88655AB Block Diagram

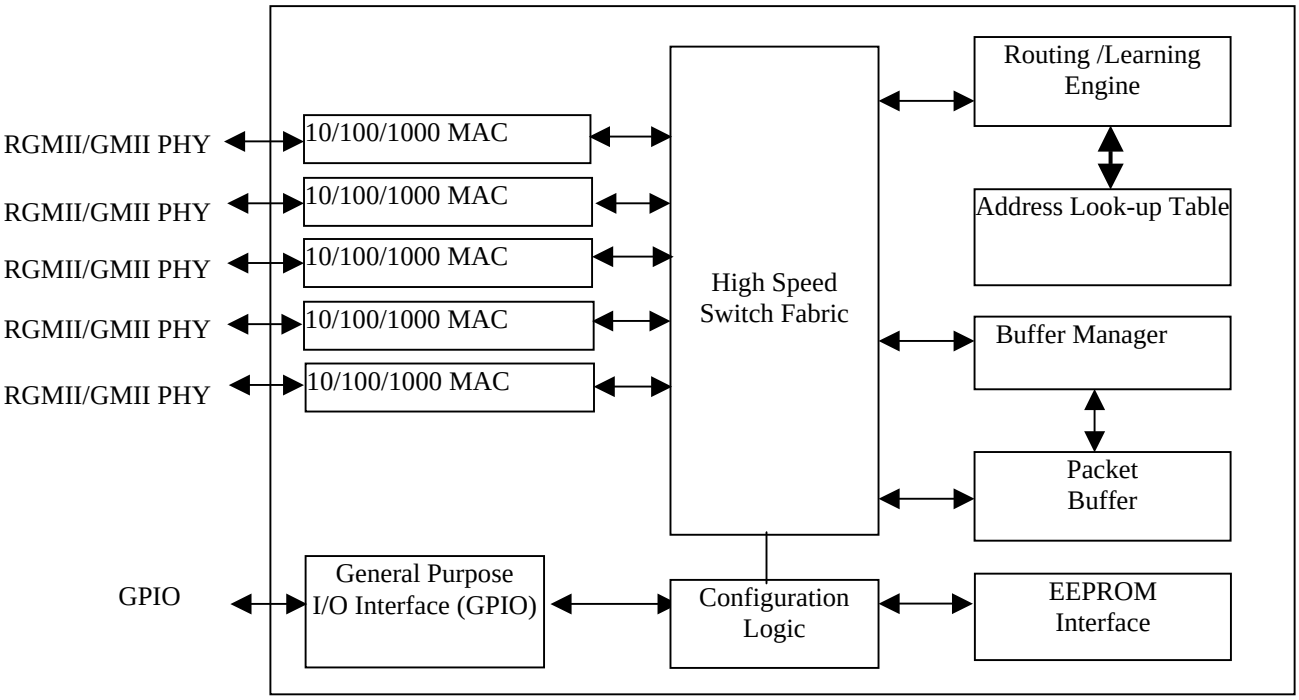


Fig-1 AX88655AB Block Diagram

1.3 Pin Connection Diagram

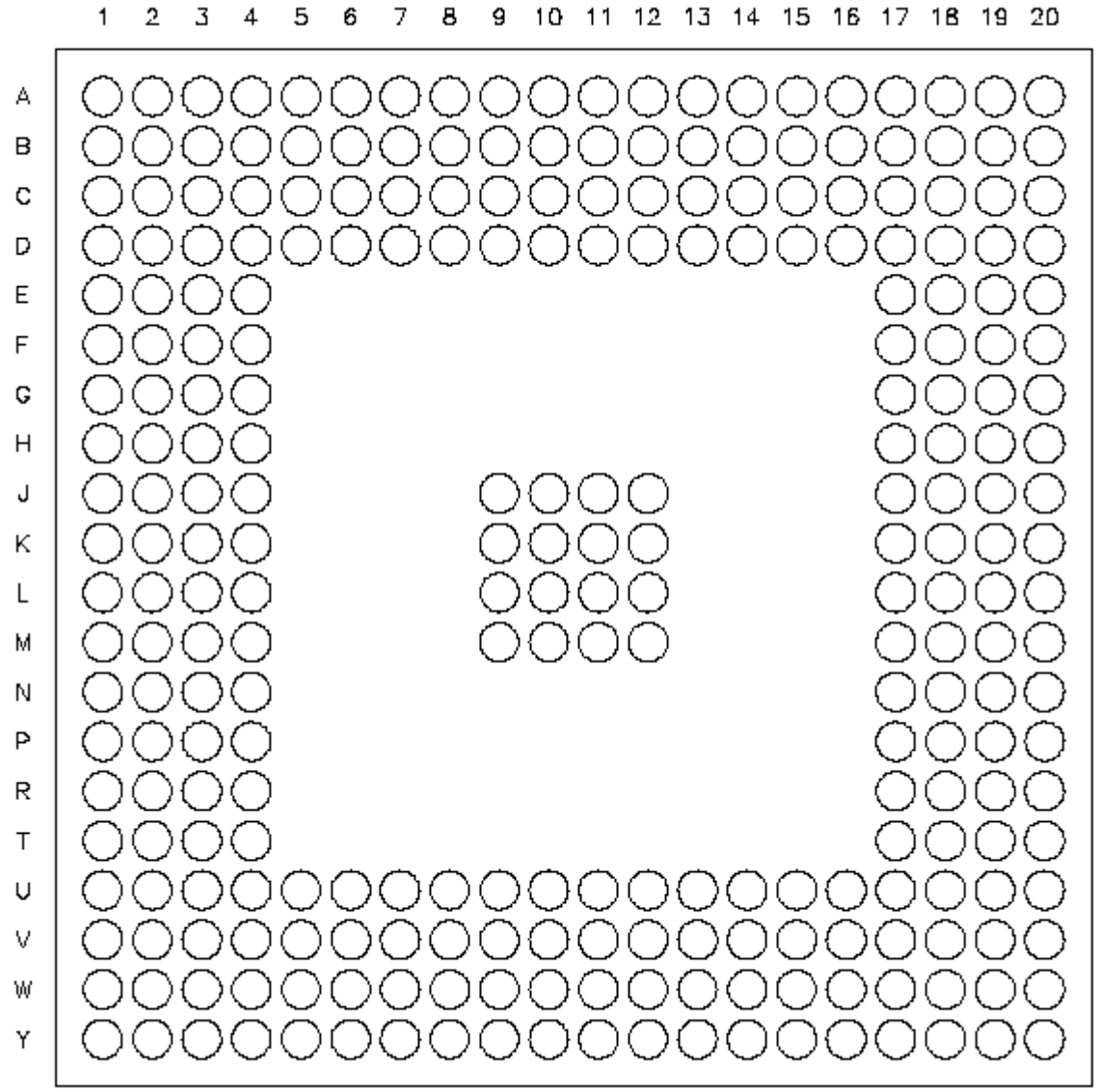


Fig-2 Top View of AX88655ABB Pin Diagram

2.0 I/O Definition

The following terms describe the AX88655AB pin-out:
All pin names with the "/" suffix are asserted low.
The following abbreviations are used in following Tables.

I	**Input**	**PU**	**Pull Up**
O	**Output**	**PD**	**Pull Down**
I/O	**Input/Output**	**P**	**Power Pin**
OD	**Open Drain**		

2.1 RGMII/GMII/MII Interface

2.1.1 RGMII/GMII/MII Interface Port 0

Signal Name	I/O	Pin No.	Description
GTX_CLK0	O	Y2	**125MHz Clock Output:** it is a continuous 125 MHz clock output to giga-PHY operating at 1000BASE-T. That is, it is a timing reference for TX_EN0 and TXD0[7:0]
TX_EN0	O	Y1	**Transmit Enable:** When TX_EN0 is asserted, data on TXD0[7:0] are transmitted onto PHY. TX_EN0 is synchronous to GTX_CLK0 in 1000BASE-T mode and synchronous to TX_CLK0 in 10/100BASE-T mode.
TXD0[7:0]	O	W1, V2, V1, U3, U2,U1 , T2, T1	**Transmit Data:** Synchronous to the rising of GTX_CLK0 in 1000BASE-T mode. And synchronous to rising edge of TX_CLK0 in 10/100BASE-T mode., For RGMII, only TXD0[3:0]
TX_CLK0	I/PD	W5	**MII Transmit Clock Input:** TX_EN0 and TXD0[3:0] are synchronous to the rising edge of this clock in 10/100BASE-T mode.
COL0	I/PD	Y5	**Collision Detect:** Active high to indicate that there is collision occurred in half duplex mode. In full duplex mode COL0 is always low.
CRS0	I/PD	U6	**Carrier Sense:** Active high if there is carrier on medium. In half duplex mode CRS0 is also asserted during transmission and asynchronous to any clock.
RX_DV0	I	U5	**Receive Data Valid:** Active high to indicate that data presented on RXD0[7:0] is valid and synchronous to RX_CLK0.
RX_CLK0	I	V5	**Receive Clock Input:** 125, 25 and 2.5 MHz is running at 1000/100/10 BASE-T mode respectively. RX_DV0 and RXD0[7:0] are synchronous to rising edge of this clock.
RXD0[7:0]	I/PD	U4, V4, W4, Y4, V3, W3, Y3, W2	**Receive Data:** Data received by the PHY are presented on RXD0 and synchronous to RX_CLK0. RXD0[3:0] is valid in 10/100/1000BASE-T and RXD[7:4] is valid only in 1000BASE-T modes. For RGMII, only RXD0[3:0]

2.1.5 RGMII/GMII/MII Interface Port 1

Signal Name	I/O	Pin No.	Description
GTX_CLK1	O	G20	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN1	O	H17	**Transmit Enable:** Please references section 2.1.1.
TXD1[7:0]	O	H18, H19, H20, J18, J19, J20, K19, K20	**Transmit Data:** Please references section 2.1.1.
TX_CLK1	I/PD	E17	**MII Transmit Clock Input:** Please references section 2.1.1.

COL1	I/PD	D18	**Collision Detect:** Please references section 2.1.1.
CRS1	I/PD	D19	**Carrier Sense:** Please references section 2.1.1.
RX_DV1	I	E19	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK1	I	E18	**Receive Clock Input:** Please references section 2.1.1.
RXD1[7:0]	I/PD	E20, F17, F18, F19, F20, G17, G18, G19	**Receive Data:** Please references section 2.1.1.

2.1.6 RGMII/GMII/MII Interface Port 2

Signal Name	I/O	Pin No.	Description
GTX_CLK2	O	A18	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN2	O	B18	**Transmit Enable:** Please references section 2.1.1.
TXD2[7:0]	O	C18, B19, A19, A20, B20, C19, C20, D20	**Transmit Data:** Please references section 2.1.1.
TX_CLK2	I/PD	C15	**MII Transmit Clock Input:** Please references section 2.1.1.
COL2	I/PD	D15	**Collision Detect:** Please references section 2.1.1.
CRS2	I/PD	D14	**Carrier Sense:** Please references section 2.1.1.
RX_DV2	I	A15	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK2	I	B15	**Receive Clock Input:** Please references section 2.1.1.
RXD2[7:0]	I/PD	D16, C16, B16, A16, D17, C17, B17, A17	**Receive Data:** Please references section 2.1.1.

2.1.7 RGMII/GMII/MII Interface Port 3

Signal Name	I/O	Pin No.	Description
GTX_CLK3	O	A11	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN3	O	C12	**Transmit Enable:** Please references section 2.1.1.
TXD3[7:0]	O	B12, A12, C13, B13, A13, C14, B14, A14	**Transmit Data:** Please references section 2.1.1.
TX_CLK3	I/PD	D9	**MII Transmit Clock Input:** Please references section 2.1.1.
COL3	I/PD	C8	**Collision Detect:** Please references section 2.1.1.
CRS3	I/PD	D8	**Carrier Sense:** Please references section 2.1.1.
RX_DV3	I	B9	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK3	I	C9	**Receive Clock Input:** Please references section 2.1.1.
RXD3[7:0]	I/PD	A9, D10, C10, B10, A10, D11, C11, B11	**Receive Data:** Please references section 2.1.1.

2.1.8 RGMII/GMII/MII Interface Port 4

Signal Name	I/O	Pin No.	Description
GTX_CLK4	O	A5	**125MHz Clock Output:** Please references section 2.1.1.
TX_EN4	O	B5	**Transmit Enable:** Please references section 2.1.1.

TXD4[7:0]	O	C6, B6, A6, C7, B7, A7, B8, A8	**Transmit Data:** Please references section 2.1.1.
TX_CLK4	I/PD	B1	**MII Transmit Clock Input:** Please references section 2.1.1.
COL4	I/PD	C1	**Collision Detect:** Please references section 2.1.1.
CRS4	I/PD	C2	**Carrier Sense:** Please references section 2.1.1.
RX_DV4	I	B2	**Receive Data Valid:** Please references section 2.1.1.
RX_CLK4	I	A1	**Receive Clock Input:** Please references section 2.1.1.
RXD4[7:0]	I/PD	A2, B3, A3, C4, B4, A4, D5, C5	**Receive Data:** Please references section 2.1.1.

2.2 Miscellaneous

Signal Name	I/O	Pin No.	Description
NC		L1, L2, L3, M2, M3, M4, N1, N2, N3, P1, P2, P3, R1,R2, R3, R4 ,T3, T4, F4, F3, G2, E1, H3,G3, C3, G1,Y9,V8, W8, Y8, V7, W7, Y7, V6, W6, Y6,U11,V12,U12,W11,V11, Y11, U10, V10 W10, Y10 U9, V9, W9,Y15,U14, V14, W14, Y14, V13, W13,Y13, W12, Y12,W18,Y19, W19,V17,Y18, W17, Y17, U16, V16, W16, Y16, V15, W15,T20,U17, U18, U19, U20, V18, V19, V20, W20, Y20,P17,N20, N19,P19,P18, P20, R17, R18, R19, R20, T17, T18, T19	NC
E_8051_EN	I	D4	Pull low, using external 8051, NC or Pull hi, using internal 8051
USE_83M	I	D3	System clock enable,0:use SYSCLK, 1:90M generate by PLL

CLK_80IN	I	L19	System clock input :85~90M
F1	I	M1	Frequency 1 input, must pull high with 4.7K ohm resistor
F2	I	M19	Frequency 2 input from PHY 125M clock source.
F2_CTL	I	D2	Frequency 2 input enable, must pull low with 4.7K ohm resistor
X_IN	I	M20	**Crystal or OSC 25MHz Input:** This is a clock source of internal PLL.
X_OUT	O	L20	**Crystal 25MHz Output:** This pin should be floating with single-ended external clock.
/RST	I	D1	**Reset:** Active Low
MDIO	I/O/PU	H2	**Station Management Data In/Out:** PHY Management Data Input and Output.
MDC	O	H1	**Station Management Data Clock Out:** PHY Management Clock.
SDIO	I/O/PU	J2	**EEPROM Data In/Out:** EEPROM Serial Data Input and Output.
SDC	I/O/PU	J1	**EEPROM Data Clock In/Out:** EEPROM Serial Clock. (Note: It is output pin if the embedded MPU is active; otherwise as input pin)
SID[4:0]	I/PD I/PD I/PD I/UP I/UP	F2, F1, E4, E3, E2	**Switch ID:** MPU can identify the switch and PHYs with this ID. Default is "00011b".
GPIO[4:0]	I/O/PU	K3, K2, K1, J4, J3	**General Purpose I/O:** The 5 GPIOs can be programmed for special application. (Note: The function is not released to user normally. Please contact with ASIX directly if any requirement)
VDD33	P	D6, D13, G4, J17, P4, U7	**3.3V +/-5% Supply Voltage.**
VDD18	P	D7, H4, N4, N17, U8, U13	**1.8V +/-5% Supply Voltage.**
AVDD18	P	M17, L17, K17	**1.8V +/-5% Supply Voltage for PLL.**
VSS	P	D12, J9, J10, J11, J12, K4, K9, K10, K11, K12, L4, L9, L10, L11, L12,, M9, M10, M11, M12, N18, U15, M18, L18, K18	**Ground**

3.0 Functional Description

3.1 Introduction

In general, the AX88655AB device is a highly integrated Layer 2 switch. It supports eight 10/100/1000 ports with on-chip MACs. It also supports integrated switching logic, packet queuing memory and packet storage memory. The AX88655AB is capable of routing-and-forwarding packets at wire speed on all ports regardless of packet size.
It is a low cost solution for eight ports Gigabit Ethernet backbone switch design. No CPU interface is required; After power on reset, AX88655AB provide an auto load configuration setting function through a 2 wire serial EEPROM interface to access external EEPROM device, and AX88655AB can easily be configured to support trunking, QoS, IEEE 802.3x flow control threshold setting, broadcast storm control ...etc functions. An overview of AX88655AB's major functional blocks is shown in Fig-1.

3.2 Packet Filtering and Forwarding Process

The switch use simple store-and-forward algorithm as packet switching method. After receives incoming packets, the packets will be stored to the embedded memory first. The AX88655AB searches in the Address-Lookup Table with DA of the packet. The packet will be forward to its destination port, if this packet's DA hits; otherwise this packet will be broadcasted. Of course, only good packets will be forward.

3.3 MAC Address Routing, Learning and Aging Process

The switch supports 4K MAC entries for switching. Two-way dynamic address learning is performed by each good unicast packet is completely received. And linear/XOR hash algorithm of the static address learning is achieved by EEPROM configuration. On the other hand, the routing process is performed whenever the packet's DA is captured. If the DA can not get a hit result, the packet is going to broadcast.

Only the learned address entries are scheduled in the aging machine. If one station does not transmit any packet for a period of time, the belonging MAC address will be kicked out from the address table. The aging out time can be program automatically through the EEPROM configuration. (Default value is 300 seconds)

3.4 Full Duplex 802.3x Flow Control

In full duplex mode, AX88655AB supports the standard flow control mechanism defined in IEEE 802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interaction. When space of the packet buffer is less than the initialization setting threshold value, AX88655AB will send out a PAUSE-ON packet with pause time equal to "xFFF" to stop the remote node transmission. And then AX88655AB will send out a PAUSE-OFF packet with pause time equal to zero to inform the remote node to retransmit packet if has enough space to receive packets.

3.5 Half Duplex Back Pressure Control

In half duplex mode, AX88655AB provide a backpressure control mechanism to avoid dropping packets during network conjection situation. When space of the packet buffer is less than the initialization setting threshold value, AX88655AB will send a JAM pattern in the input port when it senses an incoming packet, thus force a collision to make the remote node transmission back off and will effectively avoid dropping packets. And then AX88655AB will not send out a JAM packet any more if has enough space to receive one packet.

3.6 MII Polling

The AX88655AB supports PHY management through the serial MDIO/MDC interface. That is, the AX88655AB access related register of PHYs via MDIO/MDC interface after power on reset. The AX88655AB will periodically and continuously poll and update the link status and link partner's ability which include speed, duplex mode, and 802.3x flow control capable status of the connected PHY devices through MDIO/MDC serial interface.

3.7 Port-Based QoS: Port-Pair

AX88655AB provides 4 Port-Pairs for bandwidth management. Users can assign any two ports as one Port-Pair with internal registers basically. Any packets will put the high priority queue of the Port-Pair when send the packets each other. That is, two ports of each Port-Pair will obtain more bandwidth than other ports when congestion.
In addition, one port can be as the highest priority port if one All_Bit of a Port-Pair is active. That is, user can assign format of the Port-Pair as OnePort-to-All and every packets of the OnePort will put in the high priority transmit queue of other ports..

3.8 VLAN and Broadcast Storming Prevention

AX88655AB supports 8 port-based VLAN groups to ease the administration of logical groups of stations that can communicate as if they were on the same LAN, and move, add or change numbers of these groups. The scheme can prevent effectively the broadcast storming from interfering with the whole transmission performance between ports. During this time, the ports belonging to different groups are independent. Only the destination port of broadcast packets in the same group will be allowed. Furthermore, the scheme of the VLAN group dividing is very flexible. The overlapped port-groups are allowed during some operations, for example, one port can be shared by two groups, and all the other operations between these two groups remain independent except for the overlapped port. Only the overlapped port could use the same destination MAC address for two different VLAN port-groups.

The AX88655AB can enable broadcast storm filtering control by MaxStorm[1:0]. This allows limitation of the number of broadcast packets into the switch, and can be implemented on a per port basis. The threshold of number of broadcast packets is set to 64/32/16. When enabled (i.e., MaxStorm[1:0] is not 2'b00), each port will drop broadcast packets (Destination MAC ID is ff ff ff ff ff ff) after receiving 64 continuous broadcast packets. The counter will be reset to 0 every 1 second or when receiving any non-broadcast packets (Destination MAC ID is not ff ff ff ff ff ff).
When disabled (i.e., MaxStorm[1:0] is 2'b00), or the number of non-unicast packets received at the port is not over the programmed threshold, the switch will forward the packet to all the ports (except the receiving port) within the VLANs specified at the receiving port.
If Broadcast-Storm-drop is enabled, the AX88655ABB will only drop broadcast packets but not the multicast packets.

3.9 Security Operation - Port SA restriction

AX88655AB provides source MAC address security support. When OneSaSecurityMode is turned on, then the port(s) will be fixed in the secured SA and stop learning. The port(s) will forward packets with the matched SA. If any other ports receive the packet with this secures SA, this packet will be discarded. Learns a source MAC address again if UpdateSaForSecurity is turned on.

3.10 Ingress/Egress Bandwidth Control Scheme

The bandwidth control will set the maximum bandwidth that each port can support. Basically AX88655AB provides 256 bandwidth classes of 1000 Mbps with thresholds (ResolutionIngress and ResolutionEngress). In half-duplex mode, the receiving side (ingress) will drop packets or send JAM with IgressMode if it is over the bandwidth threshold. On the transmitting side (egress), if it goes over the threshold, it will stop transmitting until time is up, then transmit data again. Under full-duplex mode, if the transmitting data meet the bandwidth threshold, the bandwidth control scheme will send the drop packets or 802.3x PAUSE frame. When it expires, it will send the release packet. For the receiving side without flow control (802.3x), it will drop the packet if it goes over the threshold.

3.11 Port Mirroring

Port mirroring is a function that mirrors or duplicates traffic from one "target port" to a "mirror port". The mirror or target port mirroring can be set up for each port individually to mirror either incoming packets or outgoing packets. Incoming and outgoing traffic need not be mirrored to the same port. Unidirectional traffic on a port can only be mirrored to one mirror port. Only correct packets that would normally be handled by the AX88655AB will be mirrored. Packets with CRC errors and collision fragments etc are **not** mirrored.

- **Input mirroring:** Traffic received on a port will be sent to the mirror port as well as to any other addressed port.
- **Output mirroring:** Traffic sent out on a port will also be sent to the mirror port.

4.0 Register Descriptions

Register Tables Summary:

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
00 H	**RESERVED**								**RESERVED**								0000 H
01 H	**RESERVED**								**RESERVED**								FFFF H
02 H	**RESERVED** + RxFlowCtrl[4:0]								**RESERVED** + TxFlowCtrl[4:0]								0000 H
03 H	**RESERVED**								**RESERVED**								00FF H
04 H	**RESERVED**								**RESERVED**								00FF H
05 H	**RESERVED**																0000 H
06 H	**RESERVED**								**RESERVED**								00FF H
07 H		**RESERVED**								**RESERVED**							1215 H
08 H	**RESERVED**				**RESERVED**				**RESERVED**				**RESERVED**				7777 H
09 H	**RESERVED**				**RESERVED**				**RESERVED**				**RESERVED**				7777 H
0A H	PortPair1[4:0]								PortPair0[4:0]								0000 H
0B H	PortPair3[4:0]								PortPair2[4:0]								0000 H
0C H	LowQueueWeight[3:0]				**RESERVED**				lw_LowQueueDiscardLimit [9:0]								1060 H
0D H	HighQueueWeight[3:0]				MaxStorm[1:0]				lw_HighQueueDiscardLimit [9:0]								1060 H
0E H	**RES**	PTO	**RES**	MPS[1:0]		SR	SP	NSB	**RES**	**51TE**	**RES**	QoS[1:0]		AE	HM	DB	8880 H
0F H	**RESERVED**								MaxAge[8:0]								1865 H
10 H	Trunk47[2:0]			Trunk30[2:0]					**RESERVED**								00C0 H
11 H	**RES**	**RES**	**RESERVED**						LowQueueFlowCtrlMark[9:0]								0010 H
12 H	MaxJam[5:0]								HighQueueFlowCtrlMark[9:0]								2810 H
13 H	**RESERVED**								hw_LowQueueDiscardLimit[9:0]								0070 H
14 H	RES	SmartFC [1:0]		RES	**RESERVED**				hw_HighQueueDiscardLimit[9:0]								0070 H
15 H	Port-based VLAN Group #1								Port-based VLAN Group #0								0000 H
16 H	Port-based VLAN Group #3								Port-based VLAN Group #2								0000 H
17 H	**RESERVED**								Port-based VLAN Group #4								0000 H
18 H	**RESERVED**								**RESERVED**								0000 H
19 H	ResolutionIngress Port 1[7:0]								ResolutionIngress Port 0[7:0]								FFFF H
1A H	ResolutionIngress Port 3[7:0]								ResolutionIngress Port 2[7:0]								FFFF H
1B H	**RESERVED**								ResolutionIngress Port 4[7:0]								FFFF H
1C H	**RESERVED**								**RESERVED**								FFFF H
1D H	iso	rm	MirrorPort[2:0]		PortMirrorEn[1:0]		IngressMode		ResolutionEngress Port 7[7:0]								00FF H
1E H	**RESERVED** + UpdateSaForSecurity[4:0]								**RESERVED** + OneSaSecurityMode[4:0]								0000 H
1F H	GCLK125MHz_Dly1ns_n[7:0]								TargetPort[2:0]			JumboLeng13_10[3:0]			JumboEnable		0000 H

Note:

1. The word “Reserved” = “Res.” on the above table.
2. Care must be taken that the “Reserved” registers should keep the default value always. Change of any reserved value may be resulting in unpredictable conditions.
3. The registers can be accessed by internal MPU only. The MPU will read in configuration table, located on EEPROM at somewhere address, and programs the above registers when every time power on or after system reset.
4. Basically, the registers can be accessed with the same data format as station management (similar to MDC and MDIO) via ADC and ADIO pins.

]

4.1 Register 00

BIT	R/W	DESCRIPTION
15:8	R/W	RESERVED
7:0	R/W	RESERVED

4.2 Register 01

BIT	R/W	DESCRIPTION
15:8	R/W	RESERVED
7:0	R/W	RESERVED

4.3 Register 02

BIT	R/W	DESCRIPTION
15:12,8	R/W	FlowCtrlEnable for MAC's receive part of Port[4:0] are configured by int. or ext. 8051 0: not identify PAUSE frames by receive part of MAC 1: can identify PAUSE frames. That is, PauseTimer of MAC will be active.
7:4,0	R/W	FlowCtrlEnable for MAC's transmit part of Port[4:0] are configured by int. or ext. 8051 0: not send PAUSE frames 1: send PAUSE frames when the packet buffer run out.

4.4 Register 03

BIT	R/W	DESCRIPTION
15:8	R/W	RESERVED
7:0	R/W	RESERVED

4.5 Register 04

BIT	R/W	DESCRIPTION
15:8	R/W	RESERVED
7:0	R/W	RESERVED

4.6 Register 05

BIT	R/W	DESCRIPTION
15:0	R	RESERVED

4.7 Register 06

BIT	R/W	DESCRIPTION
15:10	R/W	RESERVED
9:0	R/W	RESERVED

4.8 Register 07

BIT	R/W	DESCRIPTION
15	R/W	RESERVED
14:8	R/W	RESERVED
7	R/W	RESERVED
6:0	R/W	RESERVED

4.9 Register 08

BIT	R/W	DESCRIPTION
15:12	**R/W**	**RESERVED**
11:9	**R/W**	**RESERVED**
8:4	**R/W**	**RESERVED**
3:0	**R/W**	**RESERVED**

4.10 Register 09

BIT	R/W	DESCRIPTION
15:12	**R/W**	**RESERVED**
11:9	**R/W**	**RESERVED**
8:4	**R/W**	**RESERVED**
3:0	**R/W**	**RESERVED**

4.11 Register 0A

BIT	R/W	DESCRIPTION
15	**R/W**	All_Bit of PortPair #1 when QoS[0] is high
14:12	**R/W**	Port_ID of PortPair #1 when QoS[0] is high
11	**R/W**	All_Bit of PortPair #1 when QoS[0] is high
10:8	**R/W**	Port_ID of PortPair #1 when QoS[0] is high
7	**R/W**	All_Bit of PortPair #0 when QoS[0] is high
6:4	**R/W**	Port_ID of PortPair #0 when QoS[0] is high
3	**R/W**	All_Bit of PortPair #0 when QoS[0] is high
2:0	**R/W**	Port_ID of PortPair #0 when QoS[0] is high

4.12 Register 0B

BIT	R/W	DESCRIPTION
15	**R/W**	All_Bit of PortPair #3 when QoS[0] is high
14:12	**R/W**	Port_ID of PortPair #3 when QoS[0] is high
11	**R/W**	All_Bit of PortPair #3 when QoS[0] is high
10:8	**R/W**	Port_ID of PortPair #3 when QoS[0] is high
7	**R/W**	All_Bit of PortPair #2 when QoS[0] is high
6:4	**R/W**	Port_ID of PortPair #2 when QoS[0] is high
3	**R/W**	All_Bit of PortPair #2 when QoS[0] is high
2:0	**R/W**	Port_ID of PortPair #2 when QoS[0] is high

4.13 Register 0C

BIT	R/W	DESCRIPTION
15:12	**R/W**	WeightForLowQue: Weight for low priority queues when QoS is active (see Appendix C)
11:10	**R/W**	Reserved
9:0	**R/W**	LowWaterMark of low priority queues when drop packets

4.14 Register 0D

BIT	R/W	DESCRIPTION
15:12	**R/W**	WeightForHighQue: Weight for high priority queues when QoS is active (see Appendix C)
11:10	**R/W**	Maximum number of broadcast frames that can be accumulated in each input frame buffer. 00: disable broadcast storm control 01: 31 frames 10: 47 frames 11: 63 frames
9:0	**R/W**	LowWaterMark of high priority queues when drop packets

4.15 Register 0E

BIT	R/W	DESCRIPTION
15	**RO**	**RESERVED**
14	**R/W**	802.3x Flow control frame recognition control 0: check for MAC control frame DA MAC address in addition to the MAC control type field 1: check only the MAC control type field
13	**R/W**	Setting for maximum length of packet that received 0: 1518 byte 1: 1522 byte
12:11	**R/W**	**RESERVED**
10	**R/W**	Software Reset (Only reset the switch kernel) 0: active 1: disable
9	**R/W**	Back-off algorithm selection 0: disable. Device will perform the IEEE standard exponential back off algorithm when a collision occurs. 1: enable. When collisions occur, the MACs will back off up to 7 slots. Note :: SuperMac v.s. FlowCtrl
8	**R/W**	0: stop generate JAM patterns after some collision that is defined by MaxJam[5:0] 1: Never stop back-pressure (Note: Only availible for Ethernet..Not FastEternet)
7	**R/W**	**RESERVED**
6	**R/W**	**RESERVED**

5	**R/W**	**RESERVED**
4:3	**R/W**	QoS selection 00: disable QoS function 01: Port-Pair Priority algorithm 10: 802.1p
2	**R/W**	AgingEnable Switch Table Entry Aging Control. Only the dynamically learned addresses will be aged. All explicit entries will not age. The aging time is programmed in register 0F. 0: disable. The table aging process is disabled. 1: enable. The table aging process is enabled and a hardware process ages every dynamically learned table entry.
1	**R/W**	Hash algorithm selection 0: XOR mapping 1: Linear mapping
0	**R/W**	**RESERVED**

4.16 Register 0F

BIT	R/W	DESCRIPTION
15:9	**R/W**	IPG1 for transmit part of all MII MACs
8:0	**R/W**	MaxAge. This is a seven-bit register containing unsigned integer for determining the address-aging timer.

4.17 Register 10

BIT	R/W	DESCRIPTION
15:13	**R/W**	Trunking selection for Port[7:4] 000: disable trunking 001: disable trunking 010: one 2-Port Trunking for Port[5:4] 011: one 2-Port Trunking for Port[5:4] 100: one 2-Port Trunking for Port[7:6] 101: one 4-Port Trunking 110: two 2-Port Trunkings for Port[7:6] and Port[5:4] 111: one 4-Port Trunking
12:10	**R/W**	Trunking selection for Port[3:0] 000: disable trunking 001: disable trunking 010: one 2-Port Trunking for Port[1:0] 011: one 2-Port Trunking for Port[1:0] 100: one 2-Port Trunking for Port[3:2] 101: one 4-Port Trunking 110: two 2-Port Trunkings for Port[3:2] and Port[1:0] 111: one 4-Port Trunking
9:0	**R/W**	Reserved

4.18 Register 11

BIT	R/W	DESCRIPTION
15:10	**R/W**	Reserved
9:0	**R/W**	LowWaterMarkForFlowCtrl. This is a ten-bit register containing unsigned integer for low priority queues whether generate PAUSE-ON or not.

4.19 Register 12

BIT	R/W	DESCRIPTION
15:10	**R/W**	MaxJam. This is a six-bit register containing unsigned integer for determining the JAM counter whether generate JAM or not.
9:0	**R/W**	HighWaterMarkForFlowCtrl. This is a ten-bit register containing unsigned integer for high priority queues whether generate PAUSE-OFF or not.

4.20 Register 13

BIT	R/W	DESCRIPTION
15:10	**R/W**	Reserved
9:0	**R/W**	HighWaterMark of low priority queues when drop packets

4.21 Register 14

BIT	R/W	DESCRIPTION
15	**R/W**	**RESERVED**
14:13	**R/W**	SmartFlowCtrl for mix-speed connection 0: disable 1: disable flow ctrl for all 10 Mbps port 2: disable flow ctrl for all 100 Mbps port 3: reserved
12	**R/W**	**RESERVED**
11:10	**R/W**	Reserved
9:0	**R/W**	HighWaterMark of high priority queues when drop packets

4.22 Register 15

BIT	R/W	DESCRIPTION
15:8	**R/W**	VLAN #1
7:0	**R/W**	VLAN #0

4.23 Register 16

BIT	R/W	DESCRIPTION
15:8	**R/W**	VLAN #3
7:0	**R/W**	VLAN #2

4.24 Register 17

BIT	R/W	DESCRIPTION
15:8	**R/W**	RESERVED
7:0	**R/W**	VLAN #4

4.25 Register 18

BIT	R/W	DESCRIPTION
15:8	R/W	RESERVED
7:0	R/W	RESERVED

4.26 Register 19

BIT	R/W	DESCRIPTION
15:8	R/W	Resolution of port #1 for ingress bandwidth control
7:0	R/W	Resolution of port #0 for ingress bandwidth control

4.27 Register 1A

BIT	R/W	DESCRIPTION
15:8	R/W	Resolution of port #3 for ingress bandwidth control
7:0	R/W	Resolution of port #2 for ingress bandwidth control

4.28 Register 1B

BIT	R/W	DESCRIPTION
15:8	R/W	RESERVED
7:0	R/W	Resolution of port #4 for ingress bandwidth control

4.28 Register 1C

BIT	R/W	DESCRIPTION
15:8	R/W	RESERVED
7:0	R/W	RESERVED

4.28 Register 1D

BIT	R/W	DESCRIPTION
15	R/W	Isolation Enable for Port-based Mirror 0: disable 1: active
14	R/W	ResolutionMode 0: Byte mode 1: Word mode
13:11	R/W	Mirror Port for Port-based Mirror
10:9	R/W	Port-based Mirror Mode 0: disable Port-based Mirror 1: Imgress 2: Egress 3: Reserved
8	R/W	Igress Mode 0: drop pkts by ARL 1: send Pause for GmacTx
7:0	R/W	Resolution of port #7 for egress bandwidth control

4.28 Register 1E

BIT	R/W	DESCRIPTION
15:12,8	**R/W**	Update Source MAC For Security Mode of each Port 0: keep one Source MAC 1: update the Source MAC
7:4,0	**R/W**	OneSaSecurityMode[4:0] 0: disable 1: active

4.28 Register 1F

BIT	R/W	DESCRIPTION
15:12,8	**R/W**	GCLK125MHz_Dly_1ns_n[4:0] 0: Delay 1ns 1: no delay
7:5	**R/W**	Target Port for Port-based Mirror
4:1	**R/W**	Max Length of Jumbo Packet: from 1K to 15K Byte
0	**R/W**	Accept Jumbo Enable 0: drop jumbo packets 1: accept jumbo packets

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.3	+4.0	V
Input Voltage	Vin	-0.3	Vdd+0.5	V
Output Voltage	Vout	-0.3	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+220	°C

Note: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+3.0	+3.6	V

5.3 DC Characteristics

(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 70°C)

Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.3	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

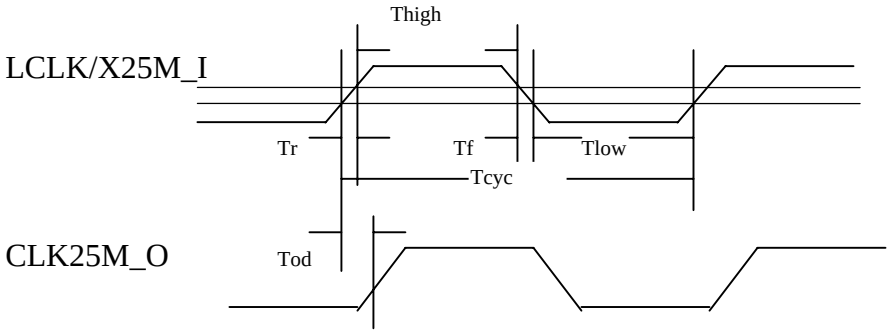
Description	SYM	Min	Tpy	Max	Units
Power Consumption	Pc		TBD		mA

Note:

1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

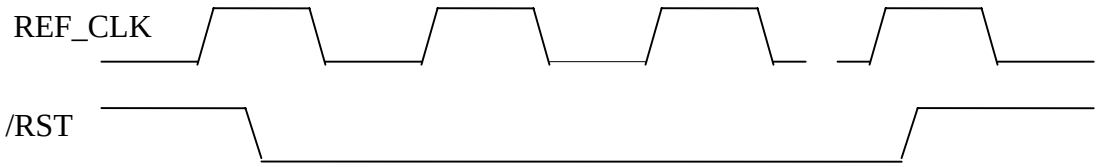
5.4 AC specifications

5.4.1 LCLK



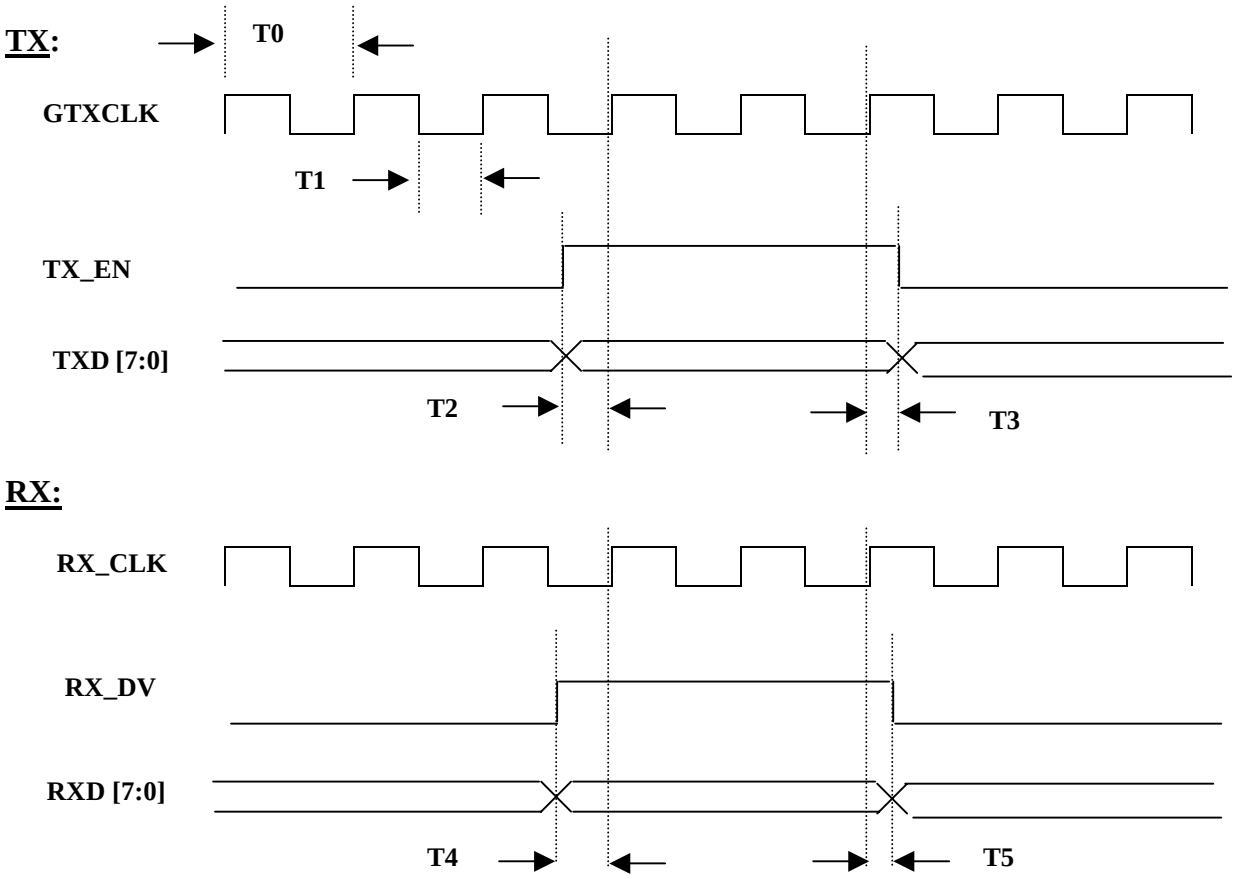
Symbol	Description	Min	Typ.	Max	Units
Tcyc	CYCLE TIME		20		ns
Thigh	CLK HIGH TIME	8	10	12	ns
Tlow	CLK LOW TIME	8	10	12	ns
Tr/Tf	CLK SLEW RATE	1	-	4	ns
Tod	LCLK TO BMCLK OUT DELAY		2		ns

5.4.2 Reset Timing



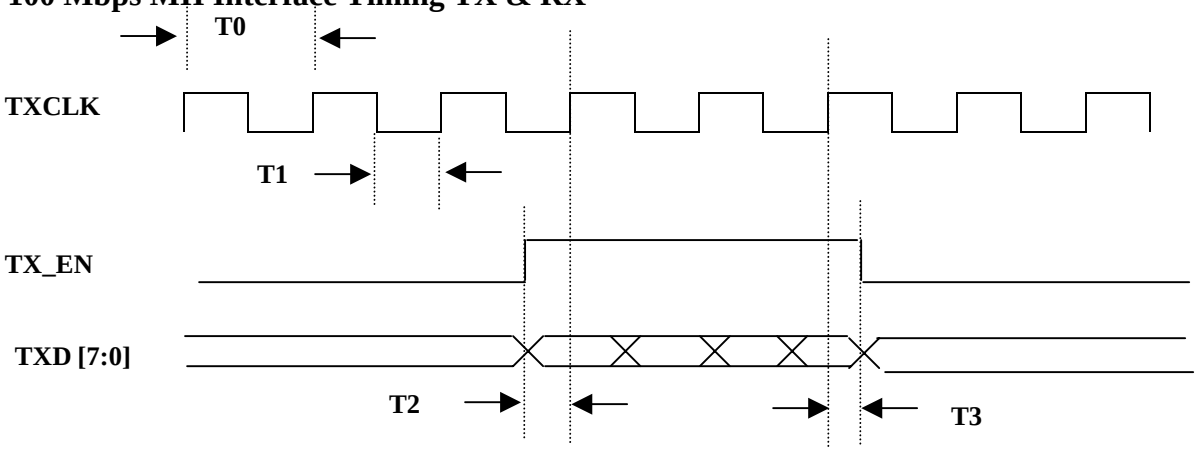
Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	10	-	-	REF_Clk

5.4.3 GMII Interface Timing TX & RX

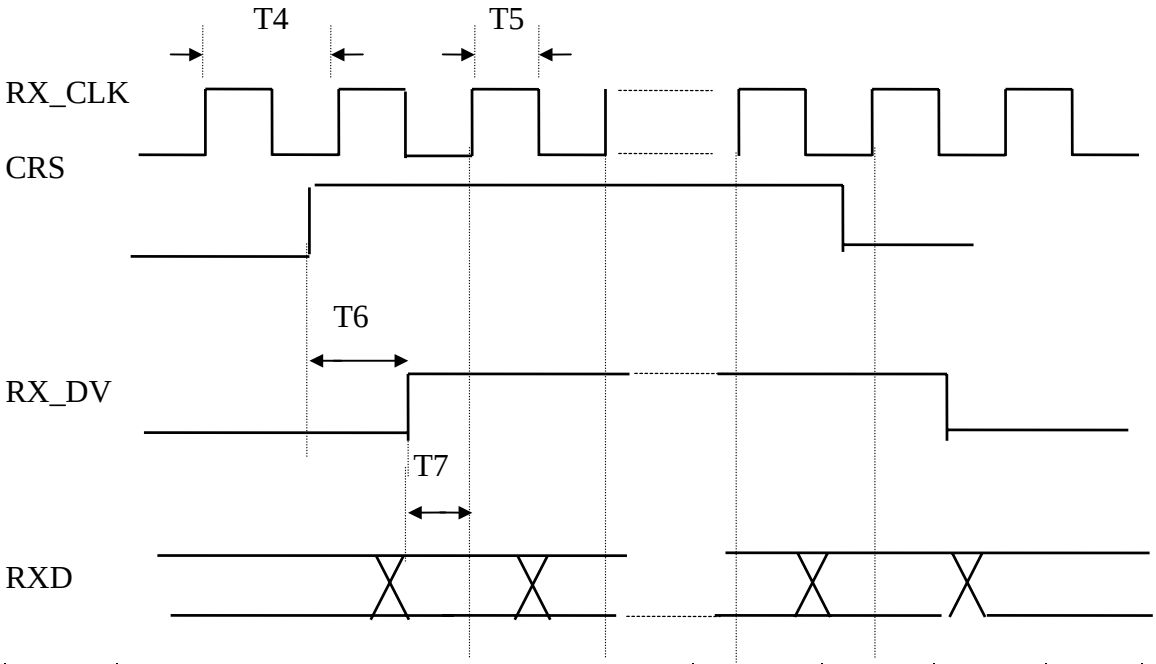


Symbol	Description	Min	Typ.	Max	Units
T0	REF_CLK Clock Cycle Time	7.998	8	8.002	ns
T1	REF_CLK Clock High Time		4		ns
T2	TX_EN and TXD data setup to REF_CLK rising edge	2.5			ns
T3	TX_EN and TXD data hold from REF_CLK rising edge	0.5			ns
T4	RX_DV and RXD data setup to RX_CLK rising edge (RCVR)	2.0			ns
T5	RX_DV and RXD data hold from RX_CLK rising edge(RCVR)	0			ns

5.4.4 100 Mbps MII Interface Timing TX & RX

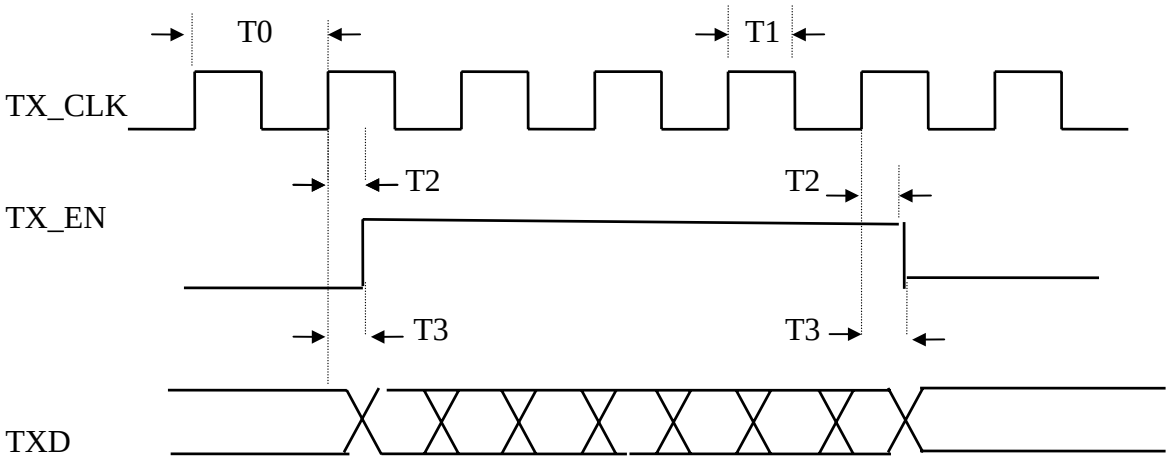


Symbol	Description	Min	Typ.	Max	Units
T0	TX_CLK Cycle Time	39.996	40	40.004	ns
T1	TX_CLK High Time	14	20	26	ns
T2	TX_EN Delay from TXCLK High	7.440		21.760	ns
T3	TXD Delay from TX_CLK High	3.410		13.320	ns

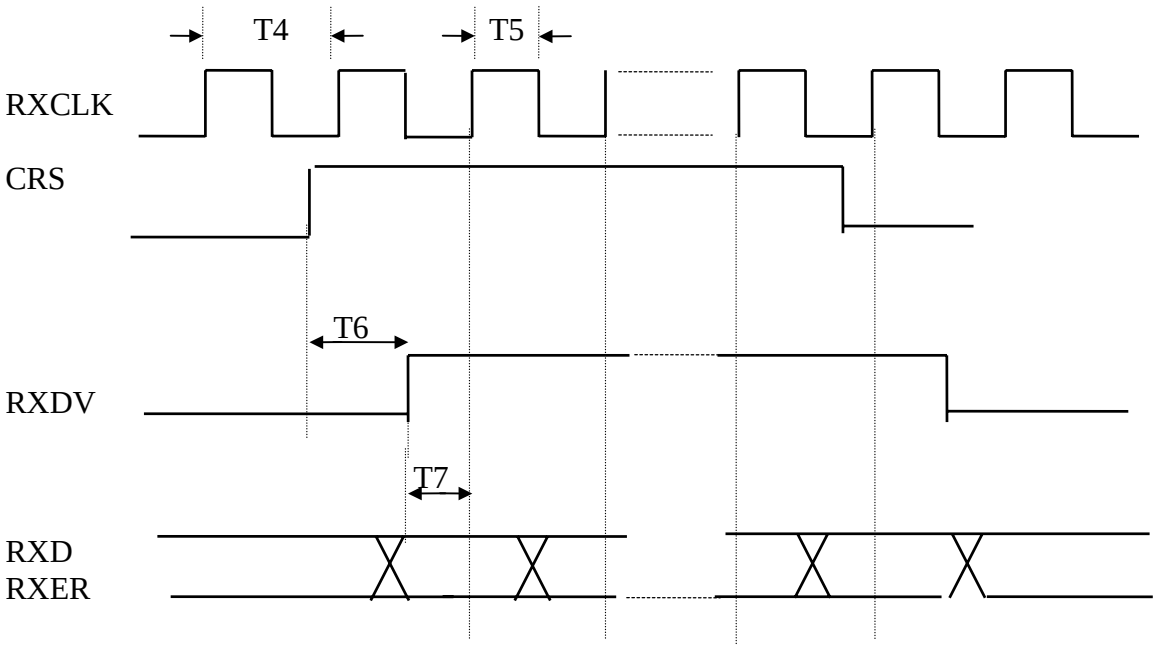


Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RX_DV Delay Requirement	40		160	ns
T7	RXD or RX_DV setup to RX_CLK rise time	10			ns

5.4.5 10 Mbps MII Interface Timing Tx & Rx

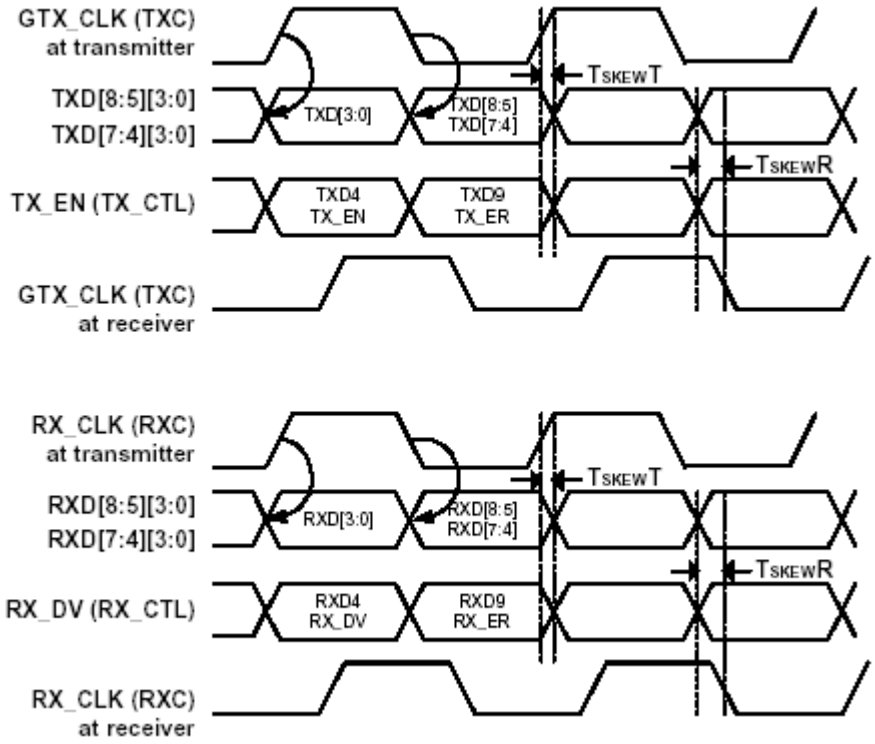


Symbol	Description	Min	Typ.	Max	Units
T0	TX_CLK Cycle Time	399.96	400	400.04	ns
T1	TX_CLK High Time	14	20	26	ns
T2	TX_EN Delay from TX_CLK High	7.440		21.760	ns
T3	TXD Delay from TX_CLK High	3.410		13.320	ns



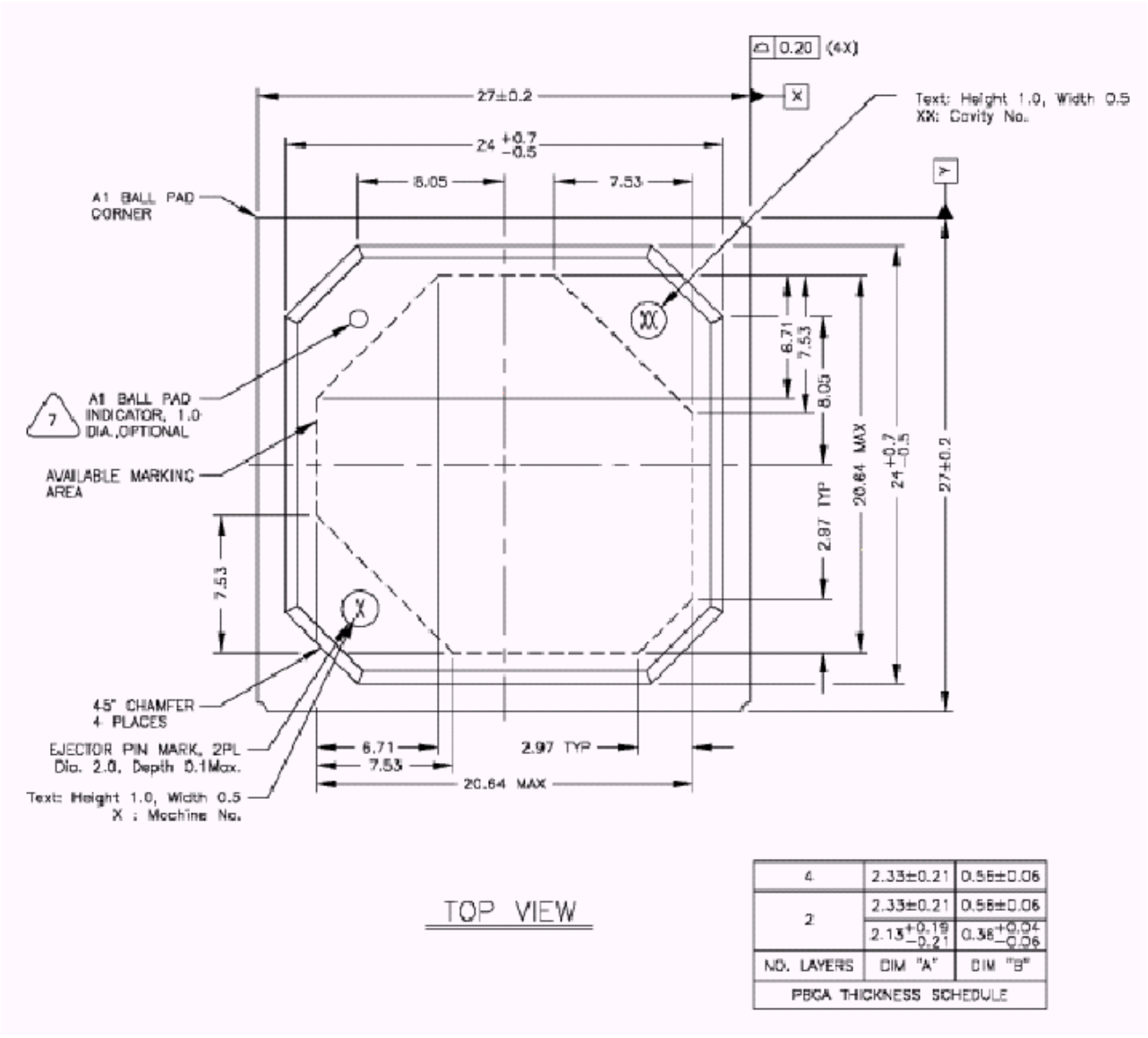
Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RX_DV Delay Requirement	40		160	ns
T7	RXD or RX_DV setup to RX_CLK rise time	10			ns

5.4.1 RGMII Interface Timing

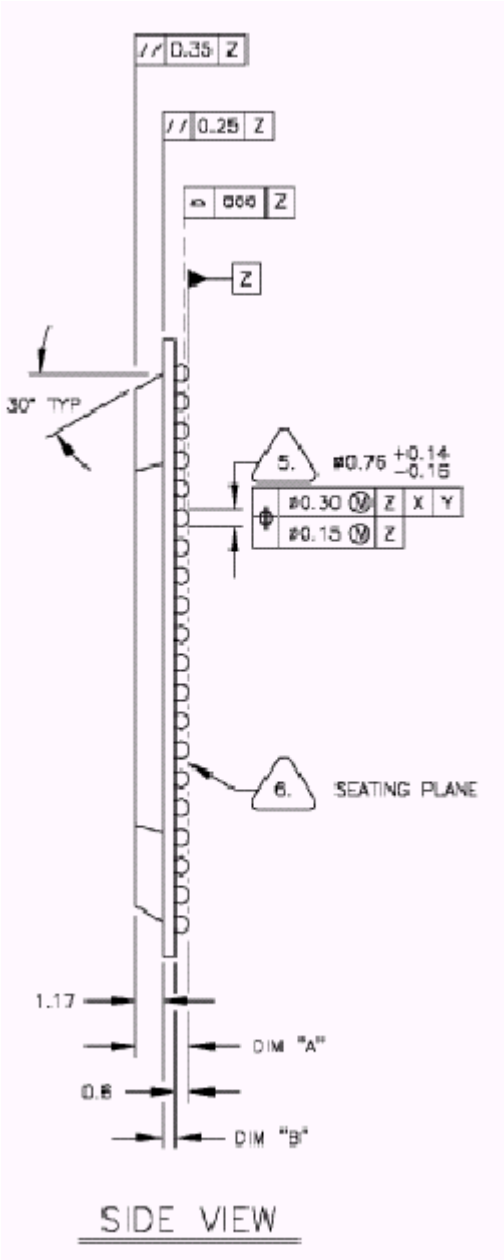


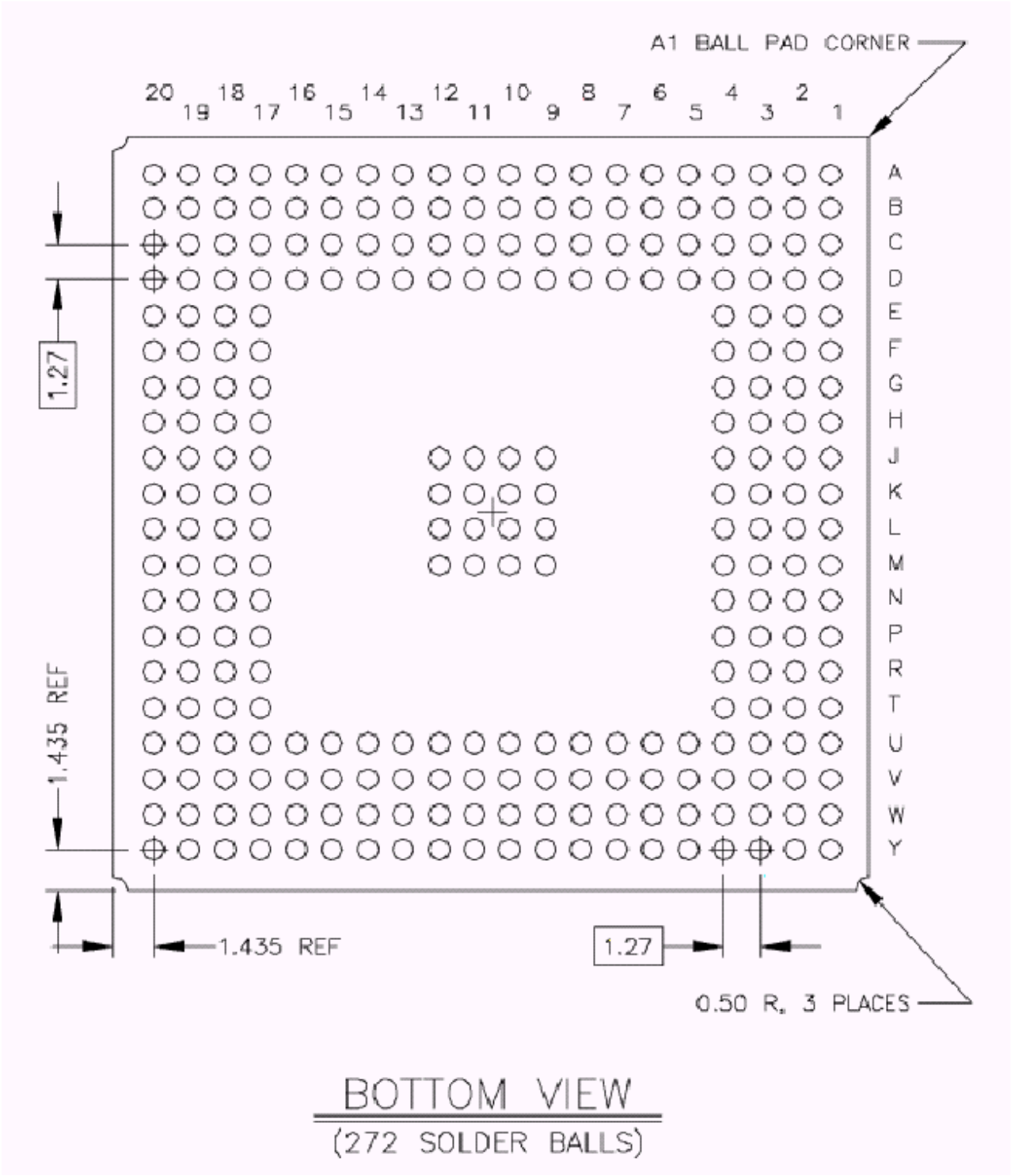
Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.8	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
$T_{CYCLE\_HIGH100}$	High Time for 100BASE-T[1]	16	20	24	ns
T_{CYCLE_HIGH10}	High Time for 10BASE-T[1]	160	200	240	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

6.0 PACKAGE INFORMATION



4	2.33±0.21	0.56±0.06
2	2.33±0.21	0.56±0.06
	$2.13^{+0.19}_{-0.21}$	$0.38^{+0.04}_{-0.06}$
NO. LAYERS	DIM "A"	DIM "B"
PBGA THICKNESS SCHEDULE		

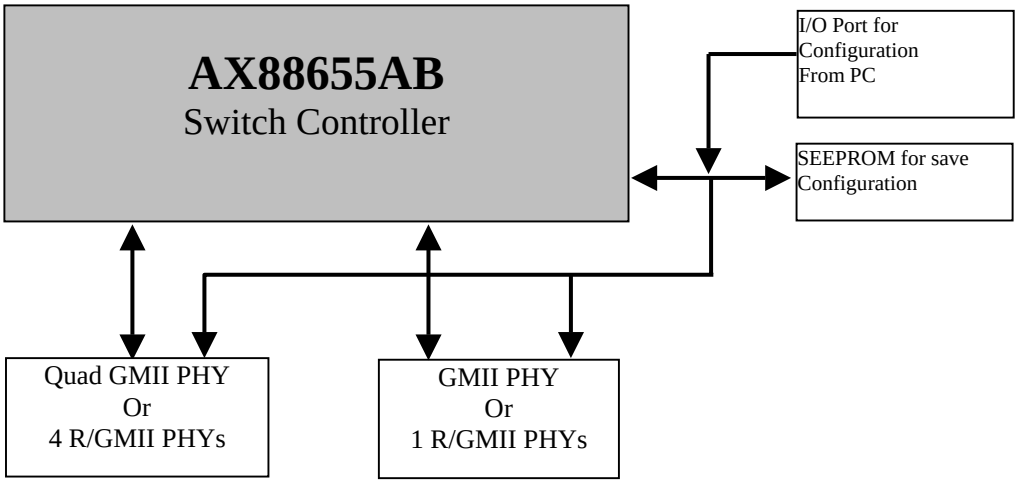




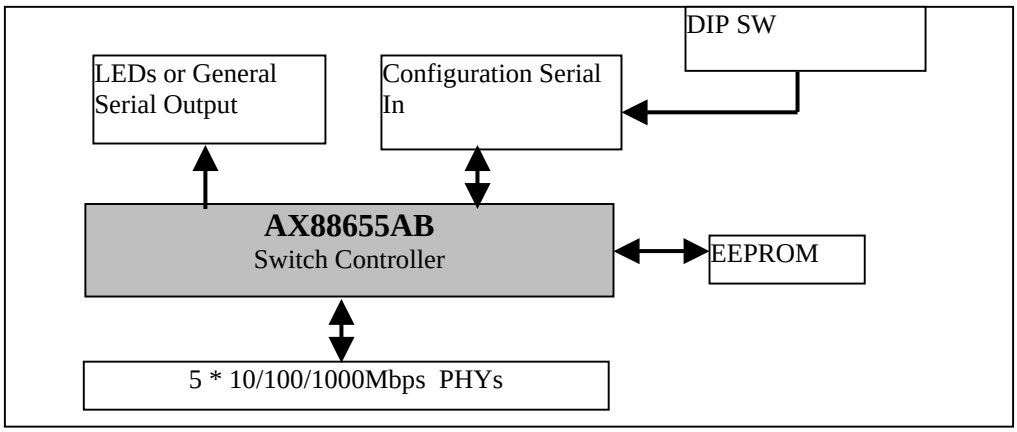
BOTTOM VIEW
(272 SOLDER BALLS)

Appendix A: System Applications

A.1 AX88655AB as 5-port SOHO high traffic power user switch



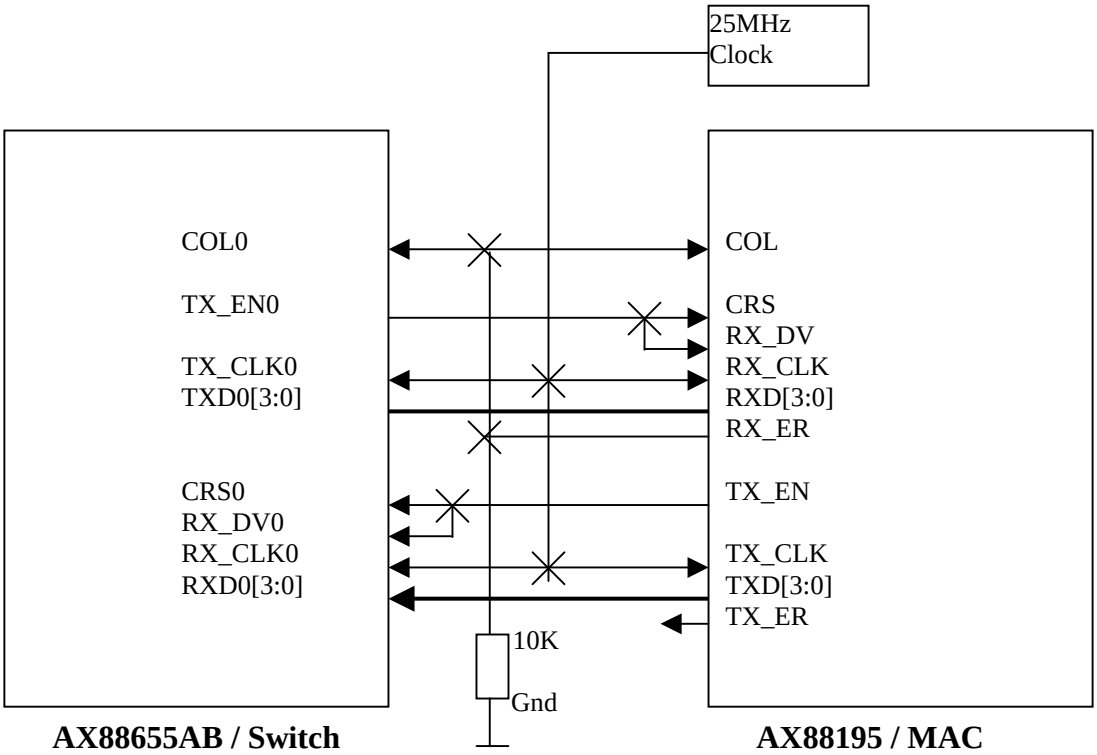
A.2 AX88655AB as 5-port Smart switch (DIP switch configurable)



Appendix B: Design Note

B.1 Using MII I/F connects to MAC

Using MII interface to connect to MAC type device application for AX88655AB is illustrated bellow.



Note: 1. The MAC needs to run at full-duplex mode.
2. Care must be taken that the receive side has enough setup and/or hold time
3. Some kind of CPU with embedded MAC can also refer to this example

Appendix C: Weight Setting for QoS

Service Ratio (High : Low)	WeightForHighQue[3:0]	WeightForLowQue[3:0]
1 : 1	4'b0100	4'b0100
2 : 1	4'b0100	4'b0010
3 : 1	4'b0110	4'b0010
4 : 1	4'b0100	4'b0001
5 : 1	4'b0101	4'b0001
6 : 1	4'b0110	4'b0001
7 : 1	4'b0111	4'b0001
8 : 1	4'b1000	4'b0001
9 : 1	4'b1001	4'b0001
10 : 1	4'b1010	4'b0001
11 : 1	4'b1011	4'b0001
12 : 1	4'b1100	4'b0001
13 : 1	4'b1101	4'b0001
14 : 1	4'b1110	4'b0001
15 : 1	4'b1111	4'b0001

Appendix D: Resolution Ingress/Egress for Bandwidth Control

Gigabit Bandwidth Ratio	ResolutionIngress / ResolutionEngress
10%	8'h1A
20%	8'h34
30%	8'h4E
40%	8'h67
50%	8'h80
60%	8'h9A
70%	8'hB4
80%	8'hC0
90%	8'hE7
100%	8'hFF

Note :

1. ResolutionMode is "Byte mode".
2. 256 level of bandwidth control supports.

Revision	Date	Comment
V. 0.5	11/07/02	Initial release.
V. 0.6	02/01/03	Modify X_IN clock from 27 to 25 and system clock from 90M to 83.3M Register 0D modify
V. 0.7	2003/4/7	1. Appendix D resolutions setting on 30% (change from 34 to 4E) 2. Change pin name from NC to new name: PIN # / New PIN name D4 / E_8051_EN M19 / F2 L19 / CLK_80_IN D3 / USE_83M D2 / F2_CTL M1 / F1 3. Modify system clock to 90M
V. 0.8	2003/6/11	1. Add RGMII timing diagram 2. TRUNKING register correction 3. modify all GMII/MII to RGMII/GMII/MII

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