SONY **CXA2521Q**

RF Amplifier for CD Players

Description

The CXA2521Q is an IC for RF signal processing of compact discs.

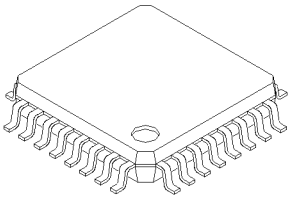
Features

- Supports quadruple speed (RF signal fc 8MHz)
- Peak hold circuit time constant of mirror circuit can be adjusted (switching function provided)
  Accurate mirror detection is possible from traverse signal of high/low speed search
- Fluctuations of characteristics are very small, which are caused by variations of resistance value and deviations of temperature characteristics for IC internal/external resistors, because the input and feedback resistors of the tracking error amplifier are externally attached
- APC (Automatic Power Control) function

Functions

- RF summing amplifier
- Focus error amplifier
- Tracking error amplifier
- APC circuit
- Focus OK detection function
- Defect detection function
- Mirror detection function

32 pin QFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{CC}	7	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	800	mW

Operating Conditions

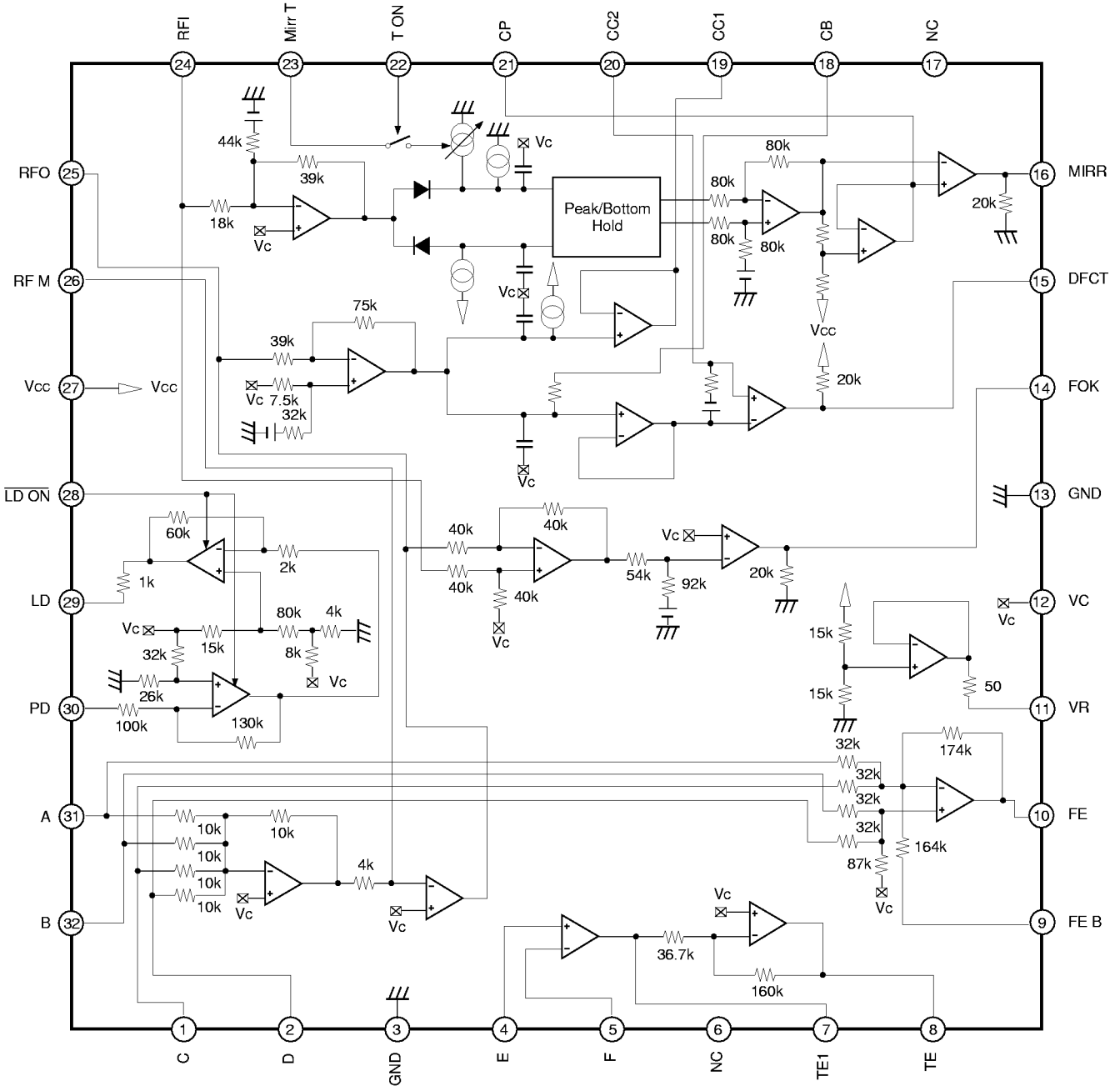
• Supply voltage	V_{CC}–GND	+4.5 to +5.5	V
• Operating temperature	Topr	–20 to +75	°C

Applications

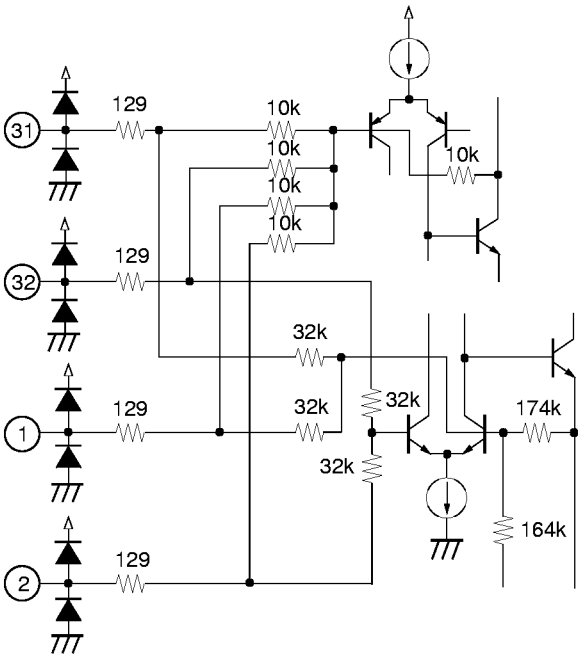
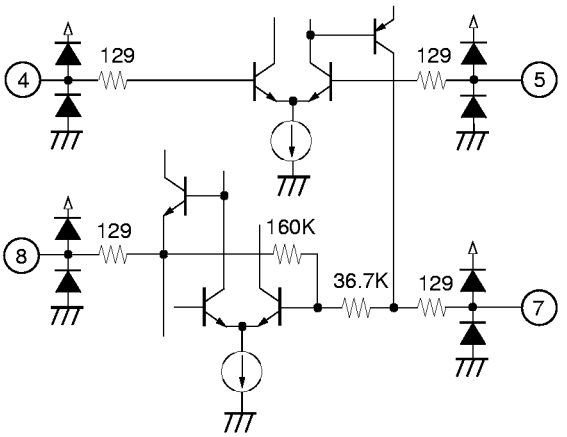
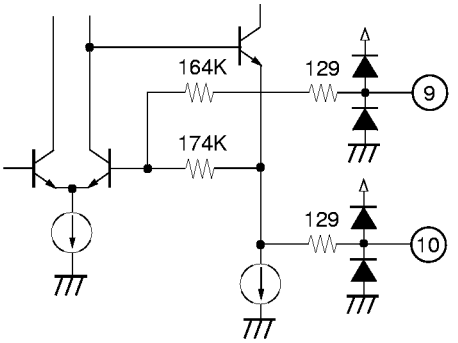
- Compact disc players
- CD-ROM drive

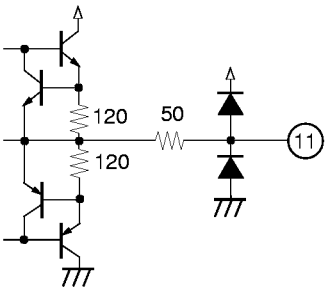
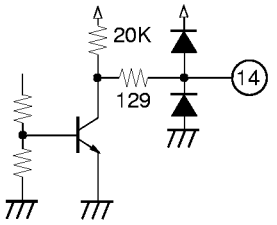
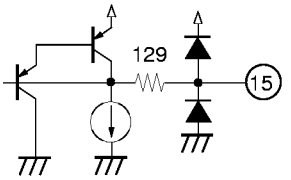
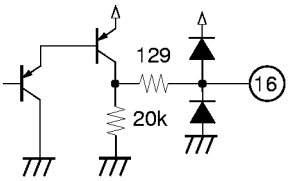
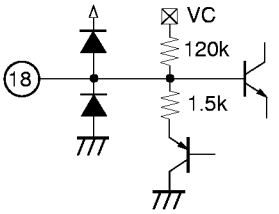
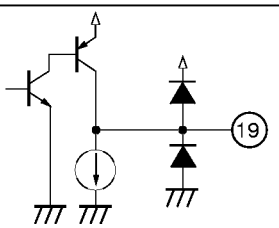
E94807–ST

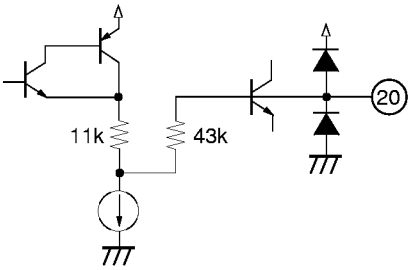
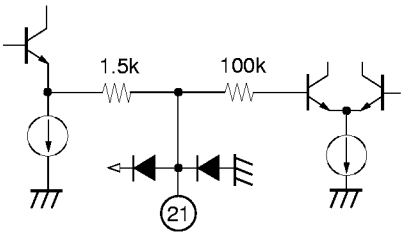
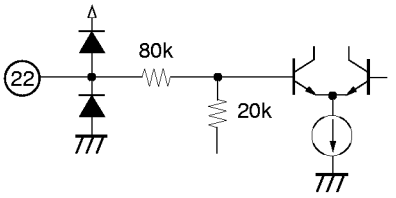
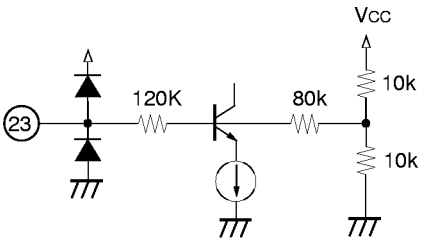
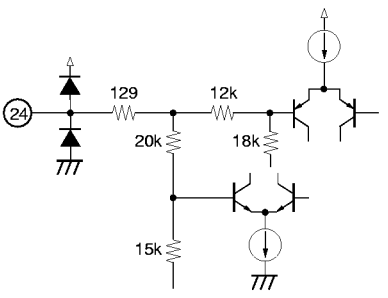
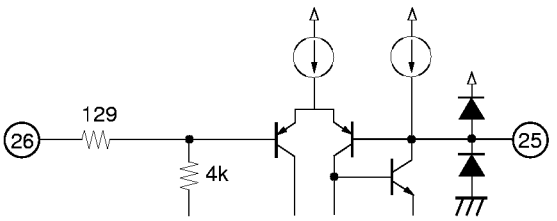
Block Diagram

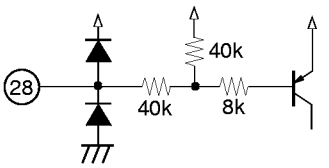
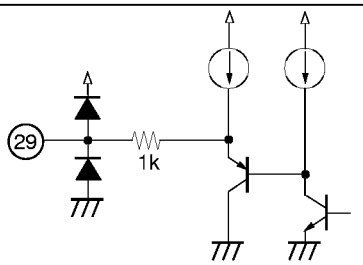
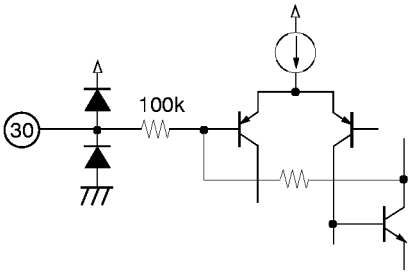


Pin Description

Pin No.	Symbol	I/O	Equivalent Circuit	Description
31 32 1 2	A B C D	I I I I		Input of RF summing amplifier and focus error amplifier.
3	GND			Ground.
4 5 7 8	E F TE1 TE	I I O O		Tracking error amplifier input for Pins 4 and 5; tracking error amplifier output and tracking error drive input for Pin 7; tracking error drive output for Pin 8.
6	NC			Not connected.
9 10	FE B FE	I O		Focus bias adjustment of focus amplifier for Pin 9; focus error amplifier output for Pin 10.

Pin No.	Symbol	I/O	Equivalent Circuit	Description
11	VR	O		(Vcc+GND)/2 DC voltage output.
12	VC	I		VC center voltage input.
13	GND			Ground.
14	FOK	O		FOK comparator output.
15	DFCT	O		Defect comparator output.
16	Mirr	O		Mirror comparator output.
17	NC			Not connected.
18	CB	I		Capacitor connection of Defect bottom hold.
19	CC1	O		Defect bottom hold output.

Pin No.	Symbol	I/O	Equivalent Circuit	Description
20	CC2	I		Input of Defect bottom hold output with capacitance coupled.
21	CP	I		Capacitor connection of mirror hold. Non-inversion input of mirror comparator.
22	T ON	I		Peak hold time constant switching. Time constant can be adjusted by connecting this pin to Vcc; fixed by connecting to GND.
23	Mirr T	I		Peak hold time constant adjustment. This is the time constant which is adjusted when Pin 22 is ON.
24	RFI	I		Input of RF summing amplifier output with capacitance coupled.
25 26	RFO RF M	O I		Non-inversion input of RF drive amplifier for Pin 26; RF signal output for Pin 25; resistance value connected between Pins 25 and 26 which determines the low frequency gain of RF drive amplifier.

Pin No.	Symbol	I/O	Equivalent Circuit	Description
27	V_{CC}			V_{CC}
28	$\overline{\text{LD ON}}$	I		APC amplifier ON/OFF switching. OFF when connecting to V_{CC}; ON when connecting to GND.
29	LD	O		APC amplifier output.
30	PD	I		APC amplifier input.

Electrical Characteristics

(Ta = +25°C, V_{CC} = +2.5V, GND = V_C, V_{EE} = –2.5V)

Measure-ment No.		Measurement Item	Symbol	SW Conditions						Bias Conditions					Measure-ment Point	Description of Output Waveform and Measurement Method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	E1	E2	E3	E4	E5						
1		Current consumption	I_{CC}					○		0V	–2.0V	0V	–2.0V	300mV	27	Pin DC current measurement	8	12	15	mA
2		Current consumption	I_{EE}					○						300mV	3 + 13	Pin DC current measurement	–15	–12	–8	mA
3	RF Amplifier	Offset voltage	V1-1										2.0V	0V	25	DC voltage measurement	–40	0	40	mV
4		Voltage gain	G1-1	○	○											V1 = 100mVpp f = 1kHz	15.5	18.5	21.5	dB
5		Frequency response	F1-1	○	○											V1 = 100mVpp f = 8MHz Difference for G1-1	–3	—	—	dB
6		Maximum output amplitude H	V1-2	○	○					300mV						DC voltage measurement	1.3	—	—	V
7		Maximum output amplitude L	V1-3	○	○					–300mV						DC voltage measurement	—	—	–0.3	V
8	FE Amplifier	Offset voltage	V2-1							0V					10	DC voltage measurement	–30	0	30	mV
9		Voltage gain 1	G2-1	○												V1 = 100mVpp f = 1kHz	17.7	20.7	23.7	dB
10		Voltage gain 2	G2-2		○											V1 = 100mVpp f = 1kHz	17.7	20.7	23.7	dB
11		Voltage gain difference	G2-3													G2-1 – G2-2	–3	0	3	dB
12		Frequency response 1	F2-1	○												V1 = 100mVpp f = 90kHz Difference for G2-1	–3	—	—	dB
13		Frequency response 2	F2-2		○											V1 = 100mVpp f = 90kHz Difference for G2-2	–3	—	—	dB
14		Maximum output amplitude H	V2-2		○					300mV						DC voltage measurement	1.9	—	—	V
15		Maximum output amplitude L	V2-3	○						300mV						DC voltage measurement	—	—	–1.9	V
16	TE Amplifier	Offset voltage	V3-1							0V	–2.0V	0V	2.0V	0V	8	DC voltage measurement	–30	0	30	mV
17		Voltage gain 1	G3-1			○										V1 = 100mVpp f = 1kHz	17.9	20.9	23.9	dB
18		Voltage gain 2	G3-2				○									V1 = 100mVpp f = 1kHz	17.9	20.9	23.9	dB
19		Voltage gain difference	G3-3													G3-1– G3-2	–3	0	3	dB
20		Frequency response 1	F3-1			○										V1 = 100mVpp f = 90kHz Difference for G3-1	–3	—	—	dB
21		Frequency response 2	F3-2				○									V1 = 100mVpp f = 90kHz Difference for G3-2	–3	—	—	dB

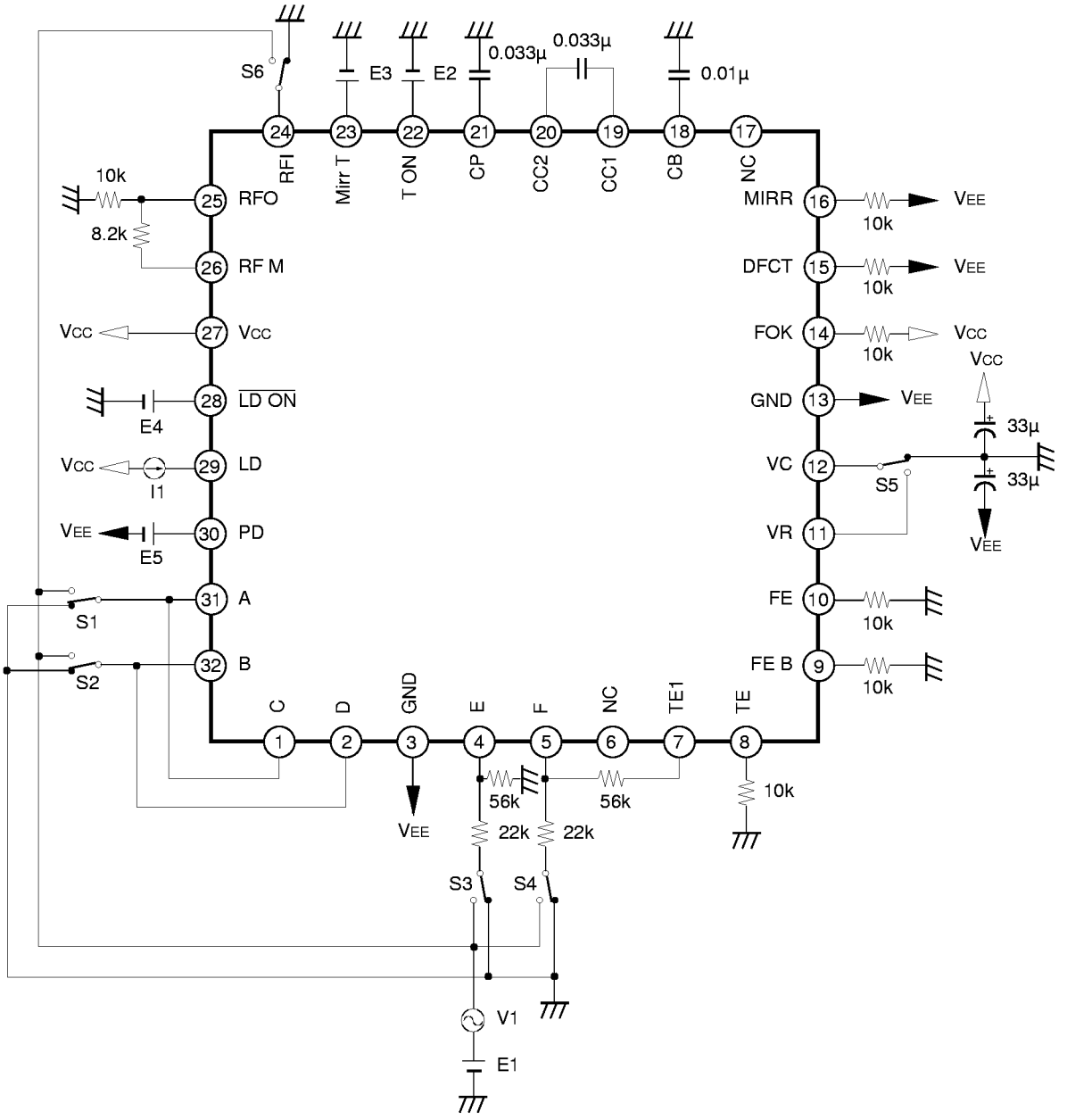
(Ta = +25°C, V_{CC} = +2.5V, GND = V_C, V_{EE} = –2.5V)

Measure-ment No.		Measurement Item	Symbol	SW Condition S1	S2	S3	S4	S5	S6	Bias Conditions E1	E2	E3	E4	E5	Measure-ment Point	Description of Output Waveform and Measurement Method	Min.	Typ.	Max.	Unit
22	TE	Maximum output amplitude H	V3-2				O			300mV	–2.0V	0V	2.0V	0V		Dc voltage measurement	1.9	—	—	V
23	TE	Maximum output amplitude L	V3-3			O				300mV						Dc voltage measurement	—	—	–1.9	V
24	FOK	Threshold voltage	V4-1						O	change					24	Pin 15 voltage where Pin 22 becomes 0V (GND)	–400	—	–300	mV
25	FOK	High level output voltage	V4-2						O	–375mV					14	V1 = 1.0Vpp f = 5kHz	2.2	–	–	V
26	FOK	Low level output voltage	V4-3						O							V1 = 1.0Vpp f = 5kHz	—	—	–1.8	V
27	FOK	Maximum operating frequency	F4-1						O							V1 = 1.0Vpp	45	—	—	kHz
28	DFCT	High level output voltage	V5-1	O	O					43mV					15	V1 = 90mVpp f = 1kHz	1.8	—	—	V
29	DFCT	Low level output voltage	V5-2	O	O											V1 = 90mVpp f = 1kHz	—	—	–2	V
30	DFCT	Minimum operating frequency	F5-1	O	O											V1 = 90mVpp	–	—	1	kHz
31	DFCT	Maximum operating frequency	F5-2	O	O											V1 = 90mVpp	2	—	—	kHz
32	DFCT	Minimum operating input voltage	V5-3	O	O											f (V1) = 50Hz at RFO output voltage	—	—	0.5	Vpp
33	DFCT	Maximum operating input voltage	V5-4	O	O											f (V1) = 50Hz at RFO output voltage	1.8	—	—	Vpp
34	MIRR	High level output voltage	V6-1						O	–0.4V	–2.0V	0V	2.0V	0V	16	V1 = 0.8Vpp f = 10kHz	1.8	—	—	V
35	MIRR	Low level output voltage	V6-2						O	–0.4V						V1 = 0.8Vpp f = 10kHz	—	—	–2	V
36	MIRR	Bottom hold frequency response	F6-1						O	–0.2V						V1 = 0.8Vpp 55% AM modulation fcarrier = 500Hz	—	400	600	Hz
37	MIRR	Bottom hold frequency response	F6-2						O	–0.4V						V1 = 0.8Vpp	—	550	900	Hz
38	MIRR	Maximum operating frequency 1	F6-3						O							V1 = 0.8Vpp	30	—	—	kHz
39	MIRR	Maximum operating frequency 2	F6-4						O		2.0V	1.5V				V1 = 0.8Vpp	80	—	—	kHz
40	MIRR	Minimum operating input voltage	V6-3						O		–2.0V	0V				f (V1) = 10kHz	—	0.1	0.2	Vpp
41	MIRR	Maximum operating input voltage	V6-4						O							f (V1) = 10kHz	1.8	—	—	Vpp

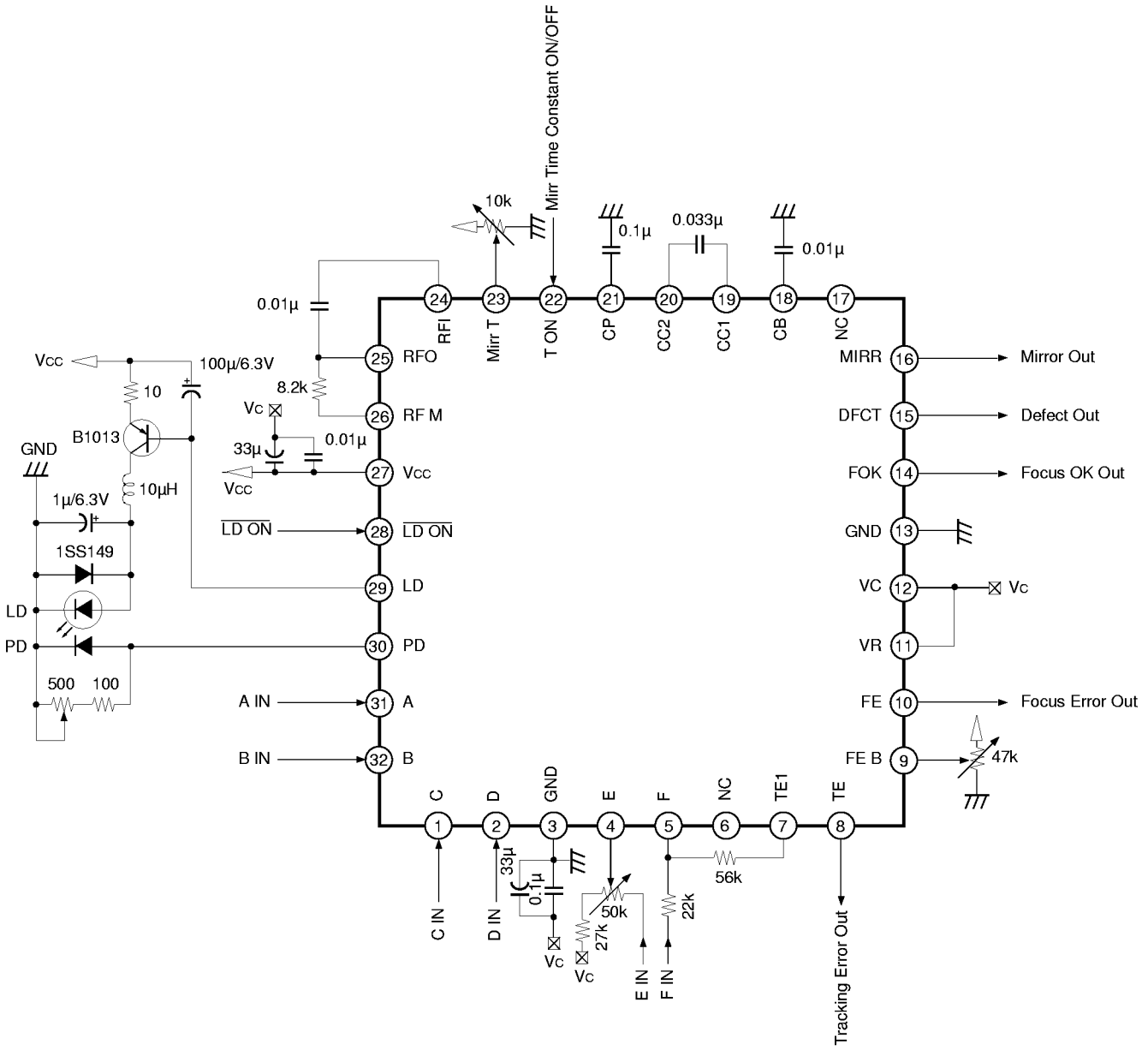
(Ta = +25°C, V_{CC} = +2.5V, GND = V_C, V_{EE} = –2.5V)

Measure-ment No.		Measurement Item	Symbol	SW Conditions						Bias Conditions					Measure-ment Point	Description of Output Waveform and Measurement Method	Max.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	E1	E2	E3	E4	E5						
42	APC	Output voltage 1	V7-1							0V	–2.0V	0V	–2.0V	69mV	29	DC voltage measurement	–	–1.6	–0.3	V
43	APC	Output voltage 2	V7-2											123mV		DC voltage measurement	–1.2	0.1	1.4	V
44	APC	Output voltage 3	V7-3											177mV		DC voltage measurement	0.8	2.1	–	V
45	APC	Output voltage 4	V7-4										2.0V	0V		DC voltage measurement	2.1	2.4	–	V
46	APC	Output voltage 5	V7-5										–2.0V			I1 = 0.8mADC DC voltage measurement	–	–	0	V
47	VC	Output voltage	V8-1					○					2.0V		11	DC voltage measurement	–0.1	–	0.1	V

Electrical Characteristics Measurement Circuit



Application Circuit

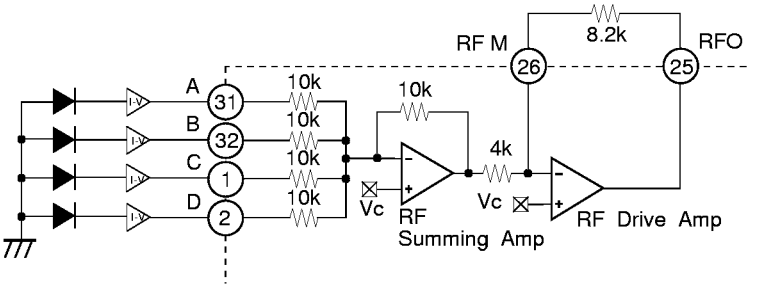


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

RF Amplifier

The signal currents from the photodiodes A, B, C and D are I-V converted, and input to Pins 1, 2, 31 and 32. These signals are added at the RF summing amplifier and inverted at the RF drive amplifier. Output is to Pin 25.



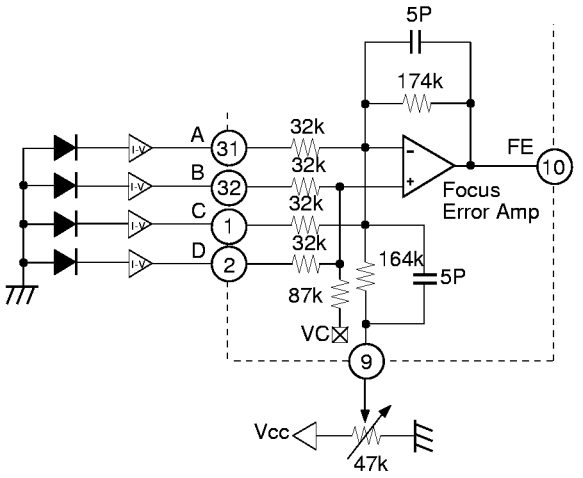
The low frequency component of RFO output voltage is as follows:

$$V_{RFO} = \frac{10k}{10k} \times \frac{8.2k}{4k} \times (A + B + C + D)$$

$$= 2.05 \times (A + B + C + D)$$

Focus Error Amplifier

The operation of (B + D) – (A + C) is performed and the resulting signal is output to Pin 10.



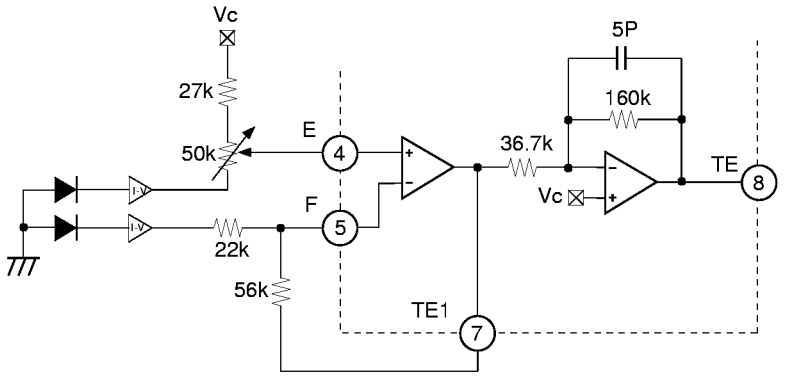
The low frequency component of FE output voltage is as follows:

$$V_{FE} = \frac{174k}{32k} \times (B + D - A - C)$$

$$= 5.43 \times (B + D - A + C)$$

Tracking Error Amplifier

The signal current from the photodiode F is I-V converted and input to Pin 5 via an input resistor. The signal current from the photodiode E is I-V converted, and input to Pin 4 after its gain is adjusted by the volume. These signals undergo operational amplification at the tracking error amplifier and tracking drive amplifier, and are output to Pin 8. The input resistance and feedback resistance of the tracking error amplifier are configured with external resistors, so that the absolute errors and deviations of temperature characteristics for IC internal/external resistors are independent of the gain.



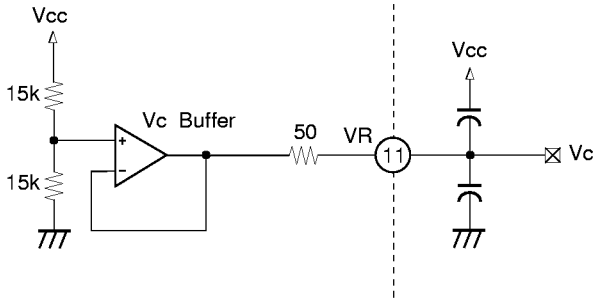
The low frequency component of TE output voltage is as follows:

$$V_{TE} = \frac{56k}{22k} \times \frac{160k}{36.7k} \times (F - E)$$

$$= 11.1 \times (F - E)$$

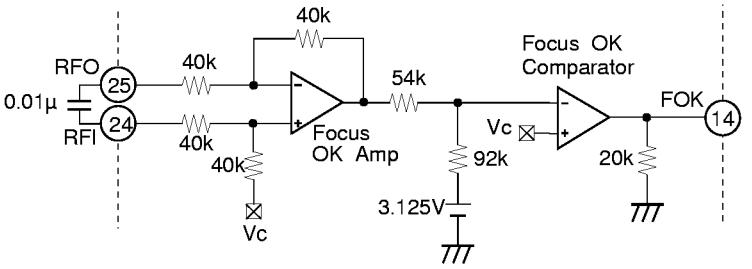
Center Voltage Generation Circuit

The center voltage of VR = (Vcc + GND) is supplied. The maximum current is approximately ±3 mA.



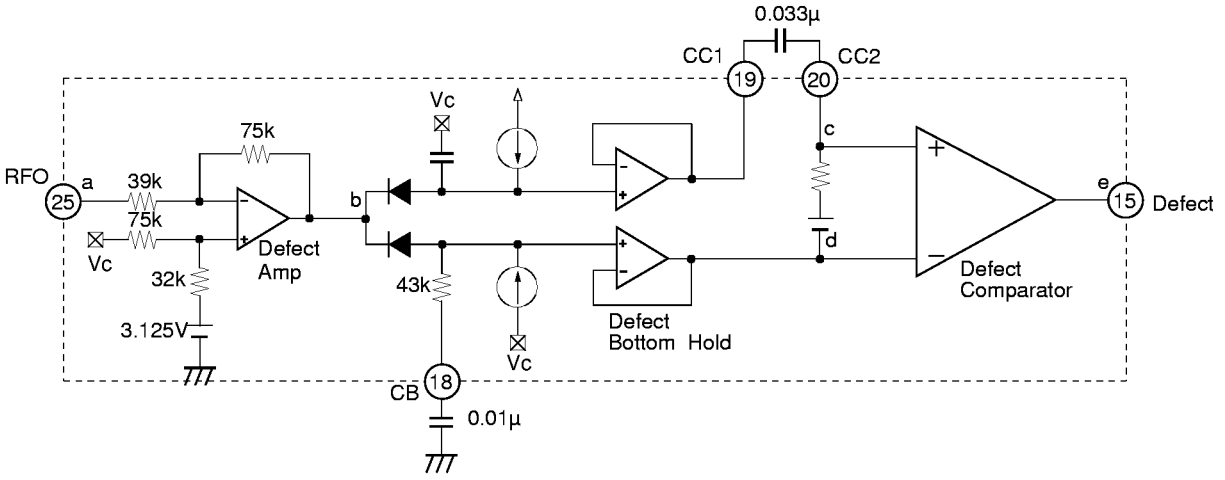
Focus OK Circuit

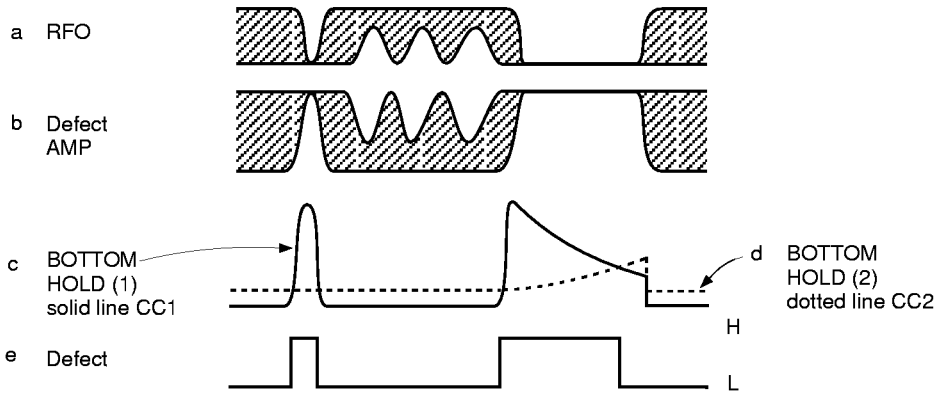
The focus OK circuit creates the timing window okaying the focus servo form the focus search state.
The low frequency component of RF can be get by obtaining the difference of the Pins 24 and 25 RF signals, whose low frequency components are removed, at the focus OK amplifier. The focus OK output is inverted when $V_{RFI} - V_{RFO} = -0.37V$. The capacitance between Pins 24 and 25 is used to determine the time constants of the mirror circuit HPF and the focus OK amplifier LPF. In normal use, with C equal to 0.01µF selected, fc is equal to 1kHz, and block error rate degradation can be prevented which is caused by RF envelope defects due to scratched discs.



Defect Circuit

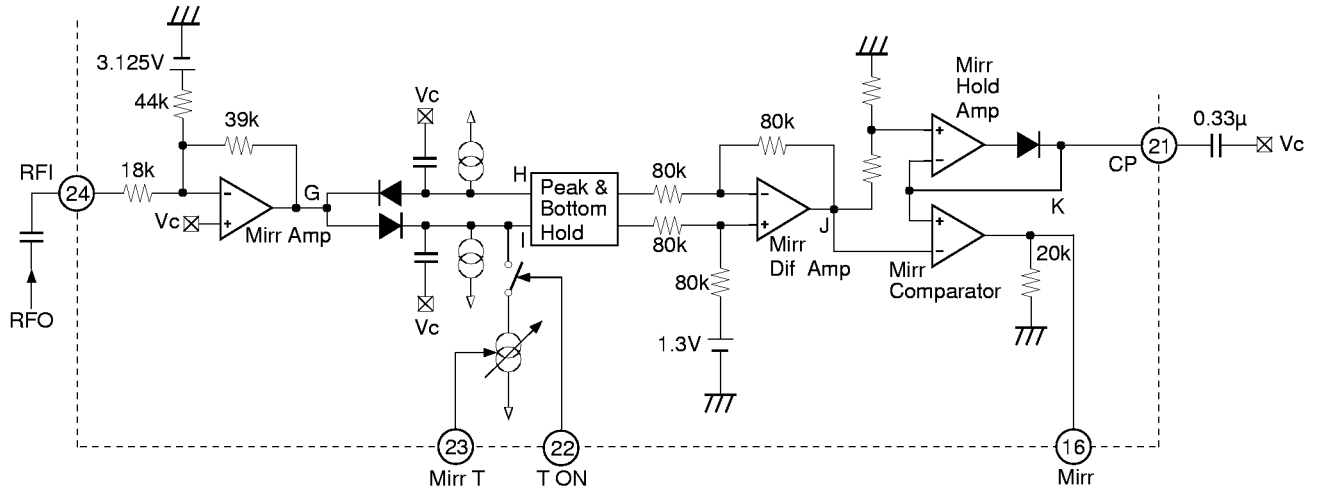
A bottom hold is performed on two time constants, long and short, after inversion of RFI signal. The mirror level is hold immediately prior to defect by short time constant bottom hold.The mirror defect detection signal is output by performing a differential + level shift with capacitor coupling and then comparing both signals.

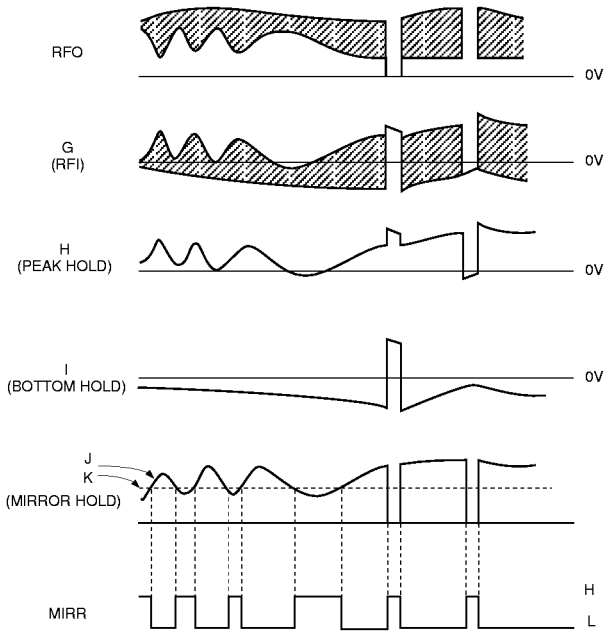


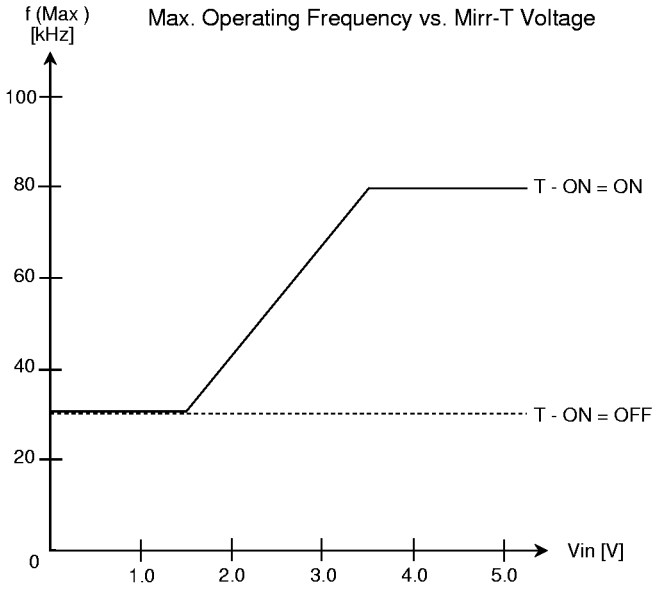


Mirror Circuit

Mirror circuit performs peak and bottom hold after RFT signal has been amplified. The peak hold is executed for Pin 22 with the time constant which follows the traverse signal of 30kHz for OFF (connection to GND) and maximum 80kHz (adjustable with DC voltage of Pin 23) for ON (connection to Vcc). The bottom hold is executed with the time constant which follows the rotation cycle envelope fluctuation.



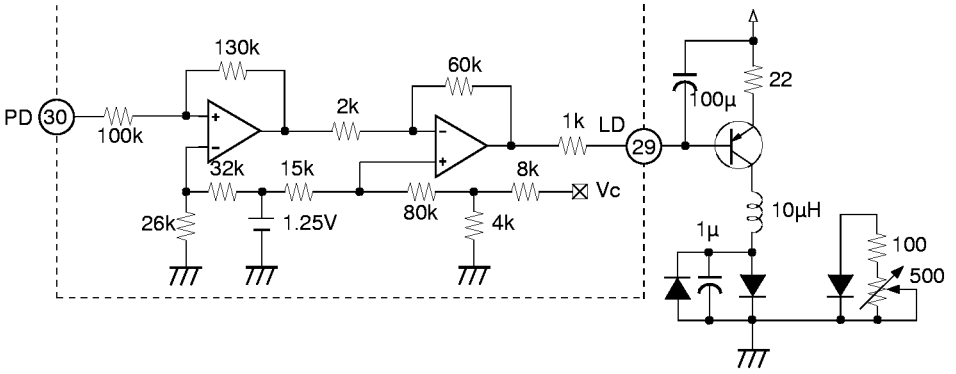




The mirror signal is output by comparing to the signal K (2/3 level of the J peak value which is peak-held with a large time constant) where the difference of hold signals H and I is obtained. The mirror output is low for tracks on the disc and high for the area between tracks (the mirror areas). In addition, a high signal is output when a defect is detected. The mirror hold time constant must be sufficiently large in comparison with the traverse signal.

APC Circuit

When the laser diode is driven with constant current, the optical output possesses large negative temperature characteristics. Therefore, the current must be controlled with the monitor photodiode to ensure the output remains constant. When $\overline{\text{LD ON}}$ pin is connected to GND, APC is ON; connected to Vcc, it is OFF.

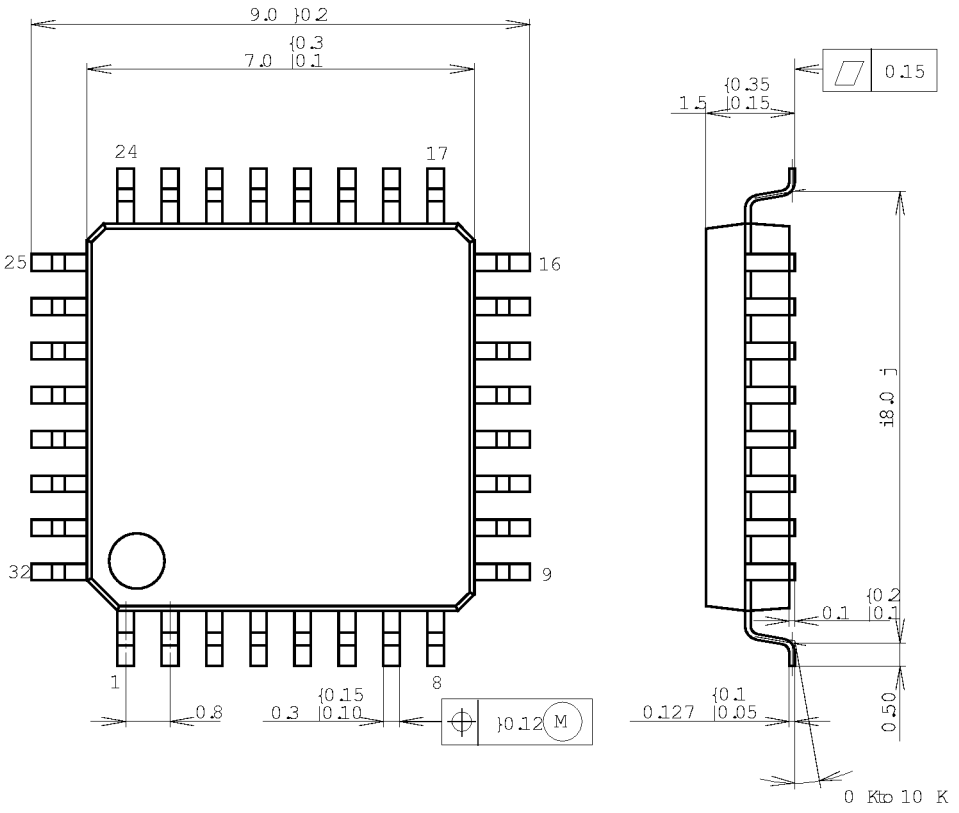


Notes on Handling

Care must be taken in handling because Pin 26 has low electrostatic strength of negative direction.

Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	*QFP032-P-0707-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42ALLOY
PACKAGE WEIGHT	0.2g