PD39208

PoE PSE Manager

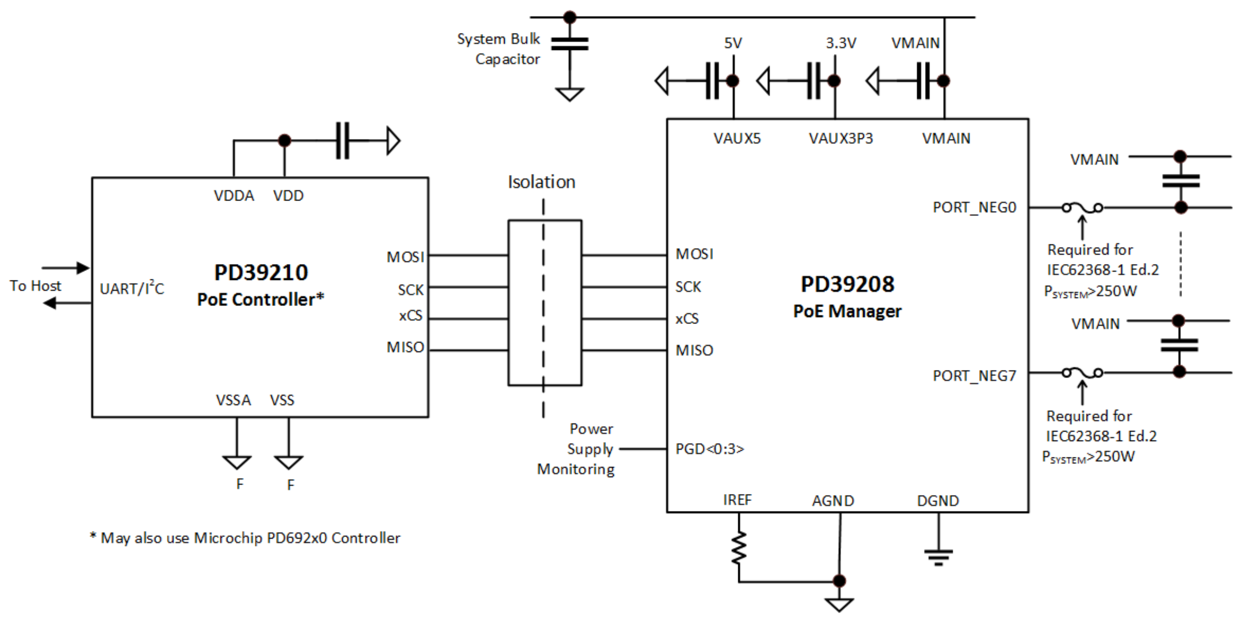
Introduction

Microchip's PD39208 Power over Ethernet (PoE) manager IC integrates power, analog, and state-of-the-art logic into a single 8 mm × 8 mm, 56-pin, plastic QFN package. The device, when used with the Microchip PD39210 PSE controller, is an optimized IEEE® 802.3af/at Power Sourcing Equipment (PSE) solution. The PD39208 may also be used with the Microchip PD692x0 family of PSE controllers or an Ethernet switch processor from a supported third-party vendor for 802.3af/at solutions.

Typical PoE Application

The following figure shows the typical PoE application of Microchip Generation 6 devices.

Figure 1. Typical PoE Application with Microchip Controller



Consult Microchip Designing an IEEE 802.3af/at PoE System Based on PD39208/PD39210.

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PoE Manager Features

- Optimized for use with PD39210 PSE controller
- Supports any Microchip PD692x0 controller
- Drives 2-pair power ports
- Single DC voltage input
- Built-in 3.3 V and 5 V regulators
- Over-temperature protection and thermal monitoring
- Low-power dissipation
- Industrial temperature range: –40 °C to 85 °C
- MSL3, RoHS compliant

Chipset Features

- Complies with IEEE 802.3af/at
- Cascade up to 6 PoE devices for 48 logical ports
- Advance system power management
- Emergency power management supporting 16 configurable power banks
- Continuous port monitoring and status
- Supports Fast and Perpetual PoE
- Supports pre-standard PD detection
- LED stream support
- Configurable load current setting
- Field upgradable

Applications

- PoE switches/routers/midspans
- Industrial automation
- Video recorders (NVR/DVR)

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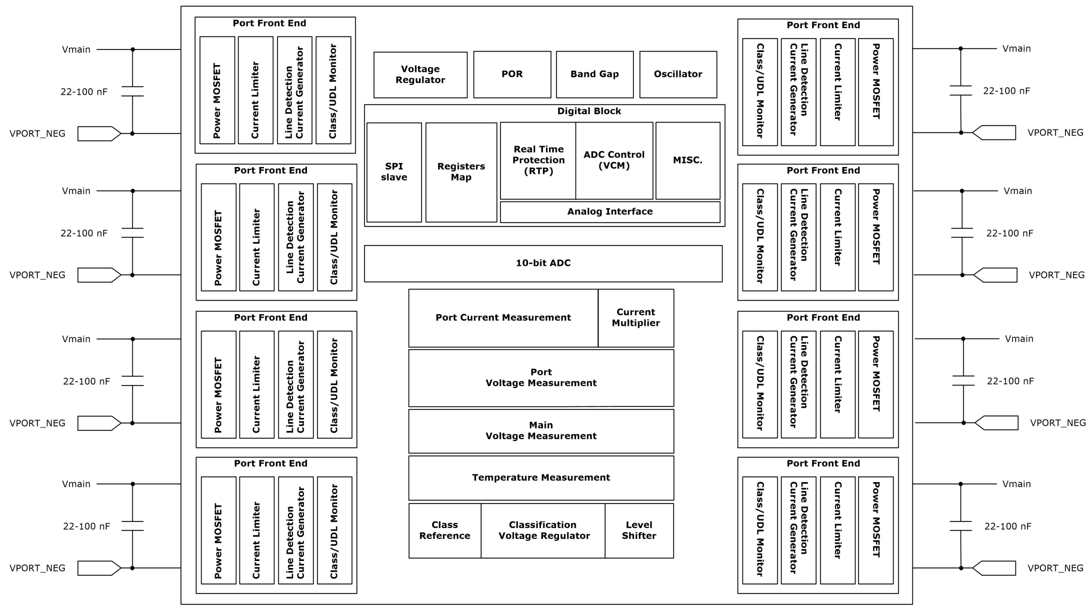
1. Functional Descriptions

The following figure shows the functional blocks of the PD39208.

Figure 1-1. PSE Manager Block Diagram



1.1 Digital Block Module

The logic main control block includes digital timing mechanisms and state machines that synchronize and activate PoE functions.

- Real-Time Protection
- Start-Up Macro
- Load Signature Detection
- Classification
- Voltage and Current Monitoring
- ADC interfacing
- Direct digital signals with analog block
- SPI communication block
- Registers

1.2 PD Detection Generator

On request from the controller to the main control module, the PD detection generator generates four different voltage levels to ensure a robust AF/AT PD detection functionality.

1.3 Classification Generator

On request from the controller to the main control module, state machine applies a regulated class event and mark event voltage to ports, as required by IEEE® standards.

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1.4 Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a pre-defined value set by AF/AT. When the current value exceeds this specific value, the system starts measuring the elapsed timing. If this interval is greater than a preset threshold, the port is disconnected.

1.5 Main Power MOSFET

The main power switching FET is used to control PoE current into the load.

1.6 10-Bit ADC

A 10-bit analog to digital converter (ADC) is used to convert analog signals into digital registers for the logic control module.

1.7 Power on Reset

Power on Reset (PoR) monitors the internal 3.3 V and 5 V DC levels. If this voltage drops below the specific thresholds, a reset signal is generated and the manager is reset.

1.8 Voltage Regulator

The voltage regulator generates 3.3 V and 5 V for internal circuitry.

1.9 Oscillator

The manager’s clock (CLK) is an internal 8 MHz clock oscillator.

1.10 SPI Communication

The managers use SPI communication in SPI slave mode to communicate with the MCU. Each manager has an address determined by ADDR0-ADDR3 pins. Addresses 0–11 are supported. The frequency between controller and manager ICs is 1 MHz.

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2. Electrical Specifications

This section describes the electrical specifications of the PD39208 device.

2.1 Absolute Maximum Ratings

PoE performance is not guaranteed when exceeding the recommended rating. Exposure to any stress in the range between the recommended rating, as listed in the following table, and the absolute maximum rating should be limited to a short time. Exceeding these ratings may impact long-term operating reliability.

Table 2-1. Absolute Maximum Ratings

Parameters	Min	Max	Units
Supply input voltage (V_{MAIN})[1,2]	–0.3	72	V
PORT_NEG[0.7]pins	–0.3	V_{MAIN} +0.5	V
V_{AUX5}	–0.3	6	V
V_{AUX3P3},DV_{DD}	–0.3	4	V
Digital pins: MISO, MOSI, SCK, CS_N, ADDR[3:0], PGD[3:0], RESET_N, TRIM	–0.3	DV_{DD}+0.3 and <4.0	V
Absolute maximum junction temperature		150	°C
Lead soldering temperature (40 s, reflow)		260	°C
Storage temperature	–65	150	°C

1. Power sequence requirement: V_{MAIN} > V_{AUX5} > V_{AUX3P3} = TRIM, DVDD.
2. EPAD is connected by copper plane on PCB to AGND. AGND is ground for IC.

Note: DRV_VAUX5 and IREF are output pins and should not apply voltage or current. DRV_VAUX5 can be left open when not used.

2.2 Recommended Operating Conditions

Table 2-2. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Maximum junction operating temperature					125	°C
V_{MAIN}	Main supply voltage	Supports full IEEE 802.3af/at functionality	44		57	V

2.3 Immunity

Table 2-3. Immunity

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ESD	ESD rating	HBM[1]	–2000		+2000	V
		CDM[2]	–500		+500	V
Surge	Lightning surge[3]	EN61000 4-5	–1		1	kV

1. ESD HBM complies with JESD22 Class 2 standard.
2. ESD CDM complies with JESD22 Class 1 standard.
3. System-level common mode 10/700 µs according to IEC61000-4-5.

2.4 Device Electrical Specifications

If not specified under conditions, the Min and Max ratings stated in the following table apply to the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25 °C ambient.

Table 2-4. Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PORT}	Port output	V_{MAIN}–V_{PORT_NEGx}	0		57	V
V_{TH}	POR threshold	Internal or external 3.3 V supply		8		V
I_{MAIN}		Main power supply current at operating mode. V_{MAIN} = 55 V		14		mA
V_{AUX5}	5 V output voltage	V_{AUX5}–AGND	4.5	5	5.5	V
V_{AUX3P3}	Internal 3.3 V output voltage	V_{AUX3P3}–AGND	3	3.3	3.6	V
I_{AUX3P3}	3.3 V output current for application use	Without external NPN			5	mA
		With external NPN transistor on V_{AUX5}			30	mA
V_{AUX3P3_IN}	3.3 V input voltage	V_{AUX3P3}–AGND	3	3.3	3.6	V
DV_{DD}	Digital 3.3 V input voltage	DV_{DD}–DGND	3	3.3	3.6	V
POR_{TP}	Power-on reset DVDD trip point	DV_{DD}–DGND	2.575	2.775	2.975	V
POR_{HYS}	Power-on reset DVDD hysteresis	POR_{TP}–DGND	0.2	0.25	0.3	V
R_{CH_ON}	Total channel resistance	R_{ds_on} + R_{sense} + $R_{bonding}$		0.34		Ω
PPWR	Port power accuracy	30 W			5	%

2.5 Port Real-Time Protection

Table 2-5. Port Real-Time Protection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{RISE}	Turn-on rise time	From 10% to 90% of the voltage difference at the VPORT_NEGx in POWER_ON state from the beginning of POWER_UP	15			µs
I_{INRUSH}	Output current in POWER_UP state	CLOAD ≤ 180 µF[1]	400	425	450	mA
T_{INRUSH}	Inrush time				65	ms
I_{PORT}	Output operating current	802.3af	10		360	mA
		802.3at	10		620	mA
I_{CUT}	Overload current	802.3af		375		mA
		802.3at		645		mA
T_{CUT}	Overload time limit		62	64	66	ms

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Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
I_{LIM}	Port current limit	802.3af	400	425	450	mA
		802.3at	790	850	892	mA
T_{LIM}	Port current limit time	$V_{MAIN}–V_{PORT\_NEGx}$ <30 V	1	2	3	ms
I_{UDL}	DC disconnect under-load current	2 pairs	6	7.5	9	mA
T_{MPDO}	PD maintain power signature dropout time limit		322	324	326	ms
T_{MPS}	PD maintain power	802.3at	46	48	50	ms
T_{OFF}	Turn off time	From V_{MAIN} to 2.8 V			500	ms

1. Can be overridden by communication command.

2.6 Port Current Monitoring

Table 2-6. Port Current Monitoring

Symbol	Conditions	Typ	Max	Units
Resolution	Reported as 14 bits	10		Bits
LSB		122.07		µA
Measurement period		16		mS
Accuracy	50 mA < I_{PORT} < 150 mA		9	%
	150 mA < I_{PORT} < 350 mA		4.5	%
	350 mA < I_{PORT} < 600 mA		3.5	%

2.7 Port Voltage Monitoring

Table 2-7. Port Voltage Monitoring

Symbol	Conditions	Typ	Max	Units
Resolution		10		Bits
LSB		58.6		mV
Measurement period		3		ms
Accuracy			3.3	%

2.8 Main Voltage Monitoring

Table 2-8. Main Voltage Monitoring

Symbol	Conditions	Typ	Max	Units
Resolution		10		Bits
LSB		58.6		mV
Measurement period		3		ms

...........continued				
Symbol	Conditions	Typ	Max	Units
Accuracy	42 V < V_{MAIN} < 50 V		3.0	%
	50 V < V_{MAIN} < 57 V		2.2	%

2.9 Temperature Monitoring

Table 2-9. Temperature Monitoring

Symbol	Conditions	Min	Typ	Max	Units
Resolution			8		Bits
LSB	Temperature = (DATA x 1.9384)–277		1.9384		°C
Measurement period			3		ms
Accuracy		–3		3	°C

2.10 Digital Interface

Table 2-10. Digital Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input logic high voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	2.2			V
V_{IL}	Input logic low voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]			0.8	V
Hyst	Input logic hysteresis voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	0.4	0.6	0.8	V
I_{IH}	Input logic high current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	–10		10	µA
I_{IL}	Input logic low current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	–10		10	µA
V_{OH}	Output logic high voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I_{OH} = –1 mA	2.4			V
V_{OL}	Output logic low voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I_{OH} = 1 mA			0.4	V

2.11 Detection

Table 2-11. Detection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OC}	Pre-detection voltage, open-circuit voltage	V_{MAIN}–V_{PORT_NEGx}, open port			7.8	V

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Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
V_{VALID}	Detection voltage	V_{MAIN}–V_{PORT_NEGx}, for IEEE 802.3 compliant signature resistance (RSIG <33 K)			9.3	V
I_{SC}	Short circuit current	V_{MAIN}–V_{PORT_NEGx} = 0 V		388	408	µA
R_{SIG_LOW}	Minimum valid detection resistance		15		19	kΩ
R_{SIG_HIGH}	Maximum valid detection resistance		26.5		33	kΩ

2.12 Classification

Table 2-12. Classification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CLASS}	Class event output voltage	V_{MAIN}–V_{PORT_NEGx}; 0 mA ≤ I_{PORT} ≤ 50 mA	15.5	18	20.5	V
V_{MARK}	Mark event output voltage	V_{MAIN}–V_{PORT_NEGx}; 0.1 mA ≤ I_{PORT} ≤ 5 mA	7	8.5	10	V
I_{CLASS_LIM}	Class event current limitation	V_{MAIN}–V_{PORT_NEGx} = 0 V	51	70	100	mA
$I_{MARK\_ LIM}$	Mark event current limitation	V_{MAIN}–V_{PORT_NEGx} = 0 V	51	70	100	mA
	Classification current thresholds	Class 0	0		5	mA
		Class 1	8		13	mA
		Class 2	16		21	mA
		Class 3	25		31	mA
		Class 4	35		45	mA
		Class Error	51		100	mA

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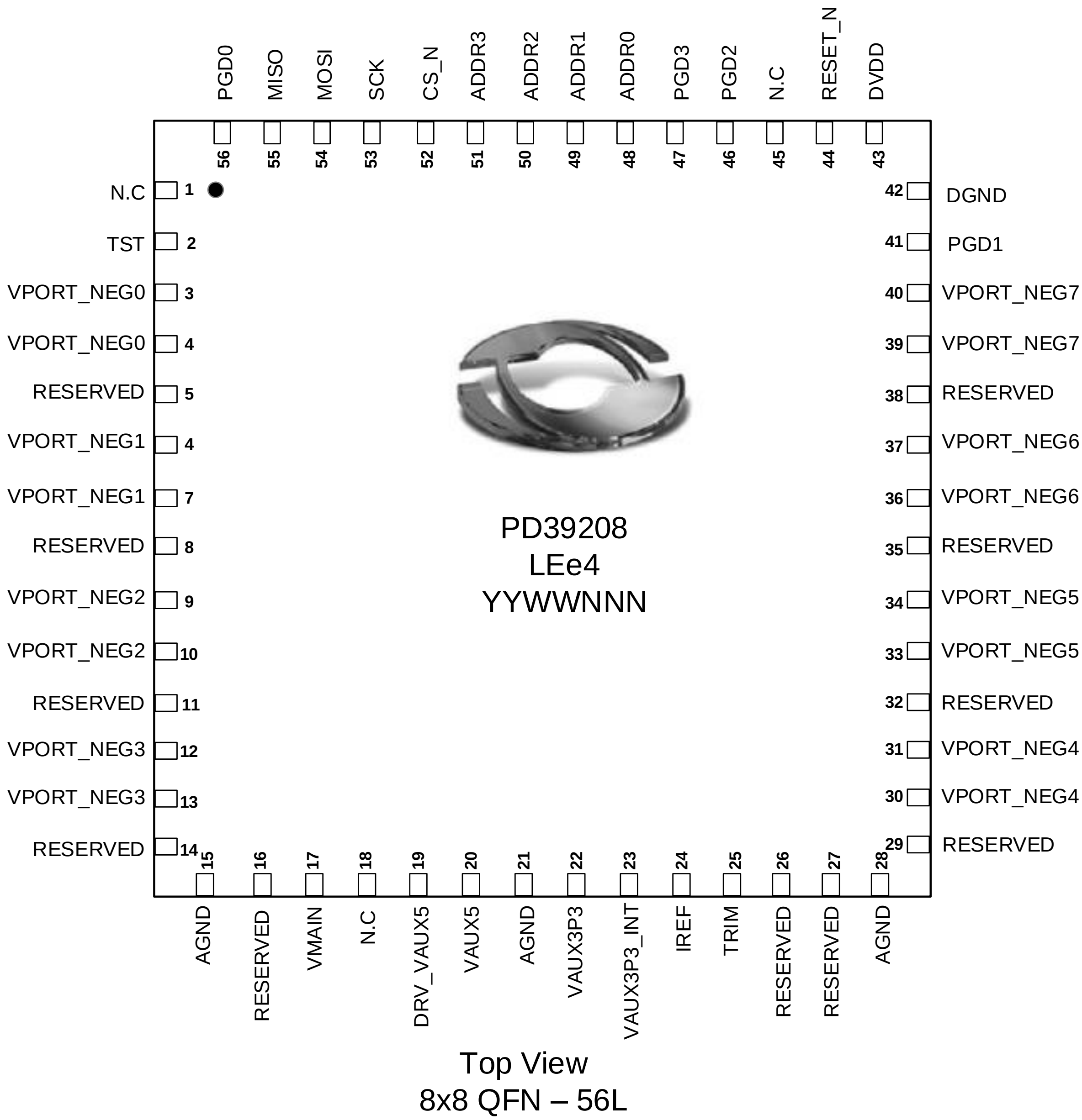
3. Pins

This section provides pin diagrams and pin descriptions for the PD39208 device.

3.1 Pin Diagrams

Figure 3-1. Pin Diagram Top View



3.2 Pin Descriptions

The following table describes the functional pins of the PD39208 manager.

Table 3-1. Pin Descriptions

Pin	Designator	Type	Description
	EPAD		Exposed PAD. Connect to analog ground. GND must have sufficient copper mass on bottom or top layer to ensure adequate thermal performance.
1,18,45	N.C.	N/A	Not connected. Leave floating.
2	TST	Digital input	Test pin for production use only. Connect to DGND.
3,4	VPORT_NEG0	Analog I/O	Negative port 0 output.
5,8,11, 14,16, 26,27, 29,32, 35,38	RESERVED	N/A	Reserved pin. Do not connect externally.
6,7	VPORT_NEG1	Analog I/O	Negative port 1 output.
9,10	VPORT_NEG2	Analog I/O	Negative port 2 output.
12,13	VPORT_NEG3	Analog I/O	Negative port 3 output.
15,21,28	AGND	Power	Analog ground.
17	VMAIN	Power	Main high voltage supply voltage. A low ESR 1 μF (or higher) bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces.
19	DRV_VAUX5	Power	Driven outputs for 5 V external regulation; if internal regulation is used, connect to pin 20. If an external NPN is used to regulate the voltage, connect this pin to Base and connect 4.7 μF capacitor between this pin and AGND.
20	VAUX5	Power	Powered by regulated 5 V. Connect 4.7 μF or higher capacitor between this pin and AGND. If an external NPN is used to regulate the voltage, connect this pin to the emitter. The collector should be connected to V_{MAIN}.
22	VAUX3P3	Power	Powered by regulated 3.3 V. A 4.7 μF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3 V regulator is used, connect it to this pin to supply the chip.
23	VAUX3P3_INT	Power	Connected to V_{AUX3P3} (pin 22) if internal 3.3 V regulator is used. Leave unconnected (Floating) if external 3.3 V regulator is used.

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Pin	**Designator**	**Type**	**Description**
24	IREF	Analog input	Reference resistor pin. Connect a 28.7 kΩ 1% resistor to AGND.
25	TRIM	Test input	Test input pin. Keep connected to V_{AUX3P3}.
30,31	VPORT_NEG4	Analog I/O	Negative port 4 output.
33,34	VPORT_NEG5	Analog I/O	Negative port 5 output.
36,37	VPORT_NEG6	Analog I/O	Negative port 6 output.
39,40	VPORT_NEG7	Analog I/O	Negative port 7 output.
41	PGD1	Digital input	Power good input from the system power supply.
42	DGND	Power	Digital ground.
43	DVDD	Power in	Regulated 3.3 V for digital circuitry. Connect voltage from pin V_{AUX3P3} or from external power supply source if used. A 1 μF or higher filtering capacitor should be connected between this pin and DGND.
44	RESET_N	Digital input	Reset input - active low (0 = reset). An external 10 kΩ pull-up resistor should be connected between this pin and DV_{DD}.
46	PGD2	Digital input	Power good input from the system power supply.
47	PGD3	Digital input	Power good input from the system power supply.
48	ADDR0	Digital input	SPI address bit 0 to set chip address.
49	ADDR1	Digital input	SPI address bit 1 to set chip address.
50	ADDR2	Digital input	SPI address bit 2 to set chip address.
51	ADDR3	Digital input	SPI address bit 3 to set chip address.
52	CS_N	Digital input	SPI bus, chip select.
53	SCK	Digital input	SPI bus, serial clock input.
54	MOSI	Digital input	SPI bus, master data out/slave in.
55	MISO	Digital output	SPI bus, master data in/slave out.
56	PGD0	Digital input	Power good input from the system power supply.

An adequate ground plane on a bottom or top layer is required for adequate thermal performance. See Designing an IEEE 802.3af/at PoE System Based on PD39208/PD39210 for additional details.

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4. Application Information

This section describes the application information of the PD39208 device.

4.1 PD Detection

The PD detection feature detects a valid IEEE 802.3af or IEEE 802.3at powered device. The PD detection is done based on four different voltage levels to ensure robust detection, as shown in the Typical IEEE 802.3at Port PoE Voltage Diagram.

4.2 Legacy Detection

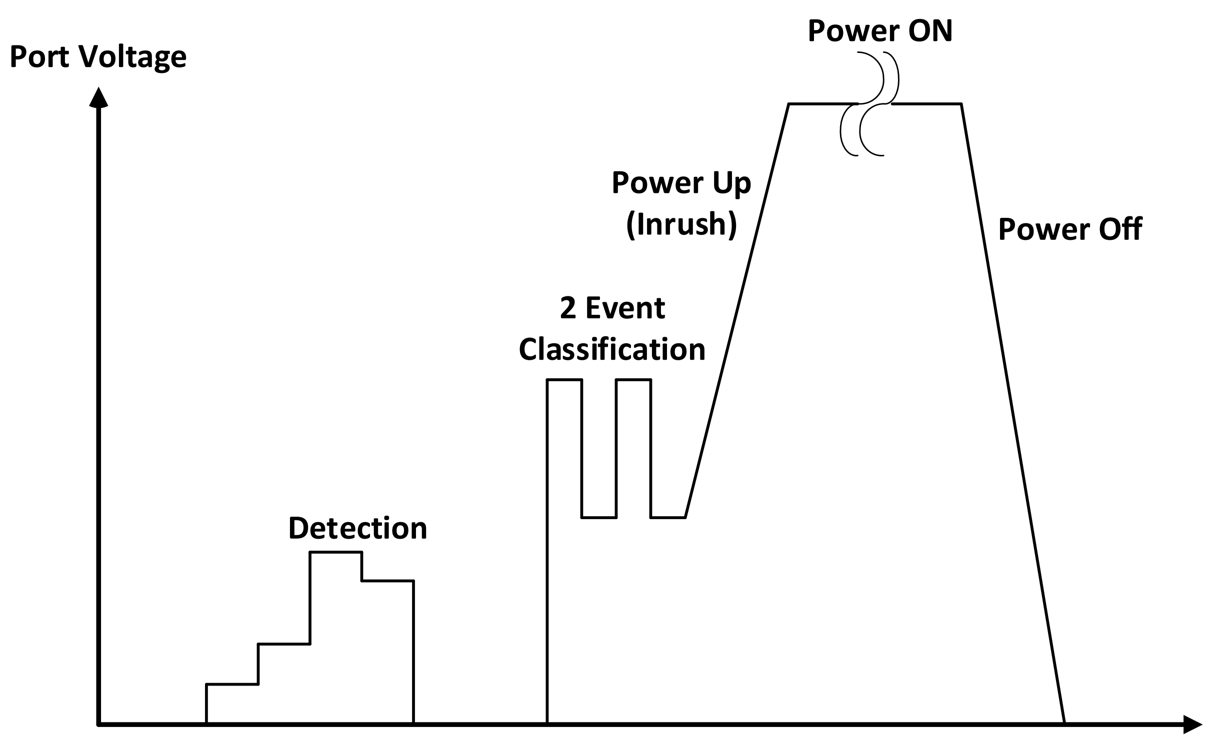
When legacy detection is enabled, the PD detection mechanism detects and powers up the legacy and pre-standard PDs as well as IEEE 802.3af and IEEE 802.3at standard compliant PDs (Classes 0–4).

4.3 Classification

The classification process takes place immediately after PD detection is successfully completed. The goal of the classification process is to detect PD class as specified in IEEE 802.3 standards.

In IEEE 802.3af mode, the classification mechanism is based on a single voltage level (single event). In IEEE 802.3at mode, the classification mechanism is based on two voltage levels (multiple events). The following figure shows the steps required for power-up, actual implementation may vary.

Figure 4-1. Typical IEEE 802.3at Port PoE Voltage Diagram



4.4 Port Start-Up

Upon a successful detection and classification process, power is applied to the load through a controlled start-up mechanism.

During this period, inrush current is limited to ILIM for a duration of TLIM (as specified in the table Port Real-Time Protection), which allows PD load to charge and allows a steady state of power condition.

4.5 Over-Load Detection and Port Shut-Down

After power-up, the PSE manager automatically initializes its internal protection mechanisms. These mechanisms are used to monitor and disconnect power from the PD when extreme conditions occur. These conditions include over-current or short ports terminals scenarios.

4.6 Disconnect Detection

The managers support the DC disconnect function as per IEEE 802.3 standards. This mechanism continuously monitors load current and disconnects power according to IUDL, TMPDO, and TMPS parameters as specified in Port Real-Time Protection.

4.7 IC Thermal Monitoring

The managers contains a thermal sensor that is sampled by the controller so that the manager die temperature is monitored at all times. To protect the PSE manager from damage, the system ports are disconnected before damage can occur.

A temperature alarm threshold can be set by the controller to send interrupt indication by the xINT_OUT pin before ports are disconnected. The temperature can be read and monitored by the host as well if required.

4.8 Over-Temperature Protection

In addition to the die thermal sensor, there are thermal sensors on each MOSFET that continuously monitors each port main MOSFETs junction temperature and shuts down the port load power when the temperature exceeds the threshold.

4.9 V_{MAIN} Out-of-Range Protection

The system automatically disconnects ports power when V_{MAIN} exceeds the pre-configured over-voltage and under-voltage thresholds.

4.10 2-Pair Ports

Operation modes include the following:

- PoE Type 1/2 class 0–4 (up to 30 W)

4.11 Port Power Limit

Port power limit (PPL) is used to configure port power limit. When a port exceeds the power limit, it gets disconnected automatically.

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4.12 Port Matrix Control

Port matrix control enables layout designers to ascribe each physical port in the system to a logical port if required.

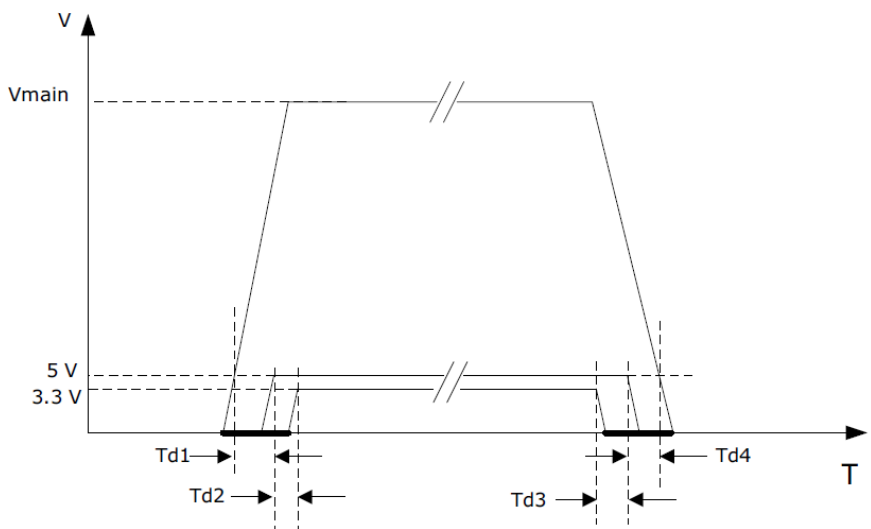
4.13 Power Good Interrupt

Interrupt from power supply directly to the manager. For systems comprising more than a single power supply, in case one power supply fails, a port shutdown mechanism is executed to maintain operation and prevent the collapse of other power supplies.

When a function is used, PGD0, PGD1, PGD2, and PGD3 should be connected to the main power supplies status indication pin. Any change of at least 1 µs on these lines triggers a pre-defined disconnection matrix. This matrix is defined by the PSE controller system power parameters. The port shutdown function reacts within 2 µs to any power good event.

4.14 Power Sequencing

Figure 4-2. Power Sequencing



For proper operation, ensure that V_{MAIN} is always the highest voltage connected to the IC.

With an external 5 V and/or 3.3 V supply:

- V_{aux5} pin voltage should never be above V_{MAIN} pin voltage.
- V_{aux3p3} pin voltage should never be above V_{aux5} pin voltage.
- The maximum 3.3 V slew rate is 100 ms.
- Td1: V_{MAIN} should be raised before or at the same time as 5 V.
- Td2: 5 V should be raised before or at the same time as 3.3 V.
- Td3: 3.3 V should be dropped before or at the same time as 5 V.
- Td4: 5 V should be dropped before or at the same time as V_{MAIN}.

For details about PD39208 5 V and 3.3 V power supply connection options, see *AN3615 Designing an IEEE® 802.3af/at PoE System Based on PD39210 + PD39208 Chipset*.

4.15 Ground

The digital ground and analog ground should be tied together on the board in a single point only for the entire system.

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4.16 Voltage Regulator

The voltage regulator generates 3.3 V and 5 V for internal circuitry. These voltages are derived from V_{MAIN} supply. To use the internal voltage regulator connect:

- V_{AUX5} to DRV_VAUX5
- V_{AUX3P3} to VAUX3P3_INT

There are three options to reduce the managers' power dissipation by regulating voltage outside the chip.

- Use an external NPN transistor to regulate the 5 V. In this setup, the configuration of regulators pins should be as follows.
  - DRV_VAUX5 is connected to NPN BASE
  - V_{AUX5} is connected to NPN EMITTER (Connect Collector to V_{MAIN})
  - V_{AUX3P3} is connected to VAUX3P3_INT
- Supply the manager with an external 5 V voltage regulator. In this setup, regulators pins configuration should be as follows.
  - V_{AUX3P3} is connected to VAUX3P3_INT
  - DRV_VAUX5 is not connected (left open)
  - V_{AUX5} is connected to external 5 V
- Supply the manager with an external 3.3 V voltage regulator. In this setup, regulators pins configuration should be as follows.
  - V_{AUX5} is connected to DRV_VAUX5
  - VAUX3P3_INT is not connected (left open)
  - V_{AUX3P3} is connected to external 3.3 V

4.17 SPI Communication

The following table lists the SPI communication packet structure.

Table 4-1. SPI Communication—Packet Structure

Control Byte Selects Manager According to Address	R/W Bit	Internal Register Address	Number of Words (Read Access Only)	Data Written to IC (Write Access Only) Read from IC (Read Access Only)
8 bits	R(0)/W(1)	8 bits	8 bits	16 bits

4.17.1 SPI Addressing

The manager operates in the 8-bit address and 16-bit data. It responds to SPI transaction if the first SPI byte (IC address byte bits[7:1]) complies with the following.

Table 4-2. Manager SPI Addressing

3 Bits (bit 7:5)	4 Bits (bit 4:1)	1 Bit (bit 0)
000	Address Input Pin	Read/Write

4.17.2 Broadcast

A broadcast command is intended to instruct all connected manager ICs to perform a specific operation.

The broadcast command is a write command with the standard packet structure. In a broadcast read operation, the read data is not valid and the read operation has no impact.

Table 4-3. Manager Broadcast

3 Bits (bit 7:5)	4 Bits (bit 4:1)	1 Bit (bit 0)
001	0000	Write

Figure 4-3. SPI Timing Diagram

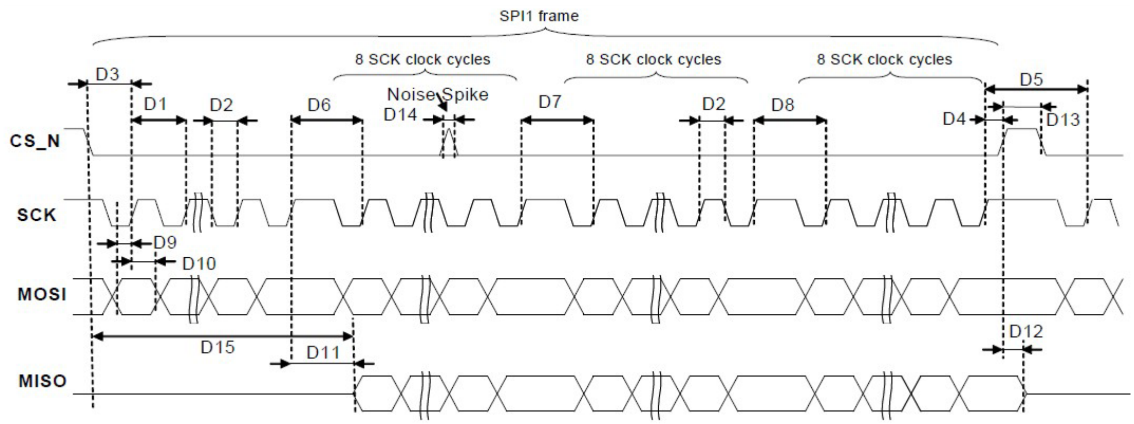


Table 4-4. SPI Timing Diagram Description

Name	Min Delay	Max Delay	Description
D1	910 ns		SPI clock period
D2	45%	55%	SPI duty cycle
D3	340 ns		SPI_CS setup to SPI clock positive edge (delay after SPI_CS active signal)
D4	340 ns		SPI_CS hold to SPI clock positive edge (delay before SPI_CS inactive signal)
D5	2 SPI clock cycles		Delay between last SCK in SPI1 frame and first SCK at adjacent SPI1 frame
D6	1 SPI clock cycle		Between byte 0 (IC address) and byte 1 (address)
D7	1 SPI clock cycle		Between byte 1 (address) and byte 2 (data)
D8	1 SPI clock cycle		Between byte 2 (MS data byte) and byte 3 (LS data byte)
D9	340 ns		MOSI setup time
D10	340 ns		MOSI hold time
D11		700 ns	MISO tri-state to valid data from clock positive edge
D12		700 ns	MISO valid data to tri-state from SPI_CS positive edge
D13	1 SPI clock cycle		SPI_CS width (Delay SPI1 frame to adjacent SPI1 frame)
D14		60 ns	Filtered glitch width
D15		D3 + D11 + 24 SPI clock cycles	MISO tri-state from SPI_CS negative edge to valid data
D16	200 ns		MISO setup to SCK positive edge
D17	200 ns		MISO hold to SCK positive edge

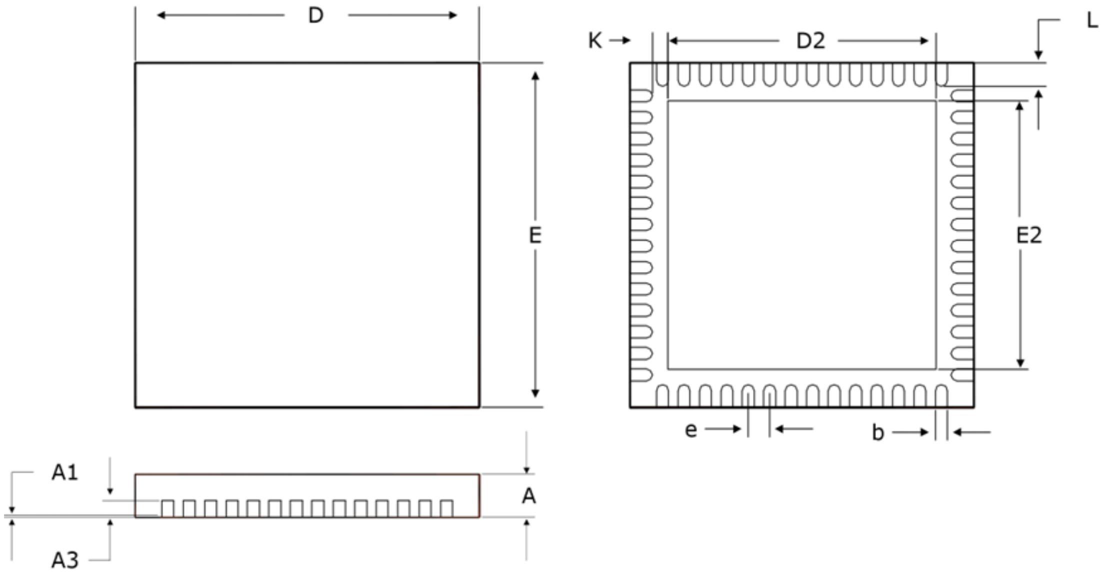
5. Package Information

This section describes the package of the PD39208 device.

5.1 Package Outline Drawing

The following figure shows the package drawing of the PD39208 device.

Figure 5-1. PD39208 Package Drawing (56-Pin QFN 8 mm × 8 mm)



The following table lists the dimensions and measurements of the PD39208 package.

Table 5-1. Package Outline Dimensions and Measurements

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note: Dimensions do not include protrusions; they should not exceed 0.155 mm (0.006 in.) on any side. Lead dimension should not include solder coverage. Dimensions are in millimeters and inches for reference.

5.2 Thermal Specifications

The following tables list the thermal specifications the PD39208 device.

Table 5-2. Thermal Specifications

Thermal Resistance	Typ	Units	Notes
θ_{JA}	19.0	°C/W	Junction-to-ambient thermal resistance.
Ψ_{JT}	0.05	°C/W	Junction-to-top thermal characterization parameter. A thermal metric derived from the difference in junction temperature (TJ) and package top temperature (TT) divided by total heating power (PH).
$\theta_{JC(top)}$	4.9	°C/W	Junction-to-case thermal resistance with heat flow through package top.
θ_{JB}	15.2	°C/W	Junction-to-board thermal resistance.

Note: All parameters are as per JEDEC JESD-51.

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5.3 Recommended PCB Layout

The following figures show the recommended PCB layout for a PD39208 56-pin QFN 8 mm × 8 mm package. Units are in mm (mils).

Figure 5-2. Top-Copper Layer

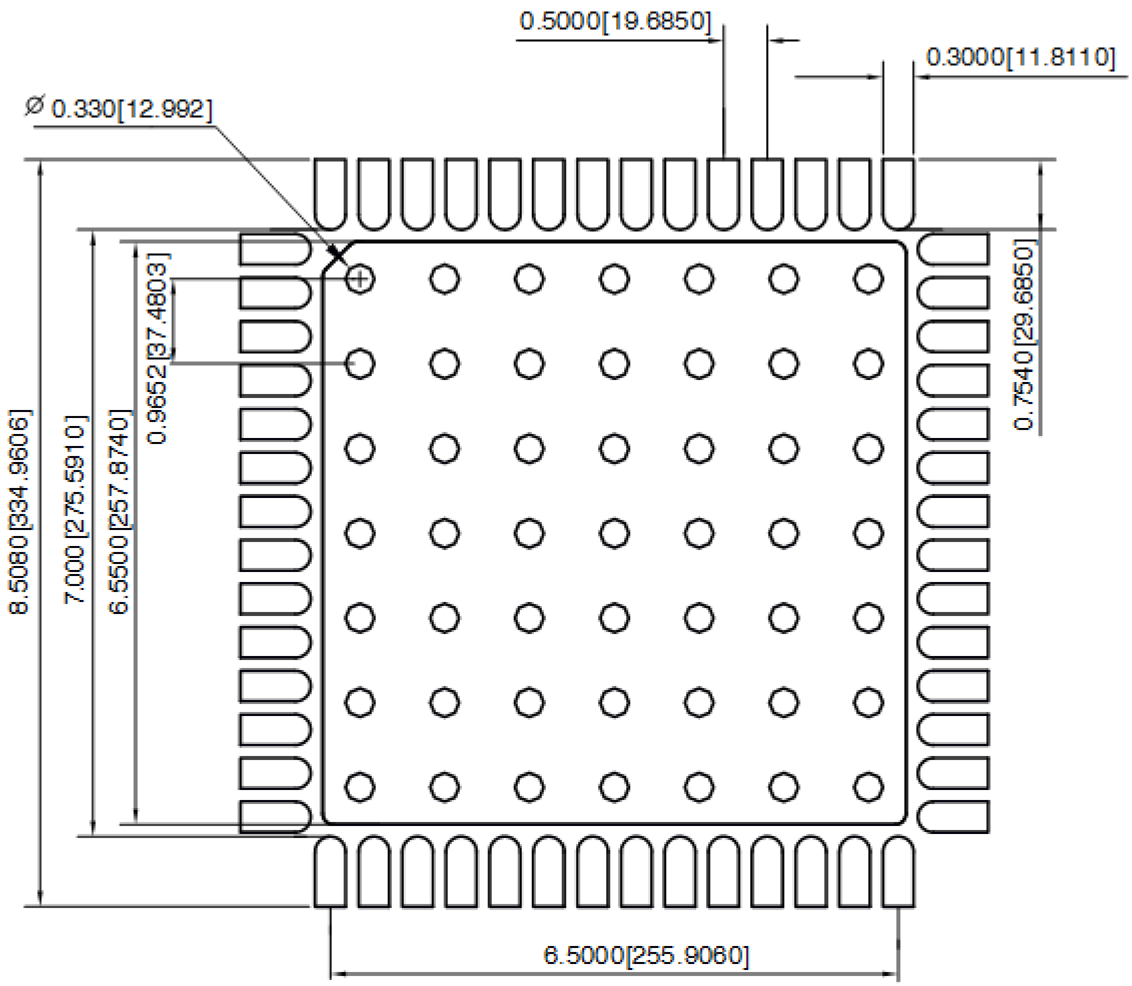


Figure 5-3. Top-Solder Paste Layer

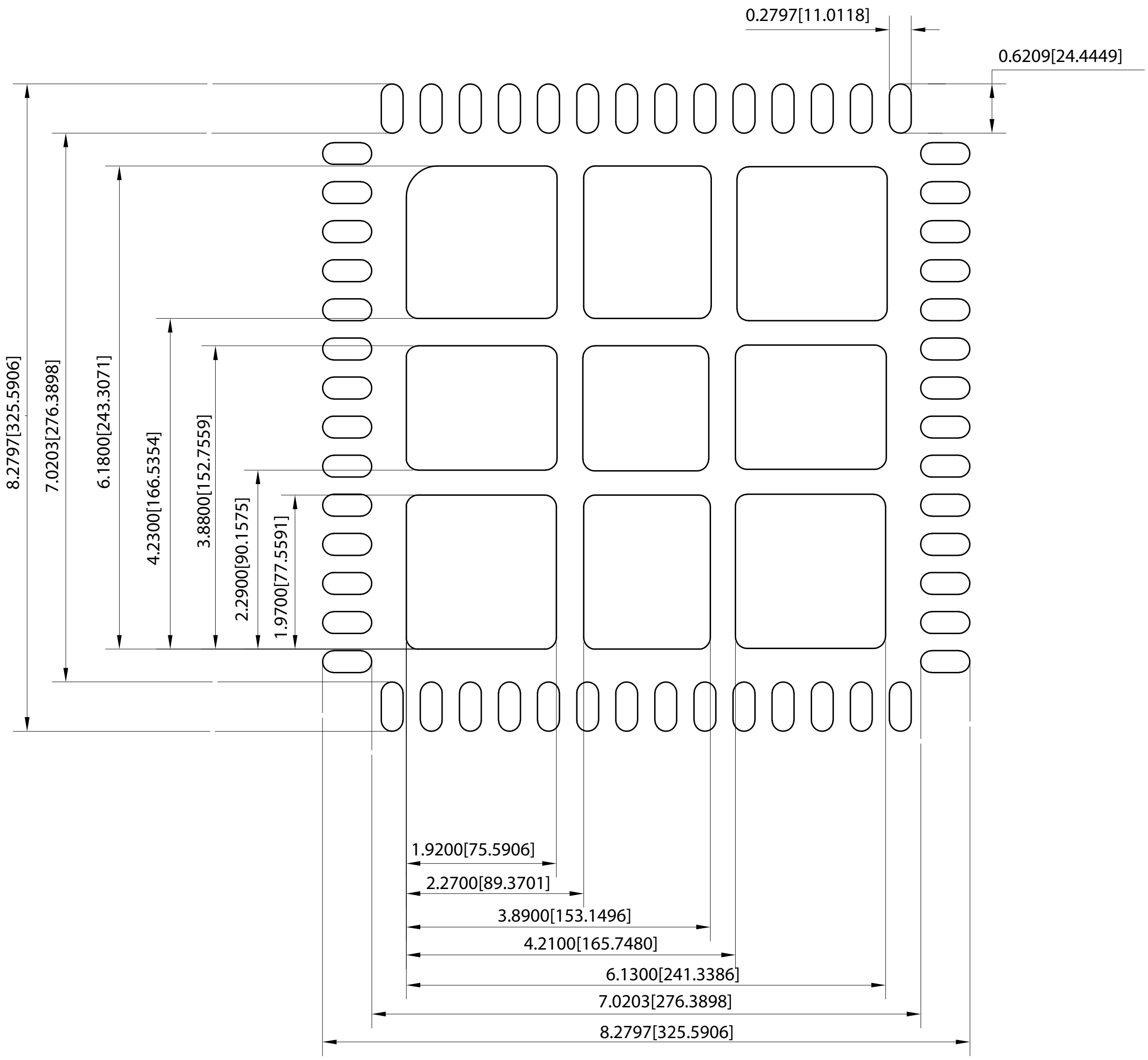


Figure 5-4. Solder Mask

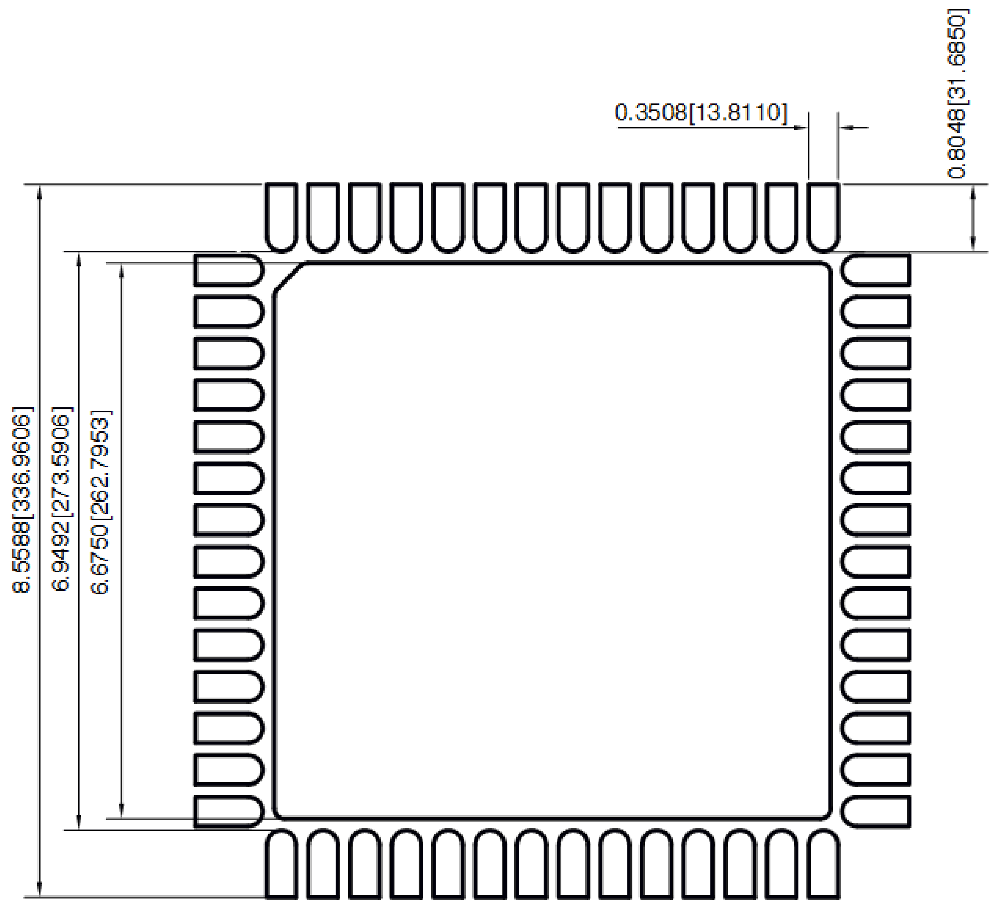


Figure 5-5. BOT and Internal Layers Copper Plane

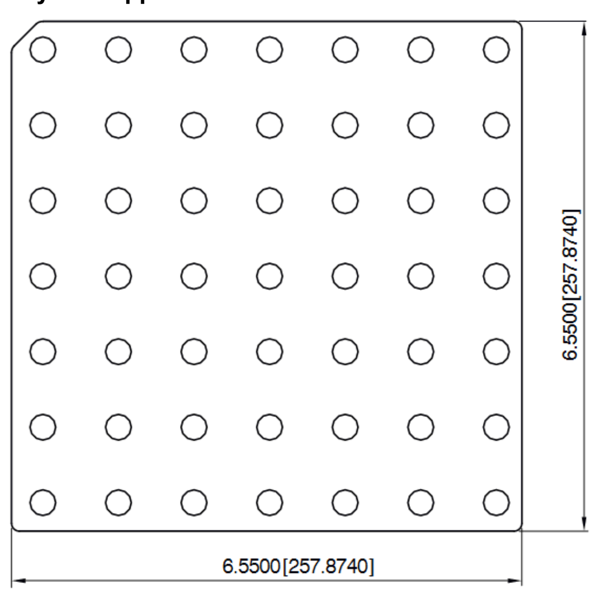
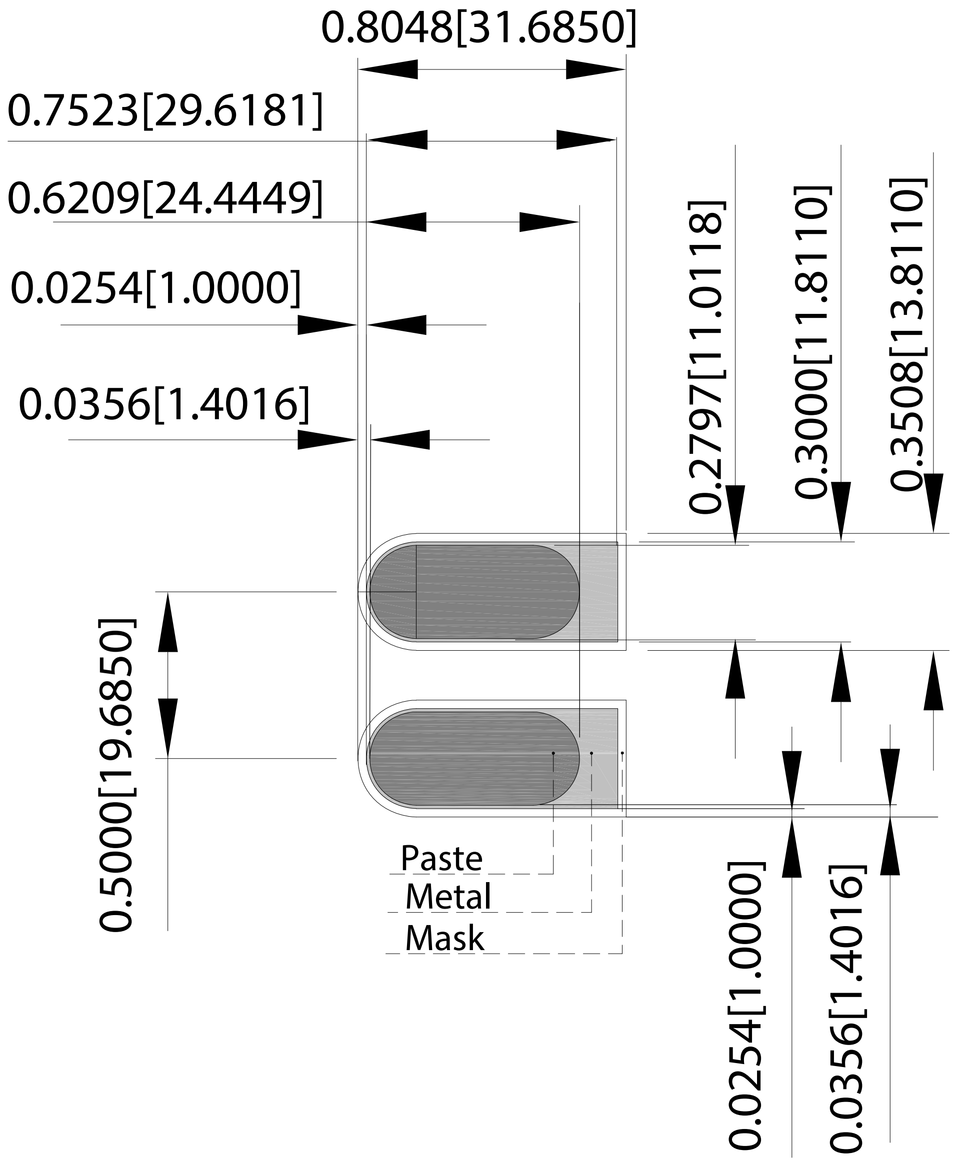


Figure 5-6. Top-Layer Pin Geometry



Note: The contract manufacturer has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil covers 65% to 80% of the thermal pad and should not allow solder to be applied to the thermal vias under the QFN package using any method they deem appropriate. Any design should be subject to system validation and qualification prior to commitment to mass production of field deployment. Use a 5 mil stencil.

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5.4 Recommended Solder Reflow Information

RoHS 6/6

Pb-free 100% Matte Tin Finish

Package Peak Temperature for Solder Reflow (40 s maximum exposure)—260 °C (0 °C, –5 °C)

Table 5-3. Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TS_{max} to Tp)	3 °C/second max	3 °C/second max
Preheat		
Temperature min (TS_{min})	100 °C	150 °C
Temperature max (TS_{max})	150 °C	200 °C
Time (ts_{min} to ts_{max})	60 s to 120 s	60 s to 180 s
Time Maintained		
Temperature (T_L)	183 °C	217 °C
Time (t_L)	60 s to 150 s	60 s to 150 s
Peak classification temperature (TP)	210 °C to 235 °C	240 °C to 255 °C
Time within 5 °C of actual peak temperature (tp)	10 s to 30 s	20 s to 40 s
Ramp-down rate	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max

Figure 5-7. Classification Reflow Profiles

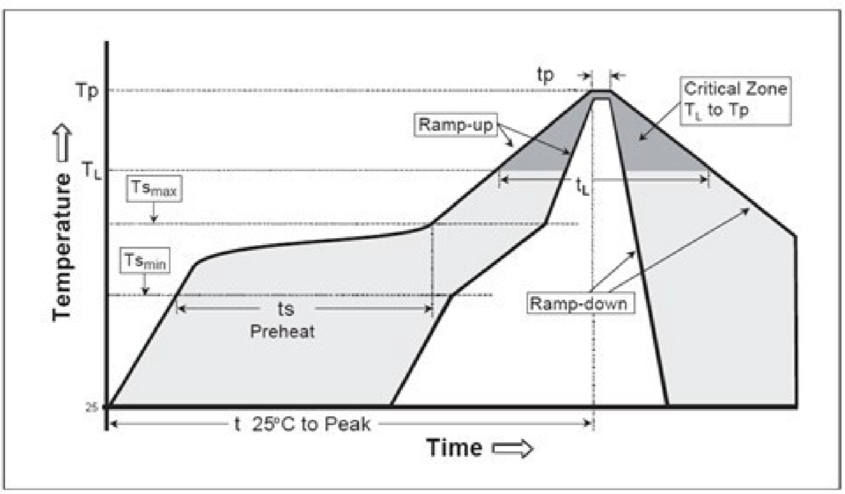

Table 5-4. Pb-Free Process—Package Classification Reflow Temperatures

Package Thickness	Volume <350 mm^3	Volume 350–2000 mm^3	Volume >2000 mm^3
Less than 1.6 mm[1]	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6 mm to 2.5 mm[1]	260 + 0 °C	250 + 0 °C	245 + 0 °C

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...........continued

Package Thickness	Volume <350 mm^3	Volume 350–2000 mm^3	Volume >2000 mm^3
Greater than or equal to 2.5 mm[1]	250 + 0 °C	245 + 0 °C	245 + 0 °C

1. Tolerance: The device manufacturer or supplier should assure process compatibility up to and including the stated classification temperature, meaning that the peak reflow temperature is 0 °C. For example, 260 °C to 0 °C, at the rated MSL value.

Note: Exceeding the ratings that are mentioned in the preceding table might cause damage to the device.

5.5 Tape and Reel Specification

This section provides the tape and reel specifications.

Figure 5-8. Tape and Reel Pin-1 Orientation

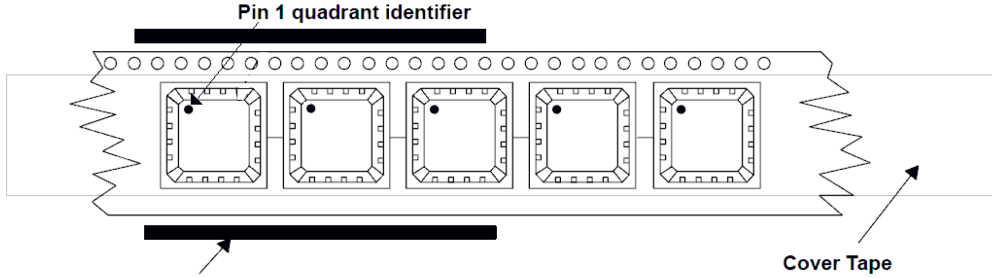

Figure 5-9. Tape Specifications

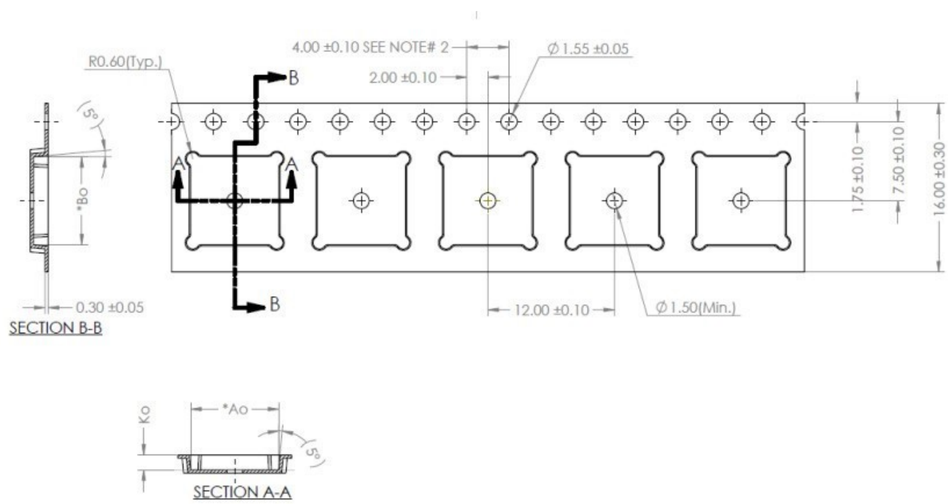

Table 5-5. Tape Mechanical Data

Dimension	Value (mm)
A0	8.35 ±0.10
B0	8.35 ±0.10
K0	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10

...........continued	
Dimension	**Value (mm)**
Width	16.00 ±0.30

Figure 5-10. Reel Specifications

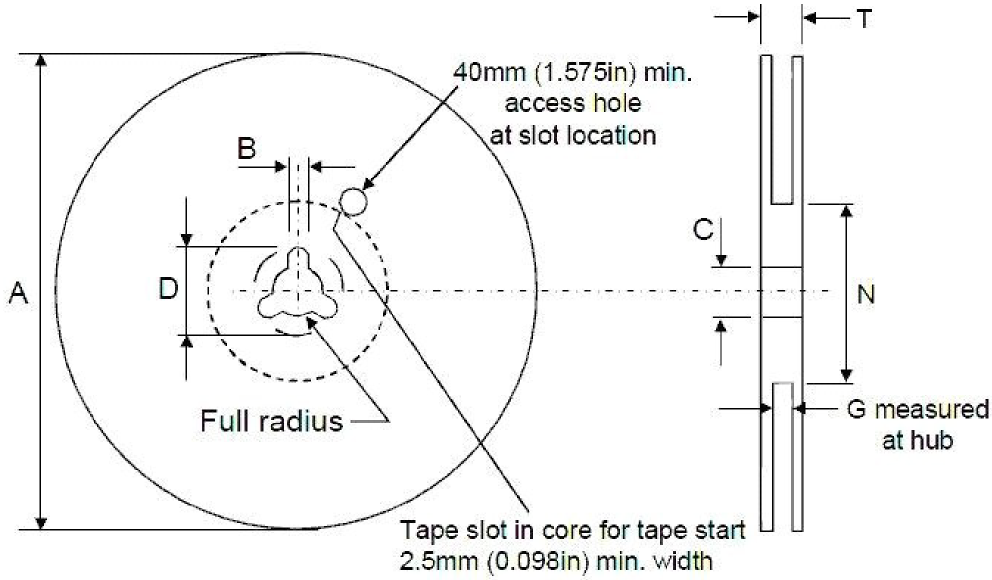

Table 5-6. Reel Mechanical Data

Dimensions	Value (mm)	Value (inch)
Tape size	16.00 ±0.3	0.630 ±0.012
A max.	330	13
B max.	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min.	20.2	0.795
N min.	50	1.968
G	16.4+2.0/–0.0	0.724 to 0.645
T max.	29	1.142

Base quantity: 2000 pieces

5.6 Reference Documents

- *PD39210 Serial Communication Protocol User Guide*
- *Microchip AN3361 Designing an IEEE 802.3af/802.3at/802.3bt-Compliant PD69208 48-Port PoE System*
- *Microchip Designing an IEEE 802.3af/802.3at-Compliant PD39208 48-Port PoE System*
- *AN3378 Surge Protection Application Note 8-Port PSE PoE Manager PD69208T4/M/4T4*
- *PD692x0+PD69208M/208T4/204T4 Implementing Perpetual PoE (PPoE) and Fast PoE*
- *PD69210 and PD69220 PoE PSE Controller Datasheet*
- *PD69200 PoE PSE Controller Datasheet*
- *PD39210 PoE PSE Controller Data Sheet*

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6. Ordering Information

The following table lists the part ordering information for the manager ICs.

Table 6-1. Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking
PD39208ILQ-TR-LE	Plastic QFN 8 mm × 8 mm (56 lead)	Tape and Reel	–40 °C to 85 °C	Microchip Logo PD39208 L E e4[1] YYWWNNN[2]

1. L= FAB code; E= V2R4; and e4= second-level interconnect.
2. YY= Year; WW= Week; and NNN= Trace code.

Note: The package meets RoHS, Pb-free of the European Council to minimize the environmental impact of electrical equipment.

The following table lists the manufacturing and ordering part numbers of the manager devices.

Table 6-2. Manufacturing and Ordering Part Numbers

Ordering Part Number	Manufacturing Part Number
PD39208ILQ-TR-LE	PD39208ILQ-TR-LE

7. Revision History

Revision	Date	Section	Description
B	11/2020	Power Sequencing	• Updated text.
		Ordering Information	• Updated "5 mm x 5 mm" to "8 mm x 8 mm".
A	07/2020		This is the initial issue of this document.

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