MP3363

Single-String, 1.8V Minimum V_{IN}, 36V V_{OUT} Boost LED Driver

DESCRIPTION

The MP3363 is a fixed-frequency converter ideal for low-current and high-current boost applications. The low 0.2V feedback voltage (V_{FB}) offers higher efficiency in white LED driver applications.

The MP3363 regulates the output voltage (V_{OUT}) up to 36V, with efficiency as high as 95%. Current mode regulation and external compensation components allow the MP3363 control loop to be optimized across a wide variety of input voltages.

The MP3363 supports analog dimming and pulse-width modulation (PWM) dimming on same pin. An input PWM signal with dimming frequency below 2kHz initiates PWM dimming, while an input PWM signal with dimming frequency above 5kHz initiates analog dimming.

Soft start, cycle-by-cycle current limit, and input under-voltage lockout (UVLO) protection prevent the sensitive external circuitry from being damaged or overstressed during start-up or potential overload current conditions.

The MP3363 is available in a TSOT23-8 package.

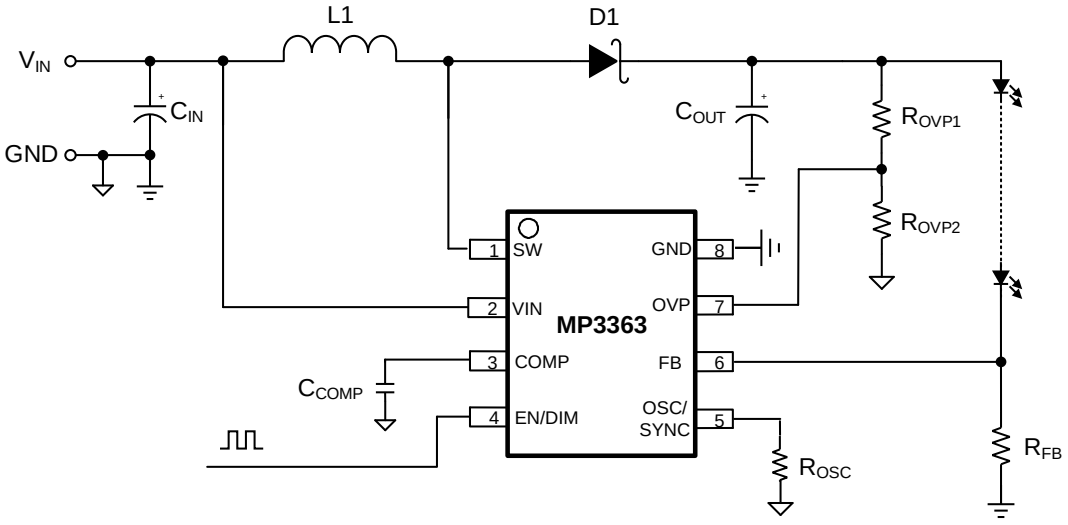
FEATURES

- Wide 1.8V to 36V Input Voltage Range
- 1A Peak Current Limit
- 0.5μA Shutdown Current
- Low 200mV Feedback Voltage (V_{FB})
- 200kHz to 2.2MHz Configurable Switching Frequency (f_{SW})
- Internal 100mΩ, 40V Power Switch
- High Efficiency
- Analog Dimming and Pulse-Width Modulation (PWM) Dimming
- Under-Voltage Lockout (UVLO) Protection
- Open/Short LED Protection
- Short FB to GND Protection
- Soft Start
- Thermal Shutdown (TSD)
- Available in a TSOT23-8 Package

APPLICATIONS

- Two AA Powered Backlighting
- LCD Backlighting
- General Lighting

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP3363GJ*	TSOT23-8	*See Below*	1

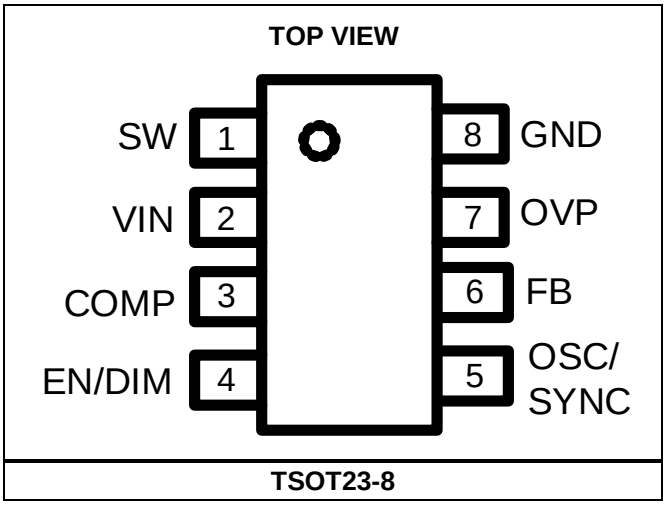
* For Tape & Reel, add suffix -Z (e.g. MP3363GJ-Z).

TOP MARKING

BLCY

BLC: Product code
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Output switch node.** The SW pin is the drain of the internal N-Channel MOSFET. Connect the inductor and rectifier to SW to complete the boost converter.
2	VIN	**Input supply.** VIN supplies power to the IC.
3	COMP	**Error amplifier (EA) output compensation.** Connect the COMP pin to a series RC network to compensate the regulator control loop.
4	EN/DIM	**EN and dimming.** Use the EN/DIM pin to enable/disable the device, or to initiate pulse-width modulation (PWM) dimming or analog dimming. The following conditions determine the EN/DIM operation: 1. To disable the IC, keep the EN/DIM pin low for 20ms. 2. To make the IC work in PWM dimming mode, apply a PWM signal with frequency below 2kHz. 3. To make the IC work in analog dimming mode, apply a PWM signal with frequency above 5kHz.
5	OSC/ SYNC	**Switching frequency setting and synchronization.** Connect a resistor to the OSC/SYNC pin to configure the switching frequency (f_{SW}) between 200kHz and 2.2MHz, or apply a pulse signal between 200kHz and 2.2MHz to synchronize f_{SW}.
6	FB	**Regulation feedback input.** The regulation threshold is 0.2V.
7	OVP	**Output over-voltage protection.** The OVP pin senses the output voltage (V_{OUT}) to protect the IC during open LED operation.
8	GND	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{SW} ..... -0.3V to +40V
All other pins..... -0.3V to +5.3V
Continuous power dissipation (T_A = 25°C) (2)
TSOT23-8.....1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±1000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 1.8V to 36V
Maximum LED load voltage (V_{LED})..... 36V
Operating junction temp (T_J) ... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
TSOT23-8	100	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 1.8V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input shutdown supply current		V_{EN} = 0V		0.5	1	μA
Input operating supply current	I_{Q1}	V_{EN} > 2V, V_{FB} = 0.5V		0.8	1.05	mA
	I_{Q2}	With switching, 400kHz			1.5	mA
V_{IN} under-voltage lockout (UVLO) threshold	V_{UVLO}	V_{IN} rising	1.5	1.6	1.7	V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			100		mV
EN/DIM input low threshold	V_{EN_L}				0.4	V
EN/DIM input high threshold	V_{EN_H}		1.2			V
EN/DIM input bias current	I_{EN}	V_{EN} = 5V			7	μA
EN/DIM input low time to disable the IC	t_{EN}	EN/DIM pulls low to disable the IC	16	20	24	ms
SW switching frequency	f_{SW}	R_{OSC} = 100kΩ	360	400	440	kHz
SW maximum duty cycle		V_{FB} = 0.15V, f_{SW} = 400kHz	90	93		%
Error amplifier (EA) transconductance	G_{EA}			250		μA/V
COMP maximum current	I_{EA}	Sourcing and sinking		30		μA
FB regulation threshold	V_{FB}		196	200	204	mV
FB input bias current	I_{FB}	V_{FB} = 0.5V			1	μA
SW on resistance	R_{ON}			100		mΩ
SW current limit	I_{LIM}	Duty = 80%	0.85	1	1.15	A
SW leakage current	I_{SW}	V_{SW} = 40V			0.3	μA
Over-voltage protection (OVP) threshold	V_{OVP}		1.12	1.2	1.28	V
OVP hysteresis	V_{OVP_HYS}			100		mV
OVP under-voltage threshold	V_{OVP_UV}			50	100	mV
Short load protection threshold	V_{SP}	V_{FB} > V_{SP}, short load protection is triggered	540	600	660	mV
Latch-off current limit	I_{CL}			2.5		A
Thermal shutdown threshold (5)	T_{SD}			170		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			20		°C

Note:

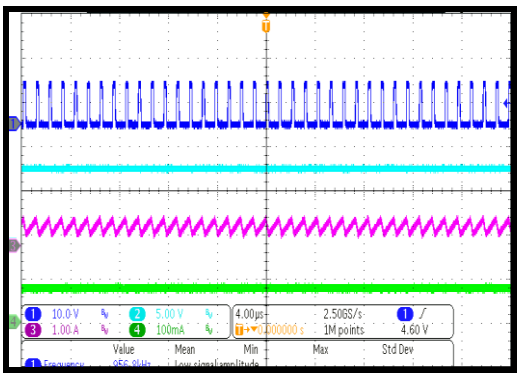
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 10V, 10 LEDs, I_{LED} = 80mA, L = 4.7µH, T_A = 25°C, unless otherwise noted.

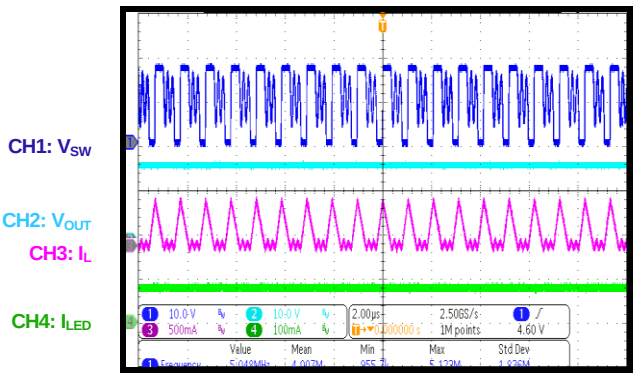
Steady State

V_{IN} = 1.8V, load = 3 LEDs



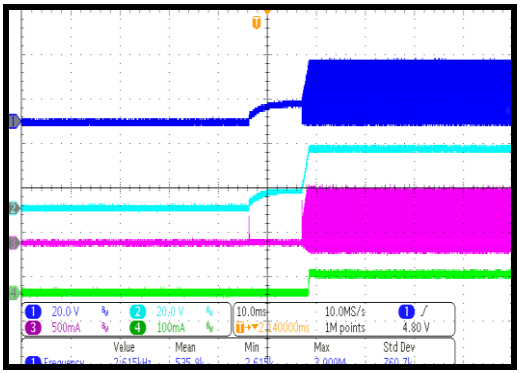
Steady State

Load = 6 LEDs



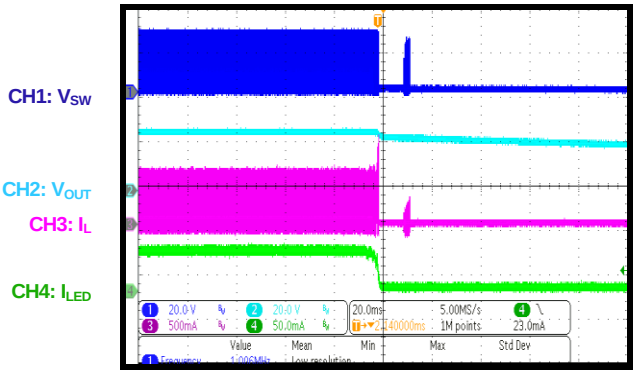
Start-Up through VIN

V_{IN} = 8V, I_{LED} = 40mA

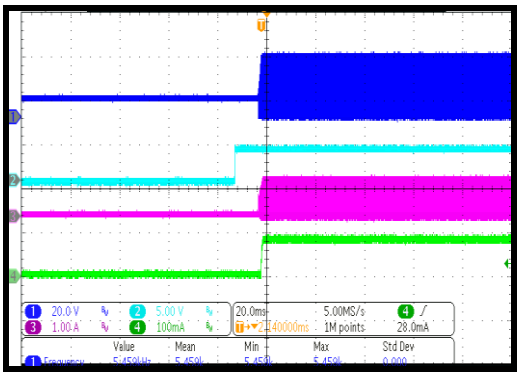


Shutdown through VIN

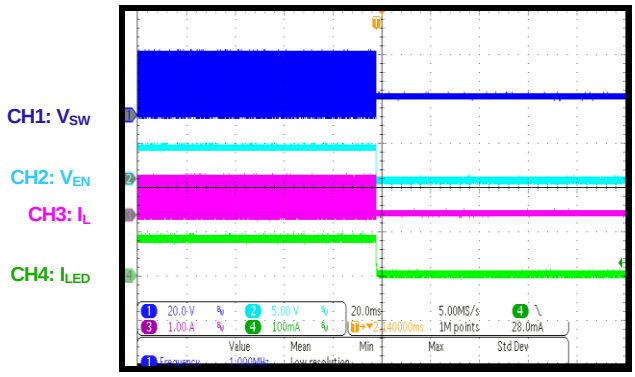
V_{IN} = 8V, I_{LED} = 40mA



Start-Up through EN



Shutdown through EN

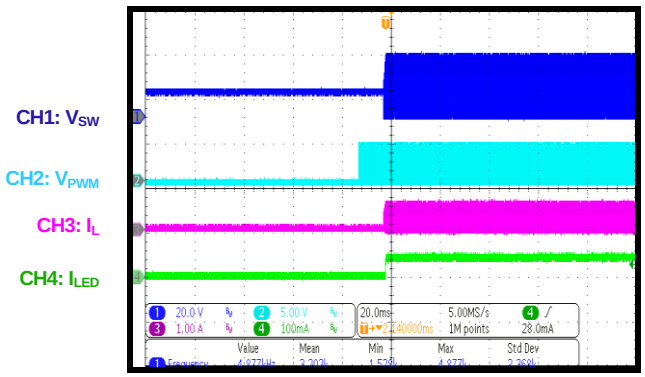


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 10V, 10 LEDs, I_{LED} = 80mA, L = 4.7µH, T_A = 25°C, unless otherwise noted.

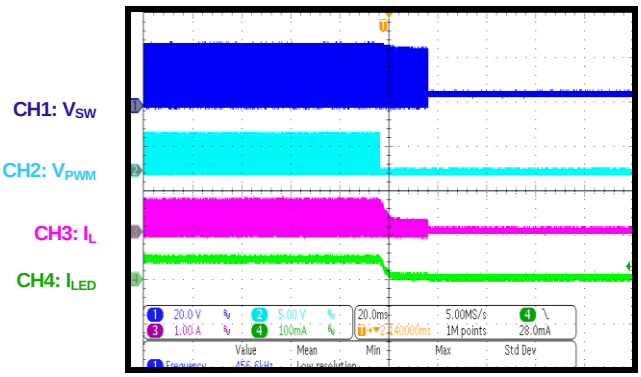
Start-Up through PWM

f_{PWM} = 10kHz, V_{IN} = 10V, PWM duty = 50%



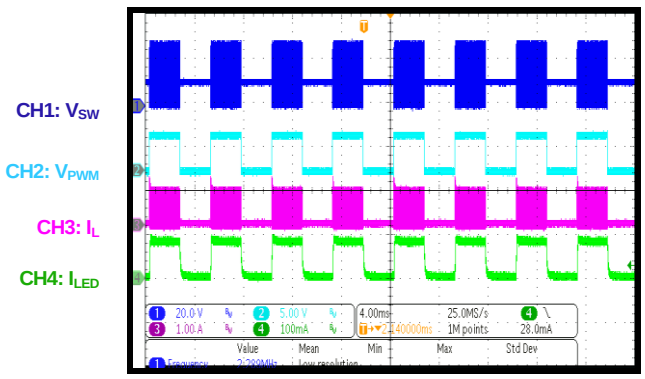
Shutdown through PWM

f_{PWM} = 10kHz, V_{IN} = 5V, PWM duty = 50%



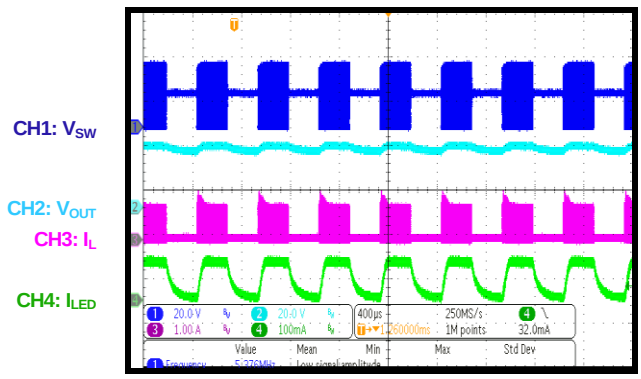
PWM Dimming

200Hz, V_{IN} = 10V, PWM duty = 50%



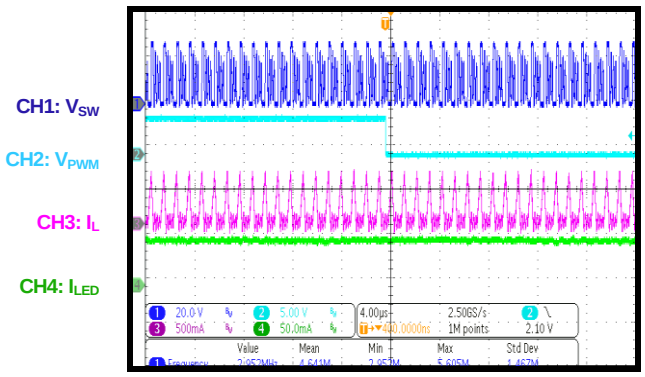
PWM Dimming

2kHz, V_{IN} = 15V, PWM duty = 50%

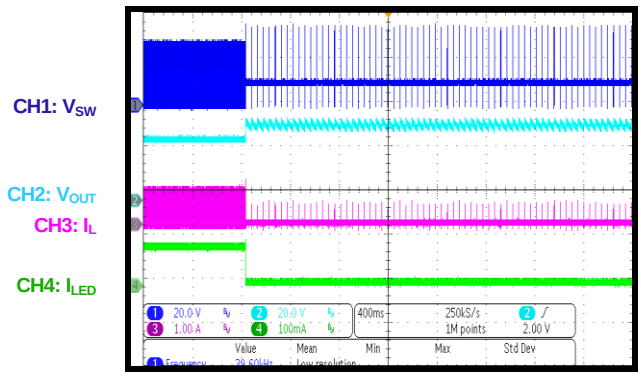


Analog Dimming

5kHz, PWM duty = 50%



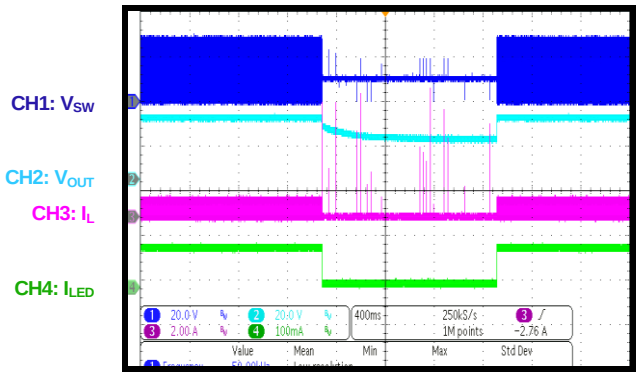
Open LED during Normal Operation



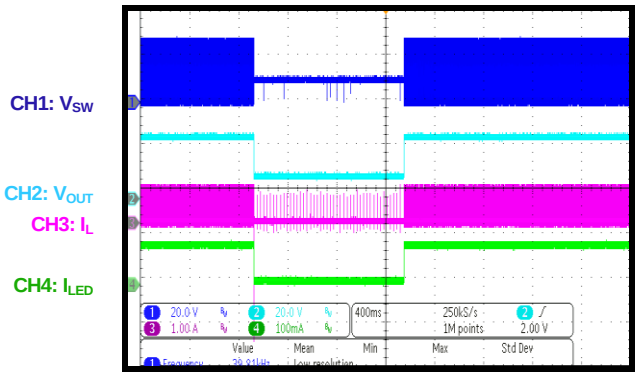
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 10V, 10 LEDs, I_{LED} = 80mA, L = 4.7µH, T_A = 25°C, unless otherwise noted.

Short Inductor during Normal Operation and Recovery



Short Diode during Normal Operation and Recovery



FUNCTIONAL BLOCK DIAGRAM

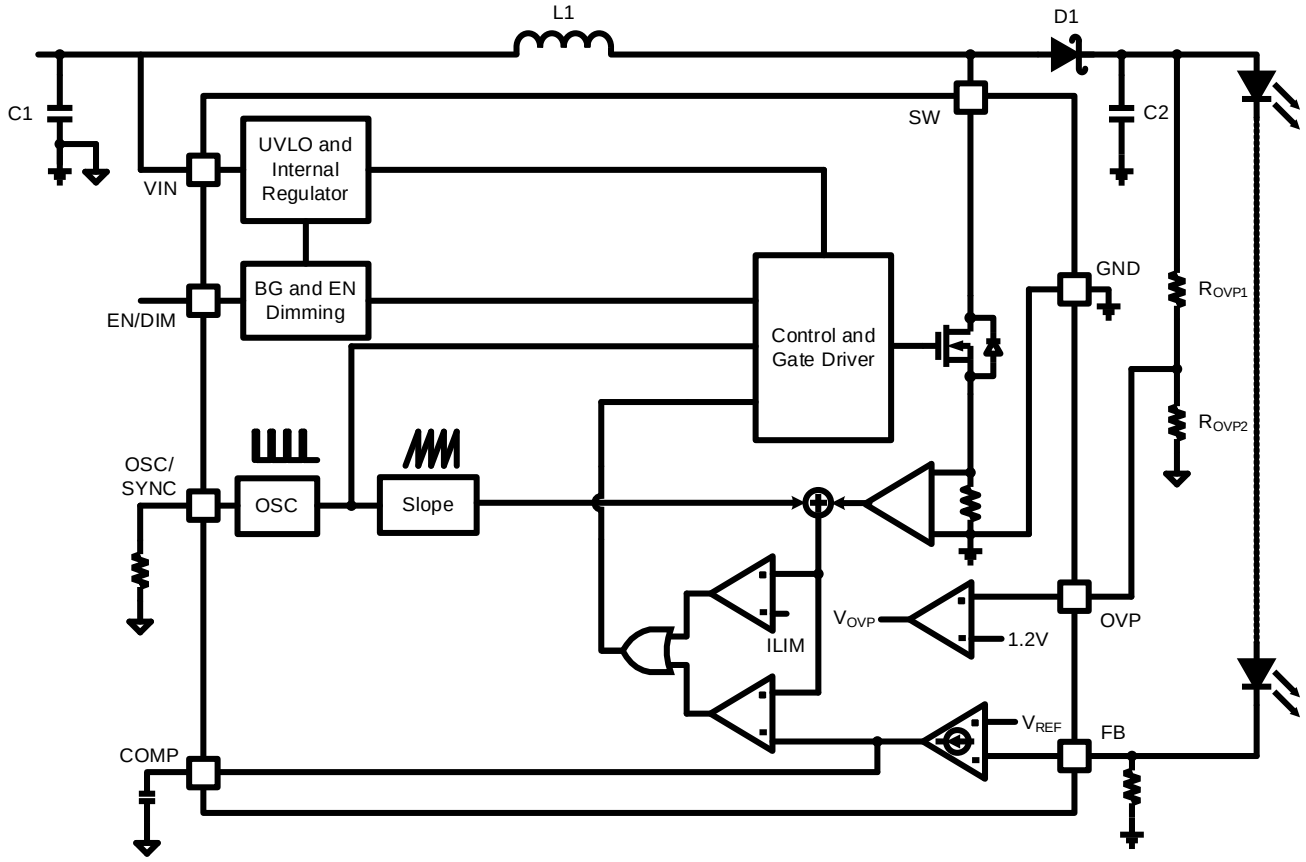


Figure 1: Functional Block Diagram

OPERATION

The MP3363 drives the internal MOSFET with current mode architecture to regulate the LED current (I_{LED}), which is measured through an external current-sense (CS) resistor.

The MP3363 employs a special circuit to regulate the internal power supply, which covers a wide input voltage (V_{IN}) range (1.8V to 36V). The switching frequency (f_{SW}) can be configured. The device integrates under-voltage lockout (UVLO), over-voltage protection (OVP), over-current protection (OCP), short LED protection, short FB to GND protection, and thermal shutdown (TSD).

Step-Up Converter

The MP3363 uses peak current control mode to regulate the output power. At the beginning of each switching cycle, the internal clock turns on the internal N-channel MOSFET (in normal operation, the minimum turn-on time is about 50ns). A stabilizing ramp is added to the CS amplifier output to prevent subharmonic oscillations for duty cycles exceeding 50%. This result is fed into the pulse-width modulation (PWM) comparator. If the summed voltage reaches the output voltage of the error amplifier (EA), the internal MOSFET turns off.

The output voltage of the internal EA is an amplified signal of the difference between the reference voltage (V_{REF}) and the FB voltage (V_{FB}).

If V_{FB} drops below V_{REF}, the EA's output increases. This results in more current flowing through the MOSFET, which increases power delivered to the output. This forms a closed loop that regulates the output voltage (V_{OUT}).

If V_{OUT} is almost equal to V_{IN} under light-load conditions, the converter runs in pulse-skipping mode. The MOSFET turns on for a minimum on time, and then the converter discharges the power to the output for the remaining period. The internal MOSFET remains off until V_{OUT} requires another boost.

Soft Start

The MP3363 implements soft start (SS) by limiting the current capability of the internal EA during start-up. The COMP voltage (V_{COMP}) jumps to its clamp voltage at the beginning of start-up. The source/sink current of the internal EA is limited to about 10μA until V_{FB} reaches 80% of the internal V_{REF} during start-up. The maximum soft-start time is limited to 10ms. This prevents the IC from always being in soft start during deep analog dimming.

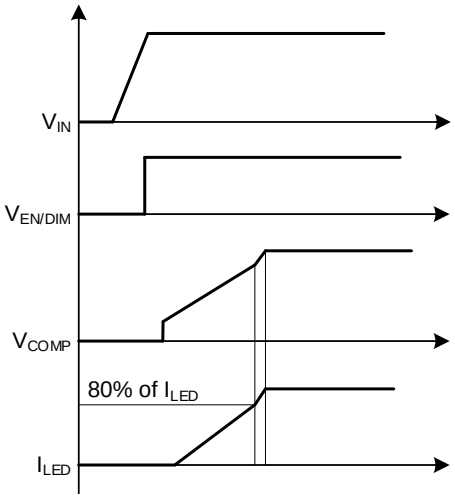


Figure 2: Soft Start Process

Enable (EN) and Dimming (DIM)

The EN/DIM pin can be used for different functions when different signals are applied on the pin. These functions are described in greater detail as below:

1. Enable/disable: If the EN/DIM pin is pulled high, the IC is enabled. If the EN/DIM pin is pulled low for 20ms, the IC is disabled.
2. PWM dimming (f_{PWM} < 2kHz): If the PWM signal has a frequency below 2kHz, the IC operates in PWM dimming mode. If the PWM signal is low in PWM dimming mode, the IC stops switching, and the output current (I_{OUT}) and V_{OUT} drop. If the PWM signal is high, the IC starts switching, and I_{OUT} and V_{OUT} begin to rise. This condition prohibits soft start.
3. Analog dimming (f_{PWM} > 5kHz): If the PWM signal has a frequency above 5kHz, the IC operates in analog dimming mode. The LED current (I_{LED}) can be changed by changing the PWM duty cycle.

I_{LED} can be calculated with Equation (1):

$$I_{LED} = \frac{V_{FB}}{R_{FB}} \times Duty \quad (1)$$

Where V_{FB} is about 200mV, R_{FB} is the feedback resistor, and Duty is the PWM signal duty.

Protections

The MP3363's protection features include UVLO, OVP, OCP, short load protection, short FB to GND protection, and TSD.

Under-Voltage Lockout (UVLO)

The MP3363 integrates V_{IN} UVLO protection. The internal circuit does not work until V_{IN} reaches the UVLO rising threshold.

Over-Voltage Protection (OVP)

Over-voltage (OV) conditions are detected by sensing the OVP pin's voltage. If the OVP pin's voltage reaches its high threshold, OVP is triggered and the IC stops switching. The IC tries to recover once the OVP pin's voltage drops to its low threshold.

Short Load Protection

Under short load conditions, a large short current is detected by the FB sense resistor. If the FB-sensed voltage exceeds 600mV for 20 switching cycles, short load protection is triggered and the IC stops switching. The IC resumes switching once the short condition disappears.

High voltage appears on the FB pin under short load conditions. Figure 3 shows the additional components that are required to protect the FB pin from damage. If a short occurs, a diode (D1) can be used to clamp V_{FB} to about 0.3V. A Zener diode can also be used to clamp V_{FB}.

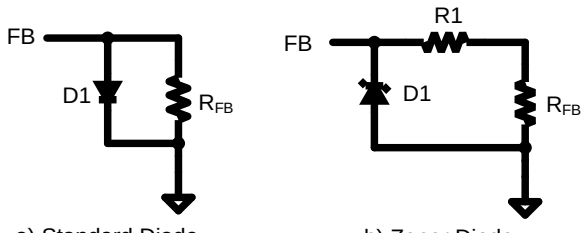


Figure 3: Short Load Protection for the FB Pin

Note that there is a short loop from the input to GND under short load conditions. Use a fuse or an external circuit to cut off the short loop.

OVP Pin Under-Voltage Protection (UVP)

If the OVP pin's voltage drops below 50mV for 10µs during normal operation, UVP is triggered and the IC stops switching. This protection is blanked during soft start.

Over-Current Protection (OCP) (Short Inductor/Diode Protection)

If there is an inductor or diode short and the MOSFET's current exceeds the latch-off current limit (typically 2.5A) for seven consecutive cycles, then OCP is triggered and the IC stops switching. Once the short disappears, the IC resumes normal operation.

Short FB to GND Protection

If V_{FB} drops below 50mV and the COMP saturation lasts for 20ms, the IC stops switching. Once the short disappears, the IC resumes normal operation.

Thermal Shutdown

Thermal shutdown prevents the MP3363 from operating at exceedingly high temperatures. If the die temperature exceeds the upper threshold (T_{SD} = 170°C), the COMP pin is pulled low. The IC resumes normal operation when the die temperature drops below the lower threshold. The hysteresis is about 20°C.

APPLICATION INFORMATION

LED Current (I_{LED}) Setting

I_{LED} is set by the LED current feedback resistor (R_{FB}). The value of R_{FB} can be calculated with Equation (2):

$$R_{FB} = \frac{200mV}{I_{LED}} \quad (2)$$

Switching Frequency Setting

The switching frequency (f_{SW}) is set by an external resistor (R_{OSC}) at the OSC/SYNC pin. f_{SW} can be estimated with Equation (3):

$$f_{SW}(kHz) = \frac{40000}{R_{OSC}(k\Omega)} \quad (3)$$

A PWM signal (200kHz to 2.2MHz) on the OSC/SYNC pin can also synchronize f_{SW}.

Selecting the Inductor

The MP3363 requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger-value inductor results in less ripple current, lower peak inductor current, and less stress on the internal N-channel MOSFET. However, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode (CCM) with high efficiency and excellent EMI performance.

Calculate the required inductance value with Equation (4):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (4)$$

Where V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{LOAD} is the LED load current, η is the efficiency, and D can be estimated with Equation (5):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (5)$$

Where V_{IN} is the input voltage.

For a given inductor value, the inductor DC current rating should be at least 40% higher than the maximum input peak inductor current for most applications. The inductor's DC resistance should be as small as possible for higher efficiency.

Over-Voltage Protection (OVP) Setting

Generally, set the OVP voltage threshold to be 10% to 20% higher than V_{OUT}. The OVP threshold can be set with a voltage divider (see the Typical Application section on page 1). The OVP threshold can be calculated with Equation (6):

$$V_{OVP}(V) = \frac{R_{OVP1} + R_{OVP2}}{R_{OVP2}} \times 1.2(V) \quad (6)$$

Selecting the Diode

Choose a diode with a voltage rating greater than the OVP threshold, and leave about a 20% margin. The current rating should be approximately two to three times greater than the LED current.

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X7R dielectrics are recommended due to their low ESR and small temperature coefficients.

Select a capacitor that limits the input voltage ripple (ΔV_{IN}) below 5% to 10% of its DC value. The capacitance can be calculated with Equation (7):

$$C_{IN} \geq \frac{\Delta I_L}{8 \times \Delta V_{IN} \times f_{SW}} \quad (7)$$

Where ΔI_L is the peak-to-peak inductor current. ΔI_L can be estimated with Equation (8):

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (8)$$

Selecting the Output Capacitor

Select an output capacitor (C_{OUT}) that limits the output voltage ripple (ΔV_{OUT}) below 1% to 5% of

its DC value, and ensures feedback loop stability. The capacitance can be estimated with Equation (9):

$$C_{OUT} \geq \frac{I_{LOAD} \times (V_{OUT} - V_{IN})}{\Delta V_{OUT} \times f_{SW} \times V_{OUT}} \quad (9)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, it is suggested to refer to Figure 4 and follow the guidelines below:

1. A high-frequency pulse current flows through the loop between the SW pin, output diode, output capacitor, and GND. Keep this loop as short as possible to reduce noise and electromagnetic interference.
2. Separate the PGND and AGND traces to reduce noise. AGND is the reference ground of all the logic signals.
3. Connect PGND and AGND to the GND pin.
4. Place the ceramic input capacitor (C_{IN}) as close to the VIN pin as possible.

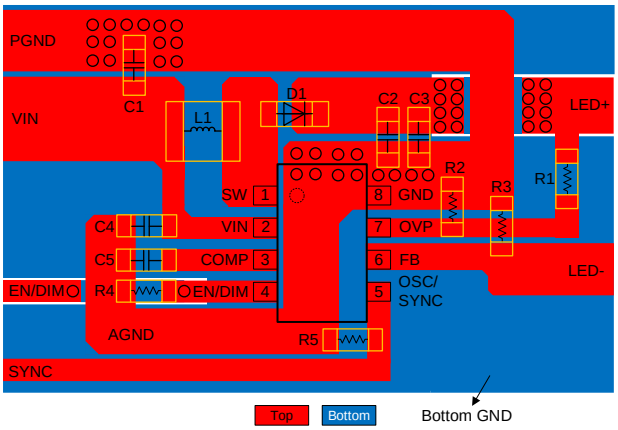


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

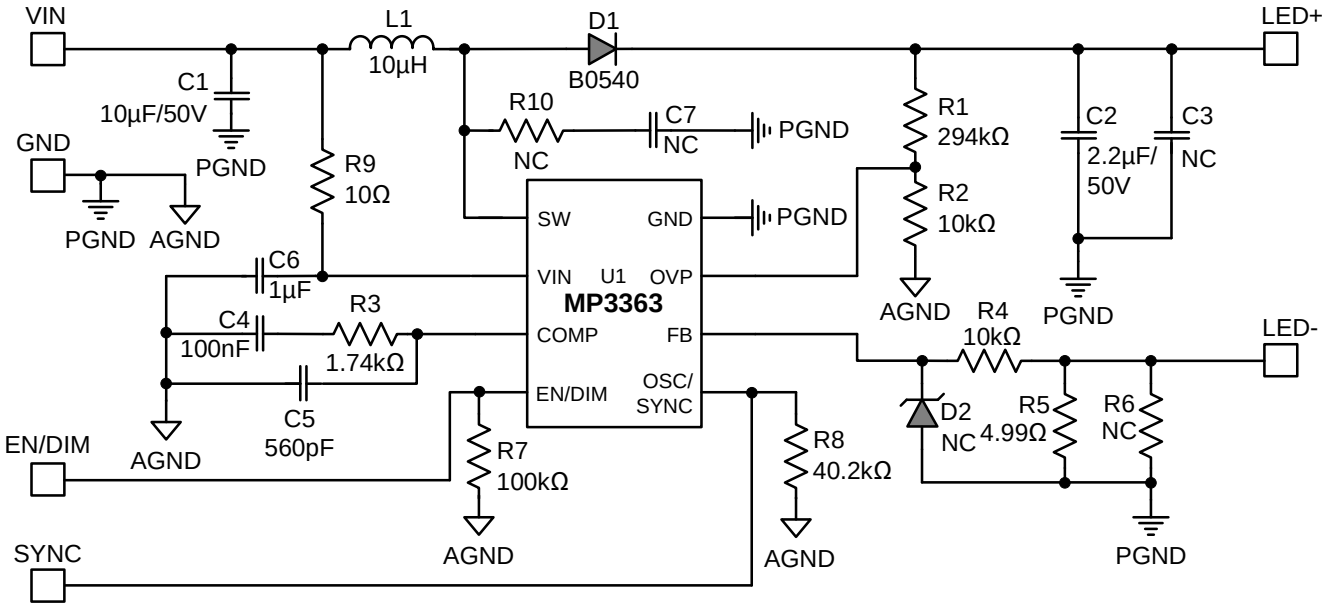
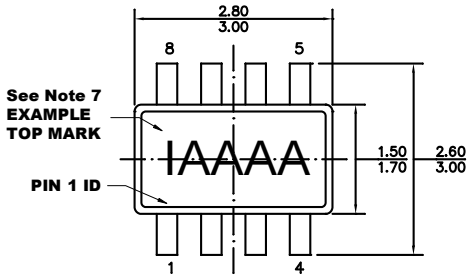


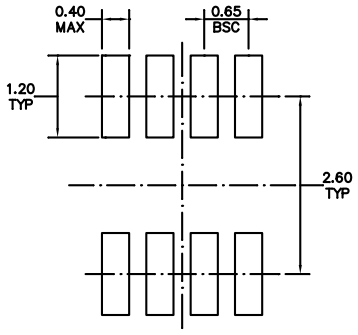
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

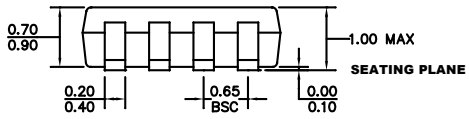
TSOT23-8



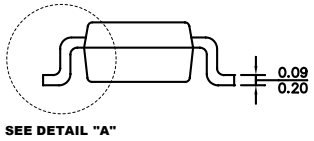
TOP VIEW



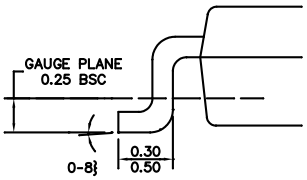
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

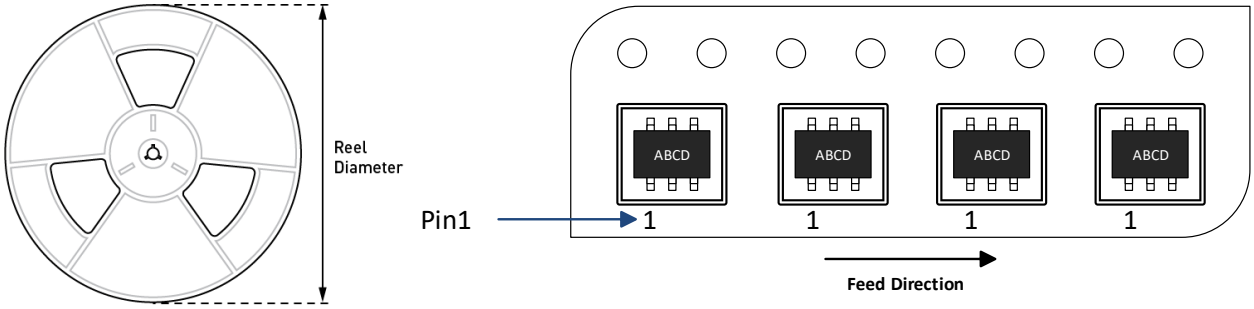


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITIES (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.1 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) WHEN READING THE TOP MARK FROM LEFT TO RIGHT, PIN 1 IS THE LOWER LEFT PIN (SEE EXAMPLE TOP MARK).

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3363GJ-Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/28/2021	Initial Release	-