MP2192

2A, 2.5V to 5.5V, Synchronous Step-Down Converter with 25μA I_Q in CSP Package

DESCRIPTION

The MP2192 is a monolithic, step-down switch-mode converter with built-in internal power MOSFETs. The MP2192 achieves 2A of continuous output current from a 2.5V to 5.5V input voltage, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2192 is well-suited for a wide range of applications, including high-performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

The MP2192 requires a minimal number of readily available, standard external components. It is available in an ultra-small CSP-6 (0.85mmx1.25mm) package.

FEATURES

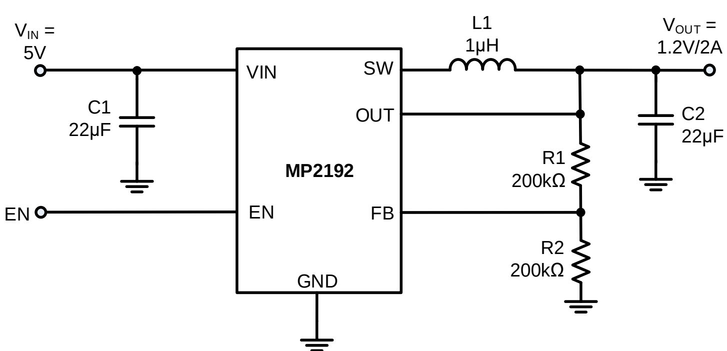
- Low 25μA I_Q
- 1.1MHz Switching Frequency
- EN for Power Sequencing
- 1% FB Accuracy
- Wide 2.5V to 5.5V Operating Input Range
- Output Adjustable from 0.6V
- Up to 2A Output Current
- 75mΩ and 45mΩ Internal Power MOSFET Switches
- 100% Duty Cycle
- Output Discharge
- V_{OUT} Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Available in a WLCSP-6 (0.85mmx1.25mm) Package
- Excellent Transient Response with Minimal Output Capacitors

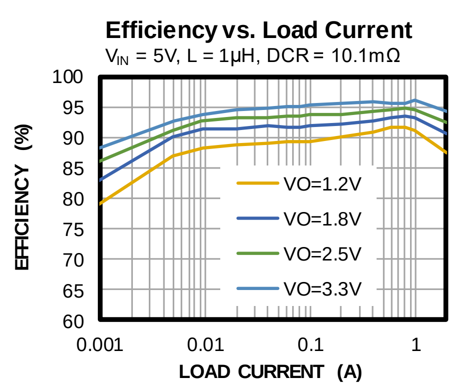
MPL Optimized Performance with MPS Inductor MPL-AL4020 Series

APPLICATIONS

- Solid State Drives (SSDs)
- Portable Instruments
- Battery-Powered Devices
- Multi-Function Printers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	V_{OUT} Range	MSL Rating
MP2192GC	WLCSP-6 (0.85mmx1.25mm)	*See Below*	Adjustable	1

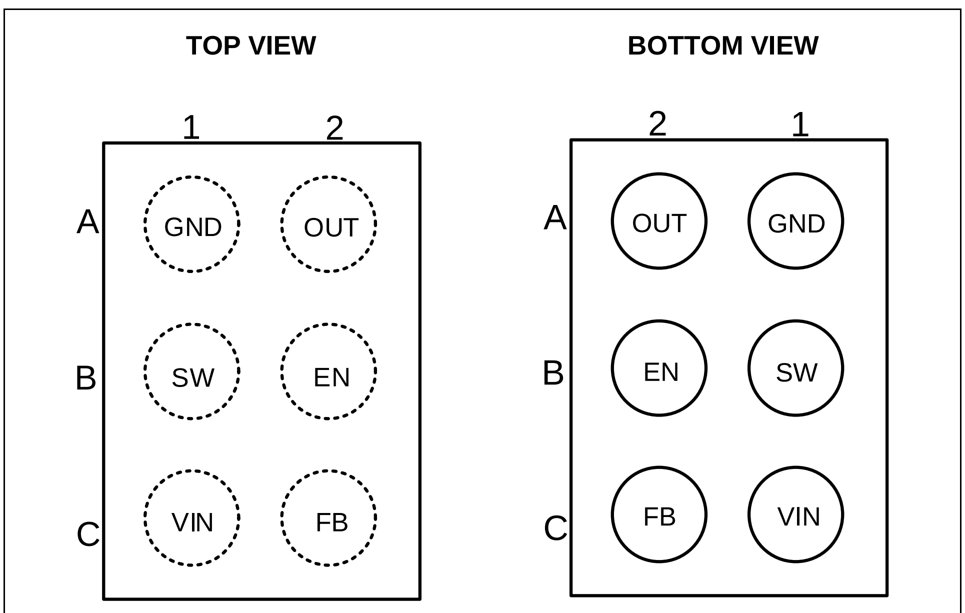
* For Tape & Reel, add suffix –Z (e.g. MP2192GC–Z).

TOP MARKING

LMY
LLL

LM: Product code of MP2192GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



WLCSP-6 (0.85mmx1.25mm)

PIN FUNCTIONS

Pin #	Name	Description
A1	GND	**Power ground.**
A2	OUT	**Output sense.** OUT is the voltage power rail and input sense pin for the output voltage. Use an output capacitor to reduce the output voltage ripple.
B1	SW	**Output switching node.** SW is the drain of the internal high-side P-channel MOSFET. Connect the inductor to SW to complete the converter.
B2	EN	**On/off control.**
C1	VIN	**Supply voltage.** The MP2192 operates from an unregulated input between 2.5V and 5.5V. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.
C2	FB	**Feedback.** An external resistor divider connected from the output to GND, then tapped to the FB pin, sets the output voltage.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW}................................ -0.3V (-5V for <10ns) to +6.5V (+10V for <10ns)
All other pins ....-0.3V to +6.5V
Junction temperature ....150°C
Lead temperature ....260°C
Continuous power dissipation (T_A = 25°C) (2) (4) 1.39W
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) .... ±2000V
Charged device model (CDM).. +1000V, -1500V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....2.5V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} $\theta_{JC(TOP)}$

EVL2192-C-00A (4)……..........90……30…°C/W
WLCSP-6 (5) ………………...141……..2…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may produce an excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EVL2192-C-00A evaluation board, 2-layer PCB.
5) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN range			2.5		5.5	V
UVLO threshold rising				2.3	2.45	V
UVLO threshold hysteresis				135		mV
Feedback voltage	V_{FB}	T_J = 25°C, 2.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 0.1A	594	600	606	mV
		T_J = -40°C to +125°C, I_{OUT} = 0.1A	591	600	609	
Feedback current	I_{FB}	V_{FB} = 0.63V		50	100	nA
P-channel MOSFET switch on resistance	$R_{DS(ON)\_P}$	V_{IN} = 5V		75		mΩ
N-channel MOSFET switch on resistance	$R_{DS(ON)\_N}$	V_{IN} = 5V		45		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, T_J = 25°C, V_{SW} = 0V and 6V		0	1	μA
P-channel MOSFET peak current limit			2.8	3.5	4.1	A
N-channel MOSFET valley current limit				2.5		A
ZCD				50		mA
On time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		220		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		300		
Switching frequency	f_{SW}	V_{OUT}=1.2V, I_{OUT}=0.5A		1100		kHz
Minimum off time	$t_{MIN-OFF}$			100		ns
Minimum on time (7)	t_{MIN-ON}			60		ns
Soft-start time	t_{SS-ON}	V_{OUT} rising from 10% to 90%		1.1		ms
EN turn-on delay		EN on to SW active		220		μs
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		13		Ω
EN input current		V_{EN} = 2V		1.2		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0	1	μA
Supply current (quiescent) Adjustable version		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 5V, T_J = 25°C		25	30	μA
Output over-voltage threshold	V_{OVP}		112%	117%	122%	V_{FB}
VOUT OVP hysteresis	V_{OVP_HYS}			13%		V_{FB}
OVP delay				12		μs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C [(6)], typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-side current		Current flowing from SW to GND		1.5		A
Absolute V_{IN} OVP		After V_{OUT} OVP is enabled		6.2		V
Absolute V_{IN} OVP hysteresis				400		mV
Thermal shutdown [(7)]				160		°C
Thermal hysteresis [(7)]				30		°C

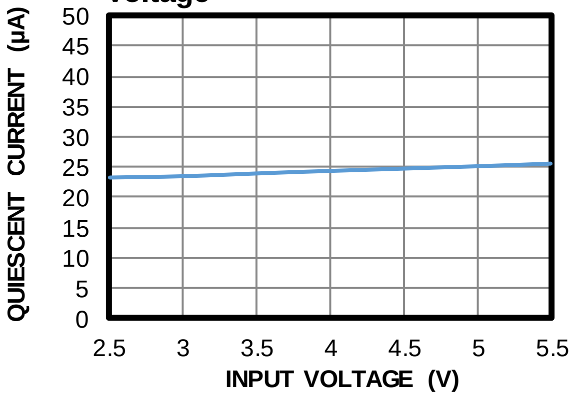
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

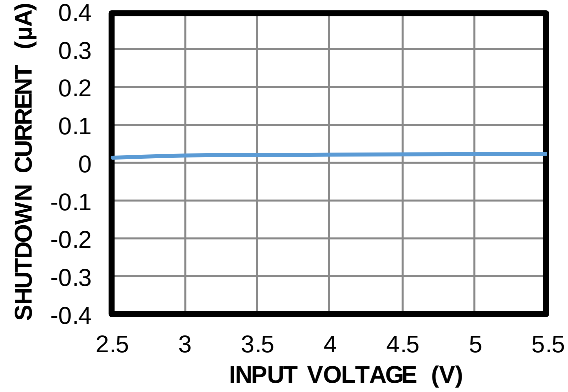
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage

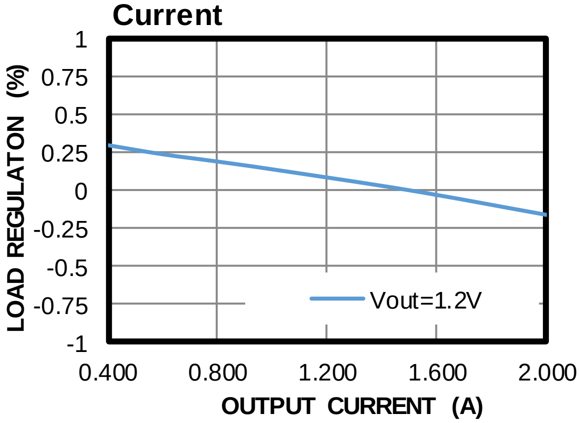


Shutdown Current vs. Input Voltage

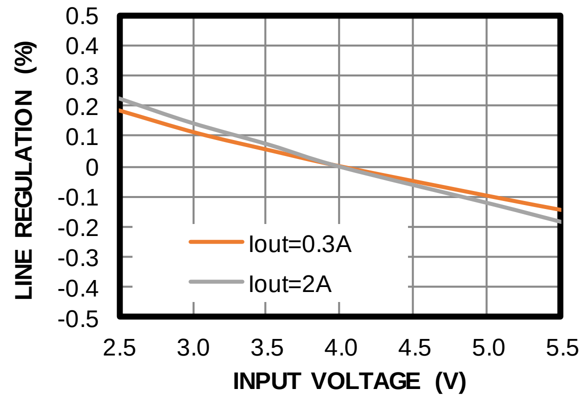
V_{EN} = 0V



Load Regulation vs. Output Current

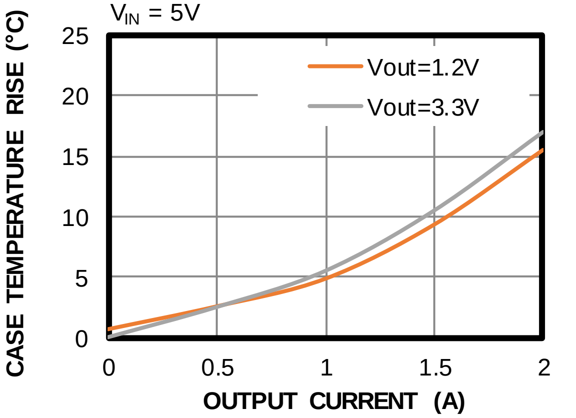


Line Regulation vs. Input Voltage



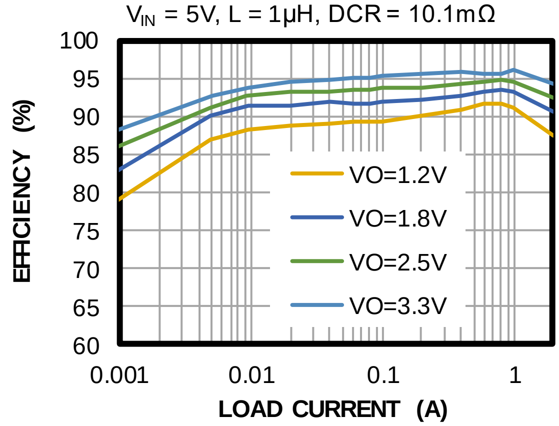
Case Temperature Rising vs. Output Current

V_{IN} = 5V



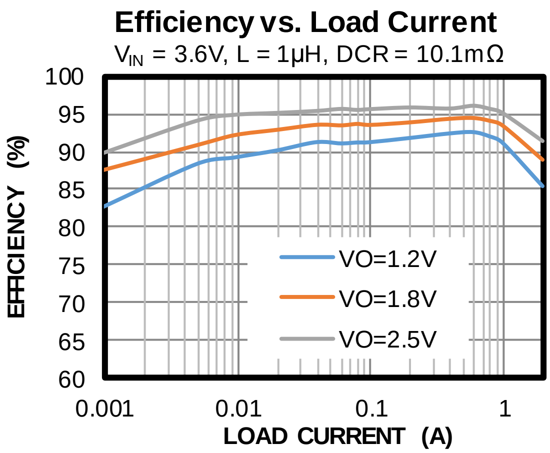
Efficiency vs. Load Current

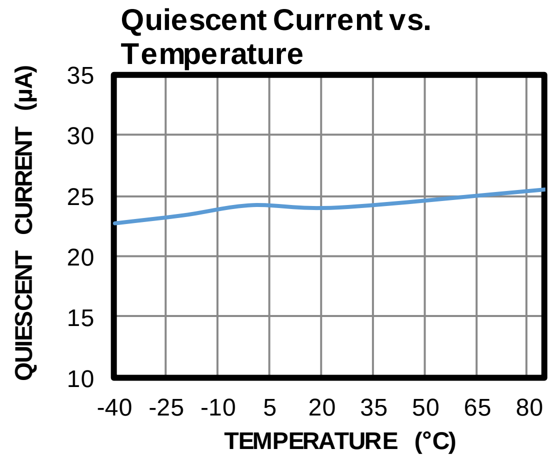
V_{IN} = 5V, L = 1µH, DCR = 10.1mΩ

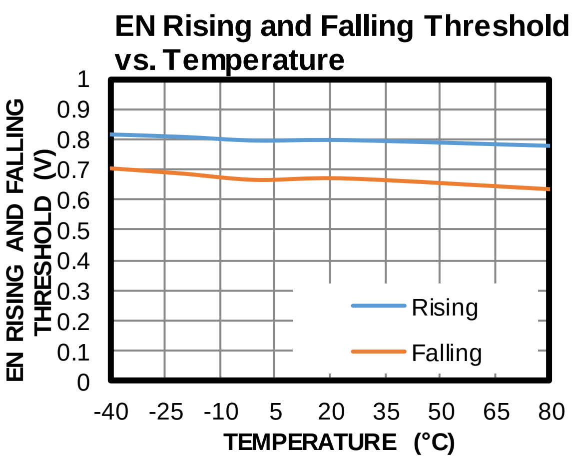


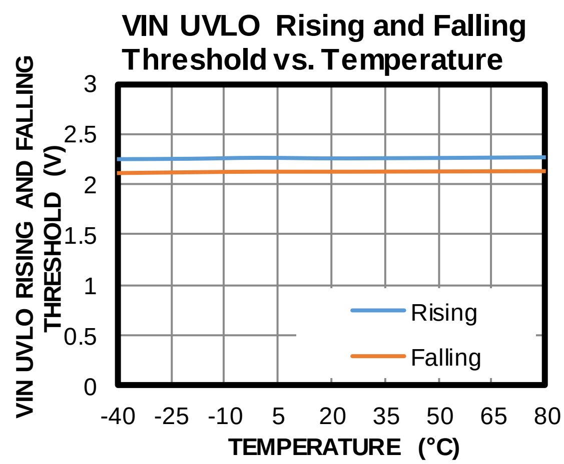
TYPICAL CHARACTERISTICS *(continued)*

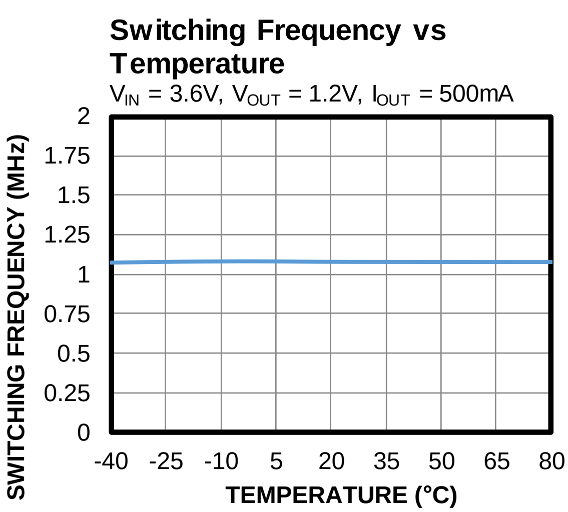
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise noted.

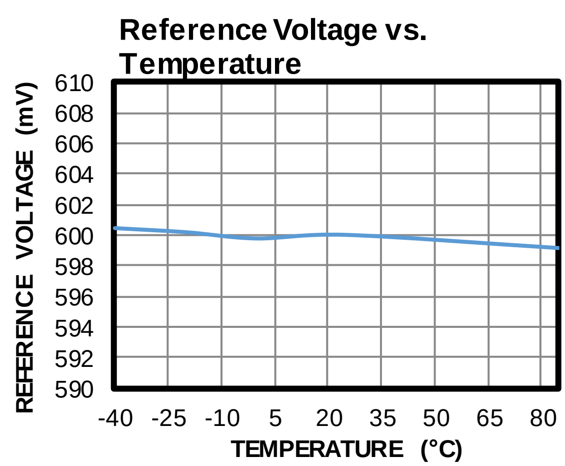






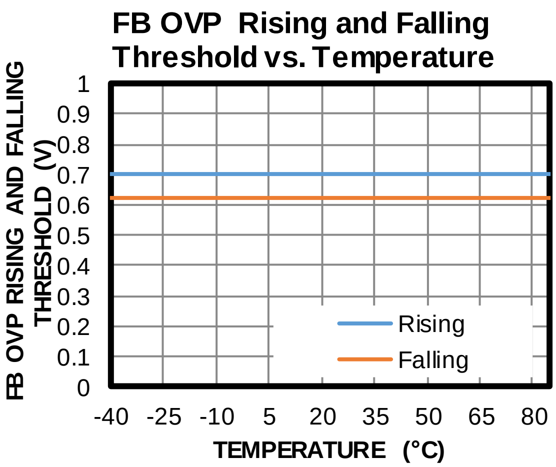


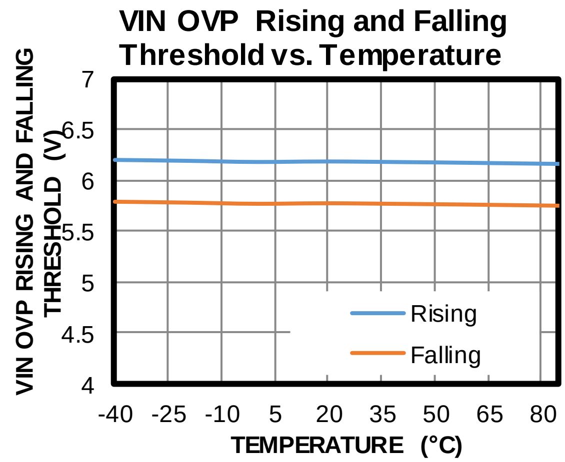


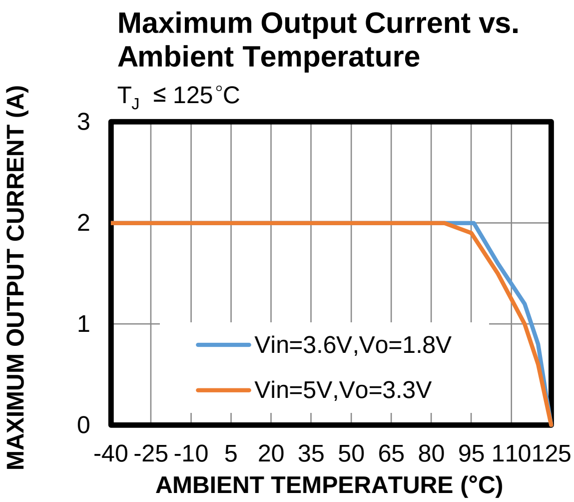


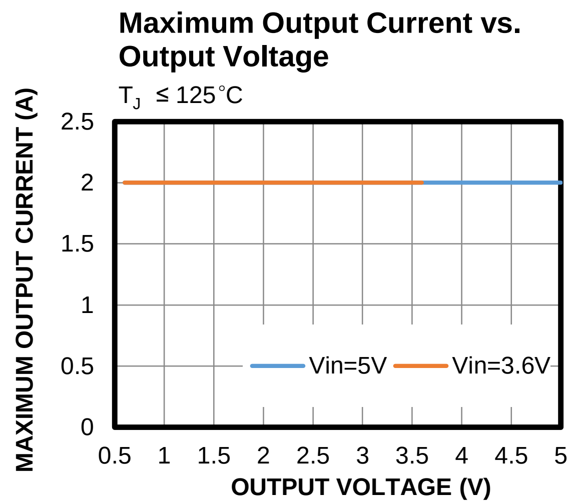
TYPICAL CHARACTERISTICS *(continued)*

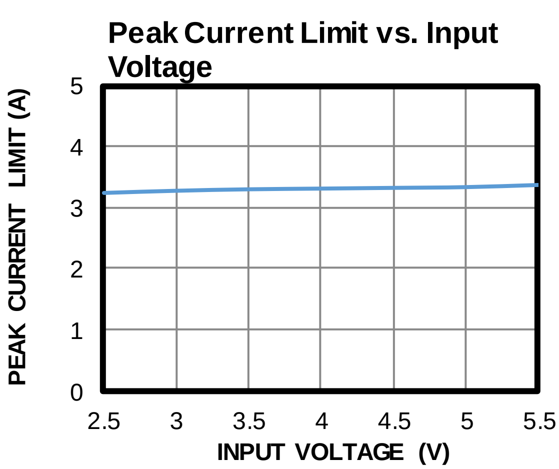
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

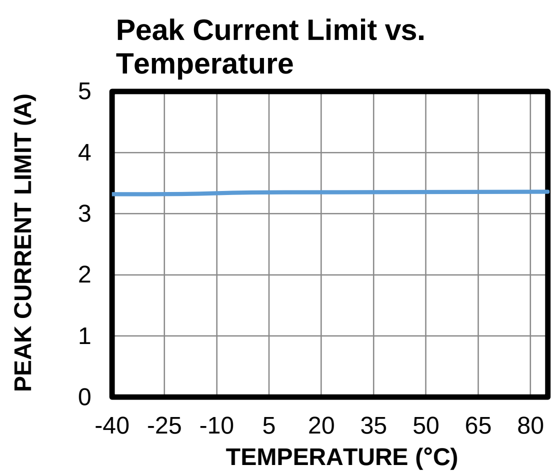










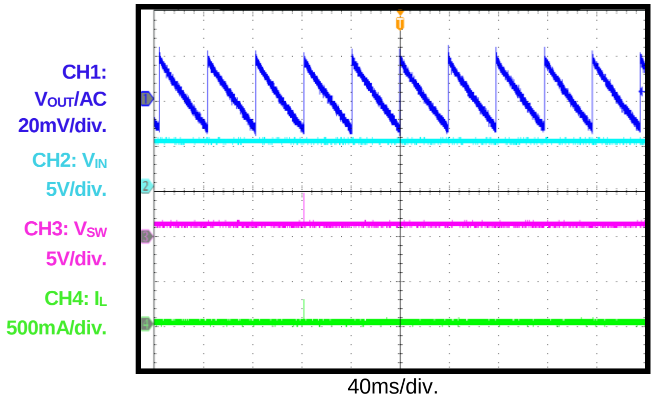


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 22μF, T_A = 25°C, unless otherwise noted.

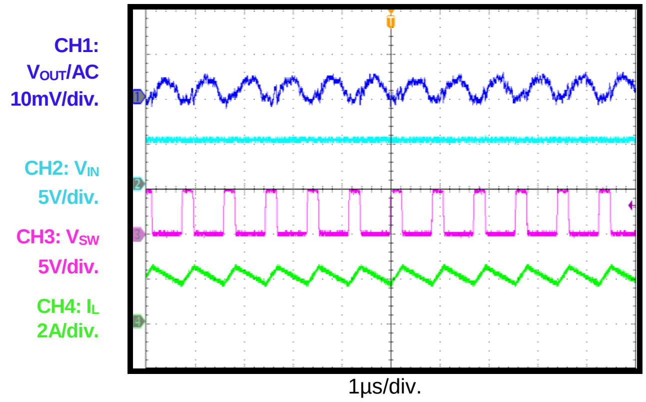
Steady State

I_{OUT} = 0A



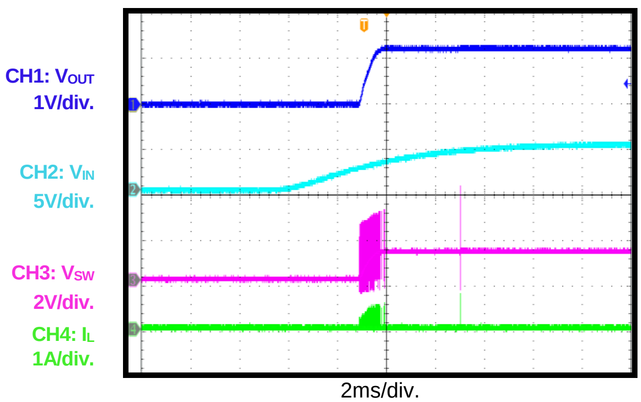
Steady State

I_{OUT} = 2A



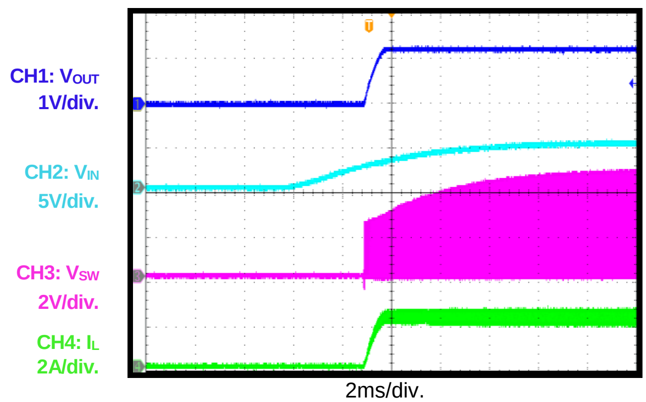
Start-Up through VIN

I_{OUT} = 0A



Start-Up through VIN

I_{OUT} = 2A



Shutdown through VIN

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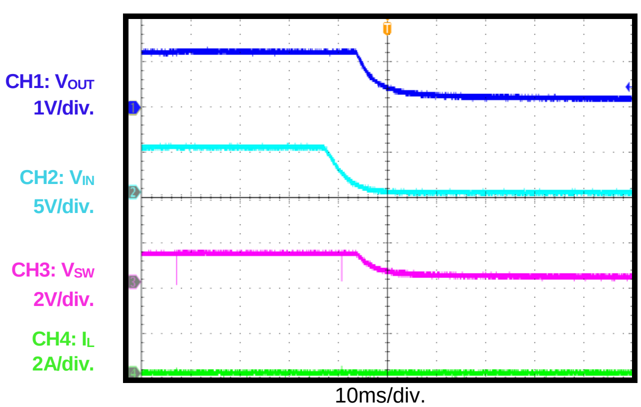
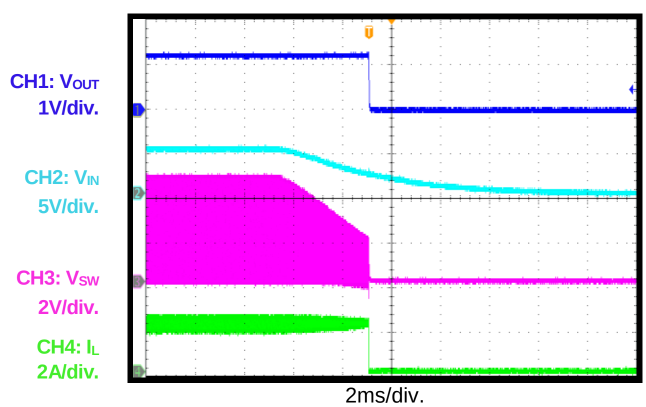


Shutdown through VIN

I_{OUT} = 2A

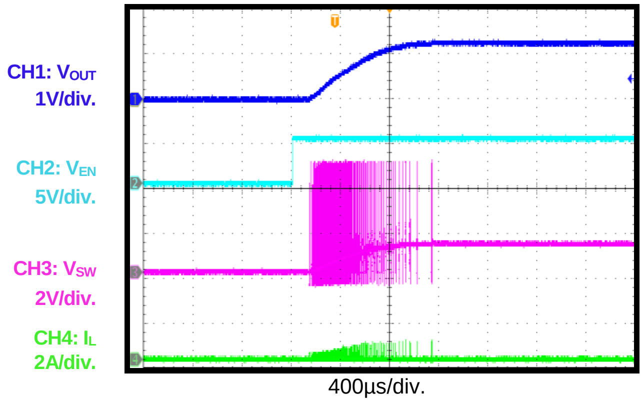


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

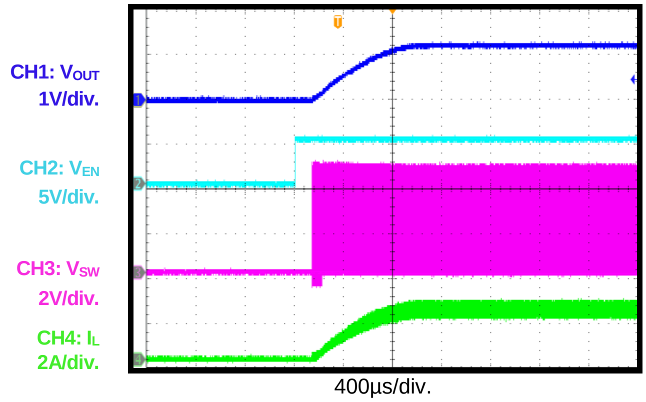
Start-Up through EN

I_{OUT} = 0A



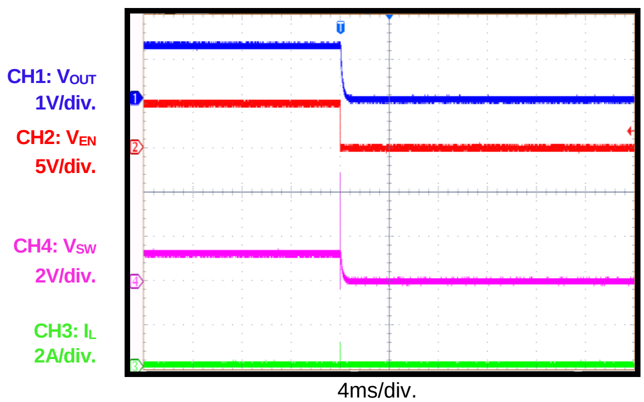
Start-Up through EN

I_{OUT} = 2A



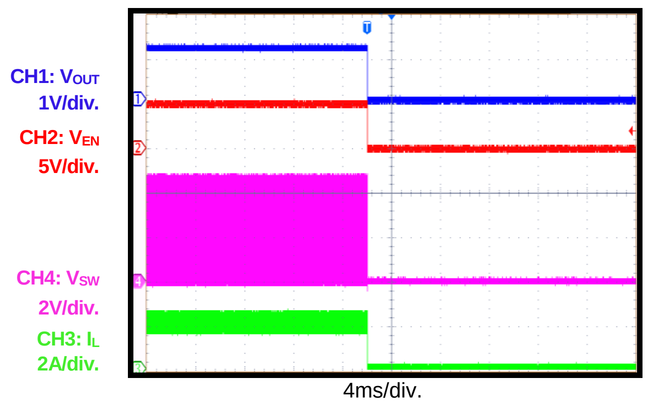
Shutdown through EN

I_{OUT} = 0A



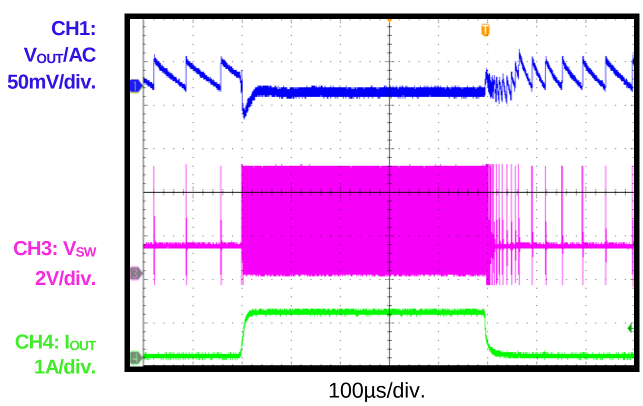
Shutdown through EN

I_{OUT} = 2A



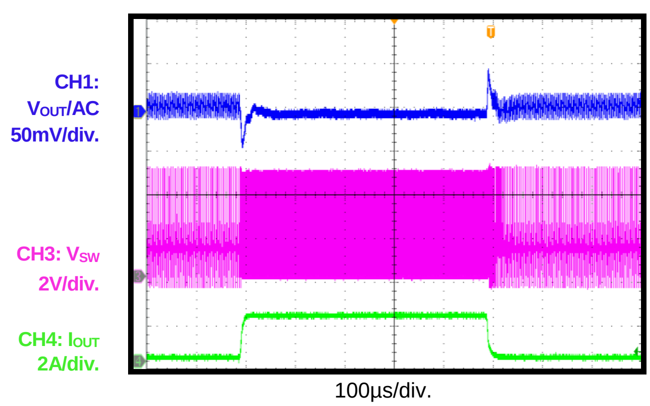
Load Transient

I_{OUT} = 0A to 1A, 1A/µs



Load Transient

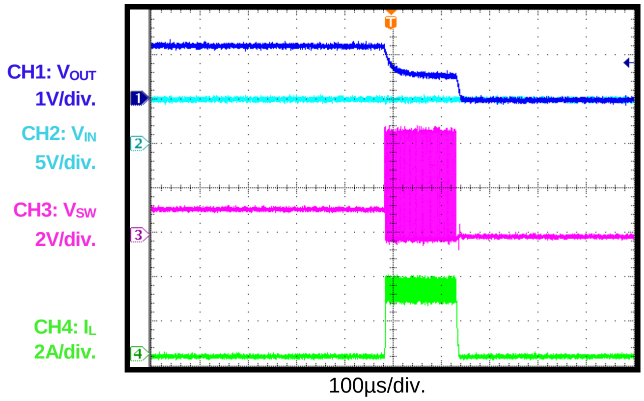
I_{OUT} = 0.1A to 2A, 1A/µs



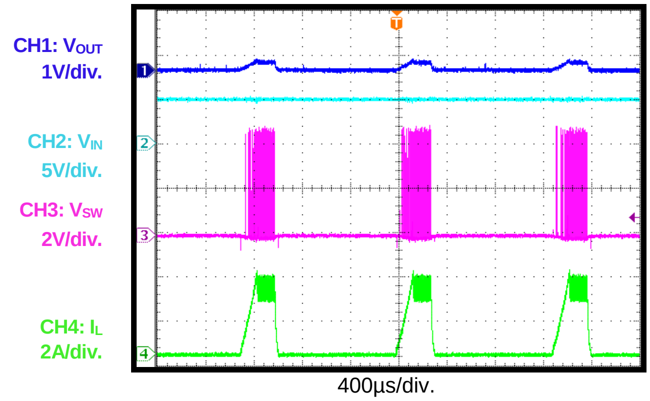
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

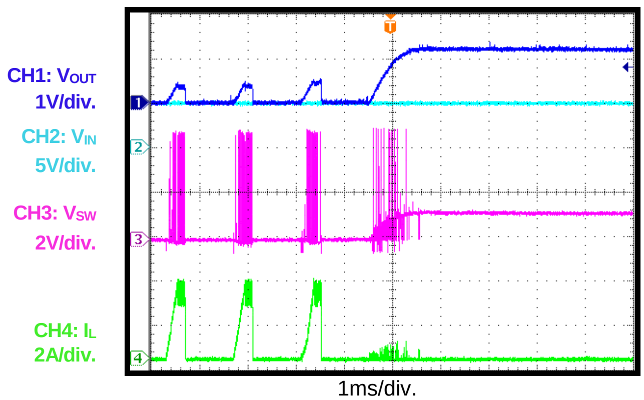
Short-Circuit Entry



Short-Circuit State



Short-Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM

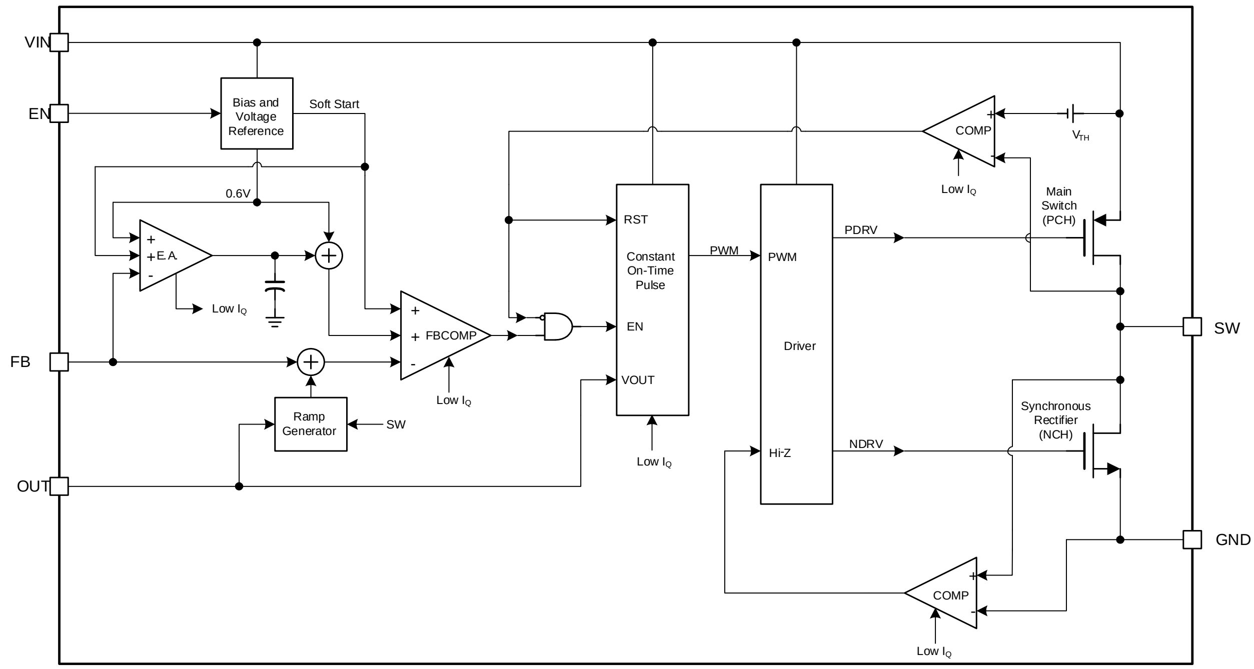


Figure 1: Functional Block Diagram

OPERATION

The MP2192 uses constant-on-time control (COT) with input voltage feed-forward to stabilize the switching frequency across the entire input voltage range. The MP2192 achieves 2A of continuous output current from a 2.5V to 5.5V input voltage, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

Constant-On-Time (COT) Control

When compared to the fixed-frequency pulse-width modulation (PWM) control, constant-on-time (COT) control offers a simpler control loop and a faster transient response. By using input voltage feed-forward, the MP2192 maintains a fairly constant switching frequency across the input and output voltage ranges. The switching pulse on time (t_{ON}) can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.91\mu s \qquad (1)$$

To prevent inductor current runaway during the load transient, the MP2192 has a fixed minimum off time of 100ns.

Sleep Mode Operation

The MP2192 features sleep mode to achieve high efficiency at extremely light loads. In sleep mode, most of the circuit blocks are turned off except for the error amplifier (EA) and PWM comparator. This reduces the operation current to a minimal value (see Figure 2).

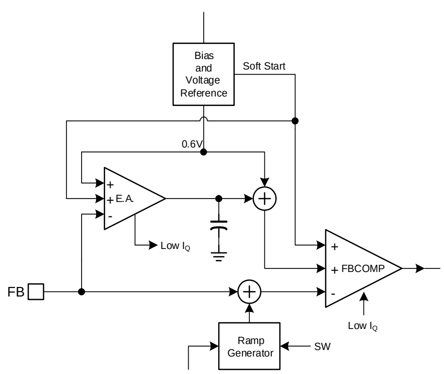


Figure 2: Operation Blocks in Sleep Mode

When the load becomes lighter, the output voltage ripple becomes larger, which then drives the error amplifier output (EAO) lower. When the EAO reaches the internal low threshold, it is clamped at that level, and the MP2192 enters sleep mode.

During sleep mode, the valley of the FB voltage (V_{FB}) is regulated to the internal reference voltage. Therefore, the average output voltage in sleep mode exceeds the output voltage in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The on-time pulse in sleep mode is longer than the on-time pulse in DCM or CCM. Figure 3 shows the relationship between the average V_{FB} and the internal reference voltage (V_{REF}) in sleep mode.

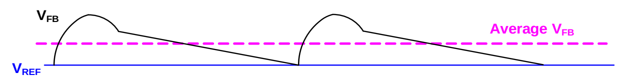


Figure 3: FB Average Voltage in Sleep Mode

When the MP2192 is in sleep mode, the average output voltage exceeds the internal reference voltage. The EAO stays low and is clamped in sleep mode. When the load increases, the PWM switching period decreases to regulate the output voltage ripple. The output voltage ripple drops relative to the PWM switching period. Once the EAO exceeds the internal low threshold, the MP2192 exits sleep mode and enters either DCM or CCM, depending on the load. In DCM or CCM, the EA regulates the average output voltage to V_{REF} (see Figure 4).

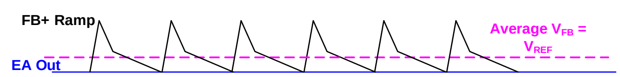


Figure 4: DCM Control

Due to the EA's clamping response time, there is always a loading hysteresis when entering or exiting sleep mode.

Advanced Asynchronous Modulation (AAM) during Light-Load Operation

The MP2192 uses advanced asynchronous modulation (AAM) power-save mode and a zero-current detection (ZCD) circuit for light-load operation.

The MP2192 uses AAM power-save mode for light loads (see Figure 5). The AAM current (I_{AAM}) is set internally. The SW on-pulse time is determined by the on-time generator and AAM comparator.

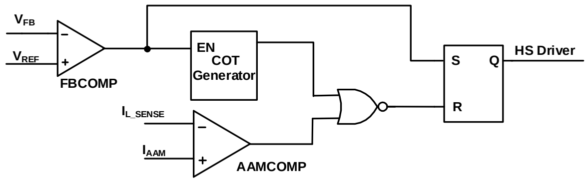


Figure 5: Simplified AAM Control Logic

Under light-load conditions, the SW on-pulse time is the longer pulse. If the AAM comparator pulse is longer than the on-time generator, the operation mode is controlled by AAM (see Figure 6).

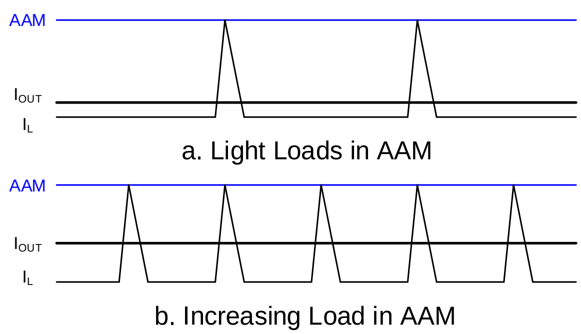


Figure 6: The AAM Comparator Controls t_{ON}

If the AAM comparator pulse is shorter than the on-time generator, the operation mode is controlled by the on-time generator (see Figure 7).

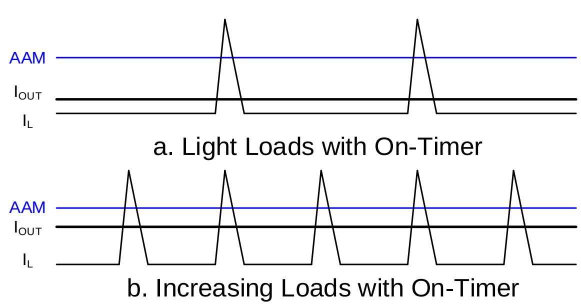


Figure 7: The On-Timer Controls t_{ON}

Figure 8 shows that when the AAM threshold decreases, t_{ON} increases gradually. For CCM, I_{OUT} must exceed at least 50% of the AAM threshold. Generally, the AAM threshold is below the inductor current during normal duty cycles.

The MP2192 uses ZCD to determine if the inductor current has started reversing. When the inductor current reaches the ZCD threshold, the LS-FET turns off.

AAM with a ZCD circuit forces the MP2192 to work in DCM under light loads, even if V_{OUT} is close to V_{IN}.

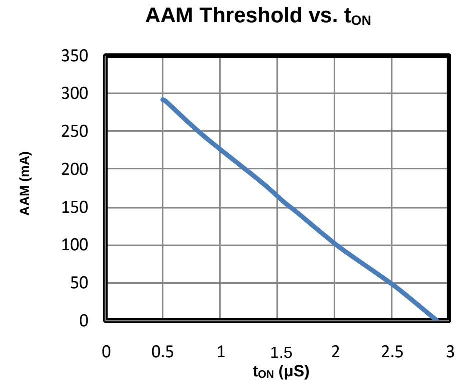


Figure 8: AAM Threshold Decreases as t_{ON} Increases

Enable (EN)

If the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.3V), the MP2192 can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MP2192. There is an internal 1MΩ resistor connected from EN to ground.

When the device is disabled, the part enters output discharge mode automatically. The device's internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start (SS)

The MP2192 has built-in soft start that ramps up the output voltage at a controlled slew rate to avoid overshooting at start-up. The soft-start time is about 1.1ms.

Current Limit

The MP2192 has a typical 3.5A HS-FET current limit. When the high-side switch reaches its current limit, the MP2192 remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

Short Circuit and Recovery

The MP2192 triggers short-circuit protection (SCP) when it reaches its current limit and attempts to recover with hiccup mode. The MP2192 disables the output power stage, discharges the soft-start capacitor, and attempts soft start again automatically. If the short-circuit condition remains after soft start ends, the MP2192 repeats this cycle until the short circuit is removed and the output rises back to the regulation level.

Over-Voltage Protection (V_{OUT} OVP)

The MP2192 monitors V_{FB} to detect over-voltage (OV) conditions. If V_{FB} rises above 117% of the target voltage, the controller enters a dynamic regulation period. During this period, the LS-FET stays on until the low-side current drops to -1.5A. This discharges the output to keep it within the normal range.

If the OV condition still remains, the LS-FET turns on again after a 1µs time delay. The MP2192 exits this regulation period when V_{FB} drops below 104% of V_{REF}. If the dynamic regulation cannot limit the increasing output voltage, and input OVP occurs when V_{IN} exceeds 6.2V, the MP2192 stops switching until the input voltage drops below 5.7V. Then the MP2192 resumes operation.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application Circuit on page 18). Select a feedback resistor (R1) that reduces the output voltage leakage current. It is recommended for R1 to be between 100kΩ and 200kΩ. There is no strict requirement for the feedback resistor. Select R1 to exceed 10kΩ. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 9 shows the feedback circuit.

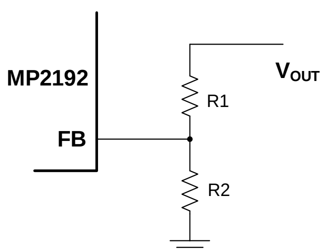


Figure 9: Feedback Network

Table 1 lists recommended resistor values for common output voltages.

Table1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

Most applications work best with a 1µH to 2.2µH inductor. Select an inductor with a DC resistance below 50mΩ to optimize efficiency.

A high-frequency switch-mode power supply with a magnetic device has strong electronic magnetic inference. Do not use unshielded power inductors. Metal alloy inductors or multiplayer chip power inductors are ideal shielded inductors because they can effectively reduce electromagnetic interference.

For most designs, estimate the inductance value with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits. Table 2 lists our power inductor recommendations.

Table 2: Power Inductor Selection

Part Number	Inductance Value	Manufacturer
MPL-AL4020-1R0	1µH	MPS
MPL-AL4020-1R2	1.2µH	MPS
MPL-AL4020-1R5	1.5µH	MPS
MPL-AL4020-2R2	2.2µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. Higher output voltages may require a 44µF capacitor to increase system stability.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1μF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Low-ESR ceramic capacitors are recommended to limit the output voltage ripple. Estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

Design Example

Table 3 lists a design example following the application guidelines for the specifications below.

Table 3: Design Example

V_{IN}	5V
V_{OUT}	1.2V
f_{SW}	1100kHz

For the detailed application schematic, see Figure 11 on page 19. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 6. For more device applications, refer to the related evaluation board datasheets.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 10 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short, and route it away from the feedback network.
5. Keep the V_{OUT} sense line as short as possible, and and away from the power inductor (especially the surrounding inductor).

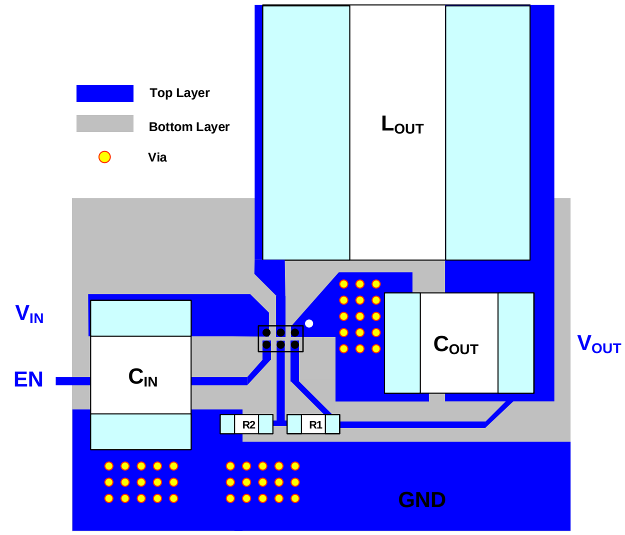


Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

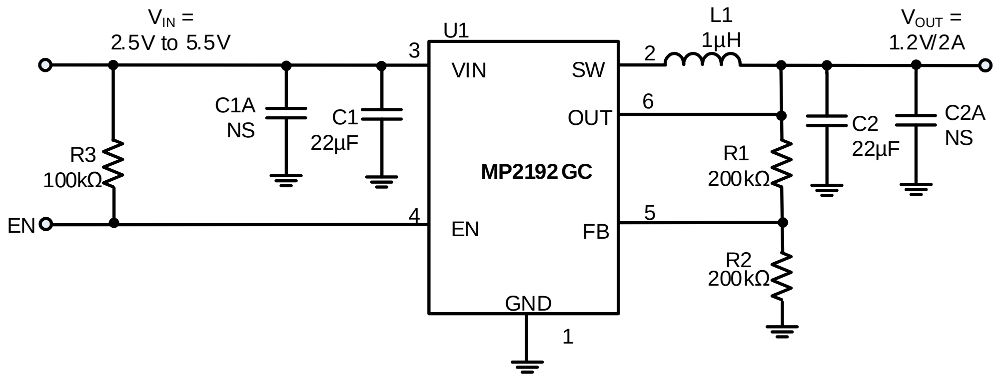


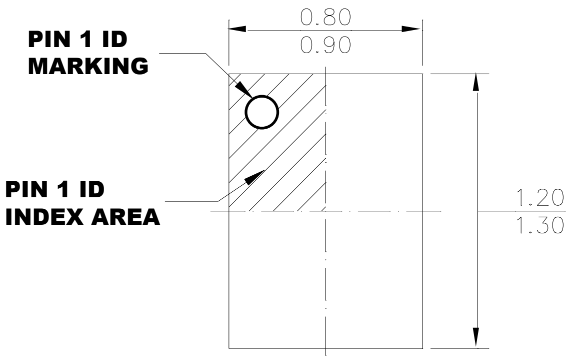
Figure 11: Typical Application Circuit for the MP2192GC

Note:

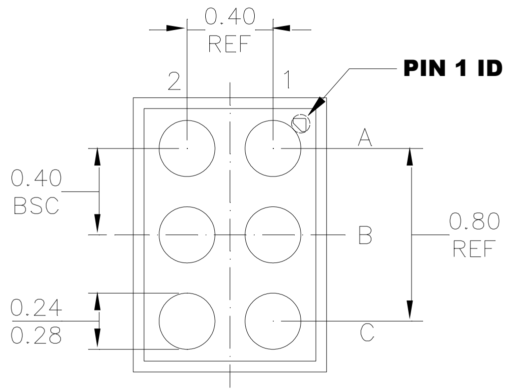
8) For applications where V_{IN} < 3.3V, additional input capacitors may be required.

PACKAGE INFORMATION

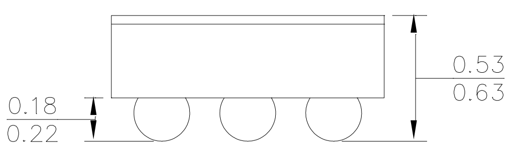
WLCSP-6 (0.85mmx1.25mm)



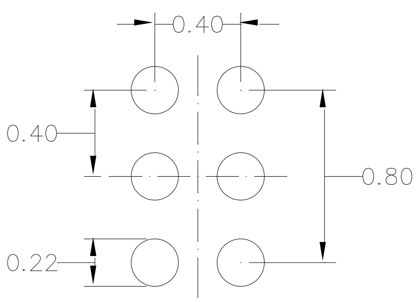
TOP VIEW



BOTTOM VIEW



SIDE VIEW

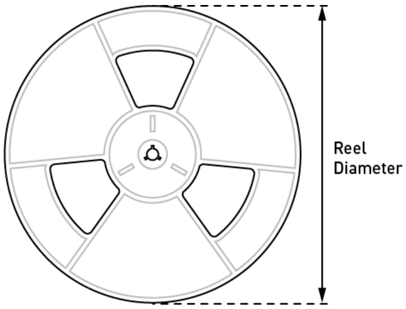


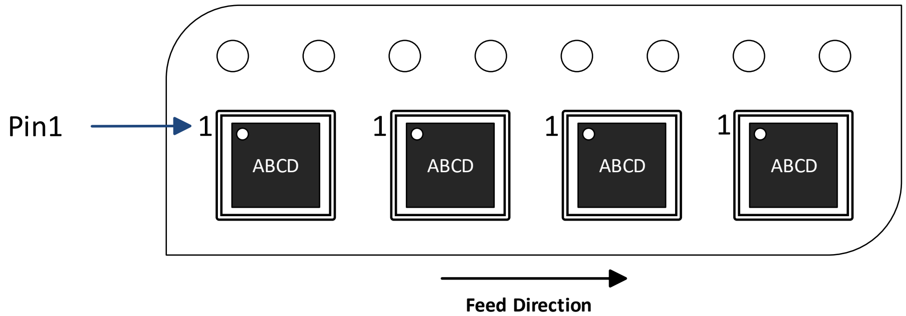
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2192GC–Z	WLCSP-6 (0.85mmx1.25mm)	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/12/2021	Initial Release	-