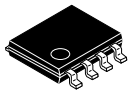
# Single-Channel High-Side Gate Drive IC

# FAN73611



SOIC8
(8−SOP)
CASE 751EG

## Description

The FAN73611 is a monolithic high−side gate drive IC that can drive MOSFETs and IGBTs operating up to +600 V. **onsemi**'s high−voltage process and commonmode noise canceling techniques provide stable operation of the high−side driver under high dv/dt noise circumstances. An advanced level−shift circuit offers high−side gate driver operation up to $V_S$ = −9.8 V (typical) for $V_{BS}$ = 15 V. The UVLO circuits prevents malfunction when $V_{DD}$ or $V_{BS}$ is lower than the specified threshold voltage. The output drivers typically source/sink 250 mA/500 mA; respectively, which is suitable for Plasma Display Panel (PDP) application, motor drive inverter, and switching mode power supply applications.

## Features

- Floating Channel of Bootstrap Operation to +600 V
- 250 mA / 500 mA Sourcing/Sinking Current Driving Capability
- Common−Mode dv/dt Noise−Cancelling Circuit
- 3.3 V and 5 V Input Logic Compatible
- Output In Phase with Input Signal
- Under−Voltage Lockout for $V_{DD}$ and $V_{BS}$
- 8−Lead Small Outline Package (SOP)
- This is a Pb−Free Device

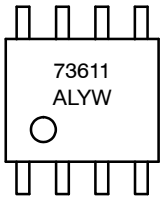
## Applications

- Electronic Ballast
- Switching−Mode Power Supply (SMPS)

## Related Resources

- AN−6076 – Design and Application Guide of Bootstrap Circuit for High−Voltage Gate−Drive IC
- AN−9052 – Design Guide for Selection of Bootstrap Components
- AN−8102 – Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

## MARKING DIAGRAM




73611 = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

## ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

## TYPICAL APPLICATION DIAGRAMS

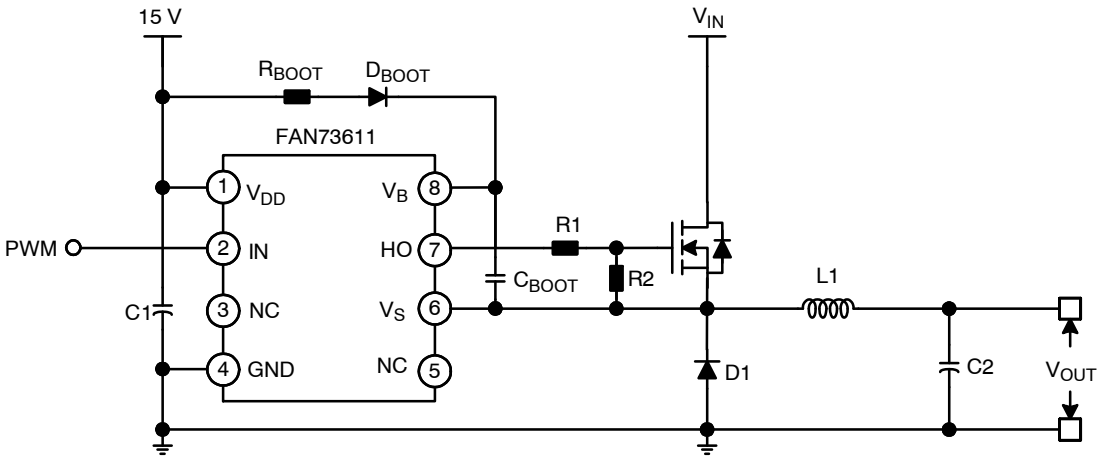



**Figure 1. Step−Down (Buck) DC−DC Converter Application**

## INTERNAL BLOCK DIAGRAM

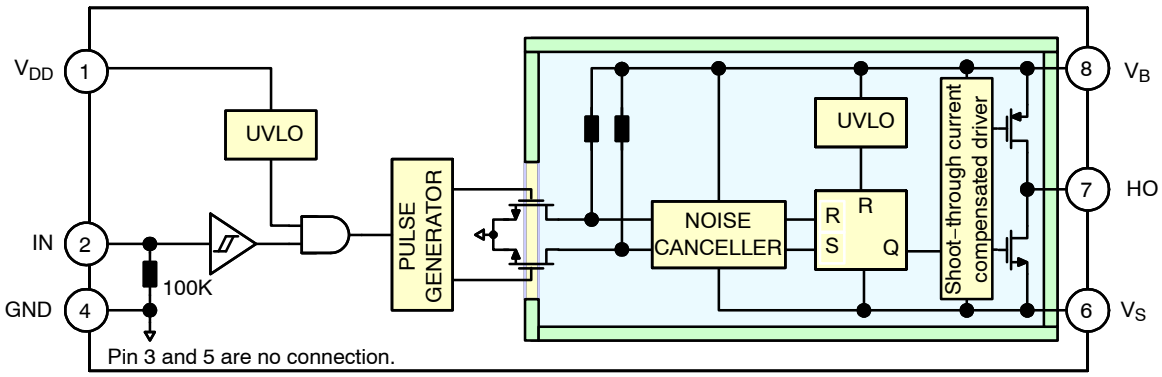



**Figure 2. Functional Block Diagram**

## PIN CONFIGURATION

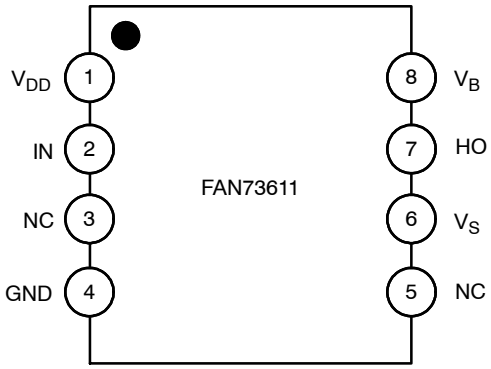



**Figure 3. Pin Configuration (Top View)**

### PIN DEFINITIONS

| Pin No. | Name | Description |
|---|---|---|
| 1 | $V_{DD}$ | Supply Voltage |
| 2 | IN | Logic Input for High−Side Gate Driver Output |
| 3 | NC | No Connection |
| 4 | GND | Ground |
| 5 | NC | No Connection |
| 6 | $V_S$ | High−Voltage Floating Supply Return |
| 7 | HO | High−Side Driver Output |
| 8 | $V_B$ | High−Side Floating Supply |

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25°C, unless otherwise specified.)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_S$ | High−Side Floating Offset Voltage | $V_B$ − 25 | $V_B$ + 0.3 | V |
| $V_B$ | High−Side Floating Supply Voltage | −0.3 | 625.0 | V |
| $V_{HO}$ | High−Side Floating Output Voltage | $V_S$ − 0.3 | $V_B$ + 0.3 | V |
| $V_{DD}$ | Low−Side and Logic Supply Voltage | −0.3 | 25.0 | V |
| $V_{IN}$ | Logic Input Voltage | −0.3 | $V_{DD}$ + 0.3 | V |
| $dV_S/dt$ | Allowable Offset Voltage Slew Rate | − | ±50 | V/ns |
| $P_D$ | Power Dissipation (Notes 1, 2, 3) | − | 0.625 | W |
| $\theta_{JA}$ | Thermal Resistance | − | 200 | °C/W |
| $T_J$ | Junction Temperature | −55 | +150 | °C |
| $T_{STG}$ | Storage Temperature | −55 | +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR−4 glass epoxy material).
2. Refer to the following standards:
   JESD51−2: Integral circuits thermal test method environmental conditions, natural convection, and
   JESD51−3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed power dissipation ($P_D$) under any circumstances.

**RECOMMENDED OPERATING RATINGS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_B$ | High−Side Floating Supply Voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High−Side Floating Supply Offset Voltage | 6 − $V_{DD}$ | 600 | V |
| $V_{HO}$ | High−Side Output Voltage | $V_S$ | $V_B$ | V |
| $V_{IN}$ | Logic Input Voltage | GND | $V_{DD}$ | V |
| $V_{DD}$ | Supply Voltage | 10 | 20 | V |
| $T_A$ | Operating Ambient Temperature | −40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**ELECTRICAL CHARACTERISTICS** ($V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15.0 V and $T_A$ = 25°C unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to GND. The $V_O$ and $I_O$ parameters are relative to $V_S$ and are applicable to the respective outputs HO.)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY SECTION** | | | | | | |
| $I_{QDD}$ | Quiescent $V_{DD}$ Supply Current | $V_{IN}$ = 0 V or 5 V, $C_{LOAD}$ = 1000 pF | – | 80 | 140 | μA |
| $I_{PDD}$ | Operating $V_{DD}$ Supply Current | $C_{LOAD}$ = 1000 pF, $f_{IN}$ = 20 kHz, RMS value | – | 80 | 160 | μA |
| $V_{DDUV+}$ $V_{BSUV+}$ | $V_{DD}$ and $V_{BS}$ Supply Under−Voltage Positive Going Threshold Voltage | $V_{DD}$ = Sweep, $V_{BS}$ = Sweep | 7.8 | 8.8 | 9.8 | V |
| $V_{DDUV−}$ $V_{BSUV−}$ | $V_{DD}$ and $V_{BS}$ Supply Under−Voltage Negative Going Threshold Voltage | $V_{DD}$ = Sweep, $V_{BS}$ = Sweep | 7.3 | 8.3 | 9.3 | V |
| $V_{DDHYS}$ $V_{BSHYS}$ | $V_{DD}$ and $V_{BS}$ Supply Under−Voltage Lockout Hysteresis Voltage | $V_{DD}$ = Sweep, $V_{BS}$ = Sweep | – | 0.5 | – | V |
| $I_{LK}$ | Offset Supply Leakage Current | $V_B$ = $V_S$ = 600 V | – | – | 10 | μA |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | $V_{IN}$ = 0 V or 5 V, $C_{LOAD}$ = 1000 pF | | 60 | 100 | μA |
| $I_{PBS}$ | Operating $V_{BS}$ Supply Current | $C_{LOAD}$ = 1000 pF, $f_{IN}$ = 20 kHz, RMS value | | 420 | 600 | μA |
| **INPUT LOGIC SECTION** | | | | | | |
| $V_{IH}$ | Logic “1” Input Voltage | | 2.5 | – | – | V |
| $V_{IL}$ | Logic “0” Input Voltage | | – | – | 0.8 | V |
| $I_{IN+}$ | Logic Input High Bias Current | $V_{IN}$ = 5 V | – | 50 | 75 | μA |
| $I_{IN−}$ | Logic Input Low Bias Current | $V_{IN}$ = 0 V | – | – | 2 | μA |
| $R_{IN}$ | Input Pull−Down Resistance | | 60 | 100 | – | kΩ |
| **GATE DRIVE OUTPUT SECTION** | | | | | | |
| $V_{OH}$ | High Level Output Voltage ($V_{BIAS}$ − $V_O$) | No Load | – | – | 0.1 | V |
| $V_{OL}$ | Low Level Output Voltage | No Load | – | – | 0.1 | V |
| $I_{O+}$ | Output High, Short−Circuit Pulsed Current | $V_{HO}$ = 0 V, $V_{IN}$ = 5 V, PW ≤ 10 μs | 200 | 250 | – | mA |
| $I_{O−}$ | Output Low, Short−Circuit Pulsed Current | $V_{HO}$ = 15 V, $V_{IN}$ = 0 V, PW ≤ 10 μs | 400 | 500 | – | mA |
| $V_S$ | Allowable Negative $V_S$ Pin Voltage for IN Signal Propagation to HO | $V_{BS}$ = 15 V | – | −9.8 | −7.0 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($V_{DD}$ = $V_{BS}$ = 15 V, $C_{LOAD}$ = 1000 pF, and $T_A$ = 25°C, unless otherwise specified.)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn−on Propagation Delay Time | $V_S$ = 0 V | 70 | 120 | 170 | ns |
| $t_{off}$ | Turn−off Propagation Delay Time | $V_S$ = 0 V | 70 | 120 | 170 | ns |
| $t_r$ | Turn−on Rise Time | | – | 70 | 140 | ns |
| $t_f$ | Turn−off Fall Time | | – | 30 | 60 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS

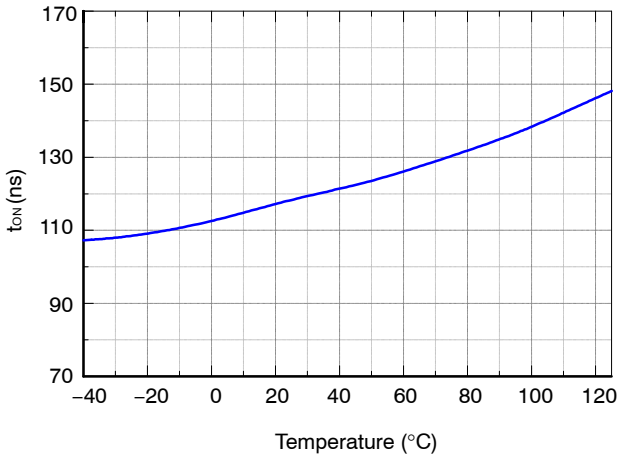



**Figure 4. Turn−On Propagation Delay vs. Supply Voltage**

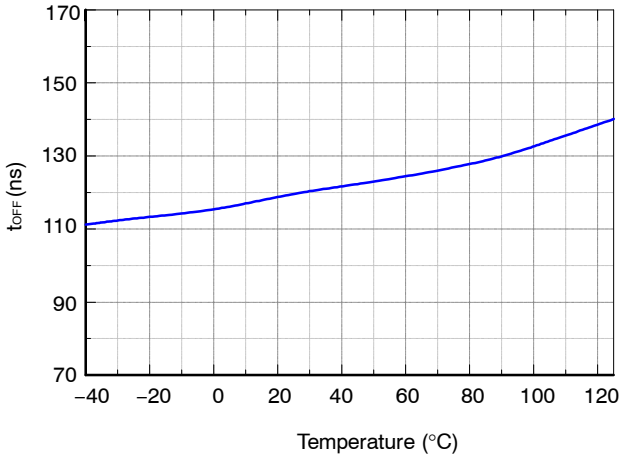



**Figure 5. Turn−Off Propagation Delay vs. Temperature**

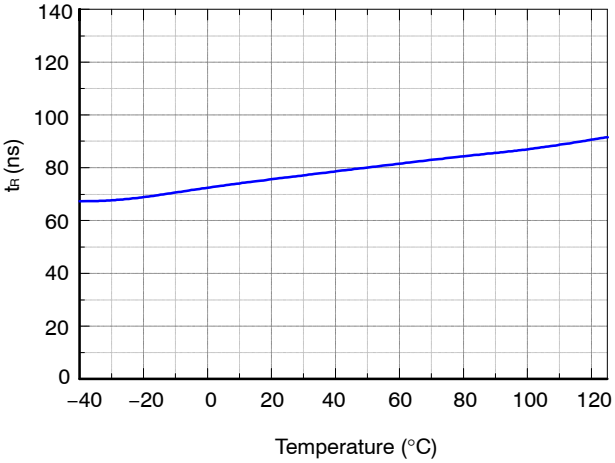



**Figure 6. Turn−On Rise Time vs. Temperature**

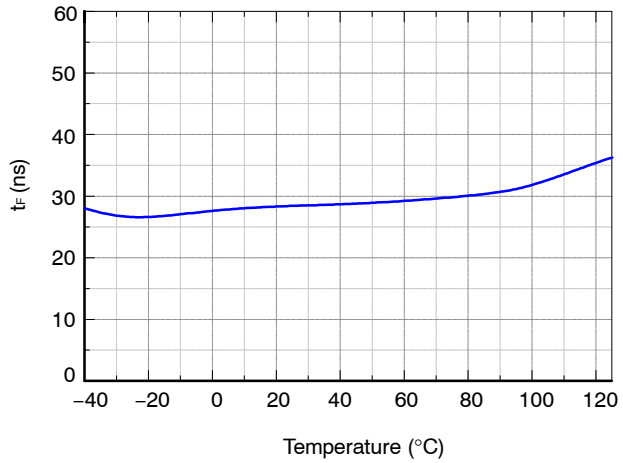



**Figure 7. Turn−Off Fall Time vs. Temperature**

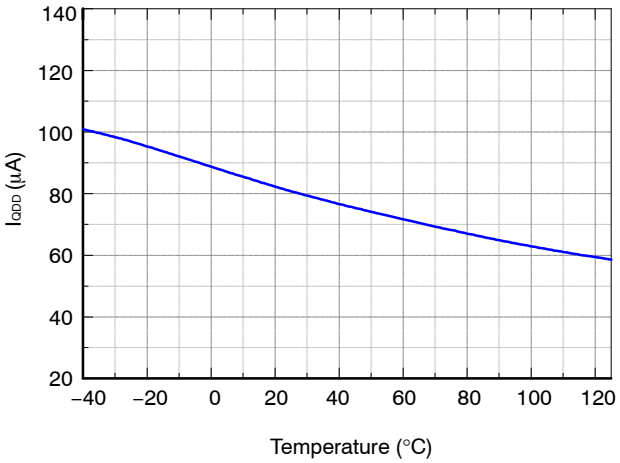



**Figure 8. Quiescent $V_{DD}$ Supply Current vs. Temperature**

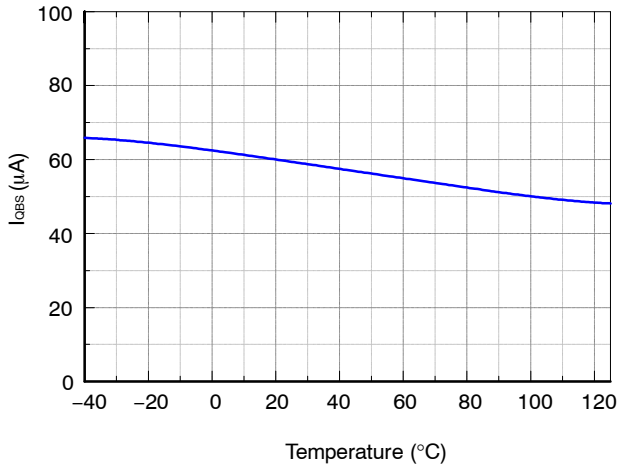



**Figure 9. Quiescent $V_{BS}$ Supply Current vs. Temperature**

## TYPICAL CHARACTERISTICS (Continued)

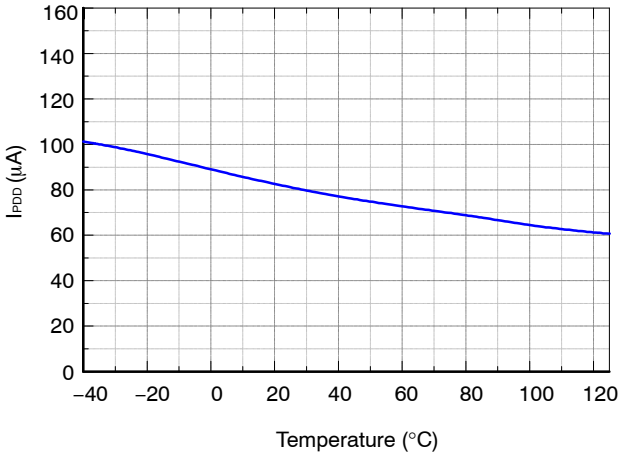



**Figure 10. Operating $V_{DD}$ Supply Current vs. Temperature**

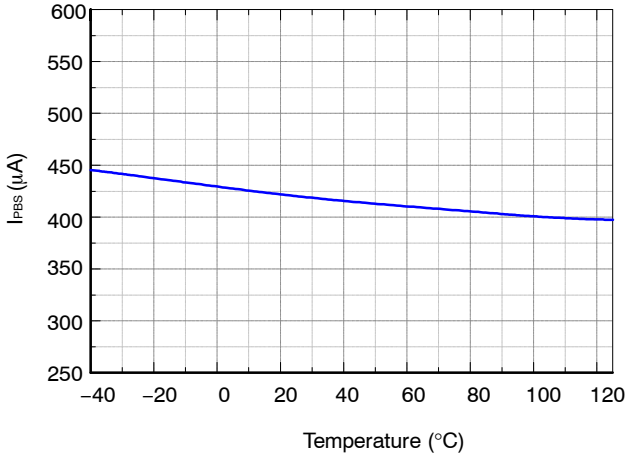



**Figure 11. Operating $V_{BS}$ Supply Current vs. Temperature**

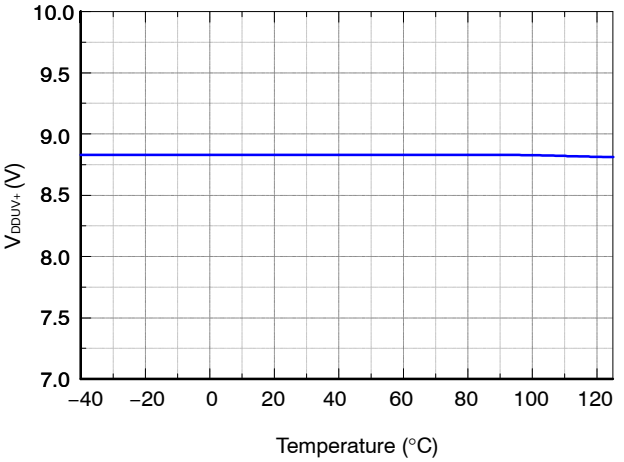



**Figure 12. $V_{DD}$ UVLO+ vs. Temperature**

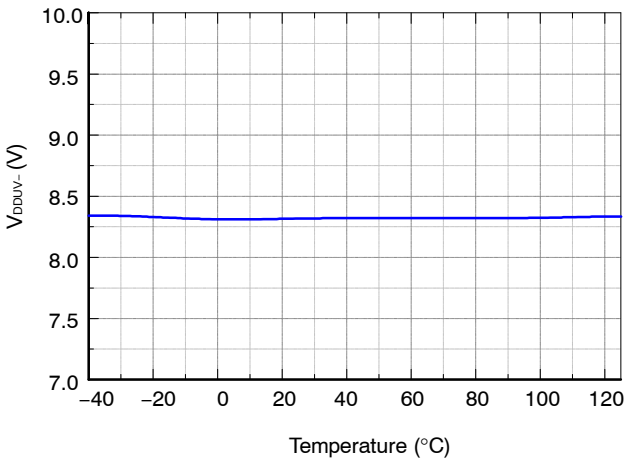



**Figure 13. $V_{DD}$ UVLO− vs. Temperature**

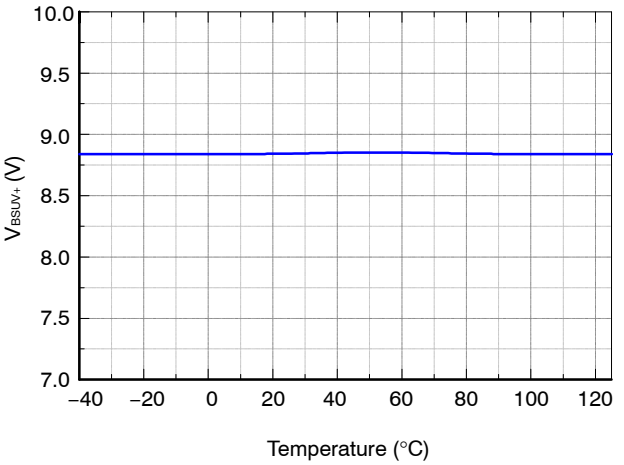



**Figure 14. $V_{BS}$ UVLO+ vs. Temperature**

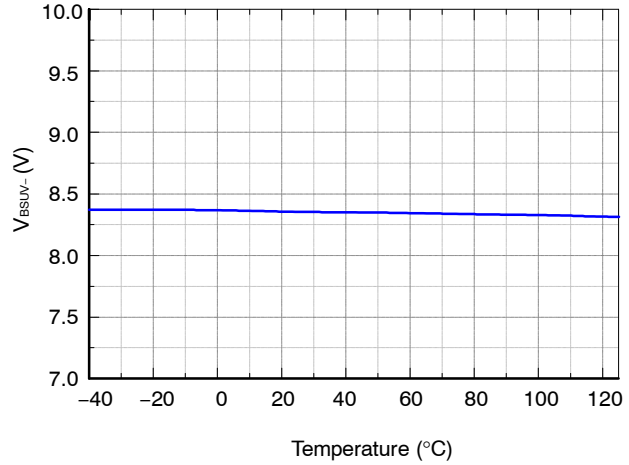



**Figure 15. $V_{BS}$ UVLO− vs. Temperature**

## TYPICAL CHARACTERISTICS (Continued)

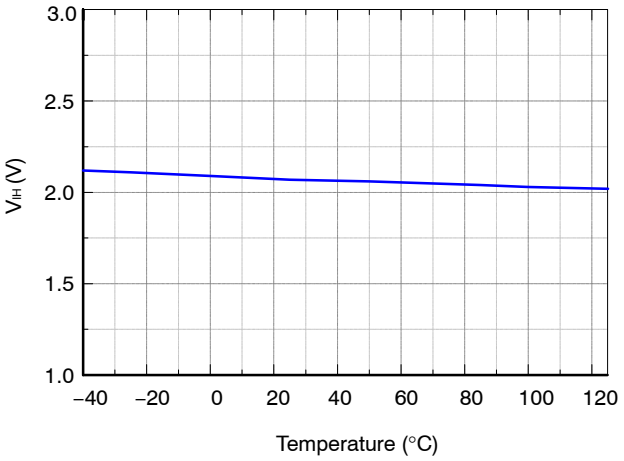



**Figure 16. Logic HIGH Input Voltage vs. Temperature**

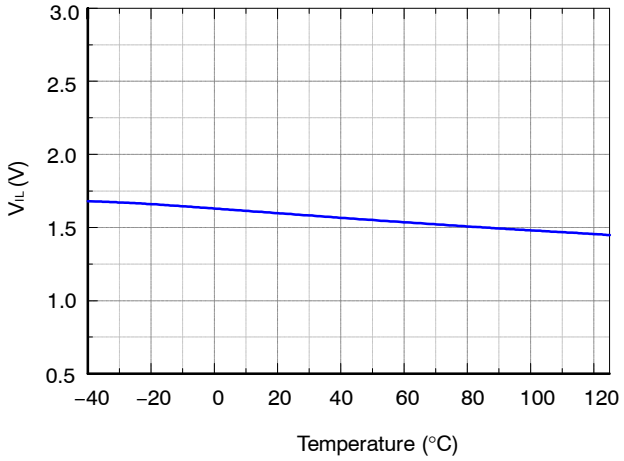



**Figure 17. Logic LOW Input Voltage vs. Temperature**

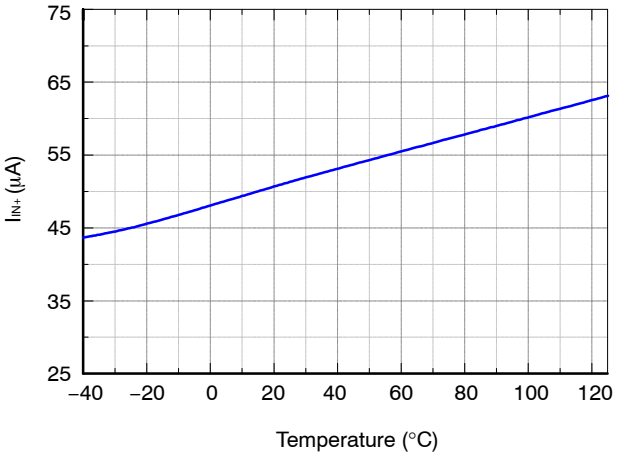



**Figure 18. Logic HIGH Input Bias Current vs. Temperature**

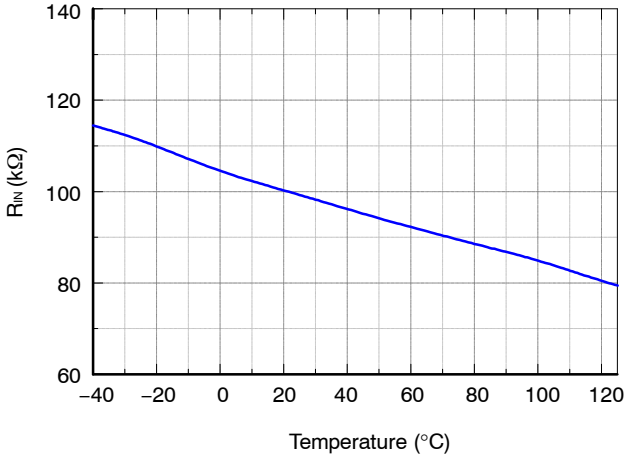



**Figure 19. Input Pull−Down Resistance vs. Temperature**

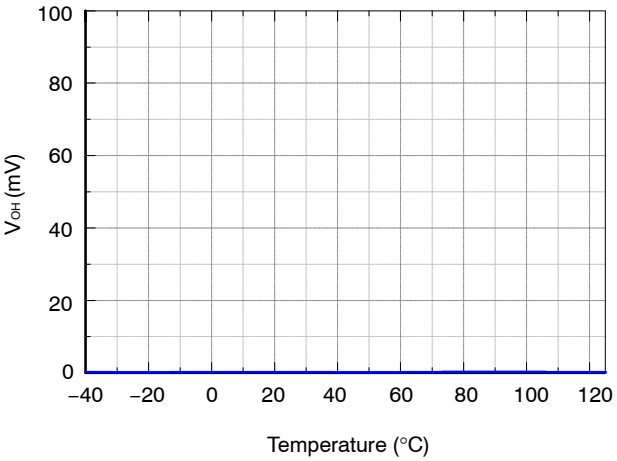



**Figure 20. High−Level Output Voltage vs. Temperature**

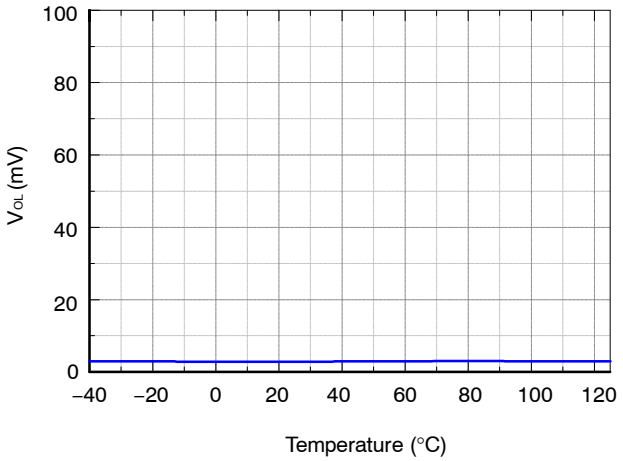



**Figure 21. Low−Level Output Voltage vs. Temperature**

## TYPICAL CHARACTERISTICS (Continued)

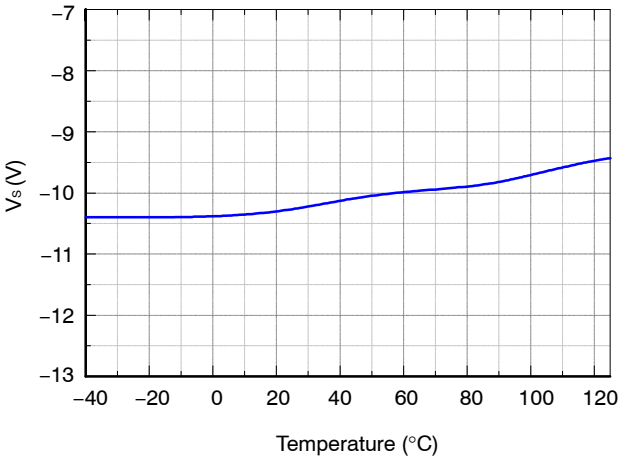



**Figure 22. Allowable Negative $V_S$ Voltage vs. Temperature**

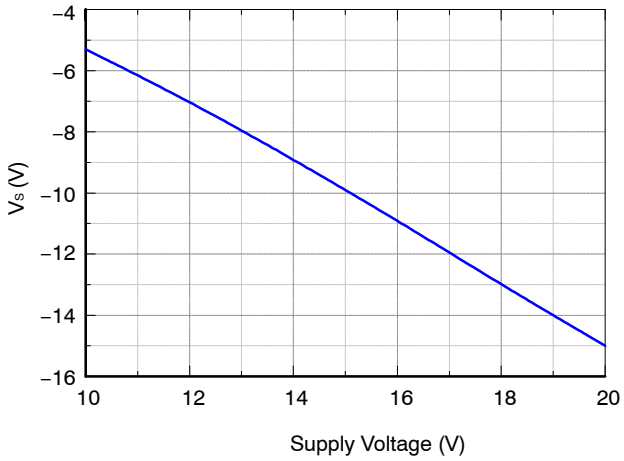



**Figure 23. Allowable Negative $V_S$ Voltage vs. Supply Voltage**

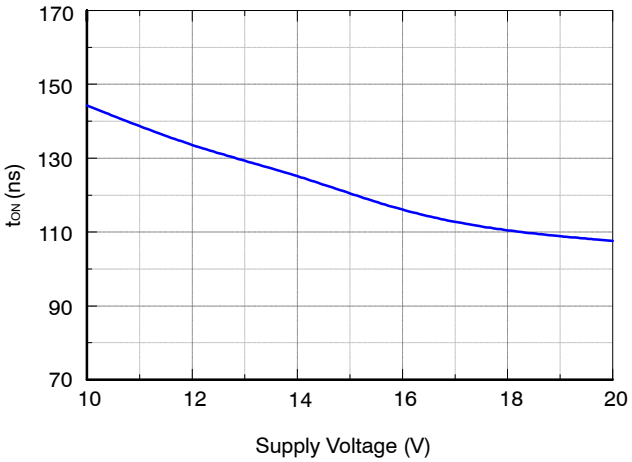



**Figure 24. Turn−On Propagation Delay vs. Supply Voltage**

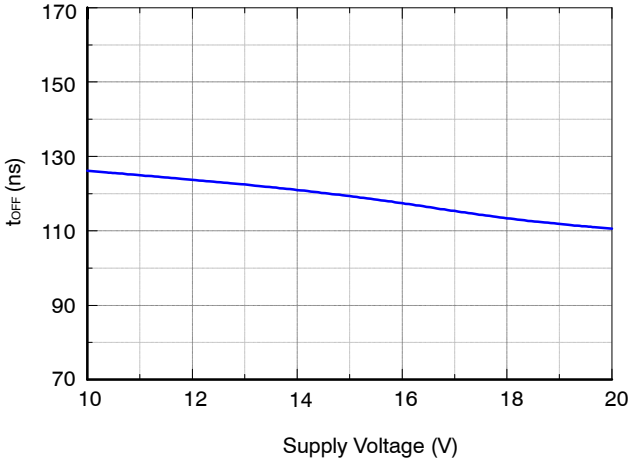



**Figure 25. Turn−Off Propagation Delay vs. Supply Voltage**

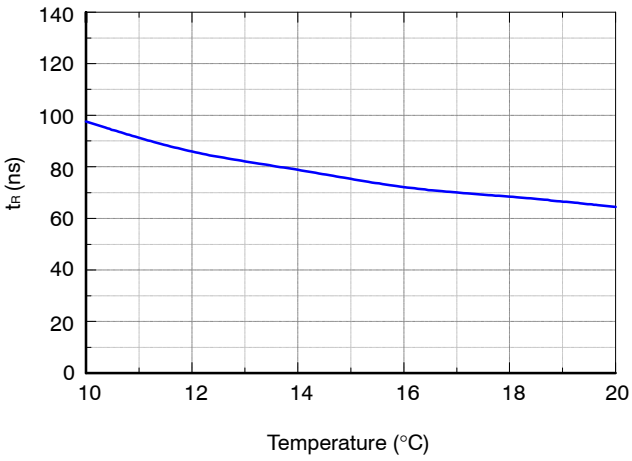



**Figure 26. Turn−On Rise Time vs. Supply Voltage**

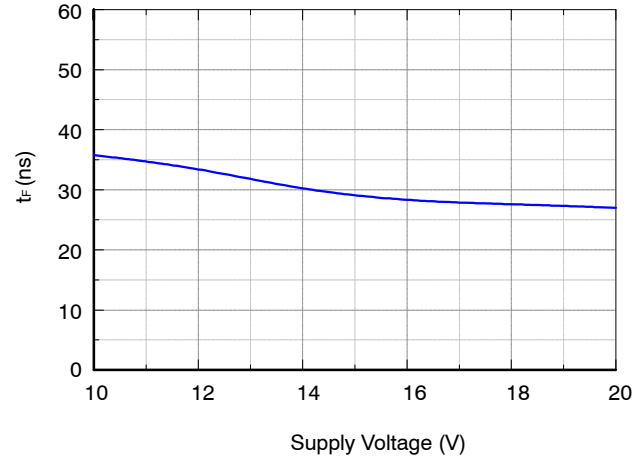



**Figure 27. Turn−Off Fall Time vs. Supply Voltage**

## TYPICAL CHARACTERISTICS (Continued)

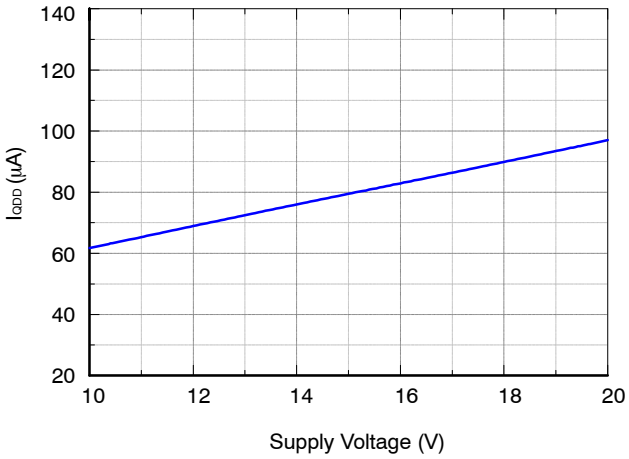



**Figure 28. Quiescent $V_{DD}$ Supply Current vs. Supply Voltage**

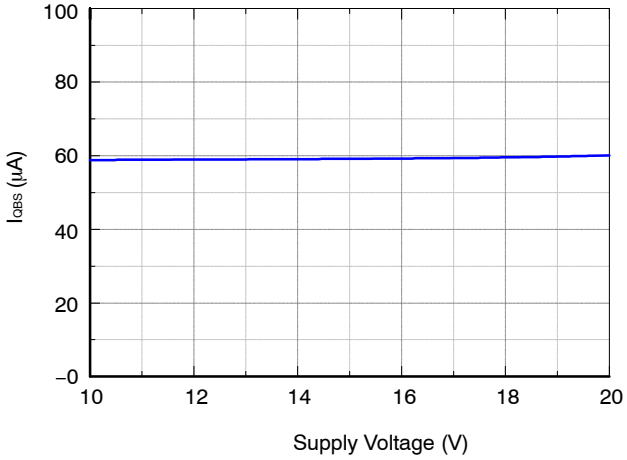



**Figure 29. Quiescent $V_{BS}$ Supply Current vs. Supply Voltage**

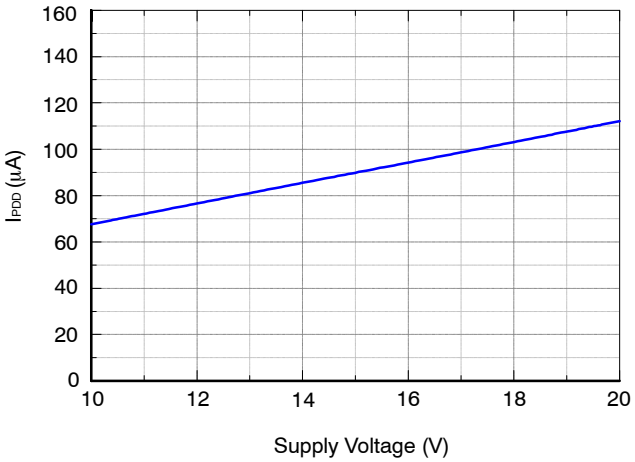



**Figure 30. Operating $V_{DD}$ Supply Current vs. Supply Voltage**

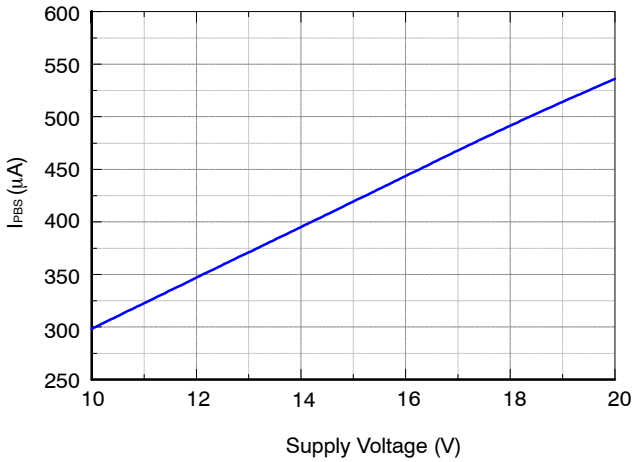



**Figure 31. Operating $V_{DD}$ Supply Current vs. Supply Voltage**

## SWITCHING TIME DEFINITIONS

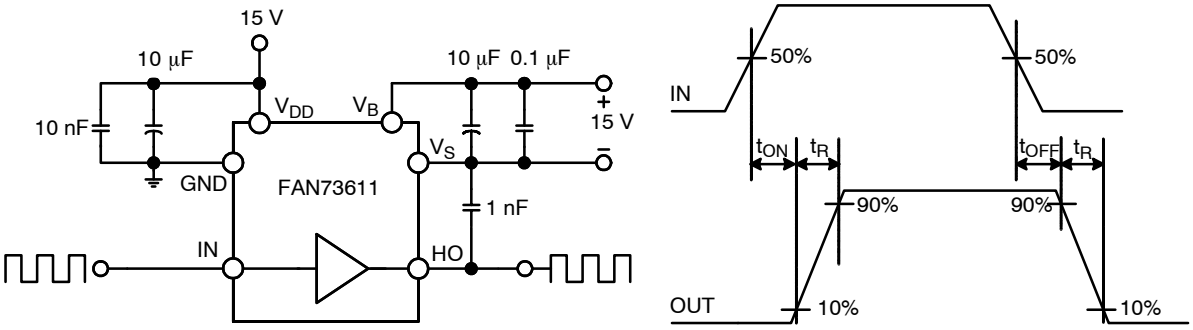



**Figure 32. Switching Time Test Circuit and Waveforms Definitions**

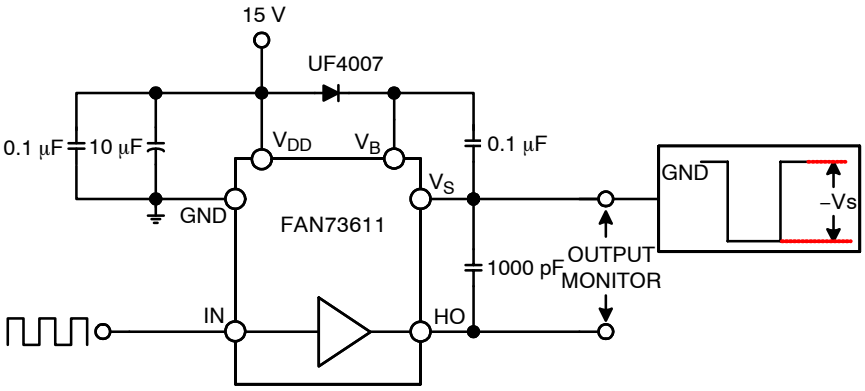



**Figure 33. Floating Supply Voltage Transient Test**

## ORDERING INFORMATION

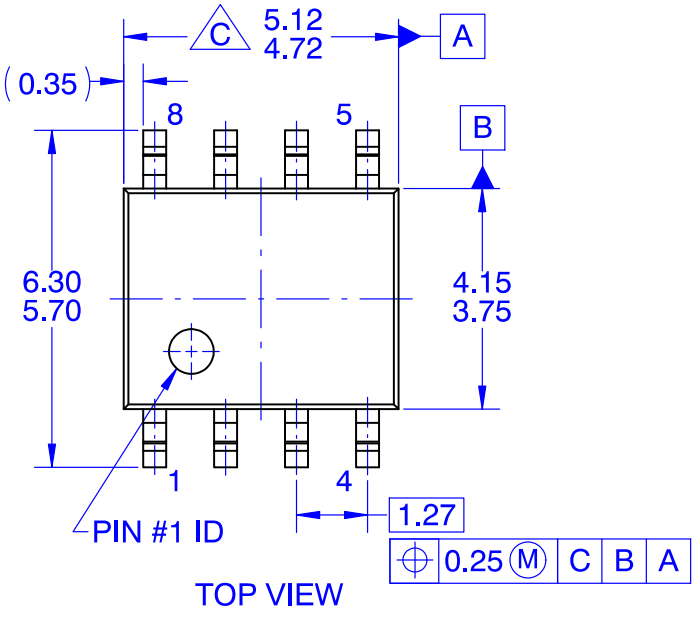
| Device | Package | Operating Temperature | Description | Shipping† |
|---|---|---|---|---|
| FAN73611MX (Note 4) | SOIC8 (8−SOP) (Pb−Free) | −40°C~+125°C | Lightning Application | 3000 / Tape & Reel |

4. This device has passed wave soldering test by JESD22A−111.

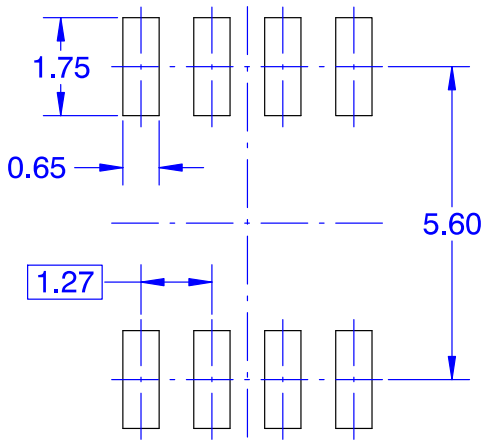
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**SOIC8**
CASE 751EG
ISSUE O

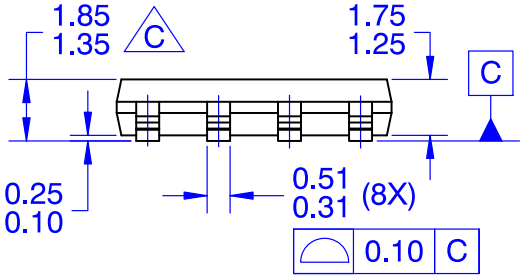
DATE 30 SEP 2016



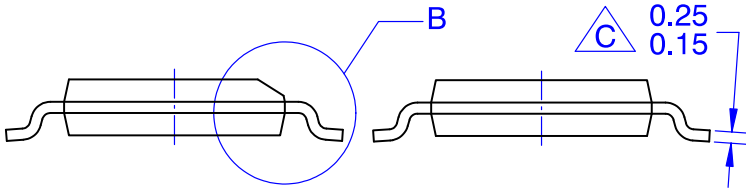

TOP VIEW



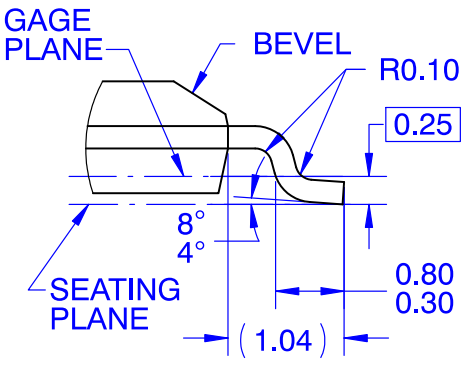

LAND PATTERN RECOMMENDATION




FRONT VIEW




SIDE VIEW




DETAIL "B"
SCALE 2:1

NOTES: UNLESS OTHERWISED SPECIFIED

A. THIS PACKAGE CONFORMS TO JEDEC MS–012 VARIATION A EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS
C OUT OF JEDEC STANDARD VALUE
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
E. LAND PATTERN AS PER IPC SOIC127P600X175–8M

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC8** | **PAGE 1 OF 1** |

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