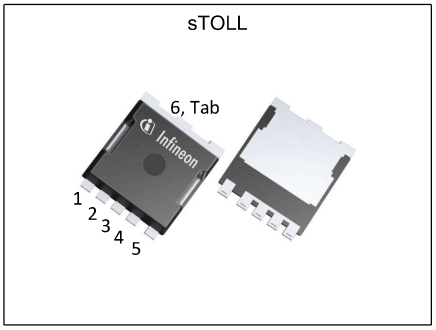
MOSFET

OptiMOS™5 Power-Transistor, 80 V



Features

- Optimized for low voltage motor drives application
- Optimized for battery powered applications
- Enables automated optical solder inspection
- 100% avalanche tested
- N-channel
- 175°C rated
- Pb-free lead plating : RoHS compliant

Product validation

Fully qualified according to JEDEC for Industrial Applications

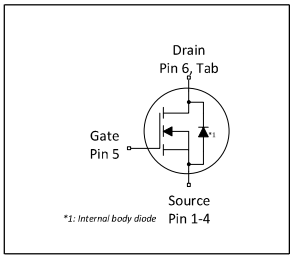


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	1.9	mΩ
I_D	290	A
Q_{oss}	112	nC
Q_G(0V..10V)	94	nC

Type / Ordering Code	Package	Marking	Related Links
IST019N08NM5	sTOLL	019N08N5	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	290 205 32	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{THJA}=40 °C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	1160	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	345	mJ	I_D=100 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	313 3.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=40 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.3	0.48	°C/W	-
Device on PCB, 6 cm² cooling area	R_{thJA}	-	-	40	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	-	3.8	V	V_{DS}=V_{GS}, I_D=148 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.6 2.2	1.9 2.85	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=6 V, I_D=50 A
Gate resistance[1)]	R_G	-	0.9	-	Ω	-
Transconductance	g_{fs}	125	190	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6600	-	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance	C_{oss}	-	1100	-	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	48	-	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	24	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	29	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	10	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	31	-	nC	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	20	-	nC	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	20	-	nC	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	32	-	nC	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	94	132	nC	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	81	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	112	-	nC	V_{DS}=40 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See ″Gate charge waveforms″ for parameter definition

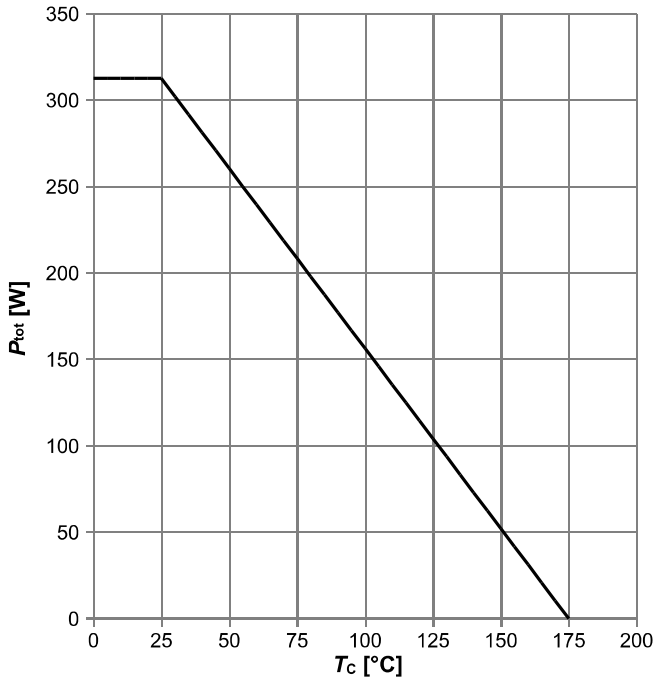
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	245	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1160	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.9	1.1	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	49	-	ns	V_R=40 V, I_F=100 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	66	-	nC	V_R=40 V, I_F=100 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

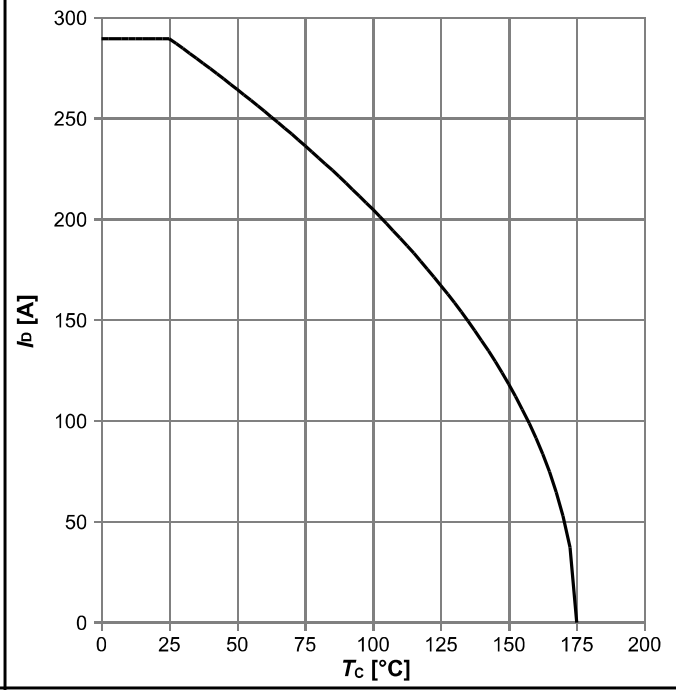
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



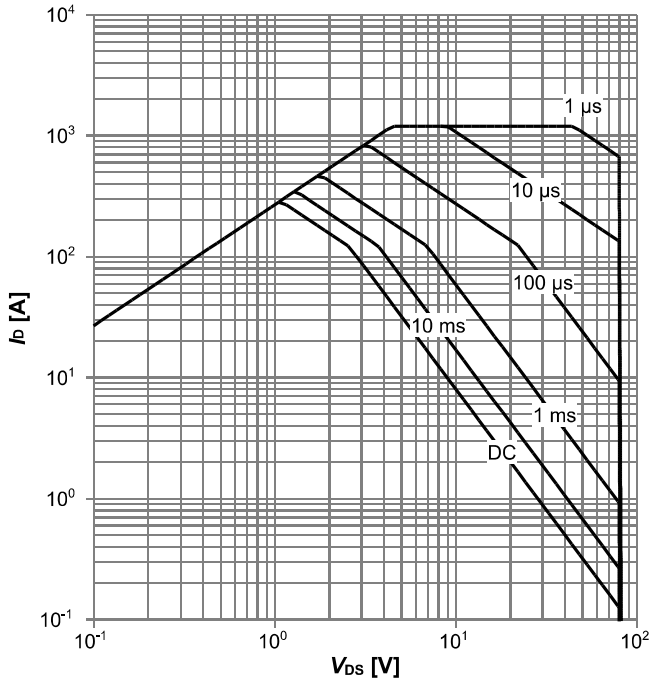
$P_{tot}=f(T_C)$

Diagram 2: Drain current



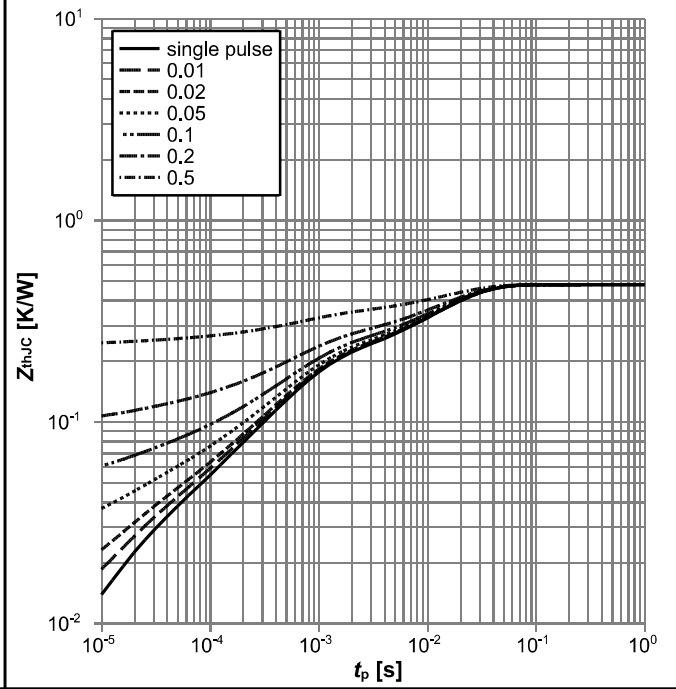
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



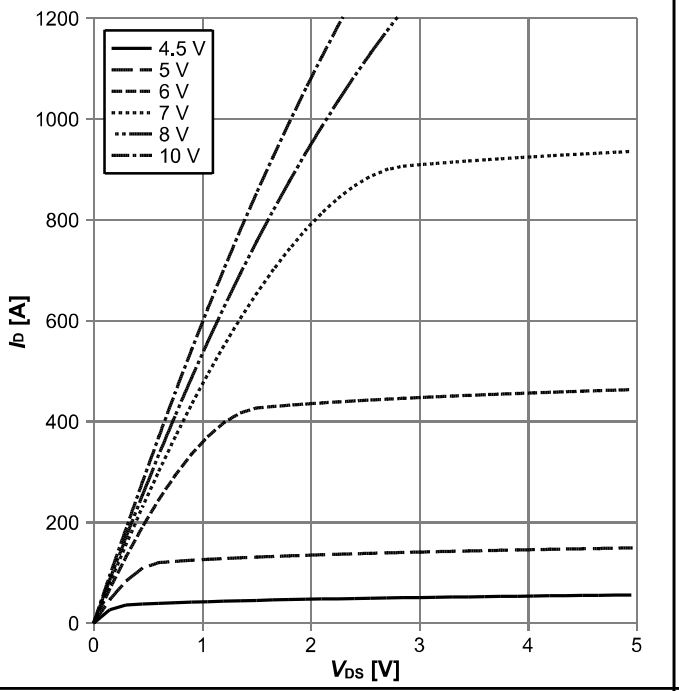
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



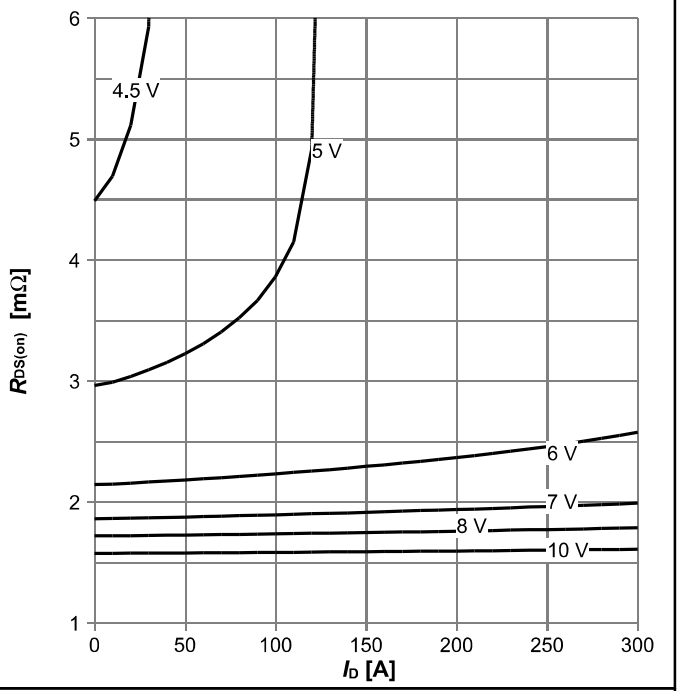
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



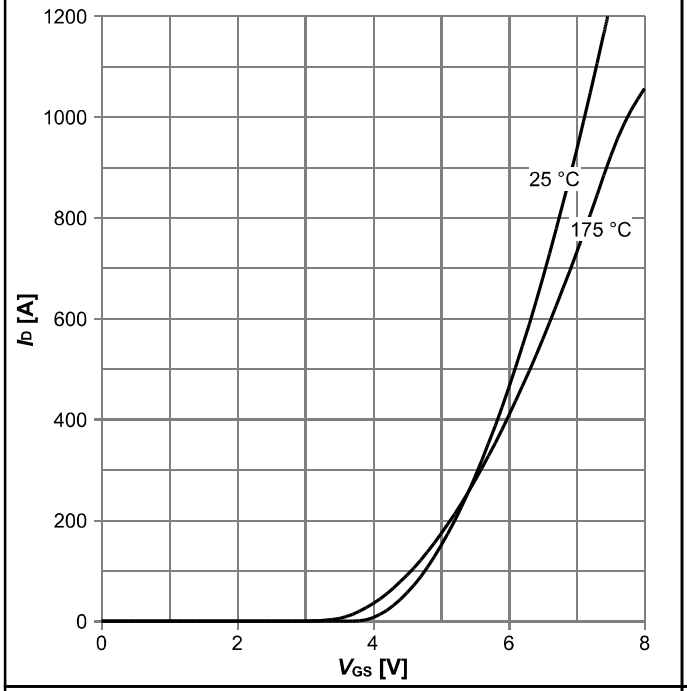
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



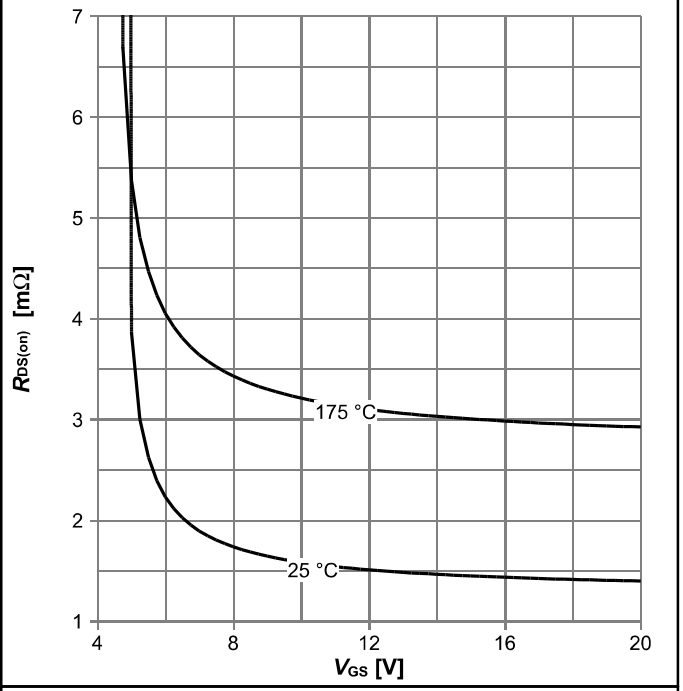
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



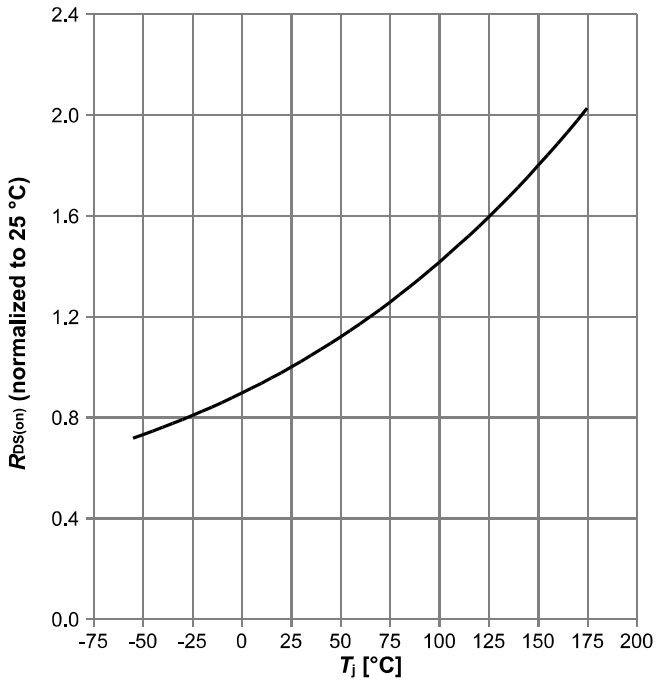
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



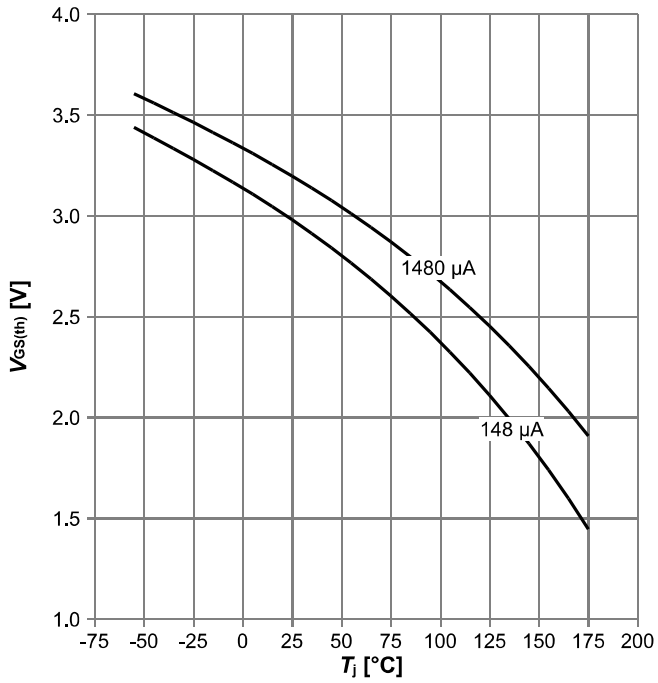
$R_{DS(on)}=f(V_{GS})$, $I_D=50$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



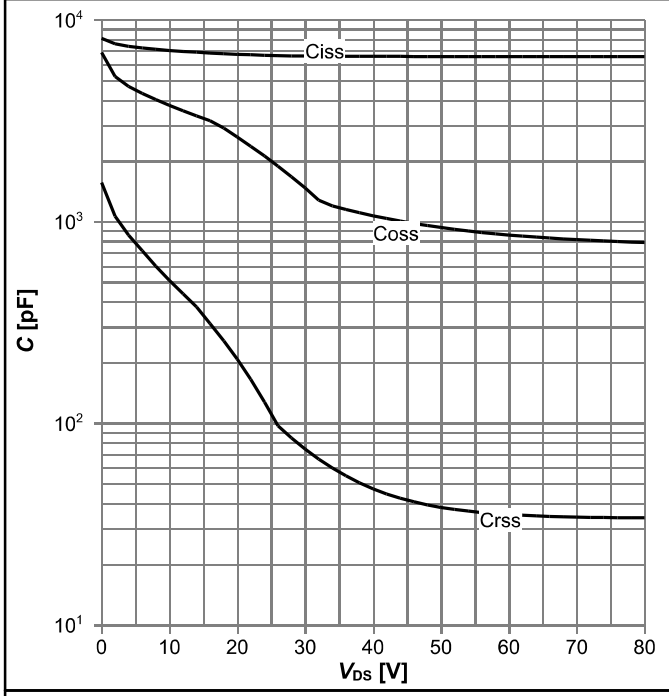
$R_{DS(on)}=f(T_j)$, I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



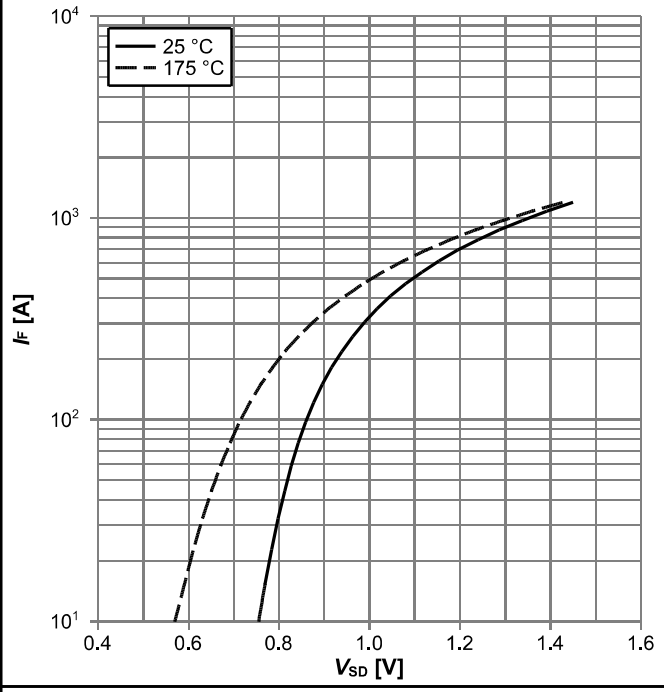
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



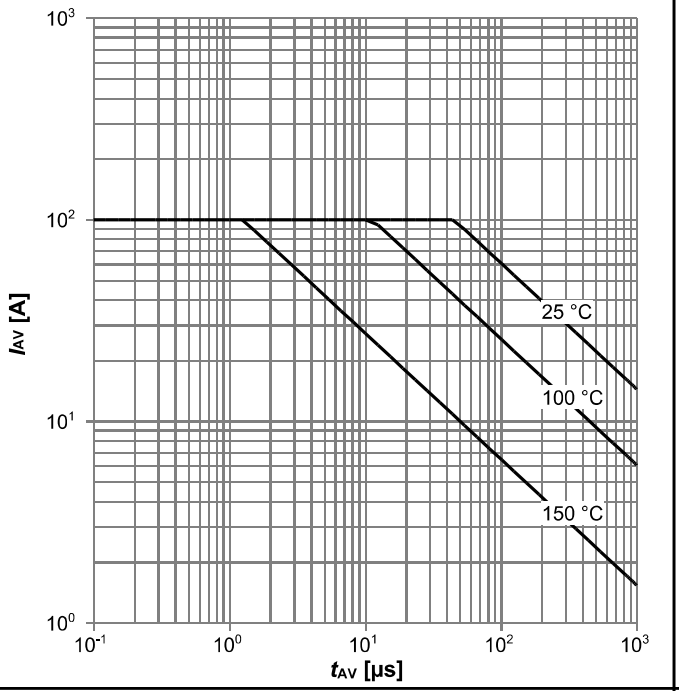
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



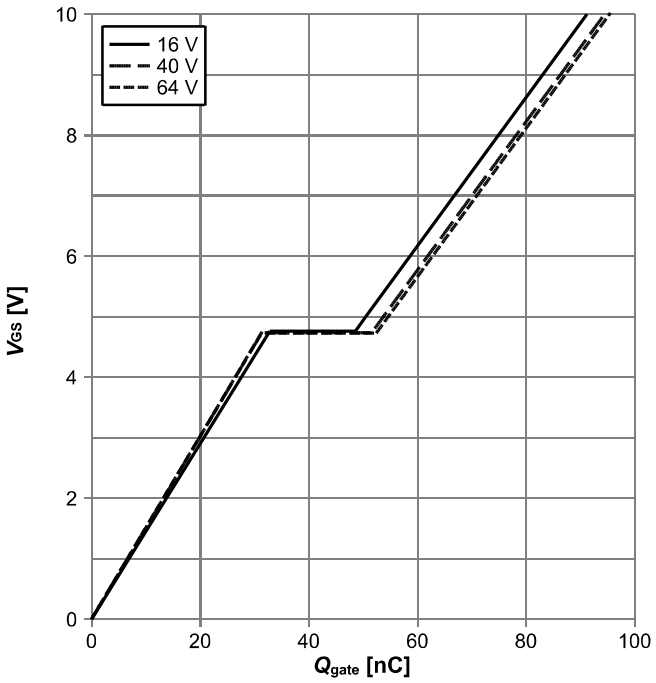
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



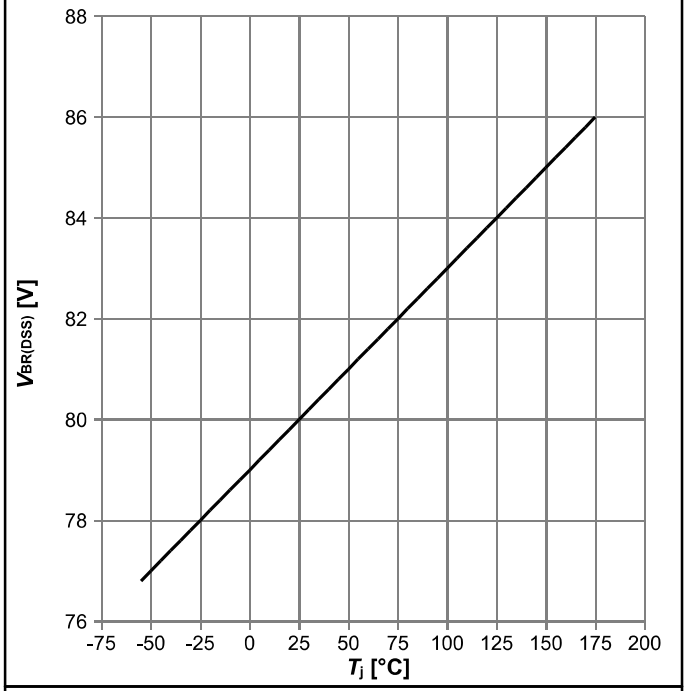
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



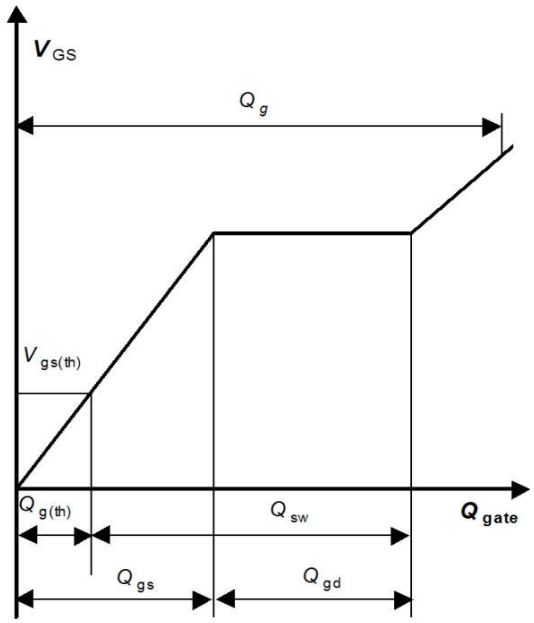
$V_{GS}=f(Q_{gate})$, $I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

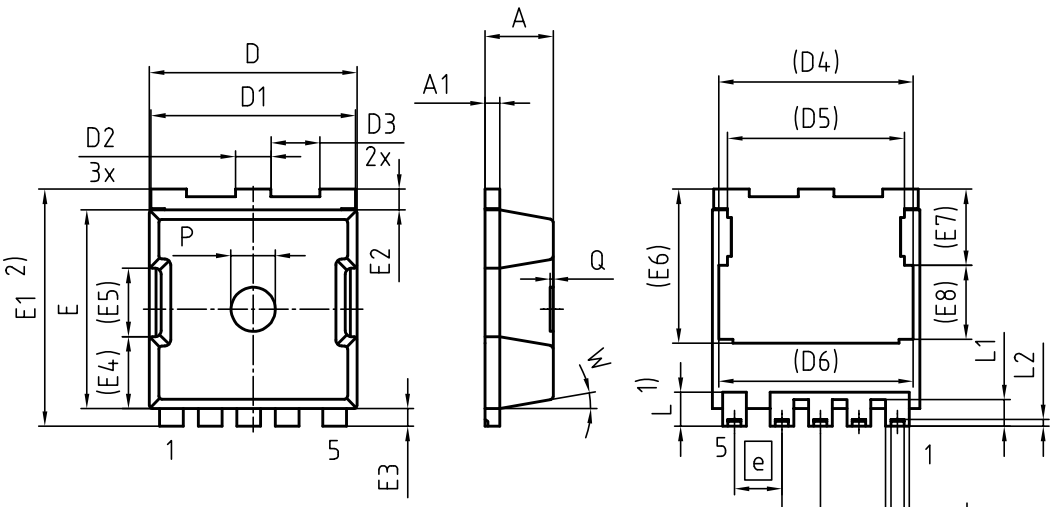


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-5-U01	
REVISION: 02	DATE: 06.05.2021	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
A1	0.40	0.60
b	0.70	0.90
b1	0.42	0.50
D	6.80	7.20
D1	6.80	7.00
D2	1.10	1.30
D3	1.55	1.75
D4	6.56	
D5	5.96	
D6	5.60	
E	6.50	6.90
E1	7.80	8.20
E2	0.60	0.80
E3	0.50	0.70
E4	2.43	
E5	2.30	
E6	5.20	
E7	2.57	
E8	2.50	
e	1.60	
e1	1.30	
L	1.05	1.25
L1	0.80	1.00
L2	0.13	0.33
P	1.40	1.60
Q	0.00	0.10
W	8.50°	11.50°

1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED.

2) EXCLUDING BURR

Figure 1 Outline sTOLL, dimensions in mm

Revision History

IST019N08NM5

Revision: 2022-01-24, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2020-11-20	Release of final version
2.1	2022-01-24	Update Part Marking

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