40 A Source and 30 A Sink, SiC Isolated Gate Driver with Slew-Rate Control and BISTs

FEATURES

- 40 A source, 30 A sink peak short-circuit (typical) drive output
- 20 A peak drive current (typical) in typical application
- Output power device resistance 0.38 Ω (typical) per channel
- 1500 V peak and DC working voltage to DIN EN IEC 60747-17
- Slew-rate control through SPI
- Low propagation delay (108 ns typical)
- 60 ns minimum pulse width
- Bipolar and Unipolar secondary side supply capability
  - V_{DD1}: 4.4 V to 7 V
  - V_{DD2} to V_{SS2}: 15 V to 23 V
  - V_{DD2} to GND_2: 12 V to 23 V
  - V_{SS2} to GND_2: −5 V to −3.25 V (Bipolar Supply Mode)
  - V_{SS2} to GND_2: 0 V (Unipolar Supply Mode)
- Protection Features:
- DESAT – SiC drain sense, 7 V (typical) threshold
  - Programmable internal DESAT blanking time
- ASC pin, secondary side driver turn-on control
- External miller clamp
- Soft shutdown, 1 µs capability, adjustable with external resistor
- V_{DD2} to V_{SS2} OVP and programmable V_{DD2} to V_{SS2} UVP
- V_{SS2} to GND_2 OVP and UVP
- Isolated fault differentiation through fault reporting pins
- SiC switch isolated temperature sense
  - 1 kHz PWM, and SPI register read
  - Temperature sense diode stack
  - Compatible with NTC using external resistor network
- Built-in self tests (BISTs)
- SPI
- Nonvolatile EEPROM registers for configurability
- Fault reporting information
- Operating junction temperature range: −40°C to +150°C
- Available in 28-lead, SOIC_W_FP package
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- SiC, MOSFET, IGBT gate drivers
- Electric vehicles (EV) and hybrid electric vehicles (HEV) traction inverters
- Switching power supplies
- Industrial inverters
- Power factor correctors

GENERAL DESCRIPTION

The ADuM4177 is an advanced isolated gate driver that provides 5.7 kV RMS isolation employing Analog Devices, Inc., *i*Coupler® technology. The ADuM4177 provides 8.3 mm creepage in a 28-pin wide body SOIC package. The devices are suitable for applications that require insulation against working voltages of 1060 V RMS and 1500 V DC for the lifetime of the device. Combining high speed CMOS and monolithic transformer technology, these isolated gate drivers provide outstanding performance characteristics suitable for driving the demanding needs of high performance silicon carbide (SiC) switches. Serial-peripheral interface (SPI) communication allows for user-programmable operating modes and fault readback. Additional BISTs makes the ADuM4177 suitable for ASIL D systems.

The ADuM4177 operates with an input voltage range from 4.4 V to 7 V. The output voltages can operate with bipolar gate driver supply of 12 V to 23 V positive and −5 V to −3.25 V for the negative rail provided that the voltage across V_{DD2} and V_{SS2} is within 15 V to 23 V. Multiple programmable undervoltage lockout (UVLO) levels can be obtained through SPI communication with the gate driver. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM4177 offers the benefit of true, galvanic isolation between the input and the output.

The ADuM4177 includes many advanced protection features such as the drain monitoring desaturation detection, an active short-circuit (ASC) operation, external temperature sensing, and both overvoltage protection (OVP) and undervoltage protection (UVP).

Adjustable slew-rate control is available to allow for faster edge transitions and higher efficiency when the system operating point can accommodate it. An external miller clamp allows for strong pull-down to prevent unintended miller injection induced turn on. The ADuM4177 can operate in a wide range of junction temperatures, from −40°C to +150°C.

As a result, the ADuM4177 provides reliable control over the switching characteristics of SiC switch configurations over a wide range of switching voltages.

Rev. 0

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REVISION HISTORY

7/2023—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

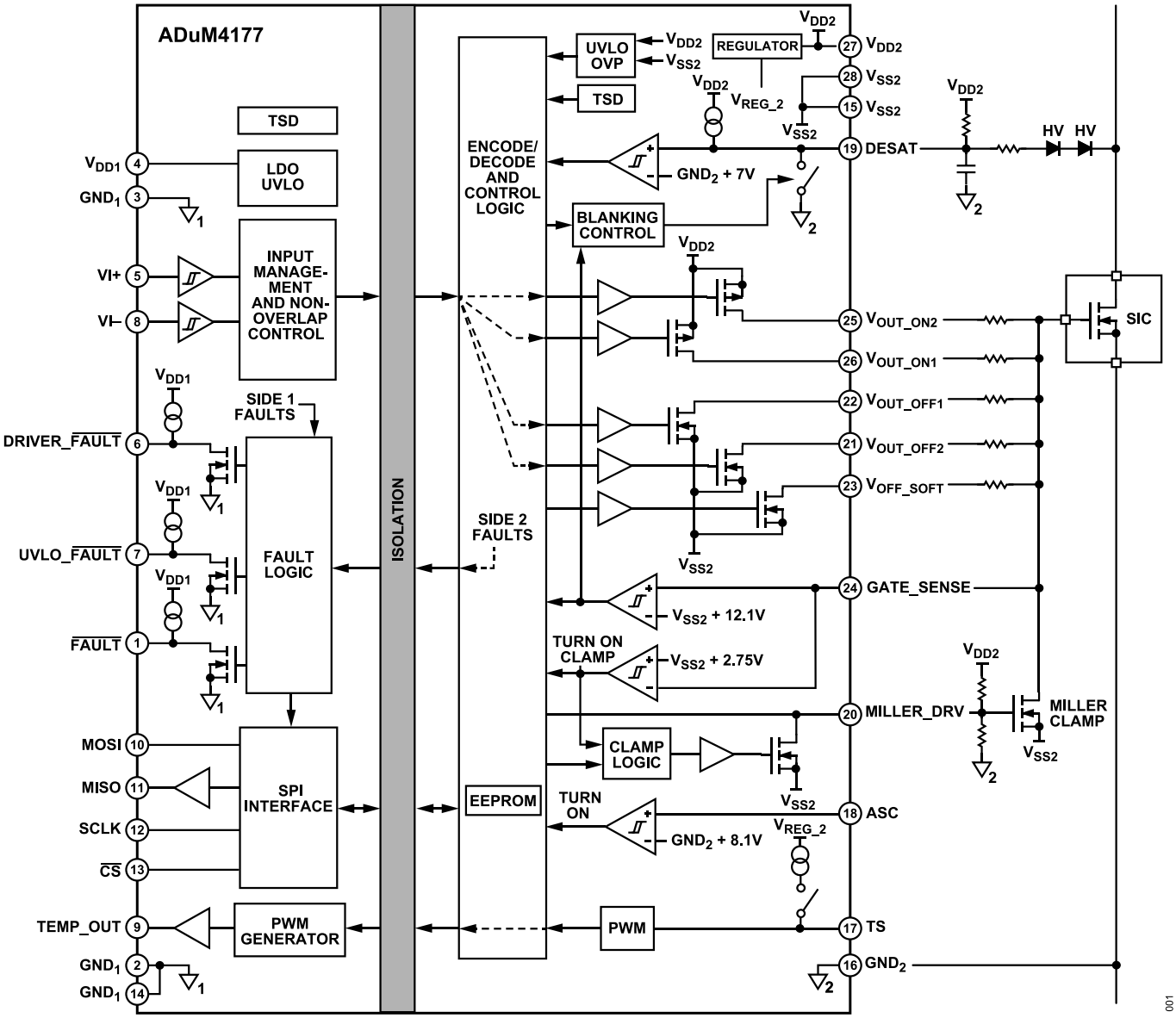

Figure 1. Functional Block Diagram

SPECIFICATIONS

Primary side voltages referenced to GND_1 and secondary side voltages referenced to GND_2, unless otherwise noted. V_{DD1} = 4.4 V to 7 V, V_{DD2} = 12 V to 23 V, V_{SS2} = −5 V to −3.25 V, T_J = −40°C to +150°C, unless otherwise noted. All minimum and maximum specifications apply over the entire recommended operating junction temperature range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5 V, V_{DD2} = 18 V, and V_{SS2} = −5 V, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Primary Side Power Supply						
V_{DD1} Input Voltage	V_{DD1}	4.4		7	V	
V_{DD1} Input Current, Quiescent	$I_{DD1(Q)\_IL}$		4.2	5	mA	V_{DD1} = 5 V, VI+ = 0 V, TS = 2.5 V
V_{DD1} Input Current, Quiescent	$I_{DD1(Q)\_IH}$		11.4	14	mA	V_{DD1} = 5 V, VI+ = 5 V, TS = 2.5 V
V_{DD1} Input Current Delta, SPI active	$\Delta I_{DD1(SPI)}$		3.8	6	mA	V_{DD1} = 5 V, with 0101... bit stream on SPI channels at 455 kHz
Secondary Side Power Supply						
V_{DD2} Input Voltage	V_{DD2}	12		23	V	
V_{DD2} Input Current, Quiescent	$I_{DD2(Q)}$		13	16	mA	V_{DD2} = 18 V, V_{SS2} = −5 V, VI+ = 0 V, No fault, $\overline{CS}$ = 5 V
V_{SS2} Input Voltage	V_{SS2}	−5		−3.25	V	Bipolar Mode (Default)
	V_{SS2}		0		V	Unipolar Mode
UVLO						
Positive Going Threshold						
V_{DD1}	$V_{VDD1UV+}$		3.8	3.9	V	
V_{SS2}	$V_{VSS2UV+}$		−2.55	−2.45	V	
V_{DD2} (referenced to V_{SS2})	$V_{VDD2UV+0}$		14	14.1	V	VDD2_UVLO_SLCT = 000
	$V_{VDD2UV+1}$		15.9	16.1	V	VDD2_UVLO_SLCT = 001
	$V_{VDD2UV+2}$		16.9	17.1	V	VDD2_UVLO_SLCT = 010
	$V_{VDD2UV+3}$		17.9	18.1	V	VDD2_UVLO_SLCT = 011
	$V_{VDD2UV+4}$		18.9	19.1	V	VDD2_UVLO_SLCT = 100
(Default)	$V_{VDD2UV+5}$		20.9	21.1	V	VDD2_UVLO_SLCT = 101
	$V_{VDD2UV+6}$		21.8	22.1	V	VDD2_UVLO_SLCT = 110
	$V_{VDD2UV+7}$		22.8	23.1	V	VDD2_UVLO_SLCT = 111
Negative Going Threshold						
V_{DD1}	$V_{VDD1UV-}$	3.4	3.5		V	
V_{SS2}	$V_{VSS2UV-}$	−3.1	−3.0		V	
V_{DD2} (referenced to V_{SS2})	$V_{VDD2UV-0}$	13.2	13.4		V	VDD2_UVLO_SLCT = 000
	$V_{VDD2UV-1}$	15.1	15.3		V	VDD2_UVLO_SLCT = 001
	$V_{VDD2UV-2}$	16	16.2		V	VDD2_UVLO_SLCT = 010
	$V_{VDD2UV-3}$	16.9	17.1		V	VDD2_UVLO_SLCT = 011
	$V_{VDD2UV-4}$	17.8	18.1		V	VDD2_UVLO_SLCT = 100
(Default)	$V_{VDD2UV-5}$	19.7	20		V	VDD2_UVLO_SLCT = 101
	$V_{VDD2UV-6}$	20.6	20.9		V	VDD2_UVLO_SLCT = 110
	$V_{VDD2UV-7}$	21.6	21.9		V	VDD2_UVLO_SLCT = 111
Hysteresis						
V_{DD1}	$V_{VDD1UVH}$		0.3		V	
V_{SS2}	$V_{VSS2UVH}$		0.45		V	
V_{DD2}	$V_{VDD2UVH0}$		0.59		V	VDD2_UVLO_SLCT = 000
	$V_{VDD2UVH1}$		0.67		V	VDD2_UVLO_SLCT = 001
	$V_{VDD2UVH2}$		0.72		V	VDD2_UVLO_SLCT = 010
	$V_{VDD2UVH3}$		0.76		V	VDD2_UVLO_SLCT = 011
	$V_{VDD2UVH4}$		0.8		V	VDD2_UVLO_SLCT = 100

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
(Default)	$V_{VDD2UVH5}$		0.88		V	VDD2_UVLO_SLCT = 101
	$V_{VDD2UVH6}$		0.93		V	VDD2_UVLO_SLCT = 110
	$V_{VDD2UVH7}$		0.97		V	VDD2_UVLO_SLCT = 111
OVP						
Positive Going Threshold						
V_{DD2}	$V_{VDD2OV+}$	24.3	25.4	26.5	V	Referenced to V_{SS2}
V_{SS2}	$V_{VSS2OV+}$	−5.8	−5.55	−5.35	V	Referenced to GND_2
Negative Going Threshold						
V_{DD2}	$V_{VDD2OV-}$	23.3	24.4	25.5	V	Referenced to V_{SS2}
V_{SS2}	$V_{VSS2OV-}$	−6.2	−5.95	−5.75	V	Referenced to GND_2
Hysteresis						
V_{DD2}	$V_{VDD2OVH}$		1		V	Referenced to V_{SS2}
V_{SS2}	$V_{VSS2OVH}$		0.4		V	Referenced to GND_2
LOGIC INPUTS (VI+, VI−, SCLK, $\overline{CS}$, MOSI)						V_{DD1} = 4.4 V
Input Voltage Threshold						
Logic High	V_{IH}	2.7			V	
Logic Low	V_{IL}			1.3	V	
Hysteresis	V_{I_HYST}		1.0			
Internal Pull-down Resistance (VI+ and VI− Only)	R_{PD_VI}		50		kΩ	VI+ = 3 V, VI− = 3 V
THERMAL SHUTDOWN (TSD)						
Primary Side TSD						
Positive Edge	T_{TSD_POS1}		165		°C	
Negative Edge	T_{TSD_NEG1}		145		°C	
Secondary Side TSD						
Positive Edge	T_{TSD_POS2}		165		°C	
Negative Edge	T_{TSD_NEG2}		145		°C	
ISOLATED TEMPERATURE SENSE						
Temperature Sense						
TS Pin Bias Current	I_{TS}	0.19	0.21	0.23	mA	TS pin = 2.5 V
Operating Frequency	F_{TS_PWM}	9.3	10	10.7	kHz	
Sense Filter Time	t_{FILT}			3.15	ms	V_{DD1} = 5 V, V_{DD2} = 18 V, V_{SS2} = −5 V
Maximum TS Pin Voltage	V_{TS_MAX}			5	V	Referenced to V_{SS2}
TS Comparator Thresholds						Referenced to V_{SS2}
Positive Going Threshold						
Comparator 1	$V_{TS\_COMP1\_RISE}$	1.32	1.37	1.42	V	TS_COMP_SLCT[2:1] = 01
Comparator 2	$V_{TS\_COMP2\_RISE}$	2.92	2.97	3.02	V	TS_COMP_SLCT[2:1] = 10
Negative Going Threshold						
Comparator 1	$V_{TS\_COMP1\_FALL}$	1.27	1.32	1.37	V	TS_COMP_SLCT[2:1] = 01
Comparator 2	$V_{TS\_COMP2\_FALL}$	2.86	2.91	2.96	V	TS_COMP_SLCT[2:1] = 10
Hysteresis						
Comparator 1	$V_{TS\_COMP1\_HYST}$		0.05		V	TS_COMP_SLCT[2:1] = 01
Comparator 2	$V_{TS\_COMP2\_HYST}$		0.06		V	TS_COMP_SLCT[2:1] = 10
Filter Time	$t_{TS\_COMP\_FILT}$		1.64		ms	TS_COMP_FILT_DIS = 0
TEMP_OUT						V_{DD1} = 5 V
TEMP_OUT Duty Cycle	D_{TO}		12		%	TS – V_{SS2} = 3.7 V
			87		%	TS – V_{SS2} = 1.3 V
TEMP_OUT Maximum Duty Cycle	D_{TO_MAX}		98		%	
TEMP_OUT Minimum Duty Cycle	D_{TO_MIN}		2.5		%	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TEMP_OUT PMOS R_{DSON}	$R_{DSON\_TO\_PMOS}$		14	30	Ω	V_{DD1} = 5 V, Tested at 10 mA
TEMP_OUT NMOS R_{DSON}	$R_{DSON\_TO\_NMOS}$		7	15	Ω	V_{DD1} = 5 V, Tested at 10 mA
PWM Output Frequency	F_{PWM}	0.9	1	1.1	kHz	V_{DD1} = 5 V, V_{DD2} = 18 V, V_{SS2} = −5 V
DRIVE SPECIFICATIONS						
Turn on/Turn off R_{DSON}						V_{DD2} = 15 V, Tested at 500 mA
V_{OUT_ON1} R_{DSON}	R_{DSON_ON1}		0.38	0.8	Ω	
V_{OUT_ON2} R_{DSON}	R_{DSON_ON2}		0.38	0.8	Ω	GD_ON_SLEW_SLCT = 0
V_{OUT_OFF1} R_{DSON}	R_{DSON_OFF1}		0.38	0.8	Ω	
V_{OUT_OFF2} R_{DSON}	R_{DSON_OFF2}		0.38	0.8	Ω	GD_OFF_SLEW_SLCT = 0
V_{OFF_SOFT} R_{DSON}	R_{DSON_SOFT}		0.38	0.8	Ω	V_{DD2} = 15 V, Tested at 80 mA
Peak Current Per Output Pin[1]	I_{PEAKIP}		10		A	1.5 Ω external resistors
Sourcing Short-Circuit Peak Current Per Pin[1]	$I_{PEAKIP\_SC\_ON}$		20		A	0 Ω external resistors
Sinking Short-Circuit Peak Current Per Pin[1]	$I_{PEAKIP\_SC\_OFF}$		15		A	0 Ω external resistors
Pulse Width	t_{PW}	60			ns	
Internal Deadtime	t_{DT}	0.46	0.5	0.54	µs	V_{DD1} = 5 V
Propagation Delay	t_{DHL}, t_{DLH}	82	108	140	ns	No gate load
Propagation Delay Skew	t_{PSK}			32	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		11		ns	C_L = 2.2 nF, RG_{ON} = RG_{OFF} = 3.9 Ω
Miller Drive						
MILLER_DRV Rdson	R_{DSON_MC}		3	7	Ω	V_{DD2} = 15 V, Tested at 20 mA
MILLER_DRV Pull-up Current	I_{MC_PU}		10		µA	
Miller Gate Sense Threshold	V_{MG_TH}	2.4	2.75	3.1	V	Referenced to V_{SS2}
Miller Gate Sense Hysteresis	$V_{MG\_TH\_HYST}$		0.6		V	Referenced to V_{SS2}
MILLER_DRV Delay[2]	t_{MC_DLY}		60		ns	R_{PU} = 1 kΩ
Gate Sense						
Gate High Threshold	V_{GH_TH}	11.8	12.1	12.3	V	Referenced to V_{SS2}
Gate High Hysteresis	$V_{GH\_TH\_HYST}$		2		V	Referenced to V_{SS2}
Gate High Error Filter	t_{GH_FILT}	2.85	3.1	3.35	µs	V_{DD2} = 18 V, V_{SS2} = −5 V
Gate Low Threshold	V_{GL_TH}	2.9	3.0	3.1	V	Referenced to V_{SS2}
Gate Low Hysteresis	$V_{GL\_TH\_HYST}$		0.5		V	Referenced to V_{SS2}
Gate Low Error Filter	t_{GL_FILT}	2.85	3.1	3.35	µs	V_{DD2} = 18 V, V_{SS2} = −5 V
DESATURATION (DESAT) DETECTION						
DESAT Pin Current	I_{DESAT_PU}		10		µA	
Comparator Thresholds						V_{SS2} = −5 V, 0 V
Rising	V_{DESAT_RISE}	6.4	7.0	7.8	V	
Falling	V_{DESAT_FALL}	6.2	6.8	7.6	V	
Hysteresis	V_{DESAT_HYST}		0.2		V	
Delay to Soft Turn Off	t_{DESAT_DLY}	55	100	140	ns	V_{SS2} = −5 V, 0 V
Blanking Switch R_{DSON}	R_{DSON_BLANK}	6	10.6	24	Ω	V_{DD2} = 15 V, V_{SS2} = 0 V, Tested at 10 mA
DESAT Blanking Time[3]						V_{DD2} = 15 V, 23 V, V_{SS2} = −5 V, 0 V, GSR_DESAT_DIS = 1, referenced to V_{OUT} rising
Code 000	t_{BLANK_000}		−20		ns	DESAT_BLANK_SLCT = 000
Code 001 (default)	t_{BLANK_001}		80		ns	DESAT_BLANK_SLCT = 001
Code 010	t_{BLANK_010}		180		ns	DESAT_BLANK_SLCT = 010
Code 011	t_{BLANK_011}		280		ns	DESAT_BLANK_SLCT = 011
Code 100	t_{BLANK_100}		380		ns	DESAT_BLANK_SLCT = 100
Code 101	t_{BLANK_101}		480		ns	DESAT_BLANK_SLCT = 101
Code 110	t_{BLANK_110}		580		ns	DESAT_BLANK_SLCT = 110

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Code 111	t_{BLANK_111}		680		ns	DESAT_BLANK_SLCT = 111
ACTIVE SHORT-CIRCUIT (ASC)						
ASC Pin Current	I_{ASC}	100	150	200	µA	V_{ASC} = 10 V
Comparator Thresholds						V_{SS2} = −5 V, 0 V
Rising	V_{ASC_RISE}	7.4	8.1	8.9	V	
Falling	V_{ASC_FALL}	7.2	7.9	8.7	V	
Hysteresis	V_{ASC_HYST}		0.2		V	
ASC Propagation Delay						
Rising	$t_{D\_ASC\_RISE}$	60	105	140	ns	
Falling	$t_{D\_ASC\_FALL}$	80	125	170	ns	
FAULT SPECIFICATIONS						V_{DD1} = 5 V, V_{DD2} = 18 V, V_{SS2} = −5 V
Latch Time						
Deadtime	t_{PW_DT}	12.1	13.1	14.1	ms	
DRIVER_$\overline{FAULT}$	$t_{PW\_DRV\_FAULT}$	28	30	32	ms	
UVLO_$\overline{FAULT}$	$t_{PW\_UVLO\_FAULT}$	9	10	11	ms	
$\overline{FAULT}$	t_{PW_FAULT}	19	20	21	ms	
Reporting Time						
Deadtime	t_{FDEL_DT}		14		ns	
DRIVER_$\overline{FAULT}$	$t_{FDEL\_DRV\_FAULT}$		0.8	1.1	µs	
UVLO_$\overline{FAULT}$	$t_{FDEL\_UVLO\_FAULT}$		2	6.7	µs	
$\overline{FAULT}$	t_{FDEL_FAULT}		0.8	1.1	µs	
DRIVER_$\overline{FAULT}$ Pull-up Current	$I_{PU\_DRV\_FAULT}$		100		µA	
UVLO_$\overline{FAULT}$ Pull-up Current	$I_{PU\_UVLO\_FAULT}$		100		µA	
$\overline{FAULT}$ Pull-up Current	I_{PU_FAULT}		100		µA	
DRIVER_$\overline{FAULT}$ NMOS R_{DSON}	$R_{DSON\_DRV\_FAULT\_N}$		6	18	Ω	Tested at 10 mA, V_{DD1} = 5 V
UVLO_$\overline{FAULT}$ NMOS R_{DSON}	$R_{DSON\_UVLO\_FAULT\_N}$		6	18	Ω	Tested at 10 mA, V_{DD1} = 5 V
$\overline{FAULT}$ NMOS R_{DSON}	$R_{DSON\_FAULT\_N}$		6	18	Ω	Tested at 10 mA, V_{DD1} = 5 V
SPI						
Minimum SCLK Period	t_{CLK}	2.22	2.50		µs	400 kHz (typical), 450 kHz (max)
Minimum SCLK High Time	t_{HI}	0.6			µs	
Minimum SCLK Low Time	t_{LO}	1.2			µs	
Valid Data Before SCLK Falling Edge	t_{DS}	0.25			µs	
Valid Data After SCLK Falling Edge	t_{DH}	0.35			µs	
$\overline{CS}$ Falling to First SCLK Rising Edge	t_S	2.5			µs	
$\overline{CS}$ Rising Edge to $\overline{CS}$ falling Edge		4			µs	
EEPROM PROGRAM TIME	t_{PROG}			40	cycle	
COMMON-MODE TRANSIENT IMMUNITY (CMTI)	|CM|					
Static CMTI[4]		150			kV/µs	V_{CM} = 1500 V
Dynamic CMTI[5]		150			kV/µs	V_{CM} = 1500 V

[1] Peak current ratings are tested in characterization and not production tested.

[2] t_{MC_DLY} is measured from the miller gate sense threshold, V_{MG_TH}, to the MILLER_DRV rising.

[3] DESAT blanking time is measured from the output going high to DESAT blanking switch turning off.

[4] Static CMTI is defined as the largest dv/dt between GND_1 and GND_2, with inputs held either high or low, such that the output voltage remains either above 0.8 × V_{DD2} for output high or below 0.8 V for output low. Operation with transients above recommended levels may cause momentary data upsets. Tested in characterization and not production tested.

[5] Dynamic CMTI is defined as the largest dv/dt between GND_1 and GND_2, with the switching edge coincident with the transient test pulse. Operation with transients above recommended levels may cause momentary data upsets. Tested in characterization and not production tested.

SPECIFICATIONS

PACKAGE CHARACTERISTICS

Table 2. Package Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Resistance (Input Side to High-Side Output)[1]	R_{I-O}		10^{12}		Ω
Capacitance (Input Side to High-Side Output)[1]	C_{I-O}		2.0		pF
Input Capacitance	C_I		4.0		pF

[1] The ADuM4177 is considered a 2-terminal device: Pin 1 through Pin 14 and Pin 15 through Pin 28 are shorted together.

REGULATORY INFORMATION

Table 3. Regulatory Information

UL (Pending)	CSA (Pending)[1]	VDE (Pending)
Recognized under UL 1577 component recognition program[2]	Basic insulation per IEC 62368-1:2018 Ed. 3 and EN 62368-1:2020+A11:2020, 830 V RMS (1174 V PEAK) maximum working voltage	Certified according to EN IEC 60747-17[3]
Single protection, 5700 V RMS isolation voltage	Reinforced Insulation per IEC 62368-1:2018 Ed. 3 and EN 62368-1:2020+A11:2020, 415 V RMS (587 V PEAK) maximum working voltage	Reinforced insulation, 1500 V PEAK
File (Pending)	File (Pending)	File (Pending)

[1] Working voltages are quoted for pollution degree 2, material group III.

[2] In accordance with UL 1577, each ADuM4177 is proof tested by applying an insulation test voltage ≥ 6840 V RMS for 1 second (current leakage detection limit = 10 µA).

[3] In accordance with DIN EN IEC 60747-17, each ADuM4177 is proof tested by applying an insulation test voltage ≥ 2813 V PEAK for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4. Insulation and Safety-Related Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V RMS	1 minute duration
Minimum External Air Gap (Clearance)	CLR	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	CRP	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)	DTI	0.040	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material group (DIN VDE 0110, 1/89, Table 1)

DIN EN IEC 60747-17 INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

Table 5. VDE Characteristics

Description	Symbol	Characteristics	Unit	Test Conditions/Comments
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V RMS		I to IV		
For Rated Mains Voltage ≤ 300 V RMS		I to IV		
For Rated Mains Voltage ≤ 600 V RMS		I to IV		
Climatic Classification		40/125/21		
Pollution Degree per DIN VDE 0110, Table 1		2		
Maximum Working Insulation Voltage	V_{IOWM}	1060	V_{RMS}	

SPECIFICATIONS

Table 5. VDE Characteristics (Continued)

Description	Symbol	Characteristics	Unit	Test Conditions/Comments
Maximum Repetitive Insulation Voltage	V_{IORM}	1500	V_{PEAK}	
Maximum Transient Isolation Voltage	V_{IOTM}	8000	V_{PEAK}	Transient overvoltage, t_{TR} = 10 sec
Maximum Withstand Isolation Voltage	V_{Iso}	5700	V_{RMS}	1 minute withstand rating
Maximum Surge Isolation Voltage, Reinforced	V_{IOSM}	8000	V_{PEAK}	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time
Input to Output Test Voltage, Method B1	$V_{pd(m)}$	2813	V_{PEAK}	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m$ = 1 sec, partial discharge < 5 pC
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{pd(m)}$	2250	V_{PEAK}	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}$	1800	V_{PEAK}	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC
Safety Limiting Values				Maximum value allowed in the event of a failure (see Figure 2)
Maximum Junction Temperature	T_S	150	°C	
Safety Total Power Dissipation at T_A = 25°C	P_S	2.47	W	
Insulation Resistance at T_S	R_S	$>10^9$	Ω	Voltage between the input and output (V_{IO}) = 500 V

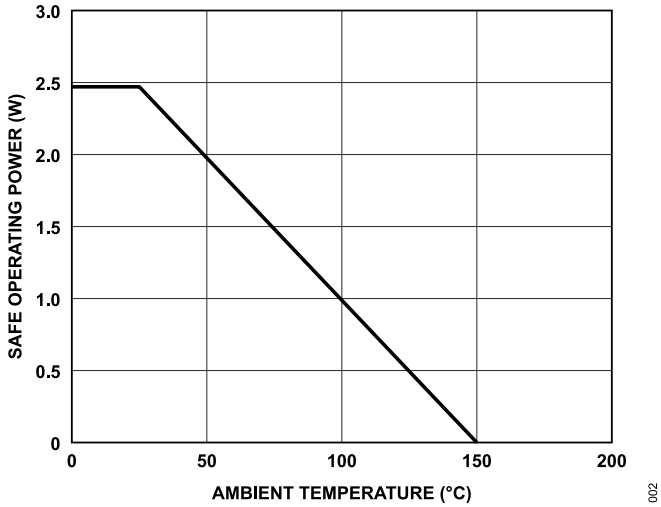

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Ambient Temperature, Per DIN EN IEC 60747-17

RECOMMENDED OPERATING CONDITIONS

Table 6. Recommended Operating Conditions

Parameter	Value
Operating Junction Temperature Range	−40°C to +150°C
Supply Voltages	
V_{DD1} Referenced to GND_1	4.4 V to 7.0 V
V_{DD2} Referenced to GND_2	12 V to 23 V ($V_{DD2} - V_{SS2}$ < 23 V)
V_{SS2} Referenced to GND_2	−5 V to −3.25 V ($V_{DD2} - V_{SS2}$ < 23 V)

ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages	
V_{DD1} to GND_1	−0.2 V to +7.5 V
V_{DD2} to GND_2	−0.2 V to +24 V
V_{DD2} to V_{SS2}	−0.2 V to +30 V
V_{SS2} to GND_2 (Bipolar Mode)	−7 V to +0.2 V
V_{SS2} to GND_2 (Unipolar Mode)	−0.2 V to +0.2 V
Primary Side Pins	
VI+, VI−, MOSI, SCLK, $\overline{CS}$ to GND_1	−0.2 V to +7.5 V, when V_{DD1} > +4.4 V, −0.2 V to +6 V, when V_{DD1} ≤ +4.4 V
$\overline{FAULT}$, DRIVER_$\overline{FAULT}$, UVLO_$\overline{FAULT}$, TEMP_OUT, MISO to GND_1	−0.2 V to V_{DD1} + 0.2 V
Secondary Side Pins	
TS to V_{SS2}	−0.2 V to +5.1 V
ASC, DESAT to GND_2	−0.2 V to V_{DD2} V
MILLER_DRV, V_{OUT_OFF1}, V_{OUT_OFF2}, V_{OFF_SOFT}, GATE_SENSE to V_{SS2}	−0.2 V to V_{DD2} V
V_{OUT_ON1}, V_{OUT_ON2} to V_{SS2}	−0.2 V to V_{DD2} + 0.2 V
Storage Temperature Range (T_{ST})	−55°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and Ψ_{JT} is the junction to top characterization parameter.

Table 8. Thermal Resistance

Package Type[1, 2]	θ_{JA}	Ψ_{JT}	Unit
RN-28-1	50.6	2.61	°C/W

[1] Thermal resistance simulated values are based on a JEDEC 2S2P thermal test board with 0 thermal vias. See JEDEC JESD-51.

[2] Case temperature is measured at the center of the package.

TRUTH TABLE

Table 10. Truth Table (Positive Logic)

VI+ Input	VI− Input	ASC	$\overline{FAULT}$	DRIVER_$\overline{FAULT}$	UVLO_$\overline{FAULT}$	V_{DD1} State	V_{DD2} State	V_{OFF_SOFT}	V_{OUT_ON}	V_{OUT_OFF}
Low	High	<9 V	High	High	High	Powered	Powered	Low	Low	High
High	Low	<9 V	High	High	High	Powered	Powered	Low	High	Low
High	High	<9 V	High	High	High	Powered	Powered	Low	Low	High
Low	Low	<9 V	High	High	High	Powered	Powered	Low	Low	High

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADuM4177

Table 9. ESD Ratings for ADuM4177, 28-Lead SOIC_W_FP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	2
FICDM	±1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS

Table 10. Truth Table (Positive Logic) (Continued)

VI+ Input	VI− Input	ASC	$\overline{\text{FAULT}}$	DRIVER_$\overline{\text{FAULT}}$	UVLO_$\overline{\text{FAULT}}$	V_{DD1} State	V_{DD2} State	V_{OFF_SOFT}	V_{OUT_ON}	V_{OUT_OFF}
X[1]	X	>9 V[2]	High	Low	High	Powered	Powered	Low	High	Low
X	X	X	Low	X	X	Powered	Powered	High	X	Low[3]
X	X	X	X	Low	X	Powered	Powered	High[4]	X	Low[3]
X	X	X	X	X	Low	Powered	Powered	High[5]	X	Low[3]
X	X	>9 V[2]	X	X	X	Unpowered	Powered	Low	High	Low
X	X	<9 V	X	X	X	Unpowered	Powered	Low	Low	High
X	X	X	X	X	X	X	Unpowered	High-Z	High-Z	Low[6]

[1] X means do not care or unknown.

[2] ASC dominance enabled.

[3] The NMOS on V_{OUT_OFF} is off during soft shutdown until the GATE_SENSE pin reaches 2.75 V, then the V_{OUT_OFF} NMOS turns on along with the miller drive.

[4] The driver only goes into soft shutdown when an actual fault occurs, such as DESAT or gate error. For fault pin mapping, see Table 14.

[5] The driver only goes into soft shutdown when an actual fault occurs, such as TSD_2, V_{DD2}/V_{SS2} UVLOs, or gate error. For fault pin mapping, see Table 14.

[6] With an unpowered V_{DD2}, the ADuM4177 tries to hold the IGBT/SiC gate voltage to a value of approximately 3 V to 5 V.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

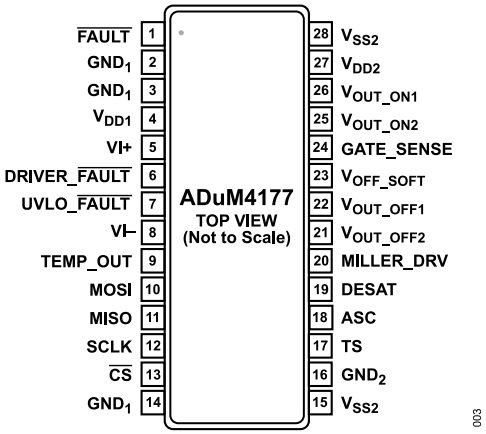

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	$\overline{\text{FAULT}}$	Negative Logic Fault Output Pin. Negative logic pin that communicates fault state of the gate driver.
2, 3, 14	GND_1	Primary Side Ground Connection. Ground reference for primary side signals.
4	V_{DD1}	Primary Side Power Supply Input. Provides current to operate the primary side of the gate driver.
5	VI+	Noninverting Input. Connect to noninverting input of the control signal.
6	DRIVER_$\overline{\text{FAULT}}$	Negative Logic Driver Fault Pin. Responds to driver related faults.
7	UVLO_$\overline{\text{FAULT}}$	Negative Logic UVLO Fault Pin. Responds to UVLO related faults.
8	VI−	Inverting Input. Connect to inverted input of control signal.
9	TEMP_OUT	Temperature Sense PWM Output Pin. Returns the PWM encoded temperature sense signal from secondary side.
10	MOSI	Main Out, Subordinate In Pin. Serial data input pin for SPI communication.
11	MISO	Main In, Subordinate Out Pin. Serial data output pin for SPI communication.
12	SCLK	SPI Reference Clock. Clock pin for SPI communication.
13	$\overline{\text{CS}}$	SPI Chip Select Pin. Negative logic chip select pin for SPI communication.
15	V_{SS2}	Secondary Side Negative Supply Connection. Lowest potential voltage on secondary side of gate driver.
16	GND_2	Secondary Side Ground Connection. Ground reference for secondary side signals.
17	TS	Temperature Sense Pin. Accepts an analog signal to convert into a PWM signal read out of TEMP_OUT pin.
18	ASC	Active Short-Circuit Pin. When ASC goes high, the output of the gate driver goes high.
19	DESAT	Switch Drain Protection Sense Input. Provides desaturation detection of the power device.
20	MILLER_DRV	Open Drain Miller Drive Pin. Connect to external miller clamp to provide strong pull-down of power device.
21	V_{OUT_OFF2}	Gate Drive Turn Off Pin 2. Provides strong turn off of power device. Can be toggled with slew-rate control by SPI settings.
22	V_{OUT_OFF1}	Gate Drive Turn Off Pin 1. Provides strong turn off of power device.
23	V_{OFF_SOFT}	Soft Shutdown Pin. Provides shut off path for gate during fault conditions requiring a soft shutdown.
24	GATE_SENSE	Switch Gate Sense Pin. Connect directly to power device gate.
25	V_{OUT_ON2}	Gate Drive Turn On Pin 2. Provides strong turn on of power device. Can be toggled with slew-rate control by SPI settings.
26	V_{OUT_ON1}	Gate Drive Turn On Pin 1. Provides strong turn off of power device.
27	V_{DD2}	Secondary Side Positive Power Supply Input Pin. Provides positive voltage rail to gate driver.
28	V_{SS2}	Secondary Side Negative Power Supply Input Pin. Provides negative voltage rail to gate driver.

TYPICAL PERFORMANCE CHARACTERISTICS

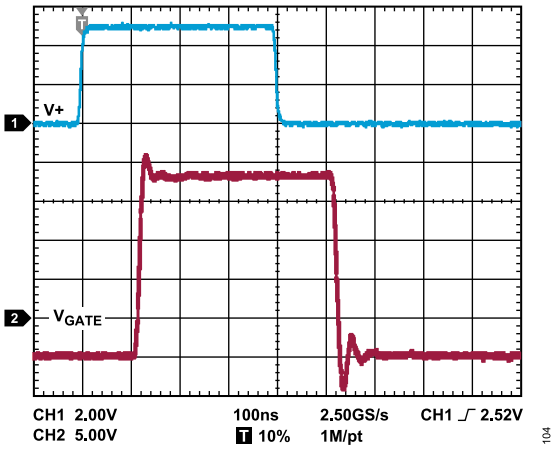

Figure 4. Output Waveform 2.2 nF Load, 3.9 Ω Series Gate Resistor (R_G), V_{DD1} = 5 V, V_{DD2} = 18 V, V_{SS2} = −5 V

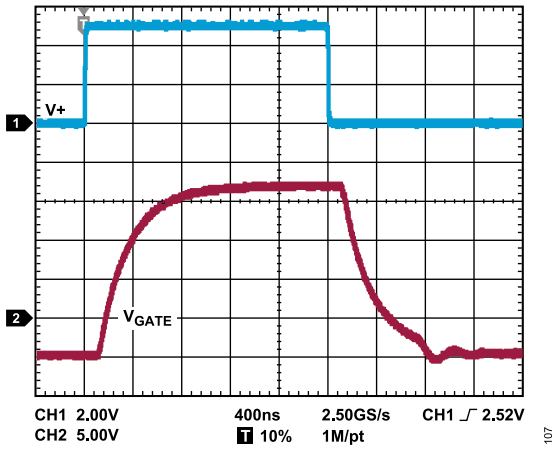

Figure 7. Output Waveform 100 nF Load, 3.9 Ω Series Gate Resistor (R_G), V_{DD1} = 5 V, V_{DD2} = 18 V, V_{SS2} = −5 V

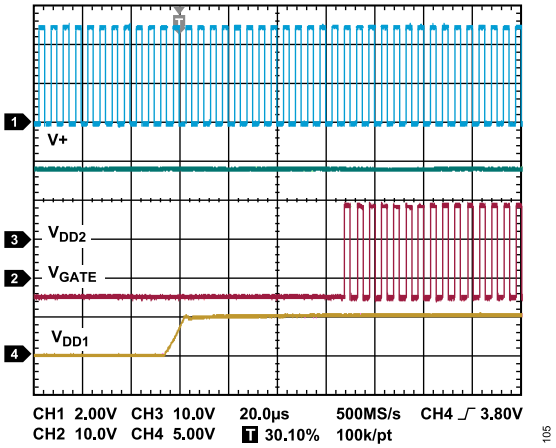

Figure 5. Typical V_{DD1} Startup to Output Valid

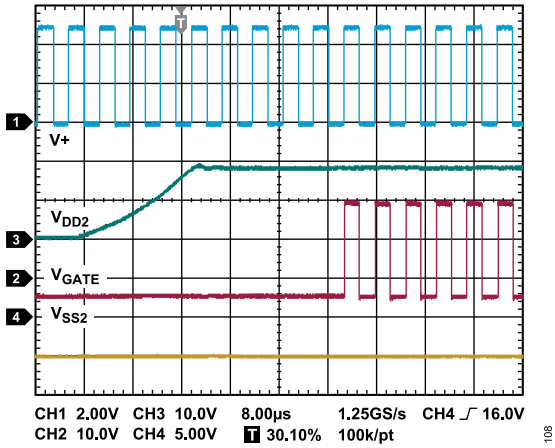

Figure 8. Typical V_{DD2} Startup to Output Valid

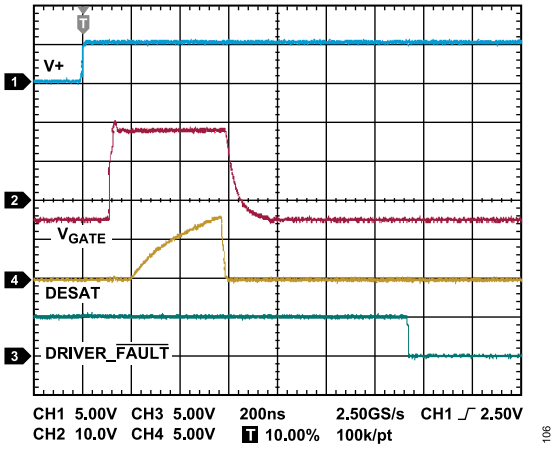

Figure 6. Example Desaturation Event and Fault Reporting, DESAT Blanking Time = 80 ns

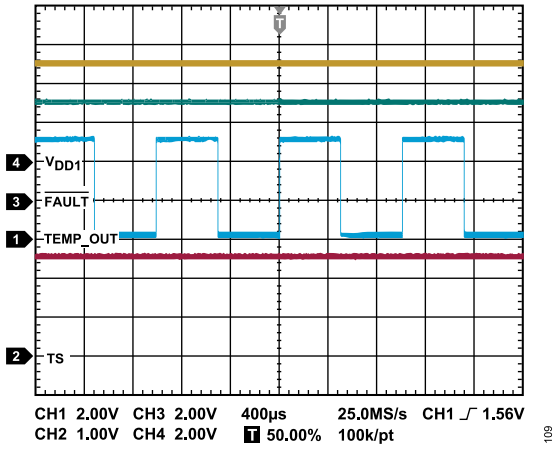

Figure 9. Temp_Out Reading, TS − V_{SS2} = 2.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

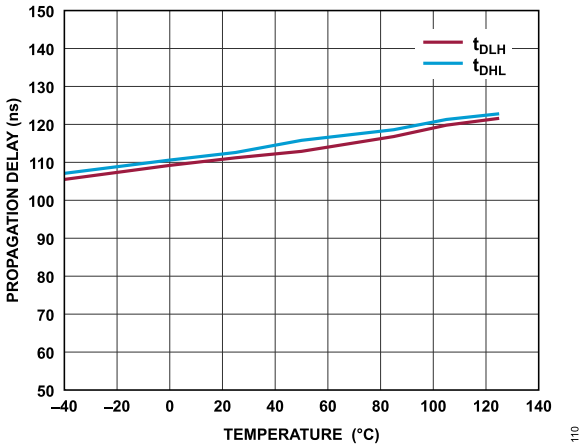

Figure 10. Propagation Delay vs. Temperature (°C), V_{DD1} = 5 V, V_{DD2} = 18 V, V_{SS2} = −5 V, 2.2 nF Load, R_G = 3.9 Ω

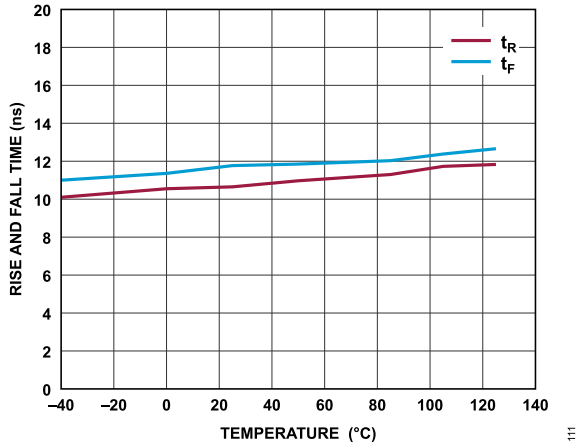

Figure 11. Rise and Fall Time vs. Temperature (°C), V_{DD1} = 5 V, V_{DD2} = 18 V, V_{SS2} = −5 V, 2.2 nF Load, R_G = 3.9 Ω

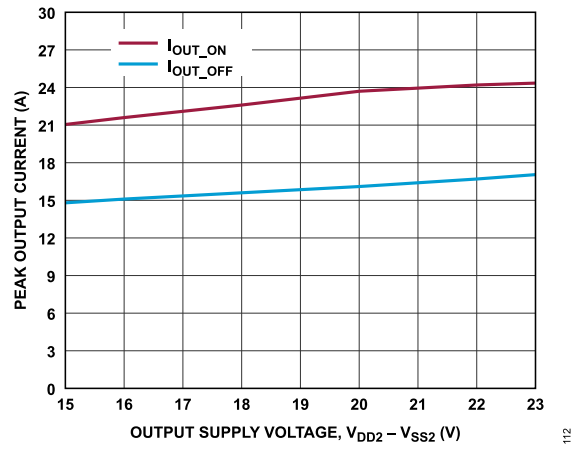

Figure 12. Peak Output Current vs. Output Supply Voltage, 0.015 Ω Series Sense Resistor, One Output Channel Active

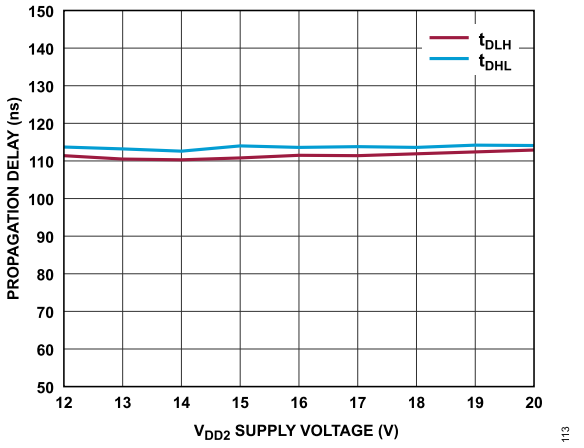

Figure 13. Propagation Delay vs. Output Supply Voltage (V_{DD2}), V_{DD1} = 5 V, V_{SS2} = −3.25 V, 2.2 nF Load, R_G = 3.9 Ω

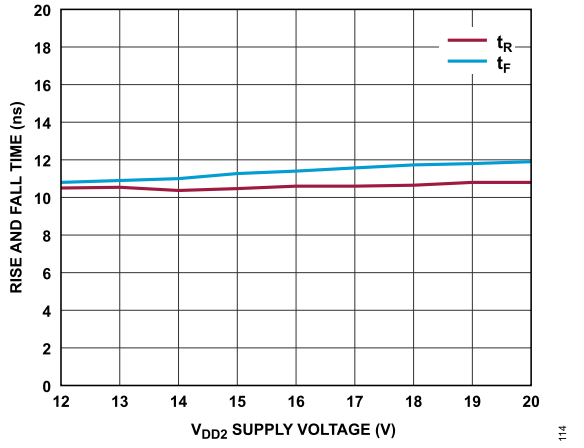

Figure 14. Rise and Fall Time vs. Output Supply Voltage (V_{DD2}), V_{DD1} = 5 V, V_{SS2} = −3.25 V, 2.2 nF Load, R_G = 3.9 Ω

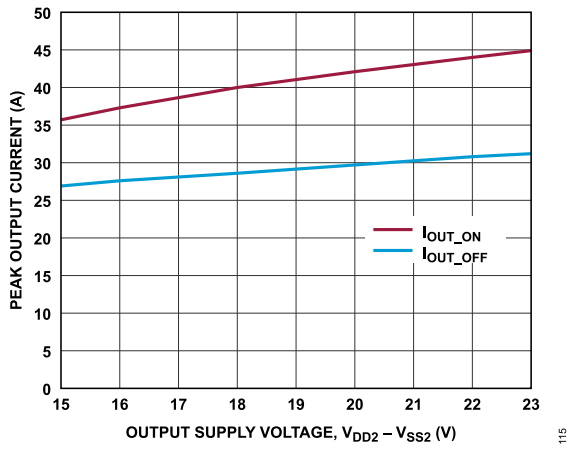

Figure 15. Peak Output Current vs. Output Supply Voltage, 0.015 Ω Series Sense Resistor, Two Output Channels Active

TYPICAL PERFORMANCE CHARACTERISTICS

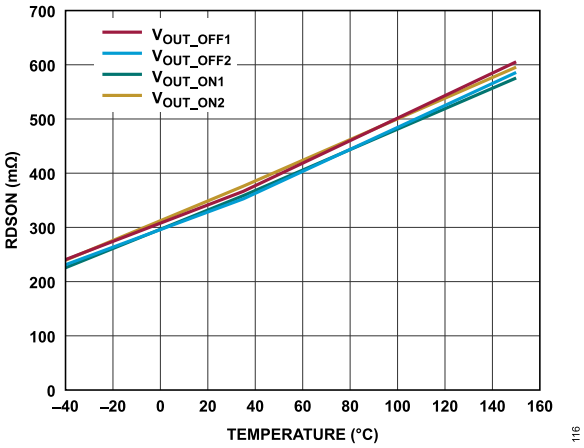

Figure 16. Output Resistance (RDSON) vs. Ambient Temperature, V_{DD2} = 15 V, V_{SS2} = 0 V, 500 mA Test Current

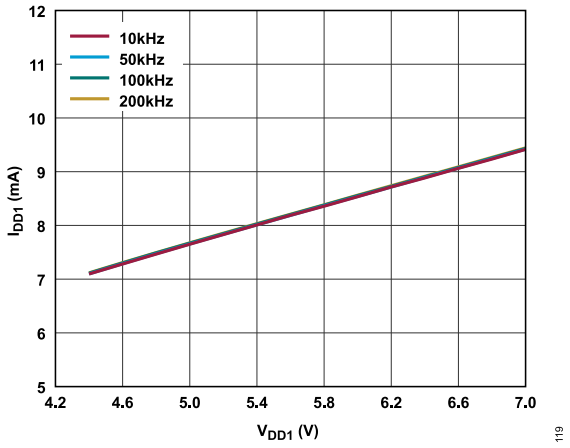

Figure 19. V_{DD1} Supply Current (I_{DD1}) vs. Supply Voltage at Various Frequency, 50% Duty Cycle

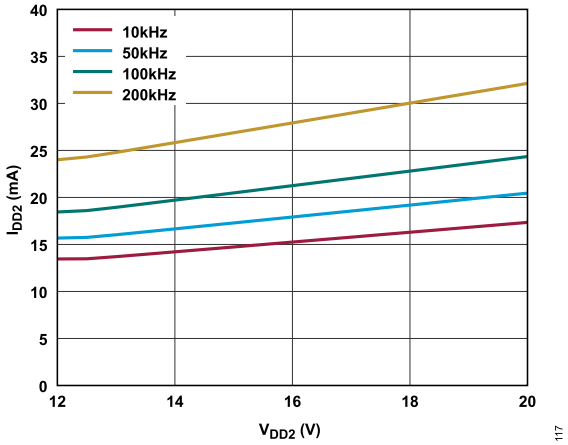

Figure 17. V_{DD2} Supply Current (I_{DD2}) vs. Supply Voltage at Various Frequency, 50% Duty Cycle, 2.2 nF Load, V_{SS2} = −3.25 V

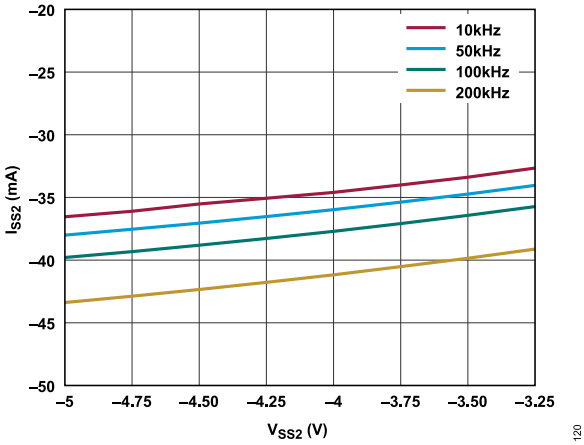

Figure 20. V_{SS2} Supply Current (I_{SS2}) vs. Supply Voltage at Various Frequency, 50% Duty Cycle, 2.2 nF Load, V_{DD2} = 18 V,

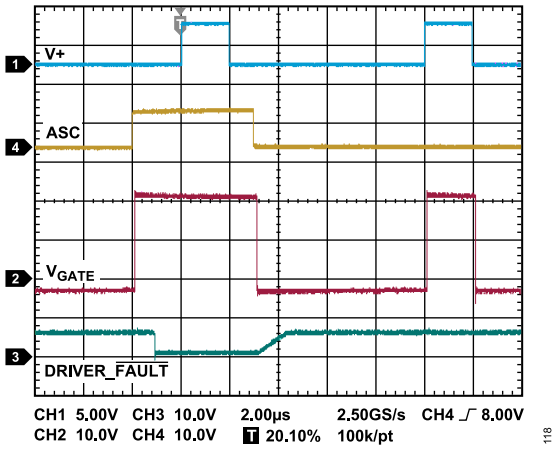

Figure 18. ASC Dominance

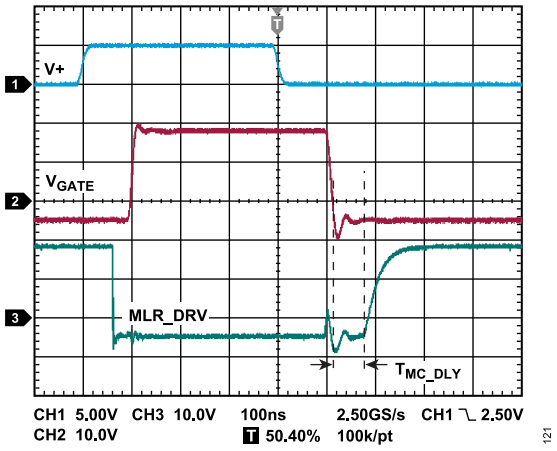

Figure 21. Miller Drive Delay, 1 kΩ Pull-Up Resistor

THEORY OF OPERATION

Gate drivers are required in situations where fast rise times of switching device gates are required. The gate signals for enhancement power devices are referenced to a source or emitter node. The gate driver must follow this source or emitter node. As such, isolation is necessary between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a complementary metal-oxide semiconductor (CMOS) output reduce the total delay time and increase the final drive strength of the driver.

The ADuM4177 achieves isolation between the control side and the output side of the gate driver using a high frequency carrier that transmits data across the isolation barrier with *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. The ADuM4177 uses positive logic on/off keying (OOK) encoding, in which a high signal is transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices and can drive in situations where shoot through conditions are present. The architecture of the ADuM4177 is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and differential coil layout. Figure 22 shows the OOK encoding used by the ADuM4177.

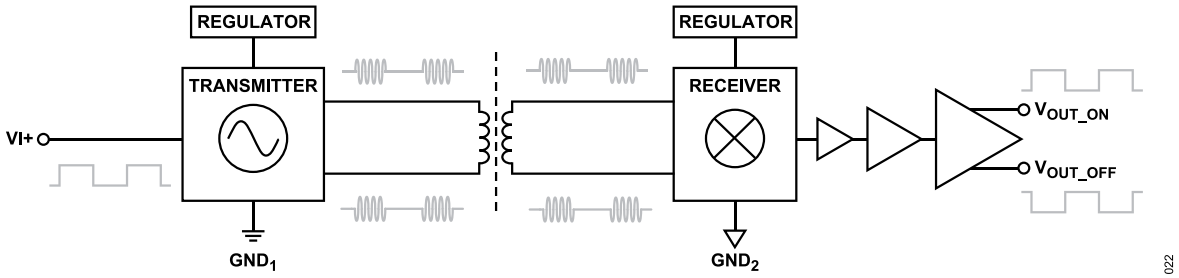

Figure 22. Operational Block Diagram of OOK Encoding

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4177 SiC gate driver requires power supply bypassing at the V_{DD1}, V_{DD2}, and V_{SS2} supply pins. Use a ceramic capacitor greater than 10 µF on V_{DD1} to GND_1. Add at least 10 µF of capacitance on V_{DD2} to V_{SS2} to provide decoupling to the secondary side circuitry. Separate decoupling capacitors must be placed between V_{DD2} to GND_2 and from GND_2 to V_{SS2}. These capacitors supply the energy to drive the power device gate on and off and must be at least 10 µF each. Large gate charge power devices may need more capacitance. This capacitance can be provided by multiple parallel capacitors. Avoid using vias on the bypass capacitor or employ multiple vias to reduce the inductance in the bypassing because board vias can introduce parasitic inductance. The total lead length between both ends of the smaller capacitor and the input or output power supply pin should not exceed approximately 5 mm.

To improve robustness against bulk current injection (BCI), the input pins (VI+, VI−, MOSI, $\overline{CS}$, and SCLK) can have series 100 Ω resistors placed to limit current. The inclusion of 100 Ω resistors in series with input lines is highly recommended.

POWER SUPPLIES

V_{DD1} Supply

V_{DD1} can be operated between 4.4 V (min) to 7 V (max). The V_{DD1} power supply powers the primary side circuitry. A UVLO is included to prevent underpowered operation. The ADuM4177 begins to operate once the V_{DD1} voltage exceeds the rising UVLO threshold, 3.8 V (typical), and continues to operate until the V_{DD1} voltage falls below the falling UVLO threshold, 3.5 V (typical). The ramp rate on the V_{DD1} pin must be kept below 1 V/ms to avoid stress on the primary side silicon. Both startup and operation have this dv/dt rate limitation.

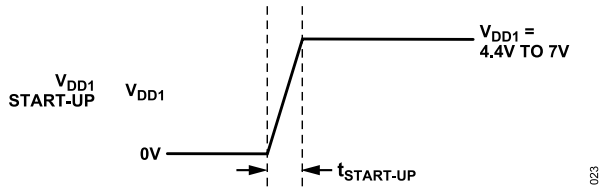

Figure 23. Start-Up dv/dt

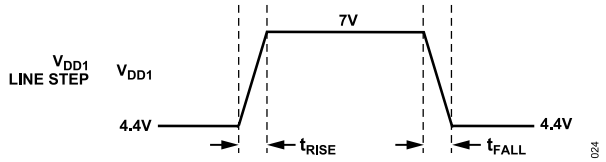

Figure 24. Line-Step dv/dt

V_{DD2}/V_{SS2} Supplies (Bipolar Mode)

The ADuM4177 allows for default bipolar output to drive power devices both positively and negatively with respect to their source/emitter node. The secondary side of the ADuM4177 is powered through the V_{DD2}, GND_2, and V_{SS2} pins. The operating range of V_{DD2} to GND_2 is 12 V (min) to 23 V (max). The maximum voltage between V_{DD2} and V_{SS2} is 23 V (max), meaning that if a negative voltage drive is used, the V_{DD2} to GND_2 voltage must be below 23 V − $|V_{SS2}|$ V. A negative drive can be obtained by supplying a −5 V (min) to −3.25 V (max) voltage between V_{SS2} and GND_2.

The ADuM4177 provides secondary side UVLO and OVP protections on both the V_{DD2} and V_{SS2} pins, ensuring that the gate drive is within tight tolerances. The V_{DD2} UVLO and OVP is referenced to V_{SS2}, ensuring a specific total gate voltage swing. The V_{SS2} UVLO and OVP is referenced to GND_2 as shown in Figure 25.

Voltage supply excursions outside of the V_{DD2} and V_{SS2} UVLO and OVP issues a fault, shut off the driver output, and enter soft shutdown. The faults latch for the prescribed timings, allowing for fault differentiation at the pin reporting level on the primary side.

The UVLO is programmable through the SPI register 0x54 Bits[2:0], VDD2_UVLO_SLCT. The values in register 0x54 are EEPROM programmable, resulting in UVLO options that persist between power cycles.

By default, the registers of the ADuM4177 are programmed to work in bipolar mode. A negative voltage within the UVLO/OVP range of V_{SS2} is required.

APPLICATIONS INFORMATION

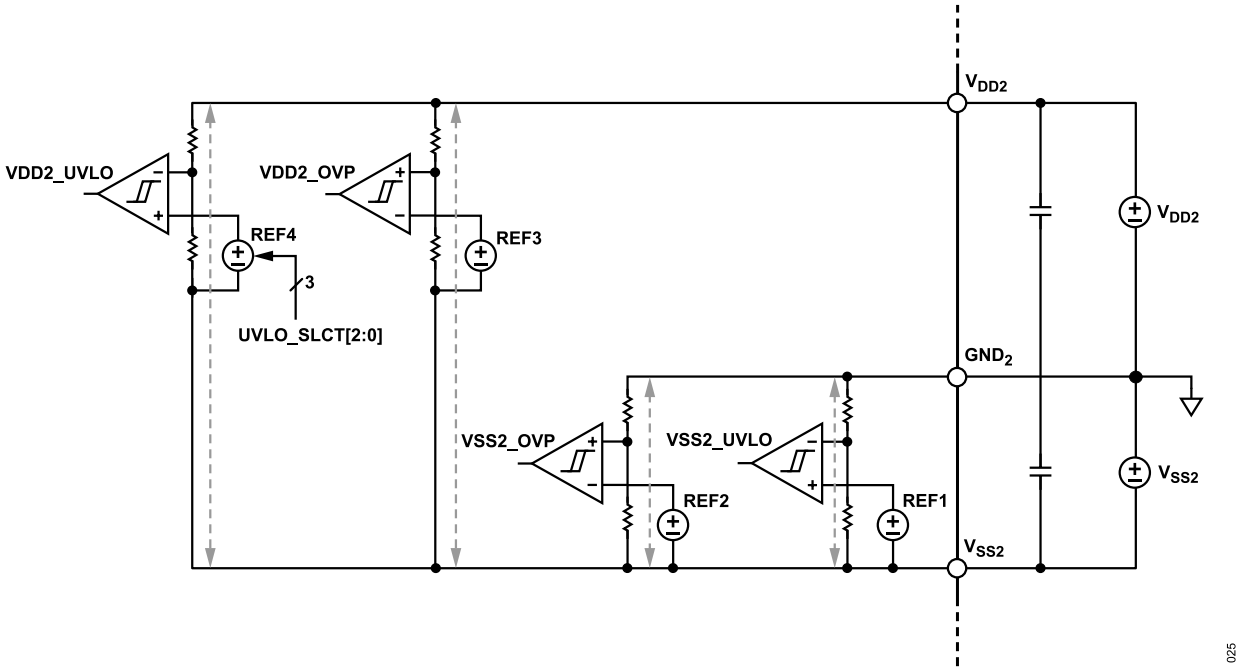

Figure 25. Functional V_{DD2}/V_{SS2} Supply UVLO and OVP

APPLICATIONS INFORMATION

V_{SS2} = GND_2 (Unipolar Mode)

To operate in unipolar mode (V_{SS2} = GND_2), register 0x52 Bits[7:0], OP_MODE must be programmed to 01101101. This is the only bit configuration that disables the V_{SS2} UVLO to be able to operate in unipolar mode. Operating with bipolar supply in unipolar mode damages the part.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay describes the time that it takes a logic signal to propagate through a component. The propagation delay to a low output can differ from the propagation delay to a high output. The ADuM4177 specifies the rising propagation delay, t_{DLH} (see Figure 26), as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold. Similarly, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic-low threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry-standard for the gate drivers.

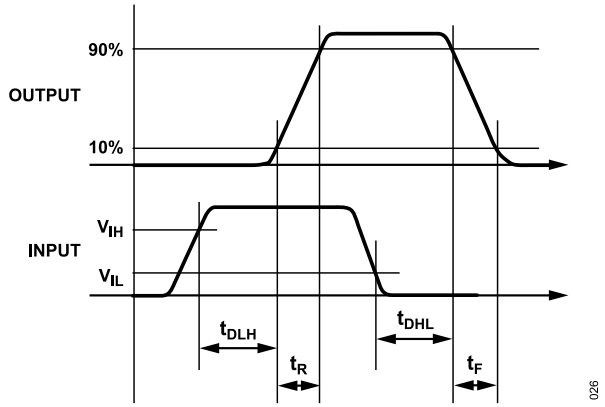

Figure 26. Propagation Delay Parameters

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4177 components operating under the same temperature, input voltage, and load conditions.

SERIAL-PERIPHERAL INTERFACE (SPI)

The SPI, consisting of the MOSI, MISO, SCLK, and $\overline{CS}$ pins, is an independent interface that is active when the primary side supply voltage is higher than the $V_{VDD1UV+}$ and secondary side V_{DD2} − V_{SS2} voltage is greater than 11.5 V (typical). For a functional block diagram of the SPI, see Figure 27. The format for an SPI bit sequence write/read is shown in Table 12. Programming is performed using the standard SPI convention of clock polarity (CPOL) = 0 and clock phase (CPHA) = 1. A full SPI bit sequence is 24 bits long.

Table 12. SPI Register Format (Except PWM Registers)

Command Field	Address Field	Data Field	CRC Field
Bit 23	Bits[22:16]	Bits[15:8]	Bits[7:0]
READ (= 0)/WRITE (= 1)	ADDR, Bits[6:0]	Data, Bits[7:0]	CRC, Bits[7:0]

Registers 0x08 and 0x09 for the PWM duty-cycle information follow a different format for the readback, see Table 13.

Table 13. Register 0x08, 0x09 PWM Format

MISO Read		
Data Field	**Data Field**	**CRC Field**
Bits[23:20]	Bits[19:8]	Bits[7:0]
0000	Data, Bits[11:0]	CRC, Bits[7:0]

The PWM register format allows a larger data field to properly send the duty-cycle information in a single read step.

Cyclic redundancy check (CRC) is used to ensure proper integrity of a read/write operation. In addition to CRC, error correcting code (ECC) is used on both primary side fuse trim and the secondary side EEPROM bits. A SNG_ERR fault occurs if the ECC successfully corrected a single bit error in the secondary side EEPROM. If a SNG_ERR fault occurs, the ADuM4177 operates normally, but there is a defect present in the part. If an uncorrected error occurs, a DBL_ERR fault is posted in the IC digital status register and shuts down the operation of the device. On the primary side, if a DBL_ERR error occurs, no action is taken to affect operation of the ADuM4177.

A communication fault occurs during an SPI write or read operation. A communication fault occurs if either not enough bits are sent during an SPI transfer, or if too many bits are sent during an SPI transfer. In either case, in the event of communication fault, the SPI transfer is aborted. A communication fault is posted to the IC1 digital status register and the IC3 digital status register. A communication fault does not affect normal operation of the ADuM4177.

APPLICATIONS INFORMATION

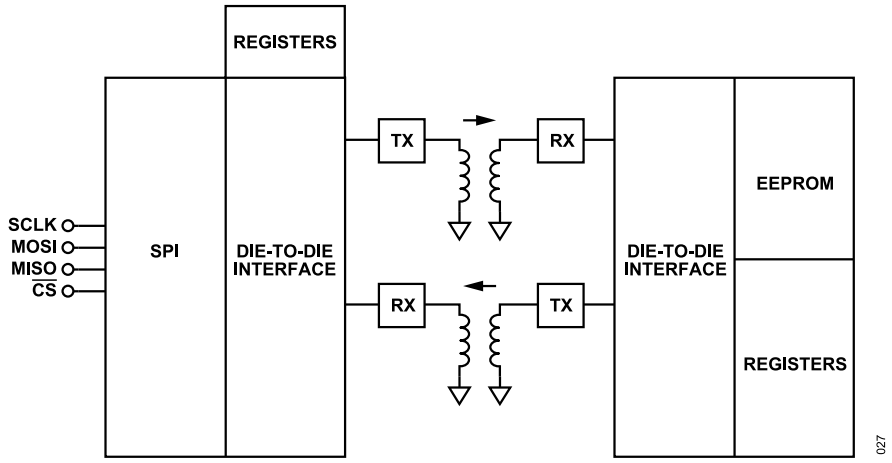

Figure 27. SPI Functional Block Diagram

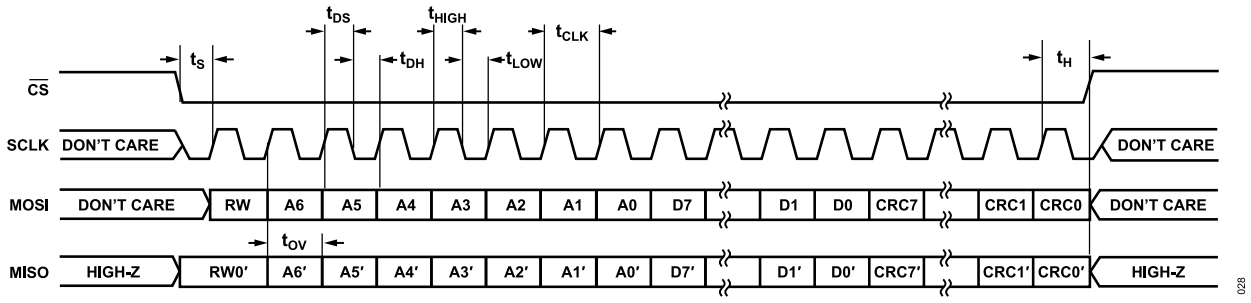

Figure 28. SPI Timing Diagram

APPLICATIONS INFORMATION

CYCLIC REDUNDANCY CHECK (CRC)

The ADuM4177 SPI word is constructed with a CRC field. The 8 bit CRC word, CRC Bits[7:0], is set to a specific value, which is associated with value of the remaining 16 bits, Data Bits[7:0], ADDR Bits[6:0], and the READ/WRITE bit.

If the user performs a write command, the correct CRC Bits[7:0] value must be calculated for the corresponding remaining 16 bits. When performing the write, all data must be transferred to the ADuM4177 device. Internally, the ADuM4177 takes the CRC Bits[7:0] value field and compare it to the remaining 16 bits. If the values correspond correctly, no error is reported. If the values do not correlate, then a CRC_error fault occurs.

When the user is reading from the MISO pin, the data read corresponds to the bit sequence shown in Table 12 for the SPI register except PWM registers. The ADuM4177 calculates the proper CRC Bits[7:0] field value as the data is transferred to the MISO pin. To determine if the data from the MISO pin is correct, the user must check the CRC Bits[7:0] field against the remaining 16 bits. If the CRC Bits[7:0] value, compared to Bits[23:8], return an incorrect result, the read must be discarded.

The CRC value is based on the PMBus CRC-8 packet check, which uses the polynomial $x^8 + x^2 + x + 1$.

When reading the PWM registers, the data read corresponds to the bit sequence shown in Table 13. Since the PWM results are longer than 8 bits (Data Bits[11:0]), the ADDR is not returned in the SPI word. The CRC is precalculated with the address value of the PWM register being read as a seed, and then the CRC is calculated with the data to be transferred (0x0, PWM results) to generate the SPI word. If an incorrect address is read from vs. what the host is expected, the CRC fails.

SIMULATING AND PROGRAMMING EEPROM

To simulate trim or write to registers but not program the available EEPROM bits, both simulate bits, Bit 0 and Bit 1, must be set to 1, and the program bit, Bit 2, must be set to 0 in the data field. To program trim, or program any EEPROM registers, both simulate bits, and the program bit, must be set to 1. This helps prevent false writes by requiring a specific 3 bit sequence to both simulate and program the register space on the secondary side. To summarize:

Simulate register values ➡ Bits[2:0] = 011

Program EEPROM/register values ➡ Bits[2:0] = 111

Figure 29 shows a flow diagram for both the simulate and program steps for the ADuM4177 secondary side register space. To determine when the programming step is complete, read the IC3 control register, address 0x42. When Bit 2 changes from a 1 to a 0, the programming cycle has completed. A programming step can take up to 40 ms (max) to complete.

During V_{DD1} startup, the SPI interface remains inactive until the first rising edge of the $\overline{CS}$ pin. After the $\overline{CS}$ pin goes high for the first time, the SPI responds when the $\overline{CS}$ pin if forced low, provided the V_{DD1} UVLO is valid and the $V_{DD2} - V_{SS2}$ supply is greater than 11.5 V (typical).

If during startup, V_{DD1} is applied while V_{DD2} is 0 V, or if V_{DD2} is lost during normal operation, the SPI interface continues to operate. The registers located on the primary side can be written to and read from. However, if any register on the secondary side is written to, no value is accepted without power present on V_{DD2}. If any registers are read on the secondary side, MISO returns all 0's if power is not present on V_{DD2}. With power not present on V_{DD2}, the SPI return receiver has no signal present, which returns only 0's.

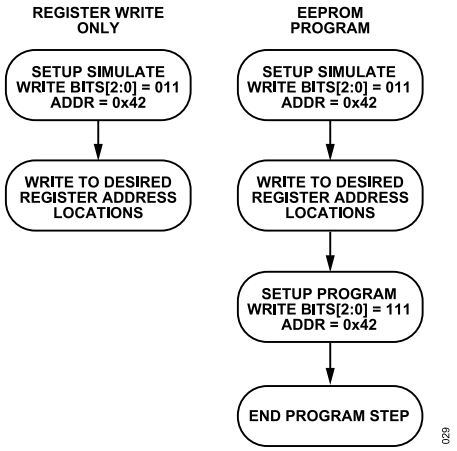

Figure 29. Simulate and Program Flow Diagram

PROGRAMMING ERROR FAULT

Some faults are written to fault registers for readback. One fault accessible by register read is the Programming Failed fault. Figure 30 shows a state diagram for the EEPROM programming flow. After 111 is written to Bits[2:0] IC3 control register, address 0x42, the EEPROM program cycle starts. If at the end of the program cycle, the EEPROM write did not complete successfully, the ADuM4177 repeats the step automatically. The ADuM4177 continues this for a total of 40 attempts if any preceding attempt is not successful. After 40 programming attempts, if errors continue, the ADuM4177 aborts the programming cycle and issue a 1 to the programming failed bit in the IC3 digital status register.

APPLICATIONS INFORMATION

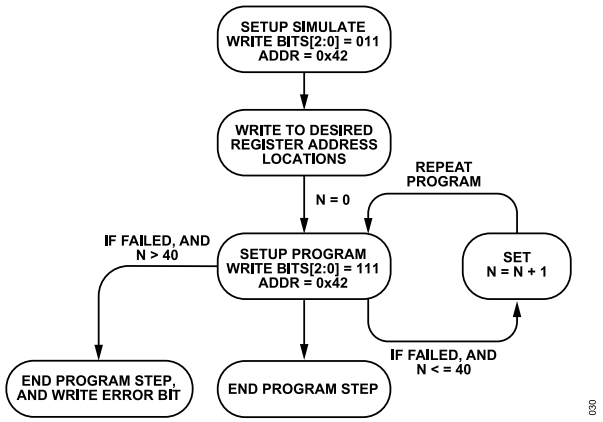

Figure 30. Programming State Diagram

DAISY-CHAINING ADUM4177

A typical daisy-chain configuration for the ADuM4177 is shown in Figure 31. Note that the resistor pull-ups (or pull-downs) must be used on each MOSI pin to avoid high impedance states when the $\overline{CS}$ pin is set high, and the MISO pin goes into a Hi-Z output state.

The ADuM4177 is able to be daisy-chained to reduce MOSI, MISO, $\overline{CS}$, and SCLK lines interfacing the controller and multiple ADuM4177 units. For the following explanation, see the configuration shown in Figure 32.

In the configuration shown in Figure 32, three units are shown connected. Each ADuM4177 expects to see some integer multiple of 24 clock cycles per cycle of the $\overline{CS}$ pin. If a noninteger number of clock cycles occurs between the falling and rising edges of the $\overline{CS}$ pin, the commands are ignored. This is important to note, as the ADuM4177 can be daisy-chained with devices that are not ADuM4177 only if the added devices also require an integer number of multiples of 24 cycles.

In this example, because there are three devices daisy-chained, each falling and rising edge of $\overline{CS}$ have 24 x 3 cycles on SCLK. This is because three packets of 24 bits need to be sent. Figure 33 shows an example transfer, where commands are sent at Node A, and responses are received at Node D.

In Figure 33, there are three separate $\overline{CS}$ rising edges. The commands sent are read into each individual ADuM4177 when the rising edge of $\overline{CS}$ occurs. C/ stands for Command, R/ stands for response, and X stands for unknown. Before the first rising edge, Edge 1, there are three commands being sent to the devices. The devices repeat the bitstream given to their MOSI pin 24 cycles after. The repeated bitstream appears on the MISO pin. When the rising edge of $\overline{CS}$ occurs, the last 24 bits seen on each of the ADuM4177 device's MOSI pin is taken into the device as a command. In this example, command C goes to ADuM4177 Device 1, command B goes to ADuM4177 Device 2, and command A goes to ADuM4177 Device 3. During the next falling edge of $\overline{CS}$, the devices are now able to send the responses to the commands, as well as take in the next bitstream of commands. Since ADuM4177 Device 3 is the last in the daisy chain, it is the first to output its response to the controller. This means response A is seen on Node D first, followed by response B, and finally response C.

If a single command is required to be sent to only one device, a read command can be given to the other devices on the chain. For example, if a write xxx command is to be given to ADuM4177 Device 2, then command B can be write xxx, while command A and command C can be read xxx. On the rising edge of $\overline{CS}$, the commands are registered to the devices, and only ADuM4177 Device 2 has a write command given to it.

There does not need to be an explicit wait time between 24 bit packets. The spaces between the 24 bit packets are drawn for clarity of bit count, and not to show actual timing. It is possible to have a single stream of 72 bits and SCLK periods in this example.

APPLICATIONS INFORMATION

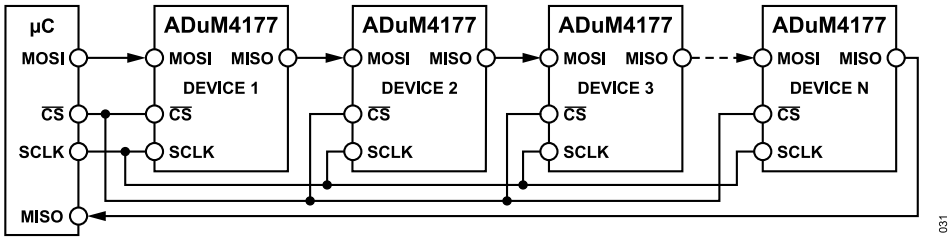

Figure 31. Daisy-Chain Diagram

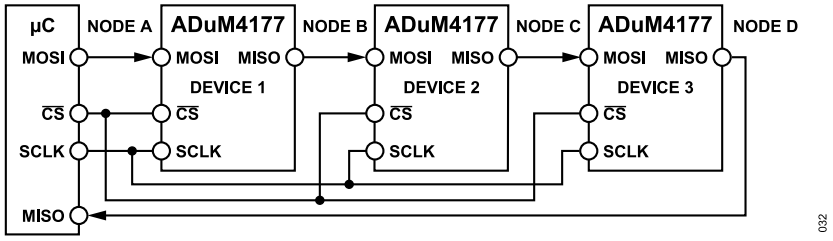

Figure 32. Daisy-Chain of Three ADuM4177 Devices

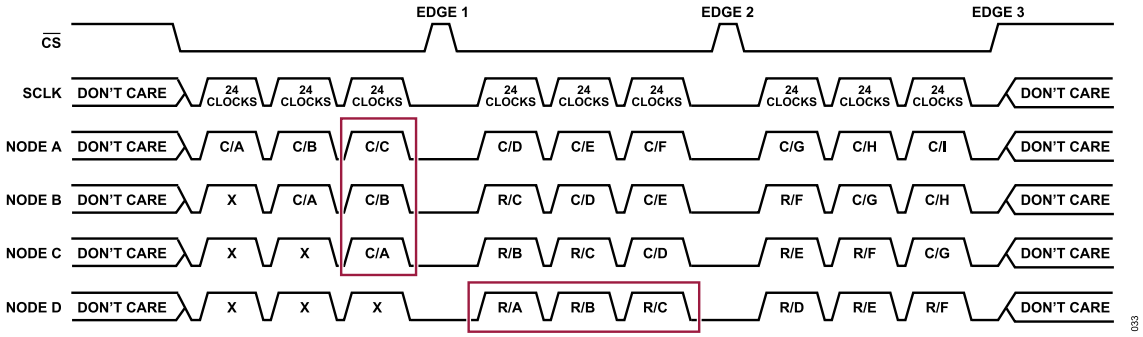

Figure 33. Example SPI Transfer of Three $\overline{CS}$ Edges

APPLICATIONS INFORMATION

TEMPERATURE SENSE

The ADuM4177 provides the ability to measure internal die temperature of the secondary side die, as well as a remote temperature sense that can be used with a diode stack or negative temperature coefficient (NTC) temperature sensor like thermistor external to the ADuM4177 to measure temperatures outside of the ADuM4177. Remote temperature sensing is performed using the TS pin and is referred to as PWM1_DUTY in register names. Internal die temperature of the secondary side ADuM4177 die is reported as PWM2_DUTY in register names.

EXTERNAL TEMPERATURE SENSE

The ADuM4177 includes an analog input pin, TS, referenced to the V_{SS2} pin on the secondary side that can report the value of the voltage on TS within a specified range operating at 10 kHz (typical). The reporting occurs on the primary side and is reported both with a 1 kHz (typical) PWM signal on the TEMP_OUT pin, as well as in SPI register 0x08 Bits[11:0] PWM1_DUTY.

TEMP_OUT ENCODING

The target TEMP_OUT duty cycle vs. TS voltage transfer function follows:

$$TEMP\_OUT\,(DUTY) = (-31.25) \times V_{TS} + 127.63 \quad (1)$$

where:

TEMP_OUT(DUTY) is the duty cycle of the TEMP_OUT pin.

V_{TS} is the voltage seen on TS pin.

The target TEMP_OUT duty cycle encoding for the ADuM4177 is −40ºC = 12% and 150ºC = 87%. The ADuM4177 TEMP_OUT duty signal has a built-in maximum duty cycle, 98% (typical), and minimum duty cycle, 2.5% (typical). If the TS voltage sense pins go outside the normal range of operation, the TEMP_OUT duty ratio is fixed by the ADuM4177.

The ADuM4177 temperature sense is designed to work with external diode sense stack. An internal 210 µA (typical) bias current is used to bias the external diode stack. The ADuM4177 also contains trim capability to calibrate manufacturing variation in a temperature sense diode stack. The ADuM4177 allows for gain and offset trimming of the duty cycle response of the TS pin to allow for calibration due to variation in temperature sensing diode stacks.

The ADuM4177 TS pin can also be used with an external NTC rather than a diode stack. A resistor network may be needed to ensure that the range of operation is within 1.3 V and 3.7 V.

Figure 37 provides typical start-up diagram for the temperature sense output PWM duty cycle. After the V_{DD2}−V_{SS2} UVLO clears, the TEMP_OUT duty cycle is valid within time t_{FILT}, 3.15 ms (max).

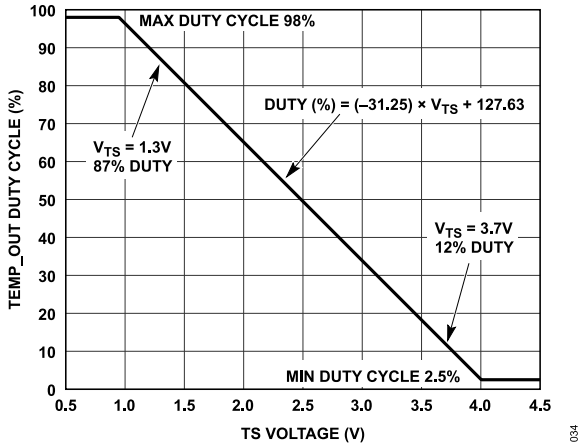

Figure 34. Typical Behavior of TEMP_OUT Duty Cycle vs. Voltage at TS Pin

APPLICATIONS INFORMATION

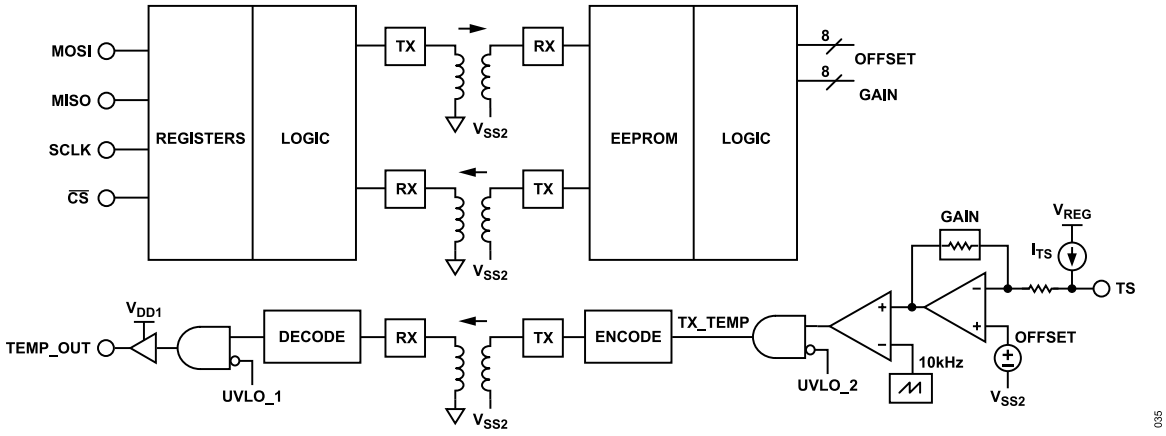

Figure 35. Temperature Sense Basic Block Diagram

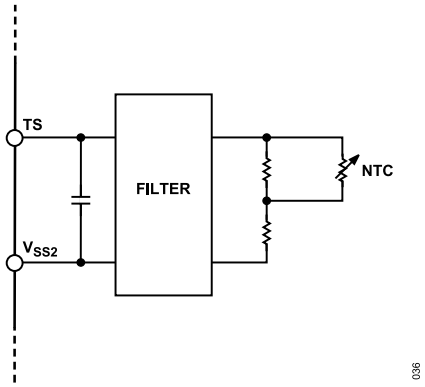

Figure 36. Example NTC Sense Element Configuration

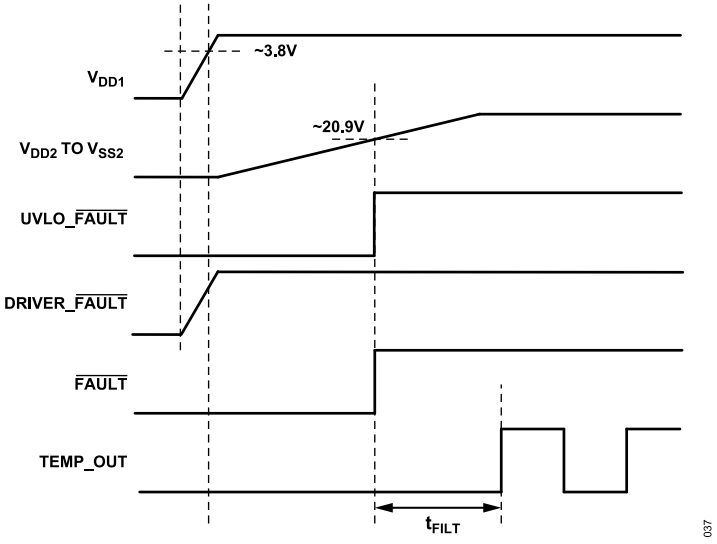

Figure 37. Temperature Sense Start-Up Diagram

APPLICATIONS INFORMATION

TEMPERATURE SENSE DUTY CYCLE REGISTER

In addition to having the TEMP_OUT pin to read the 1 kHz (typical) temperature sense duty cycle, the ADuM4177 offers two addressable registers to read the TS pin and an internal secondary side diode through the SPI, registers 0x08 and 0x09.

Register 0x08 provides the duty cycle of the TS pin voltage sensed by the diode stack, or NTC.

Register 0x09 provides temperature information for the secondary driver die of the ADuM4177. The data present in register 0x09 is the duty cycle of the equivalent temperature seen on the secondary side die. The temperature is given by the following equation:

$$T = (-6.732) \times D + 436.8 \quad (2)$$

where:

D is the duty cycle given as a %, read from register 0x09 divided by 2^{12} or 4096.

T is given as temperature in °C.

The temperature sense on the secondary side operates at 10 kHz (typical). Data is captured on the secondary side for both TS and the internal diode and transferred to the primary side at the rising edge at the start of the next cycle 10 kHz (typical) clock. ADuM4177 uses a boxcar filtering technique with the following equation:

$$val = (val_{-1}/2) + x/2 \quad (3)$$

where:

x is the new temperature sense value obtain.

val_{-1} is the previous calculated average value.

val is the new average calculation, which is transferred to IC1.

At the end of a data transfer, both TS and the internal diode PWM registers is updated. Temperature sense values are updated every 100 µs (typical) and can be obtained by a read through the SPI interface.

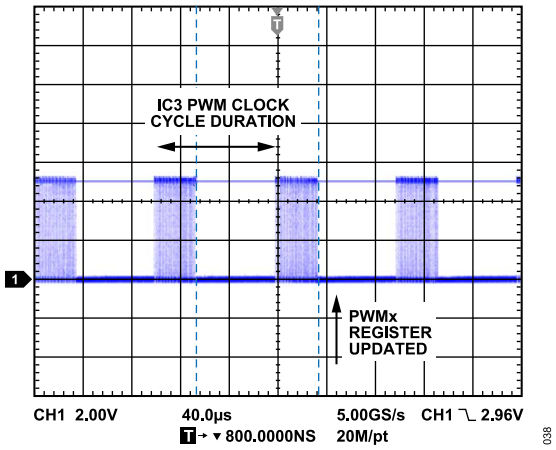

Figure 38. Temperature Sense Data Transfer

TS ANALOG INPUT

The ADuM4177 offers the ability to disable the TS pin 210 µA (typical) bias current. This can be done by setting Bit 0 in register 0x53. The default value for Bit 0 is 0, so the current bias is enabled by default.

Disabling the TS pin current allows the TS pin to be used as a pure analog input. The TS pin voltage can be monitored through the TEMP_OUT duty cycle, or one can read the TEMP_OUT duty cycle using register 0x08. The transfer curve is:

$$TEMP\_OUT(DUTY) = (-31.25) \times V_{TS} + 127.63 \quad (4)$$

where:

TEMP_OUT(DUTY) = duty cycle of the TEMP_OUT pin.

V_{TS} = voltage seen on TS pin.

APPLICATIONS INFORMATION

TS COMPARATOR THRESHOLDS

Figure 39 shows a detailed block diagram of the ADuM4177 temperature sense. The ADuM4177 has built-in comparators on the TS pin that can be configured to two different thresholds. The comparator thresholds can be set through the SPI bus writing to register 0x53. Note, only one comparator threshold can be configured at a time. The default configuration is that the TS comparator is disabled. When enabled, the comparator output maps to the driver fault flag. The TS comparator threshold does not create a fault on the secondary side, which means it does not force the driver into a soft shutdown. When enabled, the TS comparator only flags on the primary side DRIVER_$\overline{\text{FAULT}}$ pin.

TS comparator threshold 1 is a falling threshold, 1.32 V (typical). One application for this threshold is as a TS pin OT threshold.

TS comparator threshold 2 is a rising threshold, 2.97 V (typical). With the TS pin configured as a pure analog input, this threshold can be used as a high-voltage sense threshold.

Using the TS_COMP_FILT_DIS bit, the user can disable a 1.64 ms (typical) filter to the TS comparator. Setting TS_COMP_FILT_DIS to 0 enables the filter, and 1 disables the filter. This can be used to filter noise seen on the TS pin during sensing. The default state for the TS comparator filter time is 0, meaning filter is enabled.

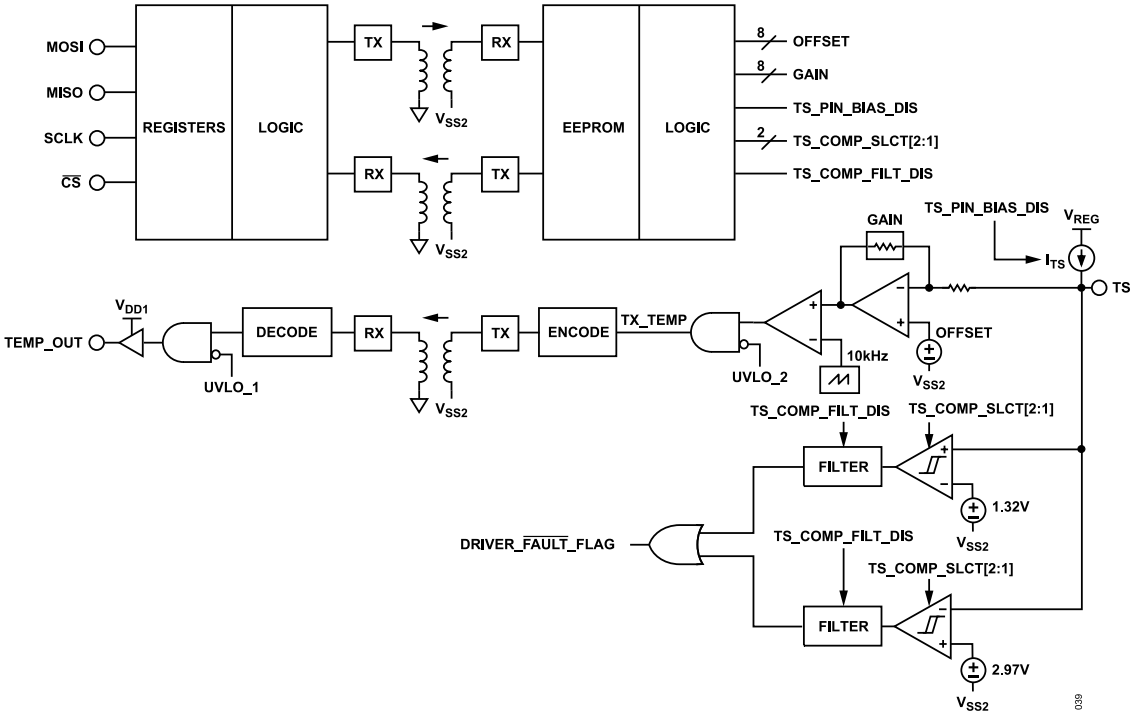

Figure 39. TS Pin Configurable Comparators

APPLICATIONS INFORMATION

TS PWM UPDATE FAULT

The primary side of the ADuM4177 requires periodic updates of the TS and internal diode temperature sense PWM data. If a PWM update is not received on the primary side within two rising edges of the TEMP_OUT PWM signal, a fault is issued to Bit 3 of the primary side digital status register, address 0x01. If a PWM update is received after the fault, the TEMP_OUT PWM signal resumes, but the fault remains posted in the primary side digital status register until it is cleared by the user.

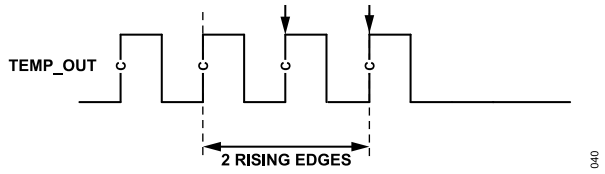

Figure 40. Example TEMP_OUT Watchdog Timing

GATE DRIVE

The ADuM4177 gate drive has integrated low Rdson, 0.38 Ω (typical), power FETs to drive up to 40 A of sourcing and 30 A of sinking peak short-circuit current. The ADuM4177 has an integrated low Rdson soft shutdown 0.38 Ω (typical) FET to realize critical shutdown requirements for SiC devices. With an external resistor, the soft shutdown can be adjusted. Using an open drain MILLER_DRV pin, the ADuM4177 can drive an external miller clamp device. Using an external miller switch allows critical component placement to reduce PCB inductance, which affects the performance of the SiC device.

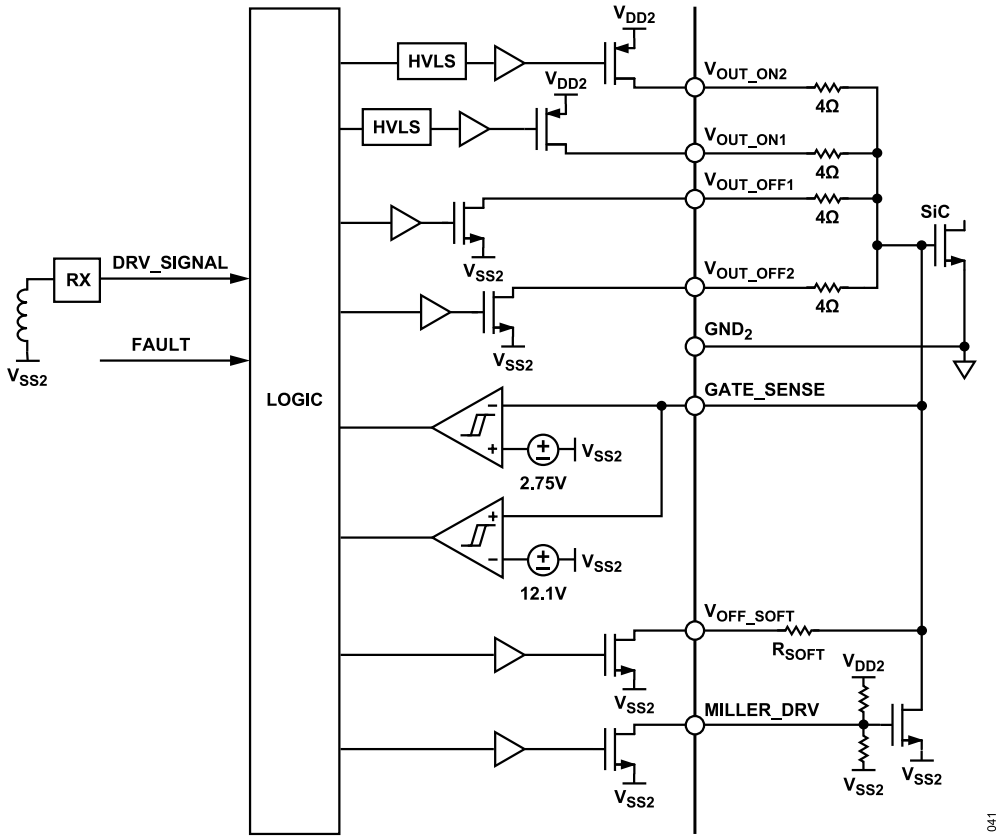

Figure 41. Driver Functional Block Diagram

APPLICATIONS INFORMATION

SLEW-RATE CONTROL

The ADuM4177 contains a programmable feature through the SPI to change the drive strength of the gate driver to change the slew rate of the rise and fall gate waveforms. The rise time and fall time can be modified individually. Figure 42 and Figure 43 show the functional diagrams for the driver output of the ADuM4177. Figure 44 shows the typical waveforms for the driver output while configuring the rising gate drive and the falling gate drive.

Since the slew-rate control signals are updated asynchronously to the driver signal, care must be taken to ensure that there is no disruption to the drive signal at the SiC gate. As shown in both Figure 42 and Figure 43, the V_{OUT_ON} and V_{OUT_OFF} slews are not updated until the first rising edge of the driver signal after either the gd_off_slew_slct and gd_on_slew_slct registers bits are updated.

Table 1 shows the typical V_{OUT_ONx} and V_{OUT_OFFx} RDSON values for configured slew-rate settings. The default configuration is for all internal gate drive FETs to be active.

The slew-rate settings can be configured in register 0x55 Bit 0 of register 0x55 controls the V_{OUT_OFF2} switch. Bit 1 of register 0x55 controls the V_{OUT_ON2} switch.

APPLICATIONS INFORMATION

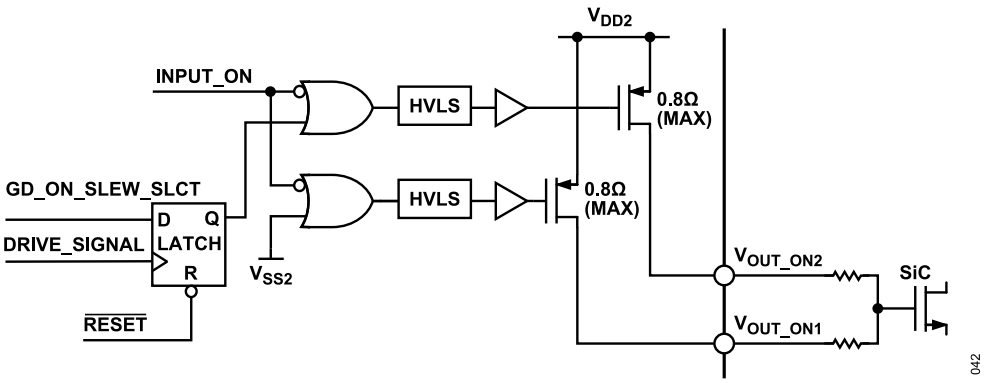

Figure 42. V_{OUT_ON} Slew-Rate Control

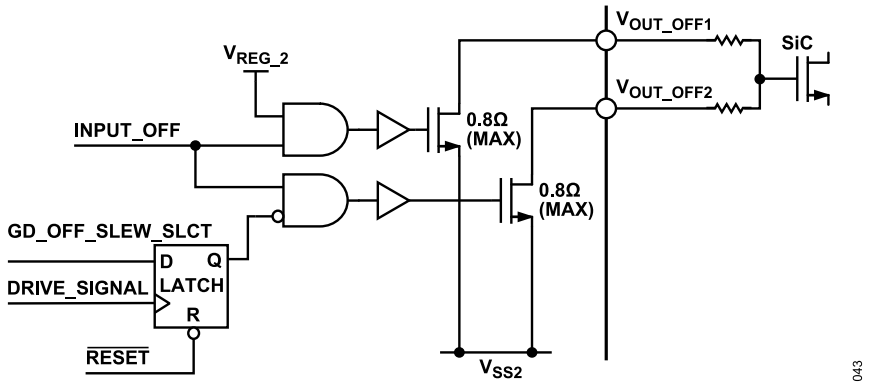

Figure 43. V_{OUT_OFF} Slew-Rate Control

APPLICATIONS INFORMATION

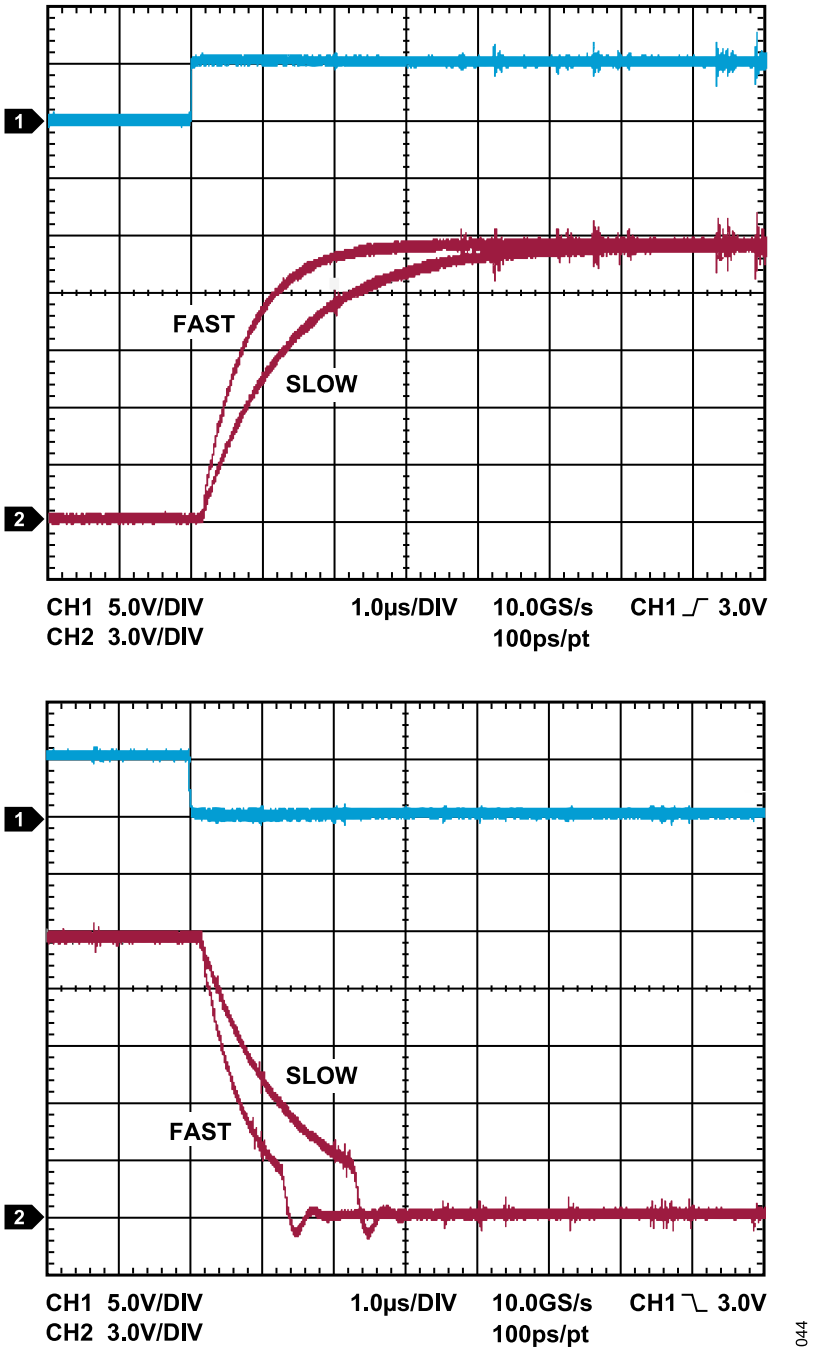

Figure 44. Slew-Rate Control Waveforms

APPLICATIONS INFORMATION

PROTECTION FEATURES

Desaturation Detection

The ADuM4177 contains an integrated DESAT function for insulated-gate bipolar transistor (IGBT) and SiC devices. During normal operation, when the power device is on, the expected drain to source voltage should be below a given value. During high current events, this voltage can rise, allowing for detection of a power device that is under a short-circuit situation, or not able to hold the drain to source voltage down. If the drain to source voltage increases higher than the DESAT threshold, the DESAT pin can be pulled up allowing for desaturation event detection. The rising DESAT threshold is 7 V (typical). The DESAT pin charging current is set using an external resistor. An internal pull-up current, 10 µA (typical), is used for open pin detection. The delay from DESAT rising to the start of the soft shutdown, t_{DESAT_DLY}, is 100 ns (typical).

The ADuM4177 DESAT function includes a gate sense control and programmable delay to blank the DESAT input after VI+ has commanded the output high. The gate sense control monitors the gate voltage to transition above 12.1 V (typical) with respect to VSS2 before initiating the programmable delay. The selected threshold is approximately the end of the miller plateau voltage. The programmable delay is selectable between −20 ns and 680 ns. Employing both functions adjusts the blanking delay to the switch size and load conditions. Noisier and/or slower switching devices need longer blanking times. The gate sense control can be disabled with the register address 0x53 Bit 4 GSR_DESAT_DIS. The programmable delay is adjusted with register address 0x54 Bits[5:3].

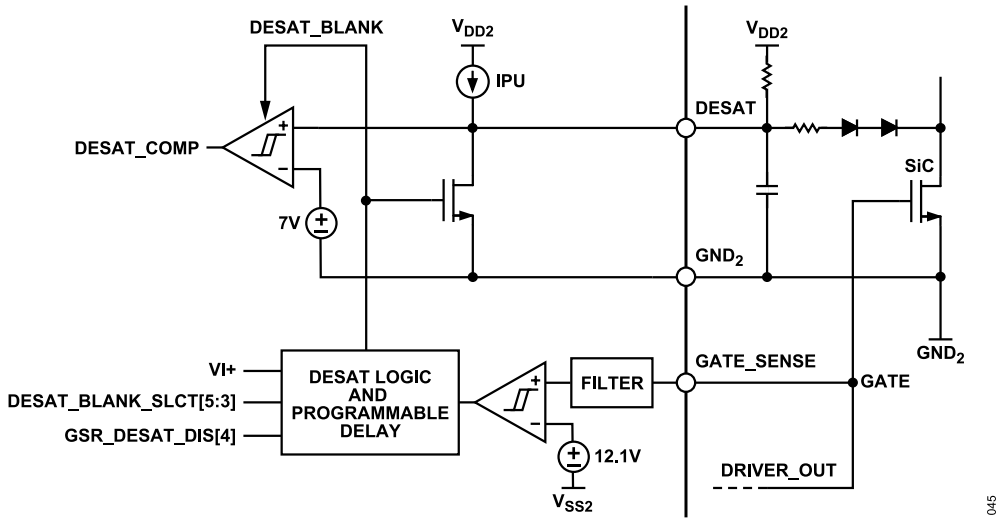

Figure 45. Typical DESAT Configuration

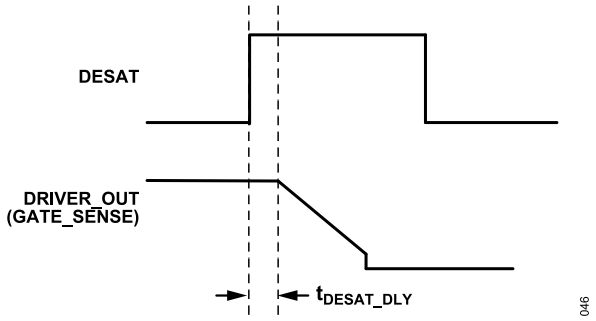

Figure 46. DESAT to Soft Shutdown Delay

APPLICATIONS INFORMATION

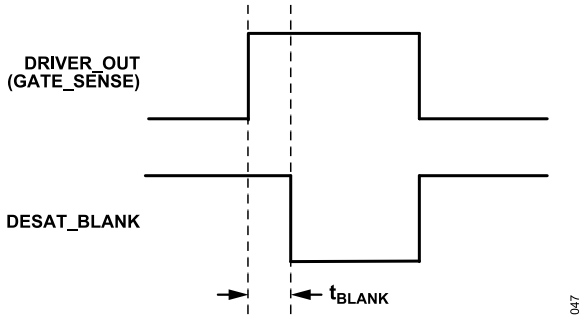

Figure 47. Example DESAT Blanking Time

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Nonoverlap Protection

The ADuM4177 has both noninverting, VI+, and inverting, VI−, input pins to control the driver output. The VI+ and VI− pins can be used to protect the driver path for overlapping signals as shown in Figure 48. If the nonoverlap timing between VI+ and VI− externally controlled dead time, t_{DEXT}, is shorter than the internal dead time, t_{DT} typically 0.5 µs, a DT_Fault is issued to the DRIVER_$\overline{FAULT}$ pin with latch time (t_{PW_DT}) of 13 ms (typical).

A functional diagram for the DT_Fault behavior is shown in Figure 51. In addition to monitoring the state of VI+ with respect to VI−, when a DT_Fault is active and both VI+ and VI− are set low, the fault clears after a 26 ms (typical) timeout.

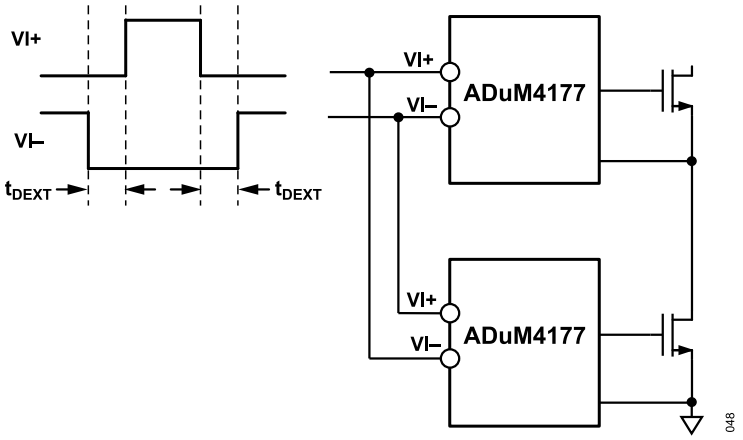

Figure 48. Nonoverlap Protection

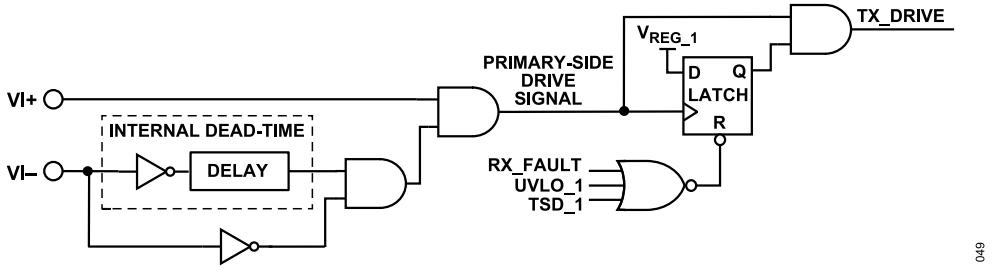

Figure 49. Functional Equivalent Diagram for Dead Time Control

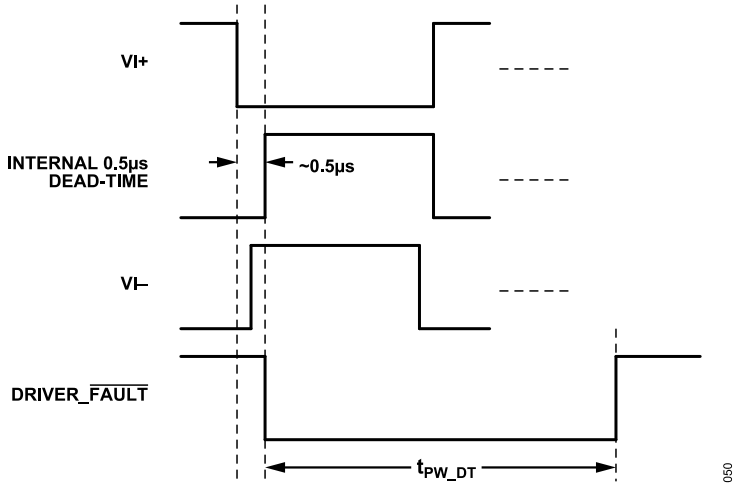

Figure 50. DT_Fault Timing Diagram

APPLICATIONS INFORMATION

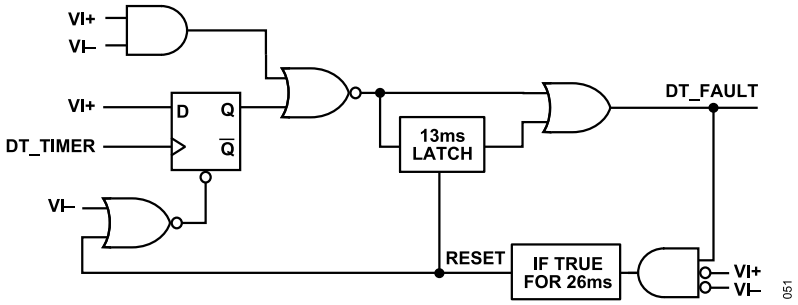

Figure 51. Dead Time Latch

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GATE_SENSE, Soft Shutdown, and Miller Clamping

The ADuM4177 has an integrated soft shutdown switch with 0.38 Ω (typical) R_{DSON}. This allows the soft shutdown time to be adjusted with an external resistor. Figure 52 shows a functional diagram for the GATE_SENSE, soft shutdown, and miller drive pins. With an external resistor, and low R_{DSON} integrated soft shutdown switch, the turn-off time for SiC switch can be adjusted to meet a 1 µs (typical) shutdown time needed for most SiC devices.

As shown in Figure 52, the ADuM4177 uses an external miller clamp switch. With an external miller clamp switch, the PCB layout can be optimized to minimize trace inductance, which impacts performance with high speed SiC devices. The Miller clamp drive pin uses the voltage on the GATE_SENSE pin to determine when to enable the miller clamp. When the GATE_SENSE pin falls to 2.75 V (typical), the MILLER_DRV is released, and the external miller switch is enabled. The miller clamp operates in both normal drive operation and soft shutdown.

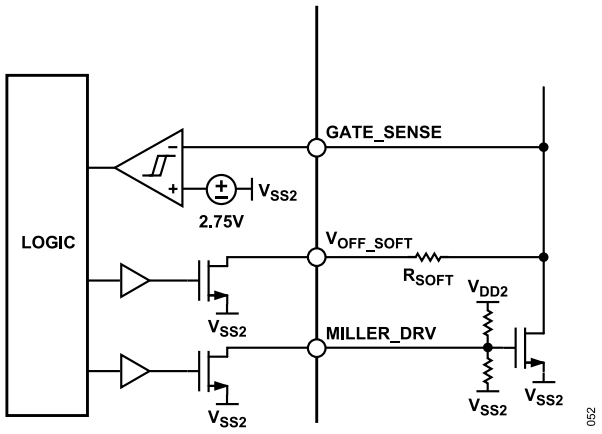

Figure 52. Soft Shutdown and Miller Drive Functions

With the gs_r and gs_f signals detecting both the rising and falling SiC gate signals, the ADuM4177 can detect short events on the SiC gate. As shown in Figure 53, with the turn-on of the driver output, if the SiC gate does not exceed 12.1 V (typical), with respect to V_{SS2}, after 3.1 µs (typical) the ADuM4177 issues a gate low fault (GL_fault). Similarly, for the turn-off of the driver output, if the SiC gate does not go below 3 V (typical), with respect to V_{SS2}, after 3.1 µs (typical) the ADuM4177 issues a gate high fault (GH_fault).

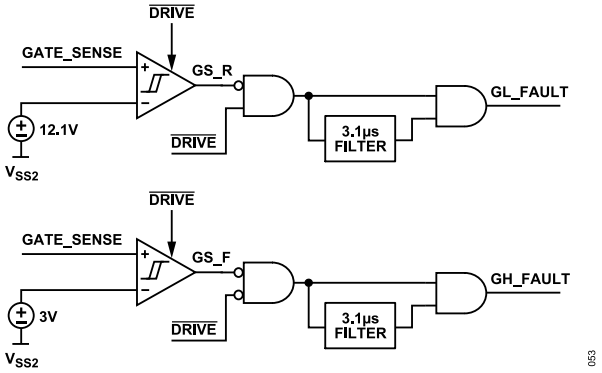

Figure 53. Gate Low and High Fault Detect

Active Short-Circuit (ASC)

The ADuM4177 is designed with an ASC pin on the secondary side. The ASC pin can be used to enable the driver output from the secondary side. The threshold of the ASC comparator is 8.1 V (typical), with an internal 150 µA (typical) pull-down current to prevent false triggering in the event of an open pin, see Figure 54.

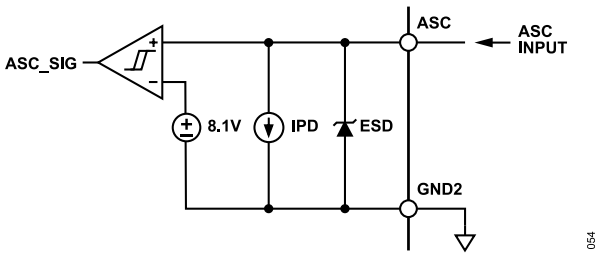

Figure 54. ASC Functional Block Diagram

Figure 55 shows a logic functional equivalent diagram of the ASC pin control of the drive signal. The asc_sig value is the signal from the ASC comparator output, the drv_signal is the drive signal from the driver receiver channel, and drive is the signal, which controls the secondary side driver stage. With no fault present, the ASC signal can freely control the driver stage. A fault generated on the secondary side overrides the ASC signal and force the driver stage to enter a soft shutdown.

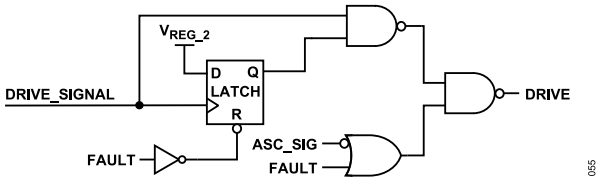

Figure 55. ASC Functional Logic

To allow the ASC to remain in control of the output in the presence of fault conditions, set register 0x53 Bit 6 (ASC_DOMIN_ENA). With ASC_DOMIN_ENA, set the ASC input that controls the V_{OUT_ON} high in the presence of most faults including DESAT. ASC does not override in case of a UVLO2 fault. When the ASC signal

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is high, the DRIVER_$\overline{\text{FAULT}}$ output is set low with any additional faults.

Figure 56 shows a timing diagram for the rising propagation delay, $t_{D\_ASC\_RISE}$, and the falling propagation delay, $t_{D\_ASC\_FALL}$. Typical ASC rising propagation delay is 105 ns (typical), while typical ASC falling propagation delay is 125 ns (typical).

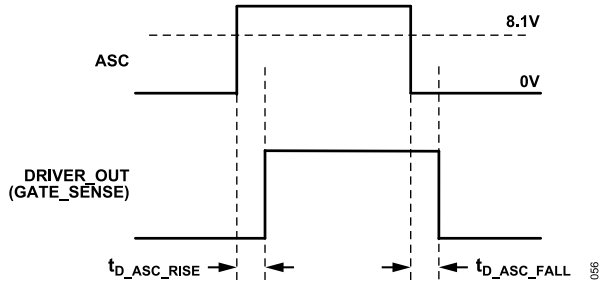

Figure 56. ASC Propagation Delays

Thermal Shutdown

The ADuM4177 contains two thermal shutdowns (TSDs). If the internal temperature of the primary or secondary side of the ADuM4177 exceeds 165°C (typical), the ADuM4177 enters a TSD fault. When the secondary side TSD occurs, the gate drive is disabled by means of a soft shutdown. The ADuM4177 does not leave TSD until the internal temperature has dropped below 145°C (typical). After reaching this temperature, the ADuM4177 exits shutdown. A fault output is available on the primary side during a TSD event on the primary and secondary side by means of the UVLO_$\overline{\text{FAULT}}$ pin.

The main cause of overtemperature is driving too large of a load for a given ambient temperature. This type of temperature overload typically affects the secondary side die because this is where the main power dissipation for load driving occurs.

FAULTS

Three fault pins on the primary side allow for fault differentiation: $\overline{\text{FAULT}}$, DRIVER_$\overline{\text{FAULT}}$, and UVLO_$\overline{\text{FAULT}}$. Figure 57 shows the functional pin equivalent diagrams for each of the fault pins. The $\overline{\text{FAULT}}$, DRIVER_$\overline{\text{FAULT}}$, and UVLO_$\overline{\text{FAULT}}$ pins have internal active pull-down NMOS devices internal to the ADuM4177 and have integrated 100 µA (typical) pull-up currents.

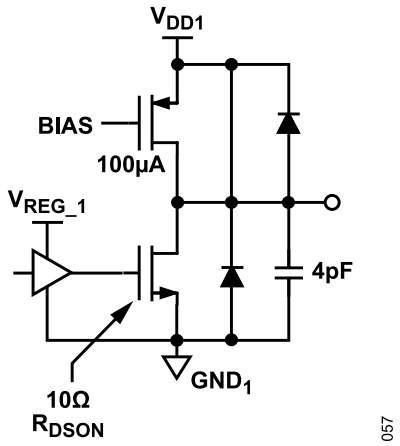

Figure 57. Fault Pin Equivalent Diagrams, $\overline{\text{FAULT}}$, DRIVER_$\overline{\text{FAULT}}$, and UVLO_$\overline{\text{FAULT}}$

Table 14 shows the details on how the faults map to the primary side fault pins. Figure 58 shows a functional diagram for the fault mapping for both the primary and secondary side of the ADuM4177. Note that the primary side TSD map to the UVLO_$\overline{\text{FAULT}}$ pin. The V_{DD1} UVLO map to both the $\overline{\text{FAULT}}$ and the UVLO_$\overline{\text{FAULT}}$ pins. There are no latch times associated with V_{DD1} UVLO and primary side TSD. Both of these faults deassert the $\overline{\text{FAULT}}$ and UVLO_$\overline{\text{FAULT}}$ pins for as long as the fault persists. As shown in Table 14 and Figure 58, the ASC pin maps to the DRIVER_$\overline{\text{FAULT}}$. There is no latch time associated with the ASC pin fault flag. The ASC pin deasserts the DRIVER_$\overline{\text{FAULT}}$ pin for as long as the ASC event persists.

Table 14. Fault Pin Mapping

Fault	$\overline{\text{FAULT}}$[1]	DRIVER_$\overline{\text{FAULT}}$[1]	UVLO_$\overline{\text{FAULT}}$[1]
Primary Side TSD	N/A	N/A	Persist
Secondary Side TSD	N/A	N/A	10 ms
VDD1 UVLO	Persist	N/A	Persist
DESAT	20 ms	30 ms	N/A
Gate error	20 ms	30 ms	10 ms
VDD2/VSS2 UVLO	20 ms	N/A	10 ms
VDD2/VSS2 OVP	20 ms	N/A	N/A
CRC error	N/A	Persist	N/A
ECC error	N/A	Persist	Persist
ASC	N/A	Persist	N/A
DT_Fault	N/A	13 ms	N/A

[1] N/A = not applicable.

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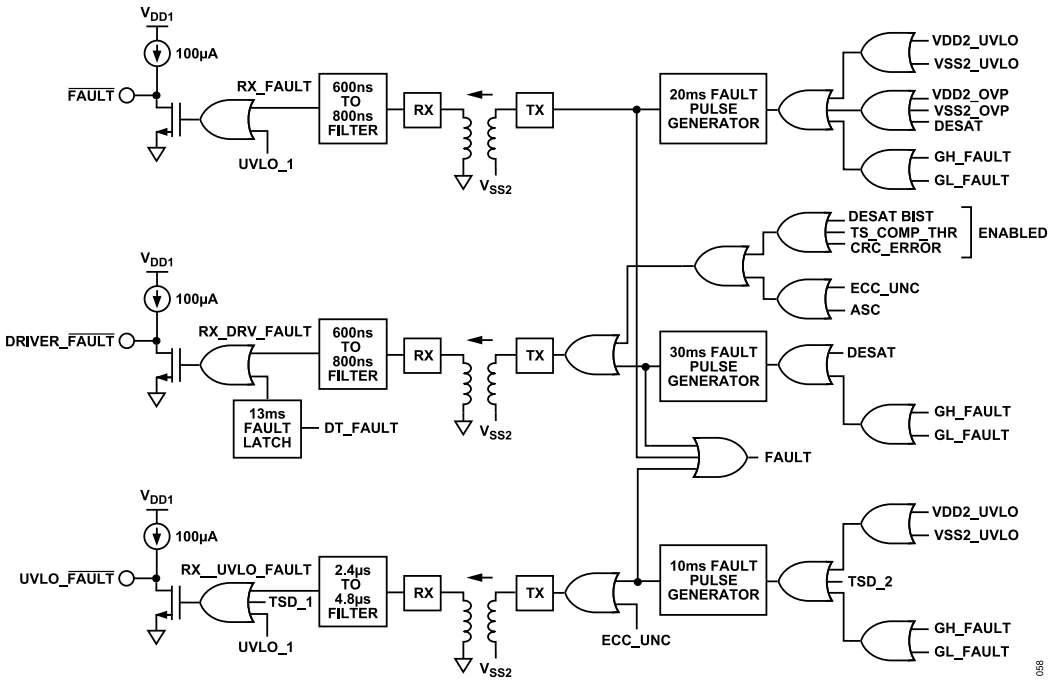

Figure 58. Fault Behavior Functional Diagram

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Fault Latch Times

Each fault pin flag has an associated latch time (t_{PW_X}) as shown in Table 15.

Table 15. Fault Latch Times

Fault Pin	Latch Time
$\overline{\text{FAULT}}$	20 ms (typical)
UVLO_$\overline{\text{FAULT}}$	10 ms (typical)
DRIVER_$\overline{\text{FAULT}}$	30 ms (typical)

If a fault occurs, the respective fault pin latches for the associated latch time. If the fault occurs for less time than t_{PW_X}, then the fault holds for only the time t_{PW_X}, see Figure 59. If a fault occurs, and it lasts longer than t_{PW_X}, then the fault holds for as long as the fault persists as shown in Figure 60.

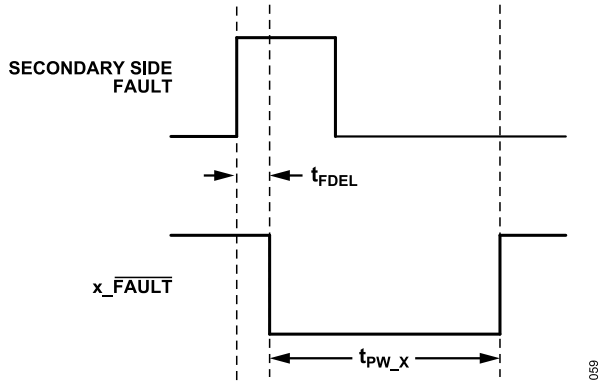

Figure 59. Fault Timing Diagram If Fault Time < t_{PW_X}

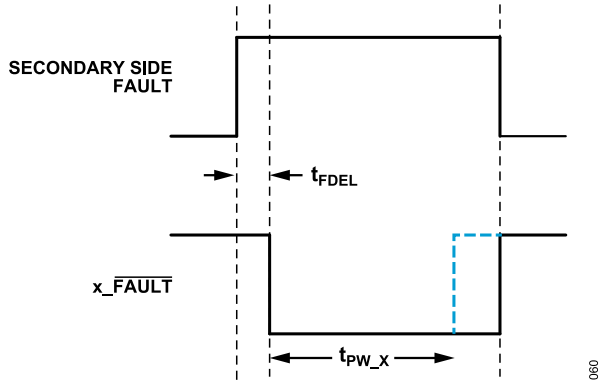

Figure 60. Fault Timing Diagram If Fault Time > t_{PW_X}

As shown in Table 14 and Figure 58, the DT_Fault maps to the DRIVER_$\overline{\text{FAULT}}$ pin. A DT_Fault can be distinguished between other DRIVER_$\overline{\text{FAULT}}$ fault events by the latch time. The DT_Fault latch time is 13 ms (typical), vs. the normal 30 ms (typical) DRIVER_$\overline{\text{FAULT}}$ latch time.

The posting time for a fault, t_{FDEL}, is the time from the fault event to the falling edge of the fault pin. This time is shown in Table 16 for each fault signal.

Table 16. Fault Reporting Times

Fault Pin	Symbol	Reporting Time Delay
$\overline{\text{FAULT}}$	t_{FDEL_FAULT}	800 ns (typical)
UVLO_$\overline{\text{FAULT}}$	$t_{FDEL\_UVLO\_FAULT}$	2 µs (typical)
DRIVER_$\overline{\text{FAULT}}$	$t_{FDEL\_DRV\_FAULT}$	800 ns (typical)

The $\overline{\text{FAULT}}$ and DRIVER_$\overline{\text{FAULT}}$ delays are discrete filters based on a 200 ns (typical) clock from a fault signal directly driven from the secondary side. The UVLO_$\overline{\text{FAULT}}$ delay is based on a pulse train that is used as a heart beat for the secondary side. A secondary side fault forces the pulse train off, indicating a fault on the primary side. In the event of power loss on the secondary side, the primary side is always guaranteed to show a fault at least on the UVLO_$\overline{\text{FAULT}}$ and $\overline{\text{FAULT}}$, provided power is present on V_{DD1}.

Configurable Faults

The ADuM4177 has two configurable faults: CRC_error and TS comparator threshold. The default state is that both CRC_error and TS comparator threshold faults do not map to any fault pin. Each fault can be configured individually. Register 0x53 is used to enable the TS pin threshold and this is done with Bit[2:1]. If either TS comparator threshold is enabled, the fault is enabled and mapped to the DRIVER_$\overline{\text{FAULT}}$ pin. Register 0x54 is used to enable the CRC_error fault and this is done with Bit 6. If enabled, the CRC_error map to the DRIVER_$\overline{\text{FAULT}}$ pin.

The CRC_error and the TS pin comparator threshold do not affect the driver state. The occurrence of either event only posts a flag on the primary side DRIVER_$\overline{\text{FAULT}}$ pin. In addition, the CRC_error and the TS pin comparator threshold are not latched. The DRIVER_$\overline{\text{FAULT}}$ low state only persists for as long as the CRC_error event, or the TS pin comparator event occurs. Figure 58 shows the functional block diagram for the configurable fault signals.

Fault Register Information

There are four registers, which post faults that occur during the ADuM4177 operation, addresses 0x00, 0x01, 0x40, and 0x41. The information posted to any of these four fault registers do not directly affect operation. If a fault occurs, and posts to a specific fault register, the register does not have to be cleared to affect operation. Using the SPI, the faults can be monitored digitally, and used for debug purposes in addition to the fault flag pins on the primary side.

The default value for a fault bit is 0. If a fault occurs, a 1 is written to the specific bit and register. To clear the information, write a 1 to the fault register and bit location. A flowchart of the fault clearing process is shown in Figure 61.

The fault registers are volatile. If power is lost on either V_{DD1} or V_{DD2}–V_{SS2}, the information stored on the respective register locations is lost.

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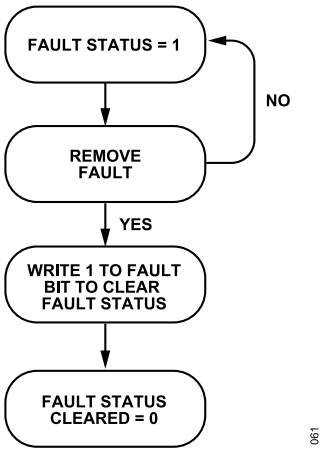

Figure 61. Status Register Flowchart

BUILT-IN SELF TEST (BIST)

The ADuM4177 has various BIST features.

For the SPI, the CRC is built-in to the overall protocol. This allows the user to ensure that the data is correct during both an SPI read and write. In addition, the ADuM4177 has a communication fault feature. If an incorrect number of bits is sent to the ADuM4177, this indicates an SPI problem. This is particularly important as it also captures errors during the transfer of data across the die-to-die interface between the primary and secondary dice within the ADuM4177.

The EEPROM on the ADuM4177 has two BIST features: ECC and a Program Fault. The ECC corrects any single bit error in any of the EEPROM registers. Any corrected or uncorrected, bit fault is notified to the user. The ECC is dynamic and active not only at startup, but during normal operation. Also built-in to the ADuM4177 EEPROM is a program fault feature. This indicates an error during any EEPROM program attempt. During programming, the ADuM4177 takes additional measures to ensure proper operation. To write to a register, the simulate bits must be set to 1, but to program an EEPROM register, both simulate bits must be set to 1 as well as the program bit. This helps prevent false programming to the EEPROM.

During startup, the ADuM4177 runs a read/write check on the following registers:

- 0x00 IC1 Analog Status
- 0x40 IC3 Analog Status

The ADuM4177 ensures that each bit can be written to and cleared. If this fails, a BIST Failed fault is written to the digital status register on both IC1 or IC3.

The DESAT circuitry includes BIST. Before the release of the UVLO_$\overline{\text{FAULT}}$ during startup, the ADuM4177 internally stimulates the DESAT comparator with high and low inputs as shown in Figure 62. The results are stored in register 0x41, Bit 2, BIST_Fault. If Register 0x53 Bit 5, DESAT_BISTOBS_ENA is set to 1, the DESAT comparator output the result of the internal comparator excitations, as long as VDD1 has been above 4 V for longer than 50 µs before VDD2 is powered up, allowing the user to observe the comparator going high and low. Three pulses of 8 µs (typical) starting low, then high, then low show that the DESAT comparator is operational. The timing for outputting the comparator results to the DRIVER_$\overline{\text{FAULT}}$ pin is shown in Figure 64.

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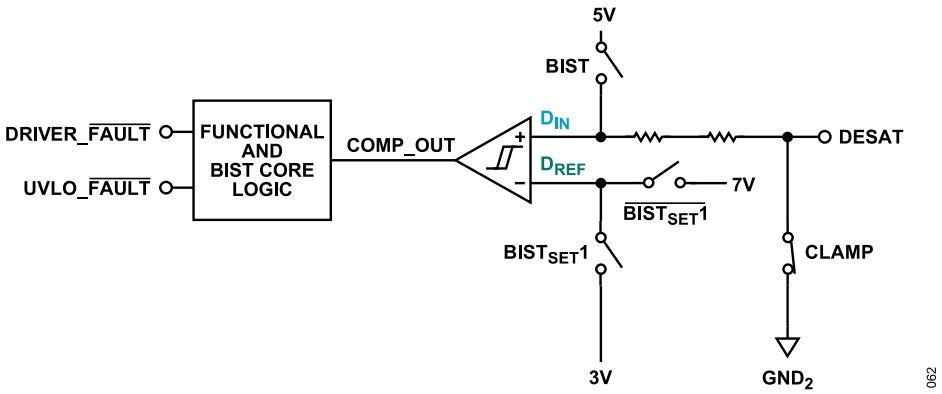

Figure 62. DESAT BIST Functional Block Diagram

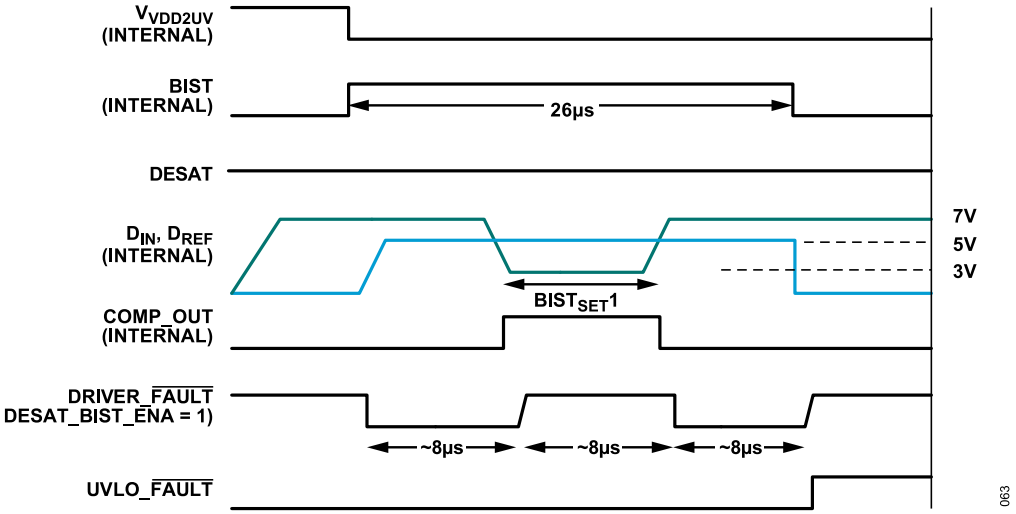

Figure 63. DESAT BIST Sequence Diagram

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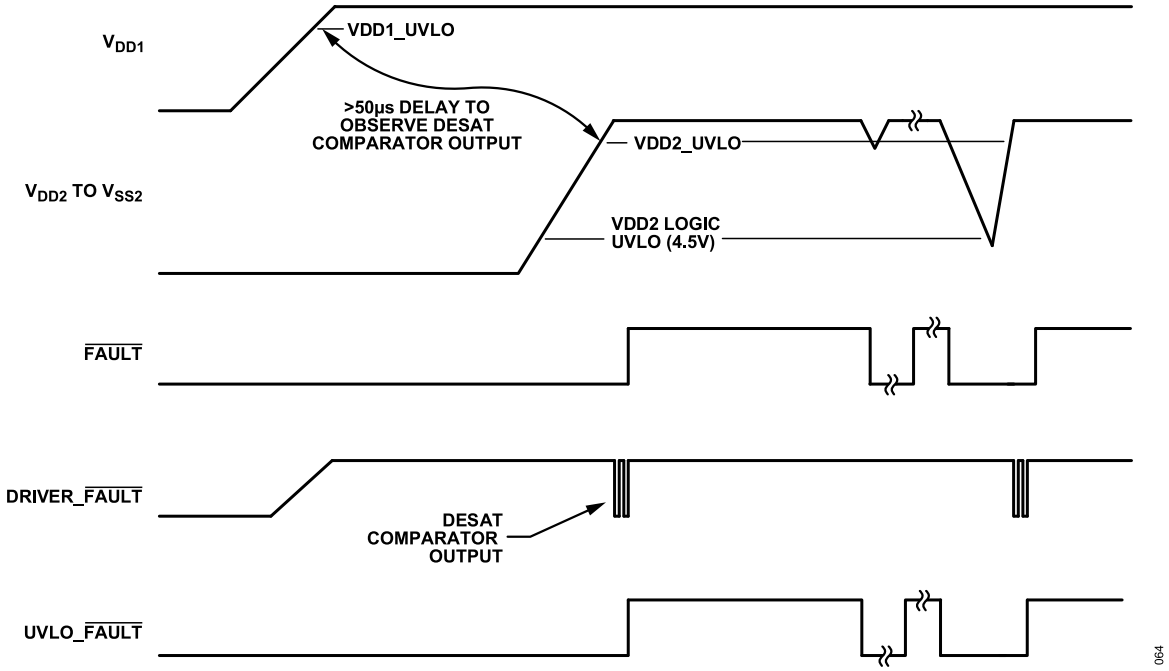

Figure 64. DESAT_BISTOBS_ENA = 1 Output Timing Example

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POWER DISSIPATION

When driving a power device gate, the driver must dissipate power. This power can lead to operation outside of specifications, and/or TSD if the following considerations are not made. Total gate charge of the device being driven dictates the loading that occurs during switching. With this value, the estimated total power dissipation (P_{DISS}) in the system due to switching action is given by the following equation:

$$P_{DISS} = Q_{TOT} \times (V_{DD2} - V_{SS2}) \times f_{SW} \quad (5)$$

where:

Q_{TOT} is the total gate charge of the power device.

$V_{DD2} - V_{SS2}$ is the voltage on the V_{DD2} with respect to V_{SS2}.

f_{SW} is the switching frequency of power device.

This power dissipation is shared between the internal on resistances of the internal gate driver switches, R_{DSON_ON} and R_{DSON_OFF}, and the external gate resistances R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4177 chip.

$$P_{DISS\_ADuM4177} = P_{DISS} \times 0.5(R_{DSON\_ON} \div (R_{GON} + R_{DSON\_ON})) + (R_{DSON\_OFF} \div (R_{GOFF} + R_{DSON\_OFF})) + P_{QUIESCENT} \quad (6)$$

where:

$P_{DISS\_ADuM4177}$ is the power dissipation of the ADuM4177.

R_{GON} is the external series resistance in the on path.

R_{GOFF} is the external series resistance in the off path.

$P_{QUIESCENT}$ is the quiescent power.

Take the power dissipation found inside the chip due to switching, adding the quiescent power losses, and multiplying it by the θ_{JA} gives the rise above ambient temperature that the ADuM4177 experiences.

$$T_{ADuM4177} = \theta_{JA} \times P_{DISS\_ADuM4177} + T_{AMB} \quad (7)$$

where:

$T_{ADuM4177}$ is the junction temperature of the ADuM4177.

T_{AMB} is the ambient temperature.

For the ADuM4177 to remain within specification, $T_{ADuM4177}$ cannot exceed 150°C (typical). When $T_{ADuM4177}$ exceeds 165°C (typical), the ADuM4177 enters TSD.

TYPICAL APPLICATION CIRCUIT

Figure 65 shows a typical application schematic of the ADuM4177.
Variations on this schematic are possible.

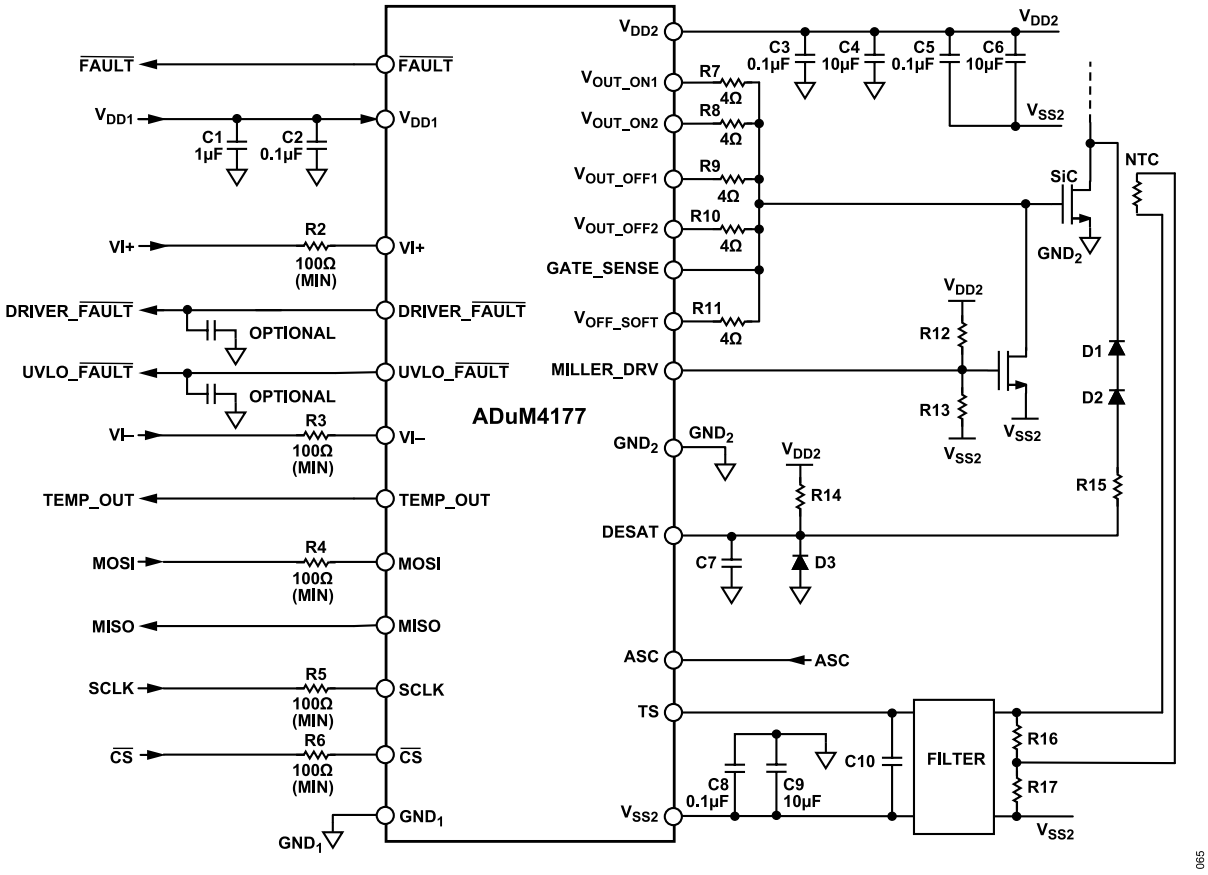

Figure 65. Typical Application Schematic

SPI REGISTERS

Table 17. ADuM4177 Register List

Address	R/W	Name	Default Setting, Bits[14:0][1]
0x00	R	IC1_ANALOG_STATUS	000 0000 0000 0000
0x01	R/W	IC1_DIGITAL_STATUS	000 0000 0000 0000
0x08	R	PWM1_DUTY	N/A
0x09	R	PWM2_DUTY	N/A
0x3F	R	IC1_CHIP_ID	000 0000 0000 0100
0x40	R	IC3_ANALOG_STATUS	000 0000 0000 0000
0x41	R/W	IC3_DIGITAL_STATUS	000 0000 0000 0000
0x42	R/W	CONTROL	000 0000 0000 0000
0x50	R/W	GAIN1	000 0000 0000 0000
0x51	R/W	OFFSET1	000 0000 0000 0000
0x52	R/W	USER_OP_MODE	000 0000 0000 0000
0x53	R/W	USER_CFG1	000 0000 0100 0000
0x54	R/W	USER_CFG2	000 0000 0000 1101
0x55	R/W	USER_CFG3	000 0000 0000 0000
0x7F	R	IC3_CHIP_ID	000 0000 0000 0101

[1] N/A = not applicable.

Address: 0x00, Reset: 0x0000, Name: IC1_ANALOG_STATUS

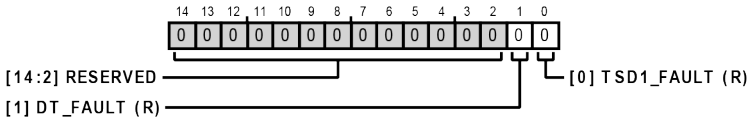

Table 18. Bit Descriptions for IC1_ANALOG_STATUS

Bits	Bit Name	Description	Reset	Access
[14:2]	RESERVED	Reserved.	0x0	R
1	DT_FAULT	Dead Time Fault.	0x0	R
0	TSD1_FAULT	IC1 Thermal Shutdown Fault.	0x0	R

Address: 0x01, Reset: 0x0000, Name: IC1_DIGITAL_STATUS

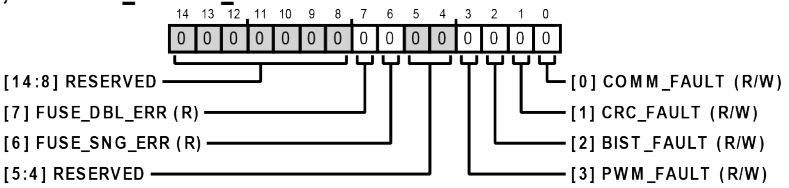

Table 19. Bit Descriptions for IC1_DIGITAL_STATUS

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	FUSE_DBL_ERR	Uncorrected Double Error in IC1 Factory Fuse Trim.	0x0	R
6	FUSE_SNG_ERR	Corrected Single Error in IC1 Factory Fuse Trim.	0x0	R
[5:4]	RESERVED	Reserved.	0x0	R
3	PWM_FAULT	Temperature Sense PWM Update Failure.	0x0	R/W
2	BIST_FAULT	IC1, Built-in Self Test Fault.	0x0	R/W
1	CRC_FAULT	CRC Error During SPI Communication.	0x0	R/W
0	COMM_FAULT	SPI Communication Failed.	0x0	R/W

SPI REGISTERS

Address: 0x08, Reset: 0x0000, Name: PWM1_DUTY

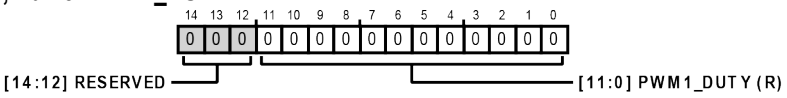

Table 20. Bit Descriptions for PWM1_DUTY

Bits	Bit Name	Description	Reset	Access
[14:12]	RESERVED	Reserved.	0x0	R
[11:0]	PWM1_DUTY	PWM1 Duty Cycle. External Temperature Measurement.	0x0	R

Address: 0x09, Reset: 0x0000, Name: PWM2_DUTY

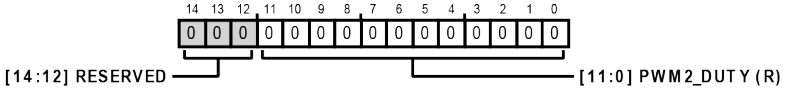

Table 21. Bit Descriptions for PWM2_DUTY

Bits	Bit Name	Description	Reset	Access
[14:12]	RESERVED	Reserved.	0x0	R
[11:0]	PWM2_DUTY	PWM Duty Cycle. Internal temperature measurement.	0x0	R

Address: 0x3F, Reset: 0x0004, Name: IC1_CHIP_ID

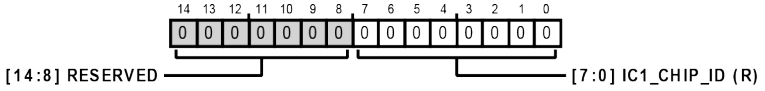

Table 22. Bit Descriptions for IC1_CHIP_ID

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	IC1_CHIP_ID	IC1 Revision Number.	0x04	R

Address: 0x40, Reset: 0x0000, Name: IC3_ANALOG_STATUS

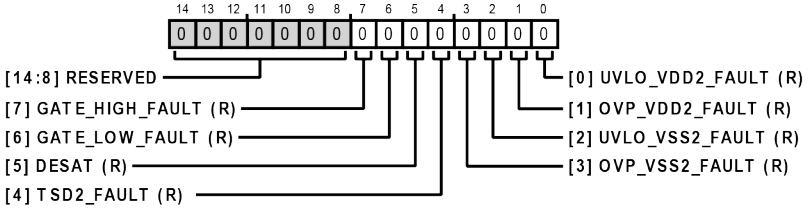

Table 23. Bit Descriptions for IC3_ANALOG_STATUS

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	GATE_HIGH_FAULT	Gate High, Expected Low.	0x0	R
6	GATE_LOW_FAULT	Gate Low, Expect High.	0x0	R
5	DESAT	DESAT Fault.	0x0	R
4	TSD2_FAULT	IC3 Thermal Shutdown Fault.	0x0	R
3	OVP_VSS2_FAULT	GND_2 to V_{SS2} Overvoltage Fault.	0x0	R
2	UVLO_VSS2_FAULT	GND_2 to V_{SS2} Undervoltage Fault.	0x0	R
1	OVP_VDD2_FAULT	V_{DD2} to V_{SS2} Overvoltage Fault.	0x0	R
0	UVLO_VDD2_FAULT	V_{DD2} to V_{SS2} Undervoltage Fault.	0x0	R

SPI REGISTERS

Address: 0x41, Reset: 0x0000, Name: IC3_DIGITAL_STATUS

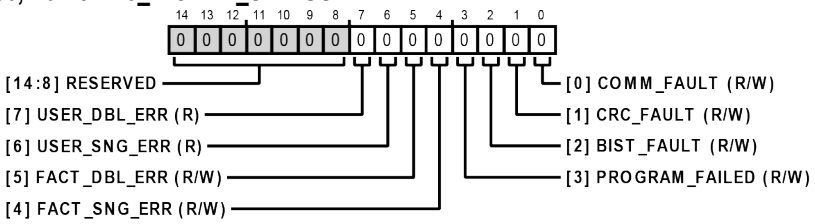

Table 24. Bit Descriptions for IC3_DIGITAL_STATUS

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	USER_DBL_ERR	User Register Uncorrectable ECC Error.	0x0	R
6	USER_SNG_ERR	User Register Single Corrected ECC Error.	0x0	R
5	FACT_DBL_ERR	Uncorrectable Factory ECC Error.	0x0	R/W
4	FACT_SNG_ERR	Single Corrected Factory ECC Error.	0x0	R/W
3	PROGRAM_FAILED	EEPROM Programming Failed.	0x0	R/W
2	BIST_FAULT	IC3, Built in Self Test Fault.	0x0	R/W
1	CRC_FAULT	CRC Error during SPI Communication.	0x0	R/W
0	COMM_FAULT	SPI Communication Failed.	0x0	R/W

Address: 0x42, Reset: 0x0000, Name: CONTROL

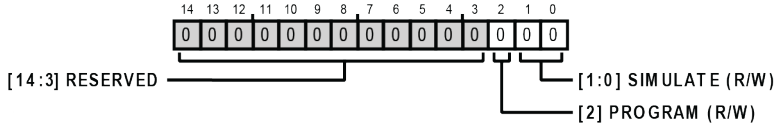

Table 25. Bit Descriptions for CONTROL

Bits	Bit Name	Description	Reset	Access
[14:3]	RESERVED	Reserved.	0x0	R
2	PROGRAM	Program EEPROM.	0x0	R/W
[1:0]	SIMULATE	Simulate EEPROM Registers.	0x0	R/W

Address: 0x50, Reset: 0x0000, Name: GAIN1

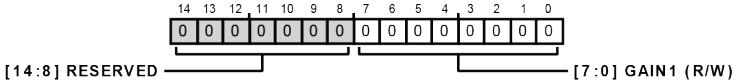

Table 26. Bit Descriptions for GAIN1

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	GAIN1	TS Gain Trim.	0x0	R/W

Address: 0x51, Reset: 0x0000, Name: OFFSET1

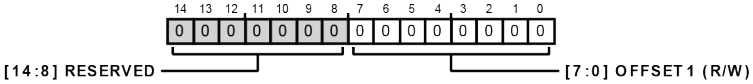

Table 27. Bit Descriptions for OFFSET1

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	OFFSET1	TS Offset Trim.	0x0	R/W

SPI REGISTERS

Address: 0x52, Reset: 0x0000, Name: USER_OP_MODE

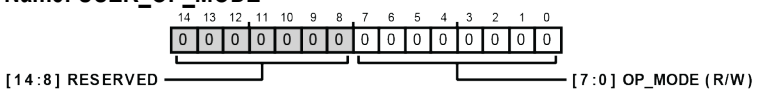

Table 28. Bit Descriptions for USER_OP_MODE

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	OP_MODE	Disable GND_2 to V_{SS2} UVLO to operate in unipolar mode.	0x0	R/W

Address: 0x53, Reset: 0x0000, Name: USER_CFG1

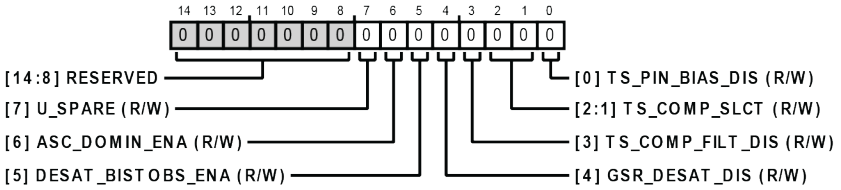

Table 29. Bit Descriptions for USER_CFG1

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	U_SPARE	Spare.	0x0	R/W
6	ASC_DOMIN_ENA	Enable ASC Dominates Over Certain Faults and DESAT.	0x0	R/W
5	DESAT_BISTOBS_ENA	Enable DESAT BIST Observability on DRIVER $\overline{FAULT}$.	0x0	R/W
4	GSR_DESAT_DIS	Disable Gate Sense Control of DESAT.	0x0	R/W
3	TS_COMP_FILT_DIS	Disable Temp Sense Filter.	0x0	R/W
[2:1]	TS_COMP_SLCT	Temp Sense Comparator Threshold Enable.	0x0	R/W
0	TS_PIN_BIAS_DIS	Disable Temp Sense 200 µA Bias Current.	0x0	R/W

Address: 0x54, Reset: 0x0000, Name: USER_CFG2

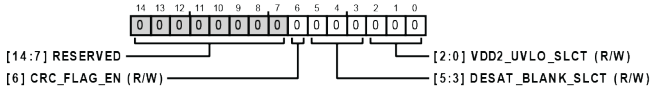

Table 30. Bit Descriptions for USER_CFG2

Bits	Bit Name	Description	Reset	Access
[14:7]	RESERVED	Reserved.	0x0	R
6	CRC_FLAG_EN	Enable CRC Fault to the DRIVER $\overline{FAULT}$ pin.	0x0	R/W
[5:3]	DESAT_BLANK_SLCT	Configure DESAT Blanking Time.	0x0	R/W
[2:0]	VDD2_UVLO_SLCT	Configure V_{DD2} − V_{SS2} Threshold.	0x0	R/W

Address: 0x55, Reset: 0x0000, Name: USER_CFG3

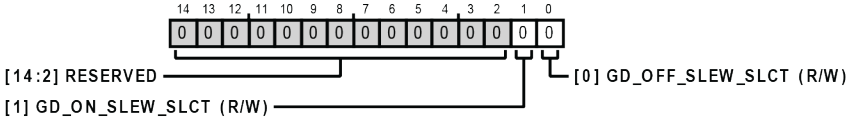

Table 31. Bit Descriptions for USER_CFG3

Bits	Bit Name	Description	Reset	Access
[14:2]	RESERVED	Reserved.	0x0	R

SPI REGISTERS

Table 31. Bit Descriptions for USER_CFG3 (Continued)

Bits	Bit Name	Description	Reset	Access
1	GD_ON_SLEW_SLCT	Enable (0) and Disable (1) the V_{OUT_ON2} FET.	0x0	R/W
0	GD_OFF_SLEW_SLCT	Enable (0) and Disable (1) the V_{OUT_OFF2} FET.	0x0	R/W

Address: 0x7F, Reset: 0x0005, Name: IC3_CHIP_ID

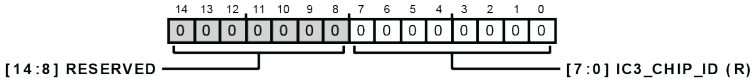

Table 32. Bit Descriptions for IC3_CHIP_ID

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	IC3_CHIP_ID	IC3 Revision Number.	0x05	R

OUTLINE DIMENSIONS

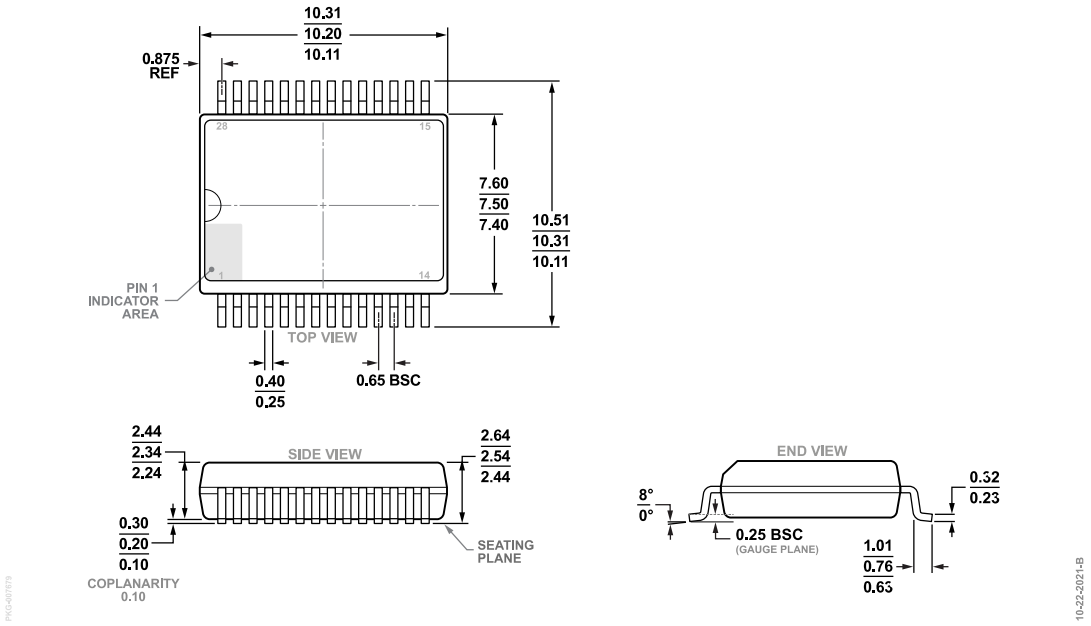

Figure 66. 28-Lead Standard Small Outline, Wide Body with Finer Pitch [SOIC_W_FP]
(RN-28-1)
Dimensions Shown in millimeters

Updated: March 29, 2023

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM4177WBRNZ	−40°C to +150°C	28-Lead SOIC (Wide, Finer Pitch)	Tube, 46	RN-28-1
ADUM4177WBRNZ-RL	−40°C to +150°C	28-Lead SOIC (Wide, Finer Pitch)	Reel, 1000	RN-28-1

[1] Z = RoHS-Compliant Part.

[2] W = Qualified for Automotive Applications.

EVALUATION BOARDS

Table 33. Evaluation Boards

Model[1]	Description
EVAL-ADuM4177EBZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

AUTOMOTIVE PRODUCTS

The ADuM4177 model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial model, therefore, designers must review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact the local Analog Devices, Inc., account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.