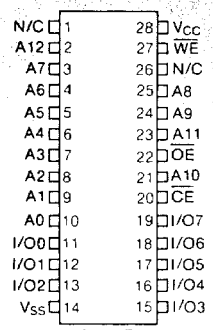
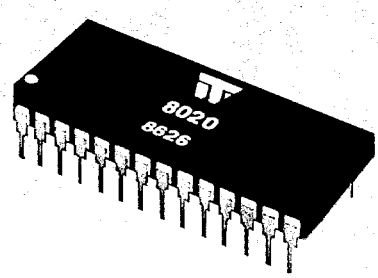
Bowmar/White Technology

8K x 8 BIT PROGRAMMABLE EEPROM 8020

PIN DIAGRAM



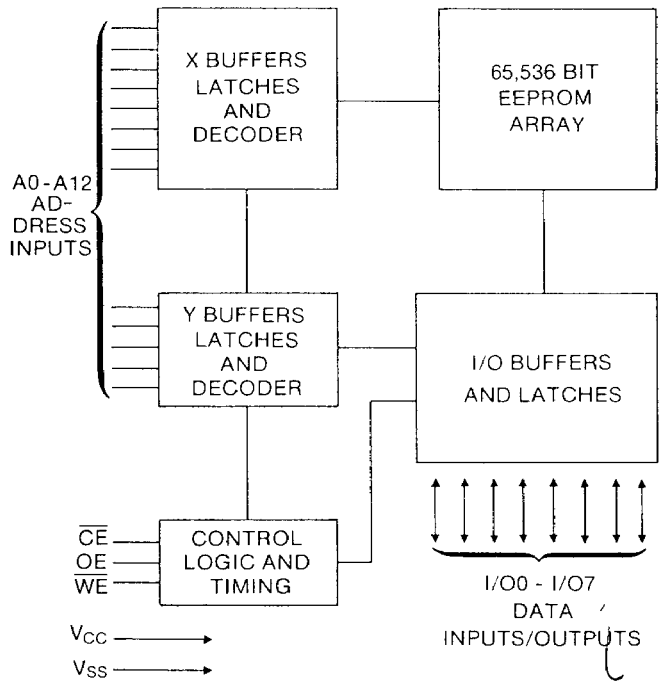
TOP VIEW



FEATURES

- Voltage: +5V and Gnd
- Operating Temperature: -55° to +200° C
- Operating Current: 10mA (Typ)
- Standby Current: 1.0mA (Typ)
- Programming Temp: -55° to +180° C
- Access Time: 250nS

BLOCK DIAGRAM



DESCRIPTION

The White Technology, Inc. 8020 is a low-power, high-performance 8K x 8 bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features, with data retention and readability to +200°C; and programmability to +180°C.

The White Technology, Inc. 8020 is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write," the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes a method for detecting the end of a write cycle, $\overline{DATA}$ polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 250nS at low power dissipation. When the chip is deselected, the standby current is less than 1.0mA.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
L	L	H	Read	Dout	Active
L	H	L	Write	Din	Active
H	X	X	Standby/Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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DEVICE OPERATION

READ The 8020 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE Writing data into the 8020 is similar to writing into a static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

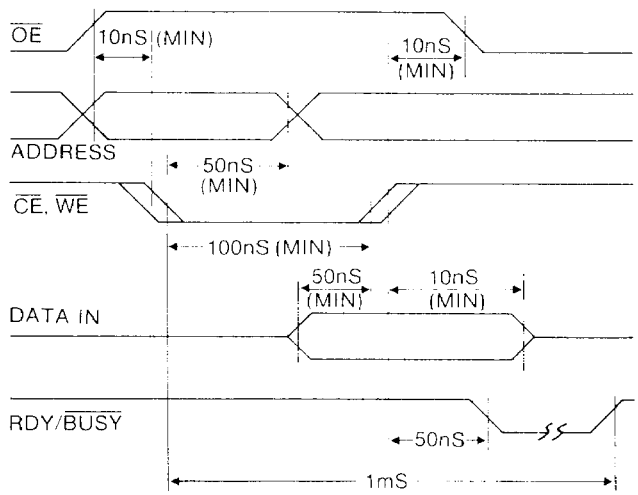
DATA POLLING The 8020 also utilizes $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the compliment of that data for I/O7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V, the write function is inhibited. (b) V_{CC} power on delay—once V_{CC} has reached 3.8V, the device will automatically time out 5mS before allowing a byte write. (c) Write Inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

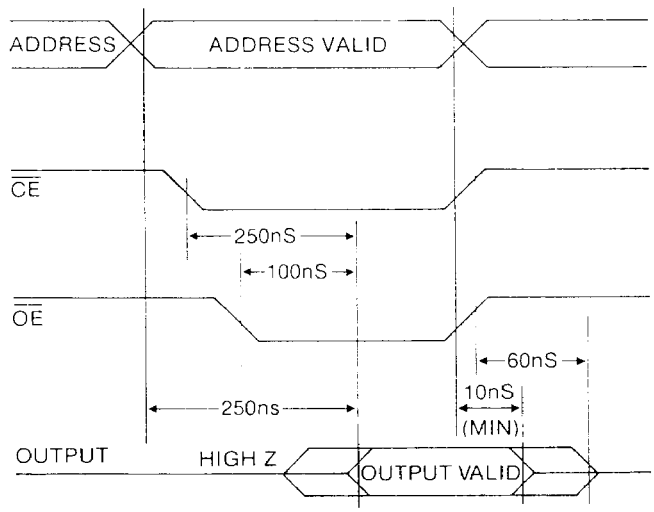
TIMING DIAGRAMS

All times are maximums unless otherwise specified.

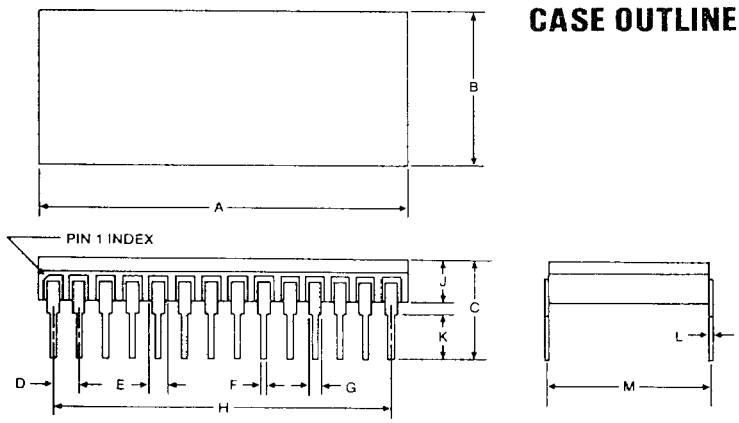
WRITE CYCLE



READ CYCLE



CASE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.250	1.550	31.8	39.4
B	0.060	0.062	1.5	1.6
C	0.375 REF.		9.5 REF.	
D	0.098	0.102	2.5	2.6
E	0.065	0.075	1.7	1.9
F	0.016	0.020	0.4	0.5
G	0.048	0.052	1.2	1.3
H	1.294	1.306	32.9	33.2
J	0.138	0.172	3.5	4.4
K	0.160	0.180	4.1	4.6
L	0.008	0.012	0.2	0.3
M	0.600 REF.		15.2 REF.	

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