74AUP1T32

Low-power 2-input OR-gate with voltage-level translator Rev. 1 — 23 November 2017 Product data sheet

1 General description

The 74AUP1T32 provides the single 2-input OR function. This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 2.3 V to 3.6 V.

The 74AUP1T32 is designed for logic-level translation applications with input switching levels that accept 1.8 V low-voltage CMOS signals, while operating from either a single 2.5 V or 3.3 V supply voltage.

The wide supply voltage range ensures normal operation as battery voltage drops from 3.6 V to 2.3 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger inputs make the circuit tolerant to slower input rise and fall times across the entire V_{CC} range.

2 Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 1.5 \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



3 Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74AUP1T32GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1					
74AUP1T32GX	-40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.35 mm	SOT1226					

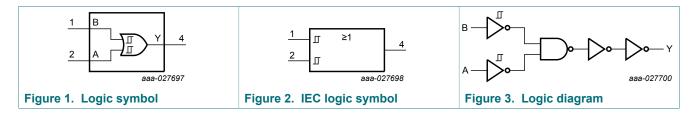
4 Marking

Table 2. Marking

Type number	Marking code ^[1]
74AUP1T32GW	5B
74AUP1T32GX	5B

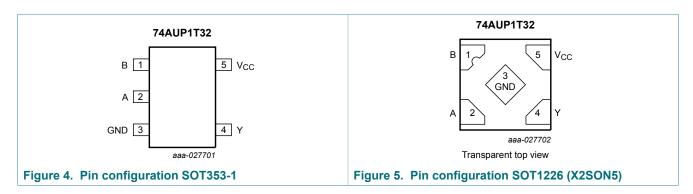
^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram



6 Pinning information

6.1 Pinning



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6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
В	1	data input
A	2	data input
GND	3	ground (0 V)
Υ	4	data output
V _{CC}	5	supply voltage

7 Functional description

Table 4. Function table [1]

Input	Output	
A	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	Н

^[1] H = HIGH voltage level;L = LOW voltage level.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
Vo	output voltage	Active mode and Power-down mode	[1]	-0.5	+4.6	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$		-	±20	mA
I _{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	250	mW

^[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed. [2] For TSSOP5 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

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^[2] For TSSOP5 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K For X2SON5 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.3	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 2	5 °C				ı	
V _{T+}	positive-going threshold	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.75	-	1.16	V
V _{T-}	negative-going threshold	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	$(V_{H} = V_{T+} - V_{T-})$				
		V _{CC} = 2.3 V to 2.7 V	0.23	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.25	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_{O} = -20 μ A; V_{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	2.05	-	-	V
		I_{O} = -3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_{O} = -2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_{O} = -4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_{O} = 20 μ A; V_{CC} = 2.3 V to 3.6 V	-	-	0.10	V
		I_{O} = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_{O} = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_{O} = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_{O} = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I _I	input leakage current	V_{I} = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.1	μA
Δl _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.1	μΑ
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	1.2	μΑ

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Low-power 2-input OR-gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Cı	input capacitance	V_{CC} = 0 V to 3.6 V; V_{I} = GND or V_{CC}	-	0.8	-	pF
Co	output capacitance	$V_O = GND; V_{CC} = 0 V$	-	1.7	-	pF
T _{amb} = -4	0 °C to +85 °C					
V _{T+}	positive-going threshold	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V_{H}	hysteresis voltage	$(V_{H} = V_{T+} - V_{T-})$				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_{O} = -20 μ A; V_{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I_{O} = -2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_{O} = -3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_{O} = -2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_{O} = -4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_{O} = 20 µA; V_{CC} = 2.3 V to 3.6 V	-	-	0.1	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I_{O} = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
II	input leakage current	V_{I} = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	μΑ
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 0 \text{ V}$ to 3.6 V; $V_{CC} = 0 \text{ V}$	-	-	±0.5	μA
ΔI_{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.5	μA
I _{CC}	supply current	$V_{I} = GND \text{ or } V_{CC}; I_{O} = 0 \text{ A}; V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	-	-	1.5	μA
ΔI_{CC}	additional supply current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V; } I_{O} = 0 \text{ A}$ [1]	-	-	0.6	μΑ
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V; } I_{O} = 0 \text{ A}$ [2]	-	-	10	μA

Low-power 2-input OR-gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = -4	10 °C to +125 °C					
V _{T+}	positive-going threshold	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold	V _{CC} = 2.3 V to 2.7 V	0.33	-	0.64	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.46	-	0.85	V
V _H	hysteresis voltage	$(V_{H} = V_{T+} - V_{T-})$				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_{O} = -20 μ A; V_{CC} = 2.3 V to 3.6 V	V _{CC} - 0.11	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	1.77	-	-	V
		I_{O} = -3.1 mA; V_{CC} = 2.3 V	1.67	-	-	V
		$I_{\rm O}$ = -2.7 mA; $V_{\rm CC}$ = 3.0 V	2.40	-	-	V
		I_{O} = -4.0 mA; V_{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_{O} = 20 μ A; V_{CC} = 2.3 V to 3.6 V	-	-	0.11	V
		I_{O} = 2.3 mA; V_{CC} = 2.3 V	-	-	0.36	V
		I_{O} = 3.1 mA; V_{CC} = 2.3 V	-	-	0.50	V
		I_{O} = 2.7 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_{O} = 4.0 mA; V_{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	V_{I} = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	μΑ
I _{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μΑ
Δl _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μΑ
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	3.5	μΑ
Δl _{CC}	additional supply current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V; } I_{O} = 0 \text{ A}$	-	-	1.8	μΑ
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V; } I_O = 0 \text{ A}$	2] _	-	18	μΑ

^[1] One input at 0.3 V or 1.1 V, other input at V_{CC} or GND. [2] One input at 0.45 V or 1.2 V, other input at V_{CC} or GND.

11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		25 °C		-40	°C to +12	25 °C	Unit	
				Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
V _{CC} = 2.3	3 V to 2.7 V; V _I	= 1.65 V to 1.95 V					<u>'</u>			
t _{pd}	propagation	A, B to Y; see Figure 6	[2]							
	delay	C _L = 5 pF		2.0	3.3	5.0	0.5	6.8	7.5	ns
		C _L = 10 pF		2.4	3.9	5.7	1.0	7.9	8.7	ns
		C _L = 15 pF		2.7	4.3	6.4	1.0	8.7	9.6	ns
		C _L = 30 pF		3.5	5.5	8.0	1.5	10.8	11.9	ns
V _{CC} = 2.3	3 V to 2.7 V; V _I	= 2.3 V to 2.7 V								
t _{pd}	propagation	A, B to Y; see Figure 6	[2]							
	delay	C _L = 5 pF		1.6	3.1	5.1	0.5	6.0	6.6	ns
		C _L = 10 pF		1.9	3.7	5.9	1.0	7.1	7.9	ns
		C _L = 15 pF		2.3	4.2	6.5	1.0	7.9	8.7	ns
		C _L = 30 pF		3.1	5.4	8.0	1.5	10.0	11.0	ns
V _{CC} = 2.3	3 V to 2.7 V; V _I	= 3.0 V to 3.6 V					l .	'		
t _{pd}	propagation delay	A, B to Y; see Figure 6	[2]							
		C _L = 5 pF		1.2	2.9	4.5	0.5	5.5	6.1	ns
		C _L = 10 pF		1.6	3.5	5.3	1.0	6.5	7.2	ns
		C _L = 15 pF		1.9	3.9	5.9	1.0	7.4	8.2	ns
		C _L = 30 pF		2.8	5.1	7.4	1.5	9.5	10.5	ns
V _{CC} = 3.0	0 V to 3.6 V; V _I	= 1.65 V to 1.95 V					I.	1		
t _{pd}	propagation	A, B to Y; see Figure 6	[2]							
	delay	C _L = 5 pF		1.8	2.7	3.7	0.5	8.0	8.8	ns
		C _L = 10 pF		2.2	3.3	4.5	1.0	8.5	9.4	ns
		C _L = 15 pF		2.6	3.7	5.0	1.0	9.1	10.1	ns
		C _L = 30 pF		3.4	4.9	6.4	1.5	9.8	10.8	ns
V _{CC} = 3.0	0 V to 3.6 V; V _I	= 2.3 V to 2.7 V	,						'	
t _{pd}	propagation	A, B to Y; see Figure 6	[2]							
	delay	C _L = 5 pF		1.5	2.6	3.9	0.5	5.3	5.9	ns
		C _L = 10 pF		1.9	3.2	4.7	1.0	6.1	6.8	ns
		C _L = 15 pF		2.2	3.7	5.3	1.0	6.8	7.5	ns
		C _L = 30 pF		2.9	4.8	6.8	1.5	8.5	9.4	ns

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Symbol	Parameter	Conditions		25 °C		-40	°C to +12	25 °C	Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
$V_{CC} = 3.0$	V to 3.6 V; V _I =	= 3.0 V to 3.6 V							'
t _{pd}	propagation	A, B to Y; see Figure 6							
	delay	C _L = 5 pF	1.1	2.6	4.0	0.5	4.7	5.2	ns
		C _L = 10 pF	1.5	3.1	4.8	1.0	5.7	6.3	ns
		C _L = 15 pF	1.8	3.6	5.4	1.0	6.2	6.9	ns
		C _L = 30 pF	2.6	4.7	7.0	1.5	7.8	8.6	ns
T _{amb} = 25	5 °C								
C _{PD}	power	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [3]							
	dissipation capacitance	V _{CC} = 2.3 V to 2.7 V	-	4	-	-	-	-	pF
Сараспапсе	V _{CC} = 3.0 V to 3.6 V	-	5	-	-	-	-	pF	

f_o = output frequency in MHz;

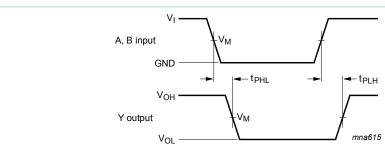
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$

^[1] All typical values are measured at nominal V_{CC} .
[2] t_{pd} is the same as t_{PLH} and t_{PHL} [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_0) \text{ where:}$ $f_i = \text{input frequency in MHz}$

11.1 Waveforms and test circuit



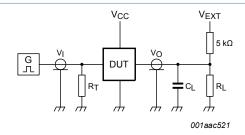
Measurement points are given in Table 9

 $\ensuremath{V_{\text{OL}}}$ and $\ensuremath{V_{\text{OH}}}$ are typical output voltage levels that occur with the output load.

Figure 6. Input A and B to output Y propagation delay times

Table 9. Measurement points

Supply voltage	Output	Input					
V _{CC}	V _M	V _M	VI	$t_r = t_f$			
2.3 V to 3.6 V	0.5 × V _{CC}	0.5 × V _I	1.65 V to 3.6 V	≤ 3.0 ns			



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C₁ = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Zo of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Figure 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V _{EXT}				
V _{CC}	C _L	R _L ^[1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t_{PZL}, t_{PLZ}		
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	2 × V _{CC}		

^[1] For measuring enable and disable times R_L = 5 k Ω .

For measuring propagation delays, setup and hold times and pulse width R_L = 1 $M\Omega$.

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12 Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm SOT353-1 = v (M) A detail X scale DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	HE	L	Lp	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

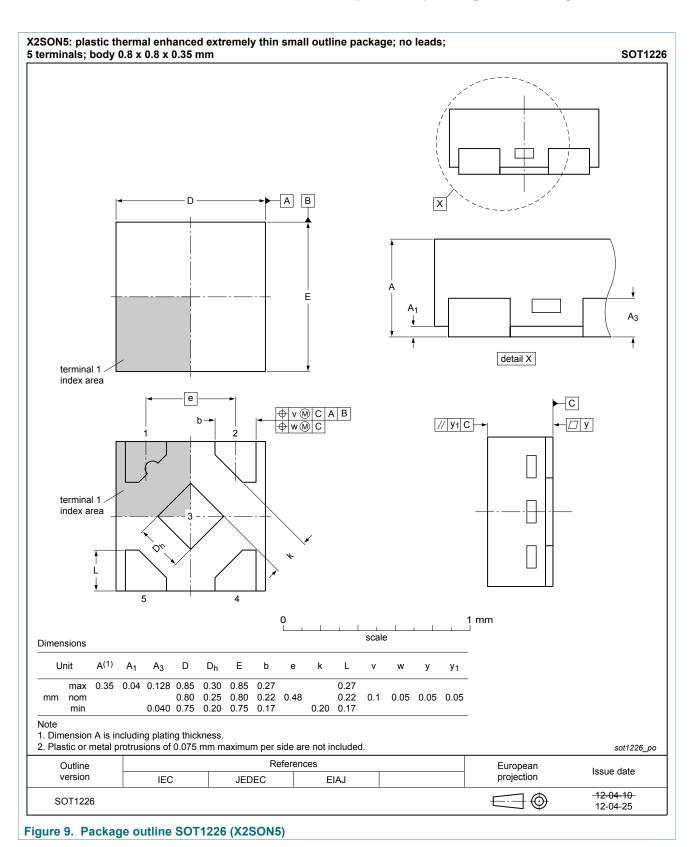
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN ISSUE DATE			
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE		
SOT353-1		MO-203	SC-88A		-00-09-01- 03-02-19		

Figure 8. Package outline SOT353-1 (TSSOP5)

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Low-power 2-input OR-gate with voltage-level translator



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Low-power 2-input OR-gate with voltage-level translator

13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T32 v.1	20171123	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- The term 'short data sheet' is explained in section "Definitions". [2] [3]
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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Low-power 2-input OR-gate with voltage-level translator

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