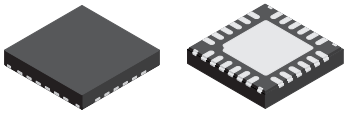
LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Wide input voltage range of 4.5 to 40 V for start/stop, cold crank, and load dump requirements
- Fully integrated LED current sinks and boost converter with internal power MOSFET
- Operate in Boost or SEPIC mode for flexible output
- Drives up to 11 series white LED in 4 parallel strings, at up to 120 mA per string (V_F = 3.3 V max).
- Programmable boost switching frequency or sync externally from 200 kHz to 2.3 MHz
- Clock-Out feature for internal switching frequency
- Adjustable boost frequency dithering to reduce EMI
- Advanced control allows minimum PWM on-time down to 0.3 µs, and avoids MLCC audible noises
- LED contrast ratio: 15,000:1 at 200 Hz using PWM dimming alone, 150,000:1 when combining PWM and analog dimming

Continued on next page...

PACKAGE:



24-Pin 4 mm × 4 mm QFN with Wettable Flank

Not to scale

DESCRIPTION

The ALT80600 is a multi-output LED driver for small-size LCD backlighting. It integrates a current-mode boost converter with internal power switch and four current sinks. The boost converter can drive up to 44 white LEDs, 11 LED per string, at 120 mA (V_F = 3.3 V max). LED sinks can be paralleled together to achieve higher currents up to 480 mA.

The ALT80600 operates from single power supply from 4.5 to 40 V; once started, it can continue to operate down to 3.9 V. This allows the part to withstand stop/start, cold crank, and load dump conditions encountered in automotive systems.

The ALT80600 can control LED brightness through external PWM signal. By using the patented 'Pre-emptive Boost' control, an LED brightness contrast ratio of 15,000:1 can be achieved using PWM dimming at 200 Hz. A higher ratio of 150,000:1 is possible when using a combination of PWM and analog dimming.

Continued on next page...

APPLICATIONS

- Automotive infotainment backlighting
- Automotive cluster
- Automotive center stack
- Automotive exterior lighting

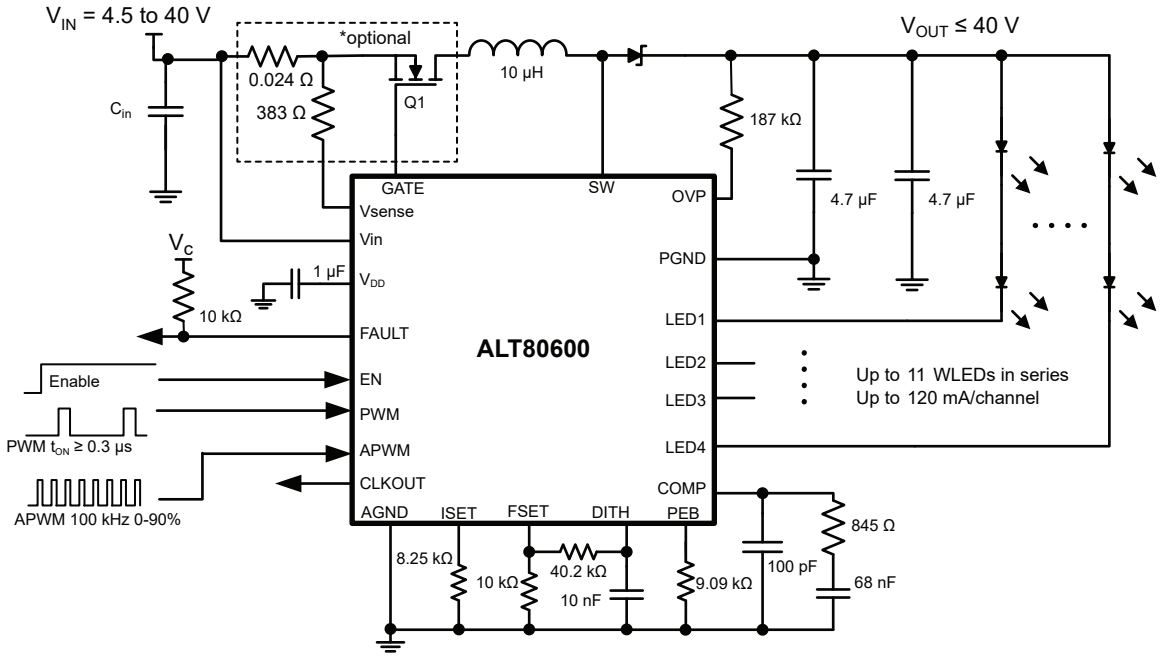


Figure 1: Typical application diagram showing ALT80600 in Boost mode

FEATURES AND BENEFITS (continued)

- Excellent input voltage transient response even at lowest PWM duty cycle
- Gate driver for optional PMOS input disconnect switch
- Extensive protection against:
  - □ Shorted boost switch, inductor or output capacitor
  - □ Shorted FSET or ISET resistor
  - □ Open or shorted LED pins and LED strings
  - □ Open boost Schottky diode
  - □ Overtemperature

DESCRIPTION (continued)

Switching frequency can be either above or below AM band. A programmable dithering feature further reduces EMI. A synchronization pin allows switching frequency to be synchronized externally between 200 kHz and 2.3 MHz. A 'Clock-Out' pin allows other converters to be synchronized to the ALT80600's switching frequency.

The ALT80600 provides protection against output short, overvoltage, open or shorted diode, open or shorted LED pin, and overtemperature. A cycle-by-cycle current limit protects the internal boost switch against high current overloads. An external P-MOSFET can optionally be used to disconnect input supply in case of output to ground short fault.

SELECTION GUIDE [1]

Part Number	Package	Packing	Leadframe Plating
ALT80600KESJSR	24-pin 4 × 4 mm wettable flank QFN with exposed thermal pad and sidewall plating	6000 pieces per reel	100% matte tin

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristi	Symbol	Notes	Rating	Unit
LEDx Pin	V_{LEDx}	x = 1..4	–0.3 to 40	V
OVP pin	V_{OVP}		–0.3 to 40	V
VIN	V_{IN}		–0.3 to 40	V
VSENSE, GATE	V_{SENSE}, V_{GATE}		Higher of –0.3 and (V_{IN} – 7.4) to V_{IN} +0.4	V
SW	V_{SW}	Continuous	–0.6 to 50	V
		t < 50 ns (repetitious, <2.5 MHz)	–1.0 to 54	V
		Single-event in case of Fault [3]	–1.5 to 60	V
FAULT	V_{FAULT}		–0.3 to 40	V
APWM, EN, PWM, CLKOUT, COMP, DITH, FSET, ISET, VDD, PEB			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[3] SW DMOS is self-protecting and will conduct when VSW exceeds 60 V.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	ES package measured on 4-layer PCB based on JEDEC standard	37	°C/W

[4] Additional thermal information available on the Allegro website.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table of Contents

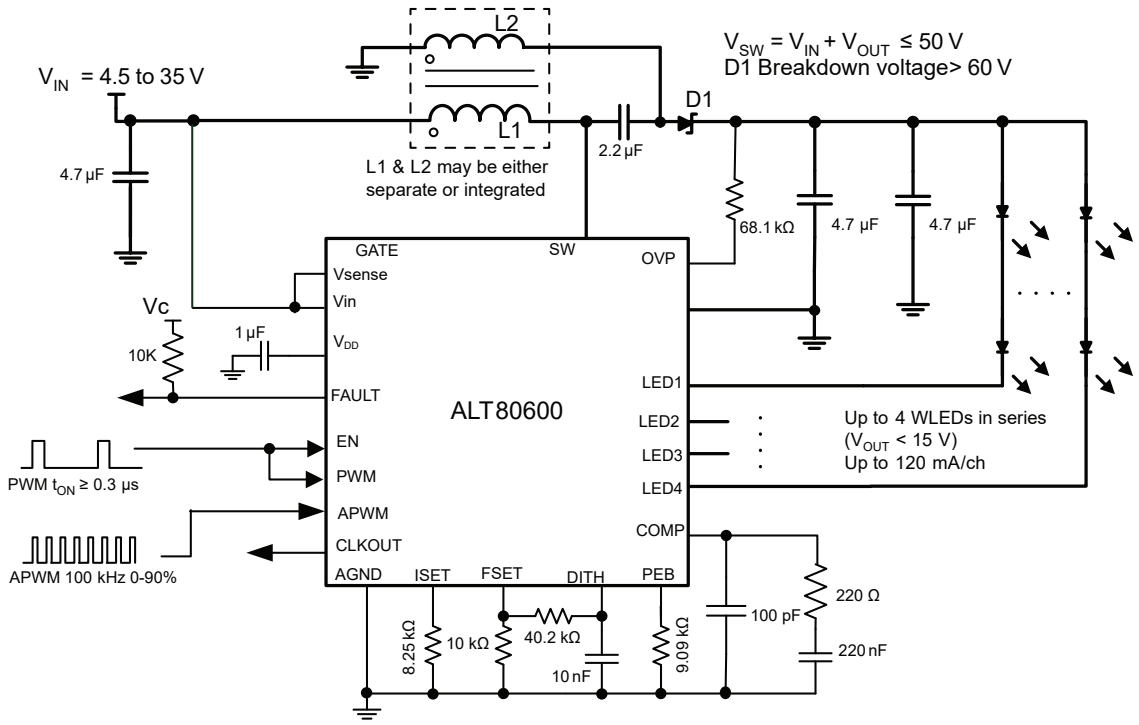


Figure 2: Typical application showing SEPIC configuration for flexible input/output voltage ratio

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

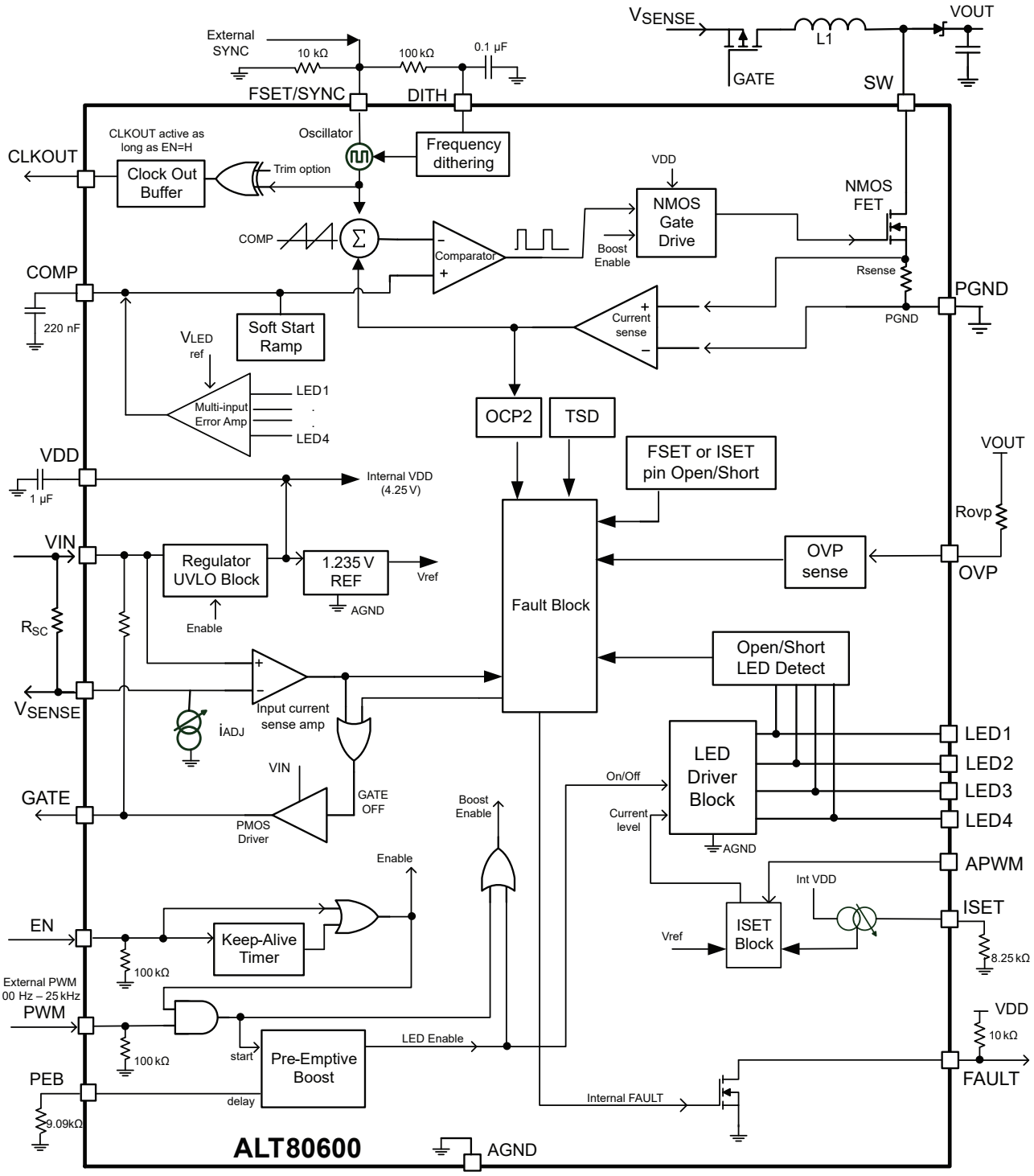
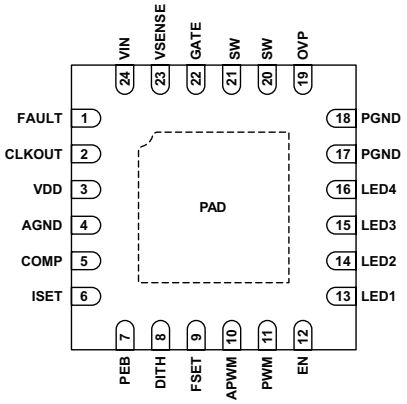


Figure 3: Functional Block Diagram

PINOUT DIAGRAM AND TERMINAL LIST



Package ES, 24-Pin QFN Pinouts

Terminal List Table

Number	Name	Function
1	FAULT	The pin is an open-drain type configuration that will be pulled low when a fault occurs. Connect a 10 kΩ resistor between this pin and desired logic level voltage.
2	CLKOUT	Logic output representing the switching frequency of internal boost oscillator. This allows other converters to be synchronized to the same f_{SW} with the same dithering modulation, if applicable. Output is active as long as EN = H.
3	VDD	Output of internal LDO (bias regulator). Connect a 1 µF decoupling capacitor between this pin and GND.
4	AGND	LED current ground. Also serves as 'quiet' ground for analog signals.
5	COMP	Output of the error amplifier and compensation node. Connect a series R_Z-C_Z network from this pin to GND for control loop compensation.
6	ISET	Connect R_{ISET} resistor between this pin and GND to set the 100% LED current.
7	PEB	Connect resistor to GND to adjust delay time (~2 to 6 µs) for Pre-Emptive Boost. Leave pin open to select shortest delay of ~1 µs.
8	DITH	Dithering control: connect a capacitor to GND to set the dithering modulation frequency (typically 1 to 3 kHz). Connect a resistor between DITH and FSET pins to set the dithering range (such as ±5% of f_{SW}).
9	FSET/SYNC	Frequency/synchronization pin. A resistor R_{FSET} from this pin to GND sets the switching frequency f_{SW} (with dithering super-imposed). It can also be used to synchronize two or more converters in the system to an external frequency between 200 kHz and 2.3 MHz (dithering is disabled in this case).
10	APWM	Analog dimming. Apply APWM clock (40 kHz to 1 MHz) to this pin, and the duty cycle of this clock determines the LED current. Leave open or connect to GND for 100%
11	PWM	Controls the on/off state of LED current sinks to reduce the light intensity by using pulse-width modulation. Typical PWM dimming frequency is in the range of 200 to 2 kHz. EN and PWM pins may be tied together to allow single-wire dimming control.
12	EN	Enables the IC when this pin is pulled high. If EN goes low, the IC remains in standby mode for up to 32k cycles, then shuts down completely.
13-16	LED1-4	LED current sinks #1 - 4. Connect the cathode of each LED string to pin. Unused LED pin must be terminated to GND through a 6.19 kΩ resistor.
17-18	PGND	Power ground for internal NMOS switching device.
19	OVP	Overvoltage protection. Connect external resistor from V_{OUT} to this pin to adjust the over voltage protection level.
20-21	SW	The drain of the internal NMOS switching device of the boost converter.
22	GATE	Output gate driver pin for external P-channel FET (optional input disconnect switch for overcurrent protection).
23	VSENSE	Connect this pin to the negative sense side of the current sense resistor R_{SC}. The threshold voltage is measured as $V_{IN} - V_{SENSE}$. There is also a fixed ~20 µA current sink to allow for trip threshold adjustment for input overcurrent protection.
24	VIN	Input power to the IC as well as the positive input used for current sense resistor.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. Must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the pad.

ELECTRICAL CHARACTERISTICS [1]: Unless otherwise noted, specifications are valid at V_{IN} = 16 V, T_J = 25°C, • indicates specifications guaranteed over the full operating temperature range with T_J = –40°C to 125°C, typical specifications are at T_J = 25°C

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS							
Operating Input Voltage Range [3]	V_{IN}		•	4.5	–	40	V
VIN UVLO Start Threshold	$V_{UVLO(rise)}$	V_{IN} rising	•	–	–	4.35	V
VIN UVLO Stop Threshold	$V_{UVLO(fall)}$	V_{IN} falling	•	–	–	3.9	V
UVLO Hysteresis [2]	V_{UVLO_HYS}			300	450	600	mV
INPUT CURRENTS							
VIN Pin Operating Current	I_{OP}	EN and PWM = H, f_{SW} = 2 MHz	•	–	13	18	mA
VIN Pin Quiescent Current	I_Q	EN = H and PWM = L, f_{CLKOUT} = 2 MHz	•	–	10	–	mA
VIN Pin Sleep Current	I_{QSLEEP}	V_{IN} = 16 V, V_{EN} = 0 V	•	–	2	10	µA
INPUT LOGIC LEVELS (EN, PWM, APWM)							
Input Logic Level-Low	V_{IL}		•	–	–	0.4	V
Input Logic Level-High	V_{IH}		•	1.5	–	–	V
Input Pull-Down Resistor	R_{EN}, R_{PWM}, R_{APWM}	Input = 5 V		60	100	140	kΩ
OUTPUT LOGIC LEVELS (CLKOUT)							
Output Logic Level-Low	V_{OL}	5 V < V_{IN} < 40 V	•	–	–	0.3	V
Output Logic Level-High	V_{OH}	5 V < V_{IN} < 40 V	•	1.8	–	–	V
CLKOUT Duty Cycle	D_{CLKOUT}	f_{SW} = 2 MHz, no external sync	•	33	50	67	%
CLKOUT Negative Pulse Width [2]	DCLKNPW	External sync = 200 kHz to 2.3 MHz		–	200	–	ns
APWM PIN							
APWM Frequency Range [2]	f_{APWM}	Clock signal applied to pin	•	40	–	1000	kHz
APWM Duty Cycle Range [2]	D_{APWM}	Clock signal applied to pin	•	0	–	90	%
VDD REGULATOR							
Regulator Output Voltage	V_{DD}	V_{IN} > 4.5 V, i_{LOAD} < 1 mA		4.05	4.25	4.45	V
VDD UVLO Start Threshold	$V_{DDUVLOrise}$	V_{DD} rising, no external load			3.2		V
VDD UVLO Stop Threshold	$V_{DDUVLOfall}$	V_{DD} falling, no external load			2.65		V
ERROR AMPLIFIER							
Amplifier Gain [2]	Gm	V_{COMP} = 1.5 V		–	1000	–	µA/V
Source Current	$I_{EA(SRC)}$	V_{COMP} = 1.5 V		–	–600	–	µA
Sink Current	$I_{EA(SINK)}$	V_{COMP} = 1.5 V		–	+600	–	µA
COMP Pin Pull Down Resistance	R_{COMP}	FAULT = 0, V_{COMP} = 1.5 V		–	1.4	–	kΩ

Continued on the next page…

ELECTRICAL CHARACTERISTICS [1] (continued): **Unless otherwise noted, specifications are valid at V_{IN} = 16 V, T_J = 25°C, • indicates specifications guaranteed over the full operating temperature range with T_J = –40°C to 125°C, typical specifications are at T_J = 25°C**

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
DITHERING CONTROL							
DITH Pin Source Current	$i_{DITH(src)}$	Output current when V_{DITH} < 0.8 V		–	20	–	µA
DITH Pin Sink Current	$i_{DITH(sink)}$	Output current when V_{DITH} > 1.2 V		–	–20	–	µA
OVERVOLTAGE PROTECTION							
OVP Pin Voltage Threshold	$V_{OVP(th)}$	OVP pin connected to V_{OUT}	•	2.25	2.5	2.75	V
OVP Pin Sense Current Threshold	$i_{OVP(th)}$	Current into OVP pin	•	143	150	157	µA
OVP Pin Leakage Current	I_{OVPLKG}	V_{OUT} = 16 V, EN = L	•	–	0.1	1	µA
OVP Variation at Output	ΔOVP	Measured at V_{OUT} when R_{OVP} = 249 kΩ		–	–	5	%
Undervoltage Detection Threshold	$V_{UVP(th)}$	Measured at V_{OUT} when R_{OVP} = 249 kΩ [2]		–	3.3	4.2	V
		Measured at V_{OUT} when R_{OVP} = 0 Ω		–	0.2	0.25	V
Secondary Overvoltage Protection	V_{OVP2}	Measured at SW pin; part latches when OVP2 is detected	•	51	55	59	V
BOOST SWITCH							
Switch On Resistance	R_{SW}	I_{SW} = 0.75 A, V_{IN} = 16 V	•	–	250	500	mΩ
Switch Pin Leakage Current	$I_{SWLKG25}$	V_{SW} = 13.5 V, PWM = VIL, T_J = 25°C		–	0.1	1	µA
	$I_{SWLKG85}$ [2]	V_{SW} = 13.5 V, PWM = VIL, T_J = 85°C		–	–	10	µA
Switch Pin Current Limit	$I_{SW(LIM)}$	IC truncates present switching cycle when primary limit is reached	•	3.0	3.65	4.5	A
Secondary Switch Current Limit [2]	$I_{SW(LIM2)}$	IC latches off when secondary limit is reached		–	4.9	–	A
Minimum Switch On-Time	$t_{SW(ON)}$		•	45	65	85	ns
Minimum Switch Off-Time	$t_{SW(OFF)}$		•	–	50	66	ns
OSCILLATOR FREQUENCY							
Oscillator Frequency	f_{SW}	R_{FSET} = 10 kΩ	•	1.95	2.15	2.35	MHz
		R_{FSET} = 110 kΩ		–	200	–	kHz
FSET Pin Voltage	V_{FSET}	R_{FSET} = 10 kΩ		–	1.00	–	V
SYNCHRONIZATION							
Sync Input Logic Level	V_{SYNCL}	FSET/SYNC pin logic Low	•	–	–	0.4	V
	V_{SYNCH}	FSET/SYNC pin logic High	•	1.5	–	–	V
Synchronized PWM Frequency	F_{SWSYNC}		•	260	–	2300	KHz
Synchronization Input Min Off-Time	$t_{PWSYNCOFF}$		•	150	–	–	ns
Synchronization Input Min On-Time	$t_{PWSYNCON}$		•	150	–	–	ns

Continued on the next page…

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS [1] (continued): Unless otherwise noted, specifications are valid at V_{IN} = 16 V, T_J = 25°C, • indicates specifications guaranteed over the full operating temperature range with T_J = –40°C to 125°C, typical specifications are at T_J = 25°C

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
LED CURRENT SINKS							
LEDx Accuracy [4]	Err_{LED}	i_{ISET} = 120 µA (R_{ISET} = 8.33 kΩ), V_{APWM} = 0 V	•	–	0.7	3	%
LEDx Matching	ΔLEDx	i_{ISET} = 120 µA, V_{APWM} = 0 V	•	–	0.8	2	%
LEDx Regulation Voltage	V_{LED}	Measured individually with all other LED pins tied to 1 V, i_{ISET} = 120 µA, V_{APWM} = 0 V	•	600	700	800	mV
I_{ISET} to I_{LEDx} Current Gain	A_{ISET}	i_{ISET} = 120 µA, V_{APWM} = 0 V	•	816	833	850	A/A
ISET Pin Voltage	V_{ISET}			0.97	1	1.03	V
Allowable ISET Current	i_{ISET}		•	20	–	144	µA
LED String Partial-Short-Detect	V_{LEDSC}	Sensed from each LED pin to GND while its current sink is in regulation; all other LED pins tied to 1 V	•	4.5	5.2	6	V
Soft-Start Ramp Up Time [2]	t_{SSRU}	Maximum time duration before all LED channels come into regulation, or OVP is tripped, whichever comes first		18	21.5	25	ms
Enable Pin Shut Down Delay [2]	$t_{EN(OFF)}$	EN goes from High to Low; exceeding $t_{EN(OFF)}$ results in IC shutdown; measured in terms of switching cycles		–	32768	–	cycles
Minimum PWM Dimming On-Time	t_{PWMH}	First and subsequent PWM pulses	•	–	0.3	0.4	µs
GATE PIN							
Gate Pin Sink current	I_{GSINK}	V_{GS} = V_{IN}, no input OCP fault		–	–113	–	µA
Gate Pin Source current	$I_{GSOURCE}$	V_{GS} = V_{IN} – 6 V, input OCP fault tripped		–	6	–	mA
Gate Shutdown Delay When Over-Current Fault Is Tripped [2]	t_{FAULTT}	V_{IN} – V_{SENSE} = 200 mV; monitored at FAULT pin		–	–	3	µs
Gate Voltage	V_{GS}	Measured between GATE and VIN when gate is fully on		–	–6.7	–	V
VSENSE PIN							
VSENSE Pin Sink Current	i_{ADJ}		•	16	20	24	µA
VSENSE Trip Point	$V_{SENSETRIP}$	Measured between V_{IN} and V_{SENSE}, R_{ADJ} = 0	•	88	100	110	mV
FAULT PIN							
FAULT Pull Down Voltage	V_{FAULT}	I_{FAULT} = 1 mA		–	–	0.5	V
FAULT Pin Leakage Current	$i_{FAULT-LKG}$	V_{FAULT} = 5 V		–	–	1	µA
THERMAL PROTECTION (TSD)							
Thermal Shutdown Threshold [2]	TSD	Temperature rising		155	170	–	°C
Thermal Shutdown Hysteresis [2]	TSD_{HYS}			–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization; not production tested.
[3] Minimum V_{IN} = 4.5 V is only required at startup. After startup is completed, IC can continue to operate down to V_{IN} = 4 V.
[4] LED current is trimmed to cancel variations in both Gain and ISET voltage.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

The ALT80600 is a multistring LED regulator with an integrated boost switch and four precision current sinks. It incorporates a patented Pre-Emptive Boost (PEB) control algorithm to achieve PWM dimming ratio over 15,000:1 at 200 Hz. PEB control also minimizes output ripple to avoid audible noise from output ceramic capacitors.

The switching frequency can be either synchronized to an external clock or generated internally. Spread-spectrum technique (with user-programmable dithering range and modulation frequency) is provided to reduce EMI. A clock-out signal (CLKOUT) allows other converters to be synchronized to the switching frequency of ALT80600.

Enabling the IC

The ALT80600 wakes up when EN pin is pulled above logic high level, provided that VIN pin voltage is over the VIN_UVLO threshold. The boost stage and LED channels are enabled separately by PWM = H signal after the IC powers up.

The IC performs a series of safety checks at power up, to determine if there are possible fault conditions that might prevent the system from functioning correctly. Power-up checks include:

- VOUT shorted to GND
- LED pin shorted to GND
- FSET pin open/shorted
- ISET pin open/shorted to GND, etc.

Only if no faults were detected, then the IC can proceed to start switching.

As long as EN = H, the PWM pin can be toggled to control the brightness of LED channels by using PWM dimming. Alternatively, EN and PWM can be tied together to allow single-wire control for both power on/off and PWM dimming. If EN is pulled low for longer than 32k clock cycles, the IC shuts off.

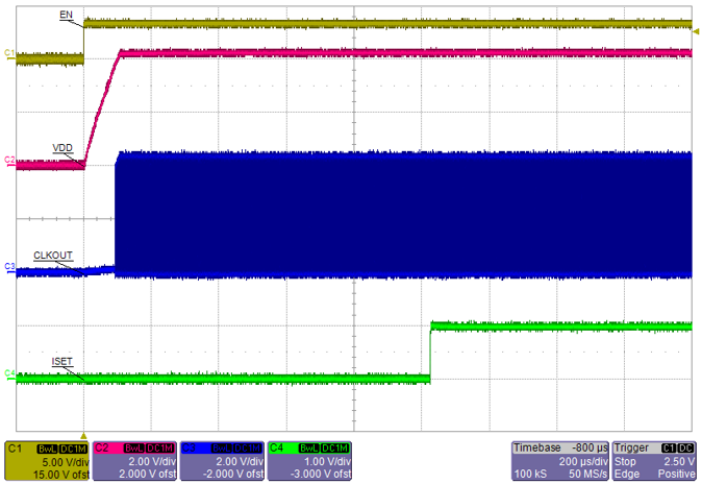


Figure 4: Startup showing EN, VDD, CLKOUT, and ISET (PWM = L). Note that CLKOUT is available as soon as V_{DD} ramps up, even though Boost stage and LED drivers are not yet enabled.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Powering Up: LED Detection Phase

The VIN pin has an undervoltage lockout (UVLO) function that prevents the ALT80600 from powering up until the UVLO threshold is reached. Once the VIN pin goes above UVLO and a high signal is present on the EN pin, the IC proceeds to power up. At this point, the ALT80600 is going to enable the disconnect switch and will try to check if any LED pins are shorted to GND and/or are not used. The LED detect phase starts when the GATE voltage of the input disconnect PMOS switch is pulled down to 3.3 V below V_{IN} and PWM = H.

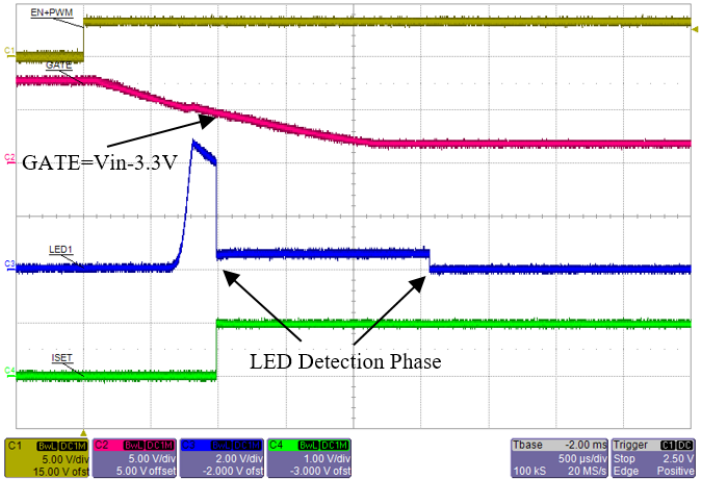


Figure 5: Startup showing EN+PWM, GATE, LED1, and ISET. Switching frequency = 2.15 MHz. Note that LED Detection Phase starts as soon as GATE pin is pulled down to 3.3 V below V_{IN}.

Once the voltage threshold on VLED pins exceeds ~120 mV, a delay of 3584 clock cycles is used to determine the status of the pins. Therefore the duration of LED Detection phase depends on the switching frequency selected:

Table 1: Duration of LED Detection phase with respect to switching frequency

Switching Frequency	Approximate Detection Time
2.15 MHz	1.67 ms
1 MHz	3.6 ms
500 kHz	7.2 ms
250 kHz	14 ms

Unused LED pin should be terminated with a 6.19 kΩ resistor to GND. At the end of LED detection phase, any channel with pull down resistor is then disabled and will not contribute to the boost regulation loop.

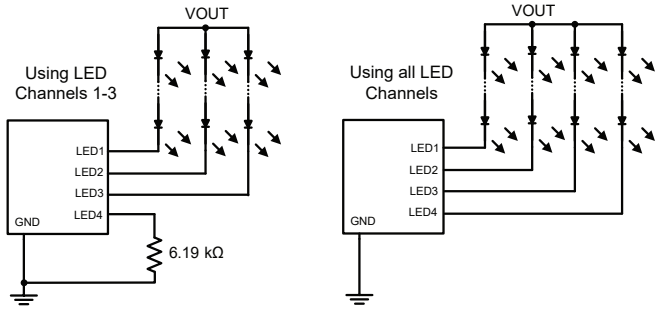


Figure 6: How to signal an unused LED channel during startup LED detection phase

Table 2: LED Detection phase voltage threshold levels

LED Pin Voltage Measured	Interpretation	Outcome
< 120 mV	LED pin shorted to GND fault	Cannot proceed with soft-start unless fault is removed
~ 230 mV	LED channel not in use	LED channel is removed from operation
> 340 mV	LED channel in use	Proceed with soft-start

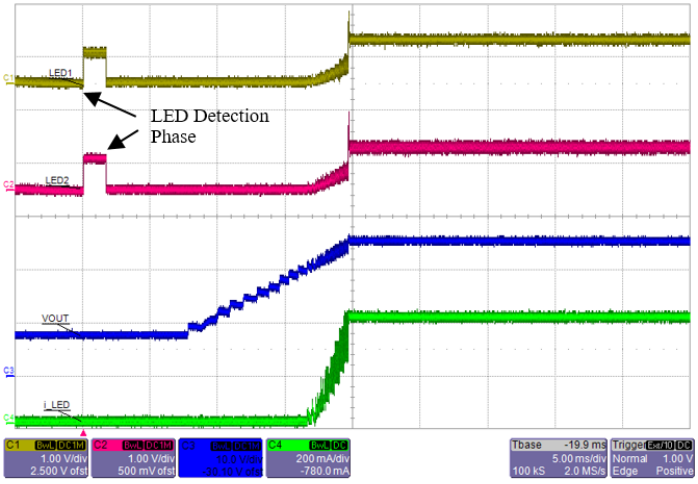


Figure 7: Normal startup showing all channels passed LED Detection phase. Total LED current = 100 mA × 4 (only LED1 and LED2 pin voltages are shown).

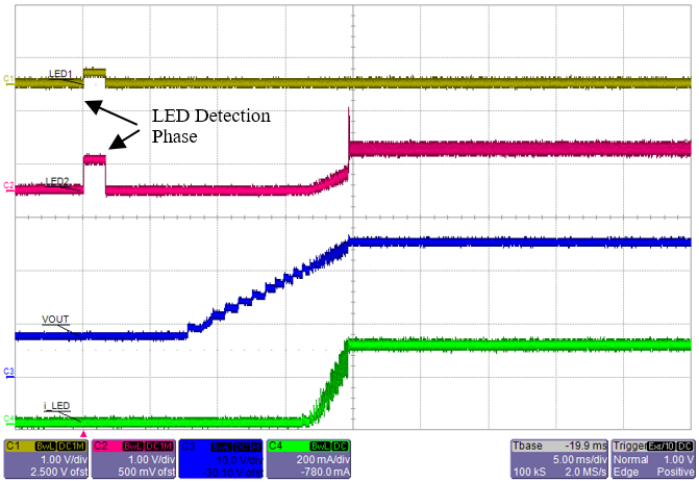


Figure 8: Normal startup showing LED1 channel is disabled. Total LED current = 100 mA × 3.

If an LED pin is shorted to ground, the ALT80600 will not proceed with soft start until the short is removed from the LED pin. This prevents the ALT80600 from ramping up the output voltage and putting an uncontrolled amount of current through the LEDs.

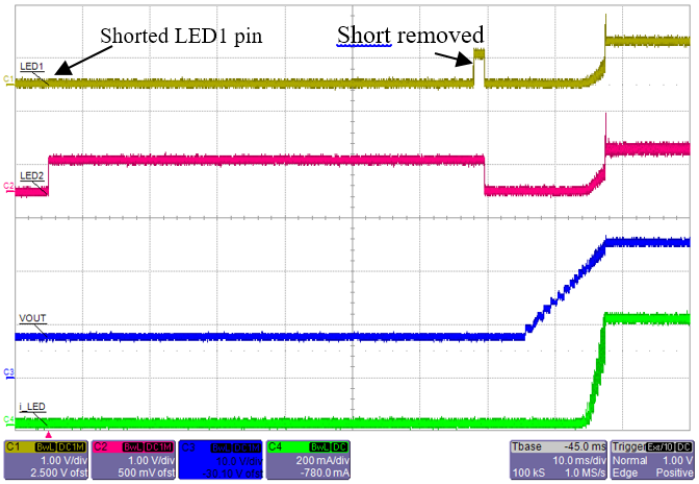


Figure 9: LED1 is shorted-to-GND initially, then released. After the fault is removed, the IC auto-recovers and proceeds with soft-start.

Power Up: Boost Output Undervoltage

During startup, after the input disconnect switch has been enabled, the output voltage is checked through the OVP (overvoltage protection) pin. If the sensed voltage does not rise above $V_{UVP(th)}$, the output is assumed to be at fault and the IC will not proceed with soft start.

Undervoltage protection may be caused by one of the following faults:

- Output capacitor shorted to GND
- Boost inductor or diode open
- OVP sense resistor open

After an UVP (undervoltage protection) fault, the ALT80600 is immediately shutdown and latched off. To enable the IC again, the latched fault must be cleared. This can be achieved by powering-cycling the IC, which means either:

- V_{IN} falls below falling UVLO threshold, or
- EN = L for >32k clock cycles (about 16 ms at 2 MHz).

Alternatively, latched fault can be cleared by keeping EN = H but pulling PWM = L for >32k clock cycles. This method has the advantage that it does not interrupt the CLKOUT signal.

Soft Start Function

During startup, the ALT80600 ramps up its boost output voltage following a fixed slope, as determined by OVP set point and Soft-Start Timer. This technique limits the input inrush current, and ensures consistent startup time regardless of the PWM dimming duty cycle.

The soft-start process is completed when any one of the following conditions is met:

- All enabled LED channels have reached their regulation current,
- Output voltage has reached 93% of its OVP threshold, or
- Soft-start ramp time (t_{SS}) has expired.

To summarize, the complete startup process of ALT80600 consists of:

- Power-up error checking
- Enabling input disconnect switch
- LED pin open/short detection
- Soft-start ramp

This is illustrated by the following startup timing diagram (not to scale):

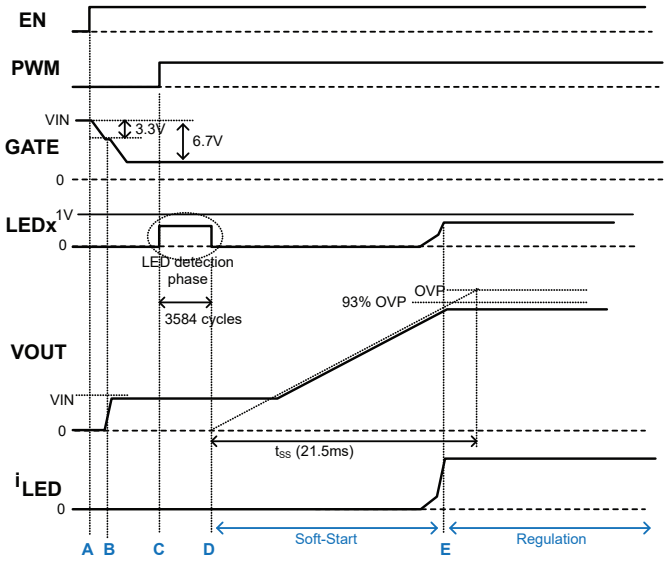


Figure 10: Complete startup process of ALT80600

Explanation of Events:

A: EN = H wakes up the IC. V_{DD} ramps up and CLKOUT becomes available. IC starts to pull down GATE slowly.

B: When GATE is pulled down to 3.3 V below V_{IN}, I_{SET} becomes enabled. IC is now waiting for PWM = H to startup.

C: Once PWM = H, the IC checks each LEDx pins to determine if it is in use, disabled, or shorted to GND.

D: Soft-Start begins at the completion of LED pin short-detect phase (3584 clock cycles). V_{OUT} ramps up following a fixed slope set by OVP and soft-start timer (21.5 ms).

E: Soft-start terminates when all LED currents reached regulation, V_{OUT} reached 93% OVP, or soft-start timer expired.

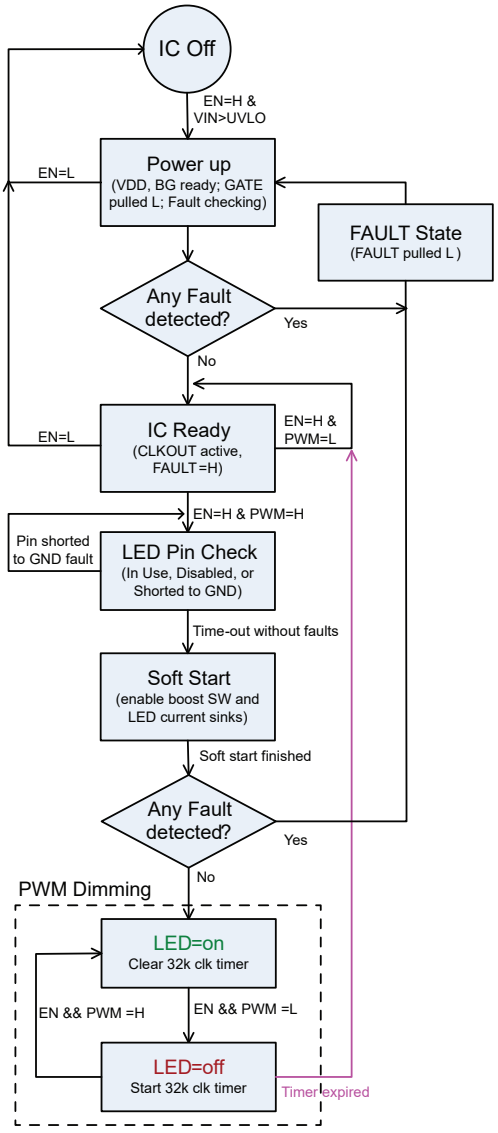


Figure 11: Startup Flow Chart

Frequency Selection

The switching frequency of the boost regulator is programmed by a resistor connected to FSET pin. The switching frequency can be selected anywhere from 200 kHz to 2.3 MHz. The chart below shows the typical switching frequency verses FSET resistor value.

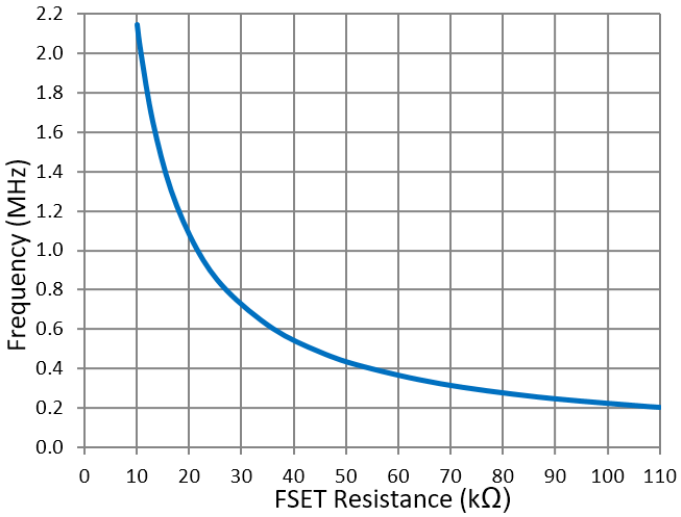


Figure 12: Switching Frequency as a function of FSET Resistance

Alternatively, the following empirical formula can be used:

Equation 1: $f_{SW} = 21.5 / (R_{FSET} + 0.2)$

where f_{SW} is in MHz and R_{FSET} is in kΩ.

If a fault occurs during operation that will increase the switching frequency, the internal oscillator frequency is clamped to a maximum of 3.5 MHz. If the FSET pin is shorted to GND, the part will shut down. For more details, refer to the Fault Mode Table section.

Synchronization

The ALT80600 can also be synchronized using an external clock. At power up, if the FSET pin is held low, the IC will not start. Only when the FSET pin is tristated to allow for the pin to rise to about 1 V, or when a sync clock is detected, the ALT80600 will then try to power up.

The basic requirement of the external sync signal is 150 ns minimum on-time and 150 ns minimum off time. The diagram below shows the timing restrictions for a synchronization clock at 2.2 MHz.

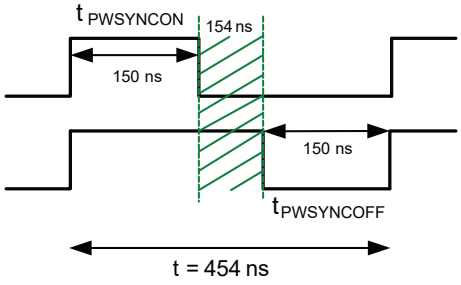


Figure 13: Pulse width requirements for an External Sync clock at 2.2 MHz

Based on the above, any clock with a duty cycle between 33% and 66% at 2.2 MHz can be used. The table below summarizes the allowable duty cycle range at various synchronization frequencies.

Table 3: Acceptable Duty Cycle range for External Sync clock at various frequencies

Sync. Pulse Frequency	Duty Cycle Range
2.2 MHz	33% to 66%
2 MHz	30% to 70%
1 MHz	15% to 85%
600 kHz	9% to 91%
300 kHz	4.5% to 95.5%

If it is necessary to switch over between internal oscillator and external sync during operation, ensure the transition takes place at least 500 ns after the previous PWM = H rising edge. Alternatively, execute the switchover during PWM = L only. This restriction does not apply if PWM dimming is not being used.

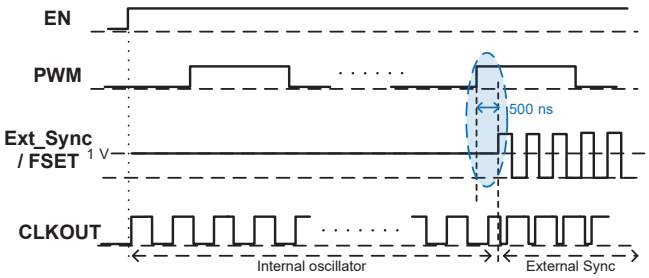


Figure 14: Avoid switching over between Internal Oscillator and External Sync in highlighted region

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Loss of External Sync Signal

Suppose the ALT80600 started up with a valid external SYNC signal, but the SYNC signal is lost during normal operation. In that case, one of the following happens:

- If the external SYNC signal is high impedance (open), the IC continues normal operation after approximately 5 µs, at the switching frequency set by R_{FSET}. No FAULT flag is generated.
- If the external SYNC signal is stuck low (shorted to ground), the IC will detect an FSET-shorted-to-GND fault. FAULT pin is pulled low after approximately 10 µs, and switching is disabled. Once the FSET pin is released or SYNC signal is detected again, the IC will proceed to soft-start.

To prevent generating a fault when the external SYNC signal is stuck at low, the circuit shown below can be used. When the external SYNC signal goes low, the IC will continue to operate normally at the switching frequency set by the R_{FSET}. No FAULT flag is generated.

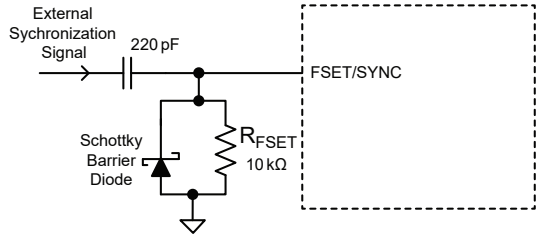


Figure 15: Countermeasure for External Sync Stuck-at-Low Fault

Switching Frequency Dithering

To minimize the peak EMI spikes at switching frequency harmonics, the ALT80600 offers the option of frequency dithering, or spread-spectrum clocking. This feature simplifies the input filters needed to meet the automotive CISPR 25 conducted and radiated emission limits.

For maximum flexibility, the ALT80600 allows both dithering range and modulation frequency to be independently programmable using two external components.

The Dithering Modulation Frequency is given by the approximate equation:

Equation 2: $f_{DM}\ (kHz) = 25 / C_{DITH}\ (nF)$

where C_{DITH} is the value of capacitor connected from DITH pin to GND.

The dithering Range is given by the approximate equation:

Equation 3: $Range\ (\pm\%) = 20 \times R_{FSET} / R_{DITH}$

where R_{FSET} is the resistor from FSET pin to GND, R_{DITH} is the resistor between DITH and FSET pins.

As an example, by using R_{FSET} = 10 kΩ, R_{DITH} = 40.2 kΩ, and C_{DITH} = 22 nF, the resulted switching frequency is f_{SW} = 2.15 MHz ±5% modulated at 1.1 kHz. This is illustrated by the following diagram.

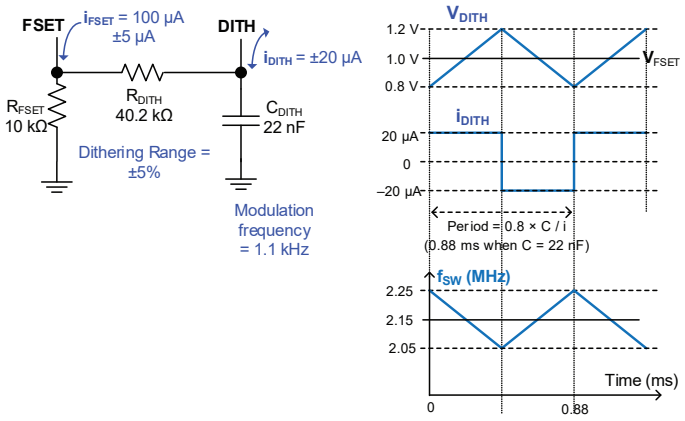


Figure 16: How to Program Switching Frequency Dithering Range and Modulation Frequency

There are no hard limits on dithering range and modulation frequency. As a general guideline, pick a dithering range between ±5% and 10%, with the modulation frequency between 1 kHz and 3 kHz. In practice, using a larger dithering range and/or higher modulation frequency do not generate any noticeable benefits.

If dithering function is not desired, it can be disabled by disconnecting the R_{DITH} between DITH and FSET pins. Connect DITH pin to VDD if C_{DITH} is not populated.

Clock Out Function

The ALT80600 allows other ICs to be synchronized to its internal switching frequency through the CLKOUT pin.

The CLKOUT signal is available as soon as the IC is enabled (EN = H), even when the boost stage is not active (PWM = L). Its frequency is the same as that of the internal oscillator. Its duty cycle, however, depends on how the switching frequency is generated:

- If f_{SW} is programmed by FSET resistor, the CLKOUT duty cycles is approximately 50%.
- If f_{SW} is controlled by external sync, the output signal has a

fixed 150 ns negative pulse width (CLKOUT = L), regardless of the external sync frequency.

This is illustrated by the following waveforms:

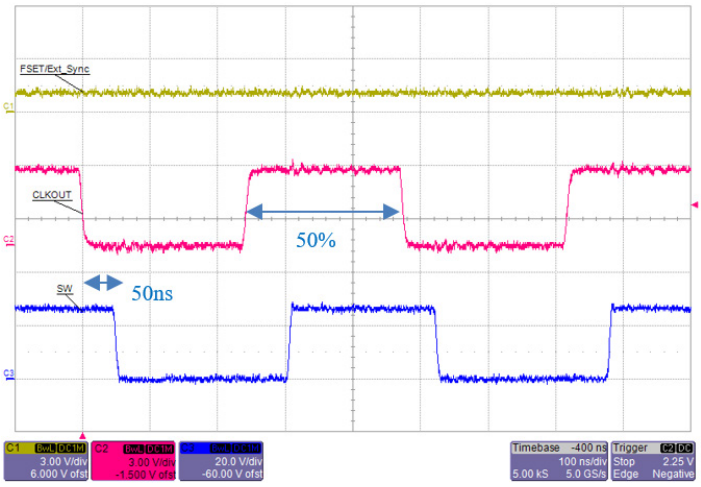


Figure 17: Without external sync, the CLKOUT signal has a fixed duty cycle of 50%. Delay from CLKOUT falling edge to SW falling edge is approximately 50 ns.

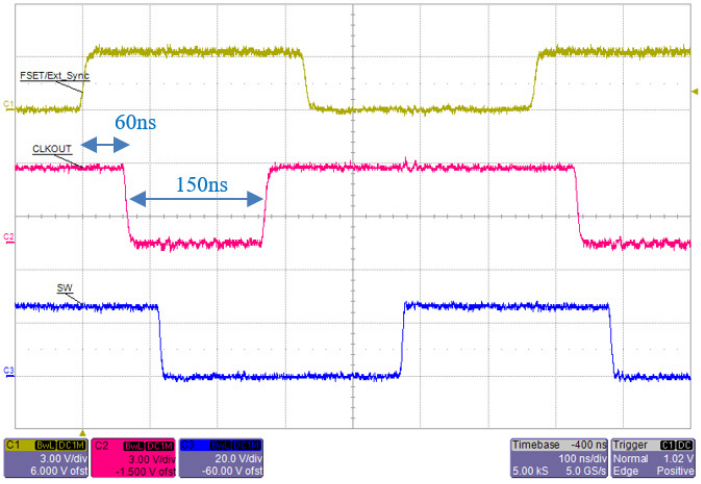


Figure 18: With external sync, the CLKOUT signal has a fixed negative pulse width of 200 ns. Delay from SYNC rising edge to CLKOUT falling edge is approximately 60 ns.

LED Current Setting

The maximum LED current can be up to 120 mA per channel, and is set through the ISET pin. Connect a resistor RISET between this pin and GND. The relation between ILED and RISET is given below:

Equation 4:

$$I_{LED} = I_{SET} \times A_{ISET}$$

$$I_{SET} = V_{ISET} / R_{ISET}$$

$$Therefore\ R_{ISET} = (V_{ISET} \times A_{ISET}) / I_{LED}$$

$$= 833 / I_{LED}$$

where I_{LED} current is in mA and R_{ISET} is in kΩ.

This sets the maximum current through the LEDs, referred to as the '100% current'. The average LED current can be reduced from the 100% current level by using either PWM dimming or analog dimming.

Table 4: ISET resistor values vs. LED current. Resistances are rounded to the nearest E-96 (1%) resistor value.

Standard Closest RISET Resistor Value	LED current per channel
6.98 kΩ	120 mA
8.25 kΩ	100 mA
10.5 kΩ	80 mA
13.7 kΩ	60 mA
21.0 kΩ	40 mA

PWM Dimming

When both EN and PWM pins are pulled high, the ALT80600 turns on all enabled LED current sinks. When either EN or PWM is pulled low, all LED current sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active.

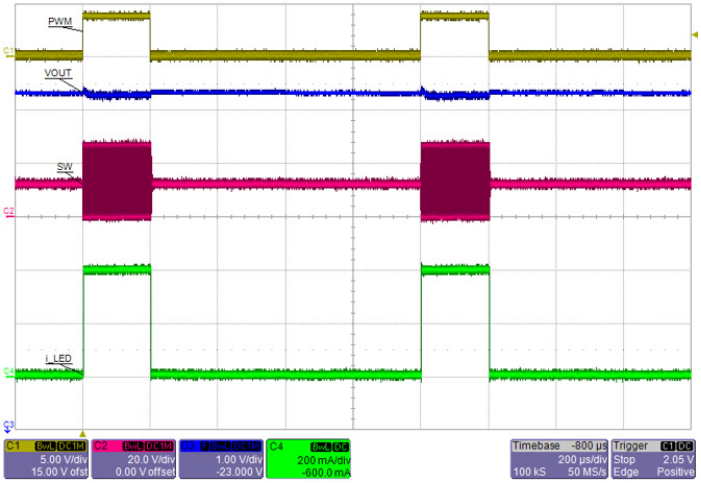


Figure 19: PWM dimming operation at 20% 1 kHz. CH1 = PWM (5 V/div), CH2 = SW (20 V/div), CH3 = V_{OUT}, CH4 = i_{LED} (200 mA/div).

By using the patented Pre-Emptive Boost (PEB) control algo-

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

rithm, the ALT80600 is able to achieve minimum PWM dimming on-time down to 300 ns. This translates to PWM dimming ratio up to 15,000:1 at the PWM dimming frequency of 200 Hz. Technical details on PEB will be explained in the next section.

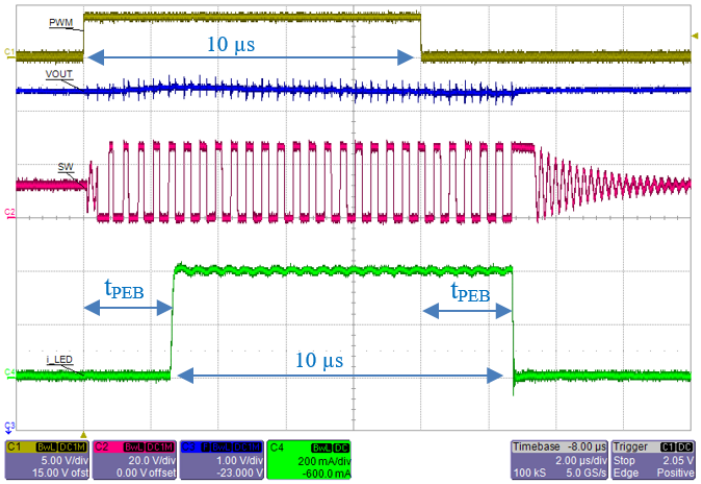


Figure 20: Zoom in view for PWM on-time = 10 µs. Notice that the LED current is shifted with respect to PWM signal. Ripple at V_{OUT} is ~0.2 V when using 2 × 4.7 µF MLCC as output capacitors.

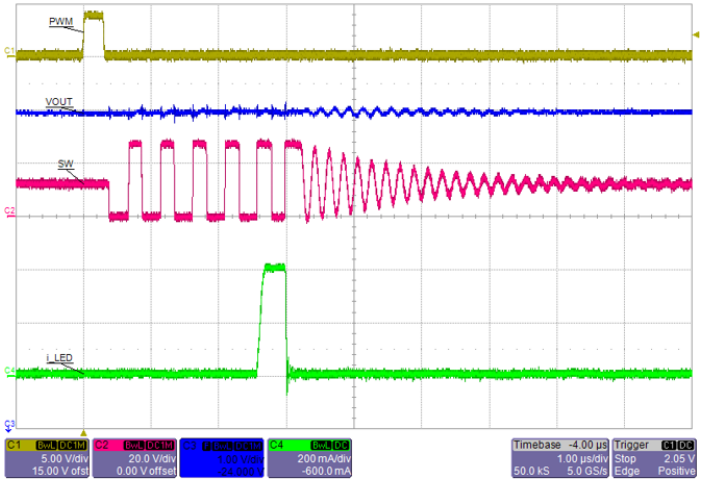


Figure 21: Zoom-in view showing ALT80600 is able to regulate LED current at PWM on-time down to 300 ns.

The typical PWM dimming frequencies fall between 200 Hz and 1 kHz. There is no hard limit on the highest PWM dimming frequency that can be used. However at higher PWM frequency, the maximum PWM dimming ratio will be reduced. This is shown in the following table:

Table 5: Maximum PWM Dimming Ratio that can be achieved when operating at different PWM Dimming Frequency

PWM Frequency	PWM Period	Maximum PWM Dimming Ratio
200 Hz	5 ms	15,000:1
1 kHz	1 ms	3,000:1
3.3 kHz	300 µs	1,000:1
20 kHz	50 µs	150:1

Pre-Emptive Boost

The basic principle of pre-emptive boost (PEB) can be best explained by the following two waveforms. The first one shows how a conventional LED driver operates during PWM dimming operation. The second one shows that of the ALT80600.

Common test conditions for both cases:

PWM = 1% at 1 kHz (on-time=10 µs), f_{SW} = 2.15 MHz, L = 10 µH, V_{IN} = 12 V, LED load = 8 series (V_{OUT} = ~25 V) at 100 mA × 4. C_{OUT} = 2 × 4.7 µF 50 V 1210 MLCC. COMP: R_Z = 280 Ω, C_Z = 68 nF.

Common scope settings:

CH1 (Yellow) = PWM (5 V/div); CH2 (Red) = Inductor current (500 mA/div); CH3 (Blue) = V_{OUT} (1 V/div); CH4 (Green) = LED current (200 mA/div); time scale = 2 µs/div.

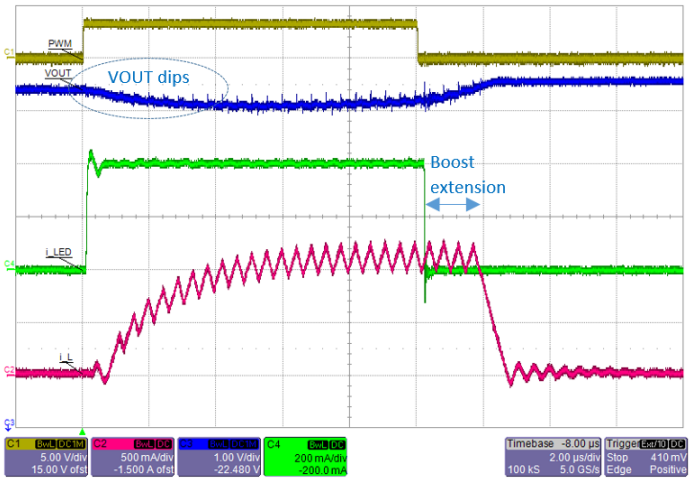


Figure 22: Traditional PWM Dimming operation where boost switch and LED current are enabled at the same time. Note that V_{OUT} shows overall ripple of ~0.5 V

When PWM signal goes high, a conventional LED driver turns on its boost switching at the time with LED current sinks. The problem is that the inductor current takes several switching cycles

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

to ramp up to its stead-state value before it can deliver full power to the output load. During the first few cycles, energy to the LED load is mainly supplied by the output capacitor, which results in noticeable dip in output voltage.

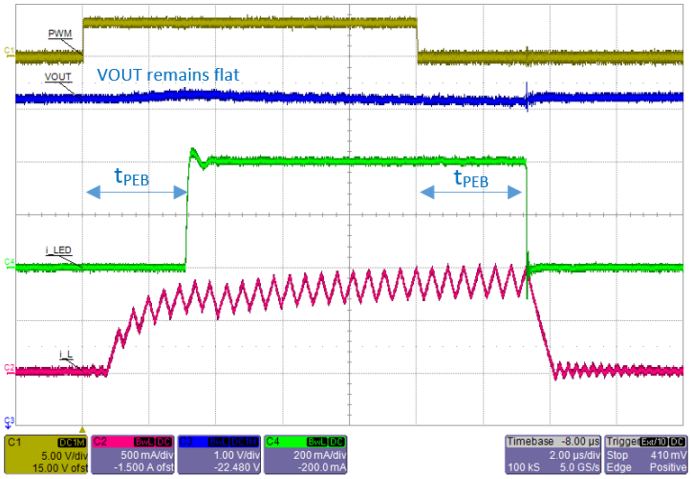


Figure 23: ALT80600 PWM dimming operation with PEB delay set to 3 µs. Note that V_{OUT} ripple is reduced to ~0.2 V.

In the ALT80600, the boost switch is also enabled when PWM goes high. However, the LED current is not turned on until after a short delay of t_{PEB}. This allows the inductor current to build up before it starts to deliver the full power to LED load. During the pre-boost period, V_{OUT} actually bumps up very slightly, while the following dip is essentially eliminated. When PWM goes low, both boost switching and LED remains active for the same delay of t_{PEB}. Therefore the PWM on-time is preserved in LED current.

PEB delay can be programmed using an external resistor, R_{PEB}, from PEB pin to GND. Their relationship is shown in the following chart:

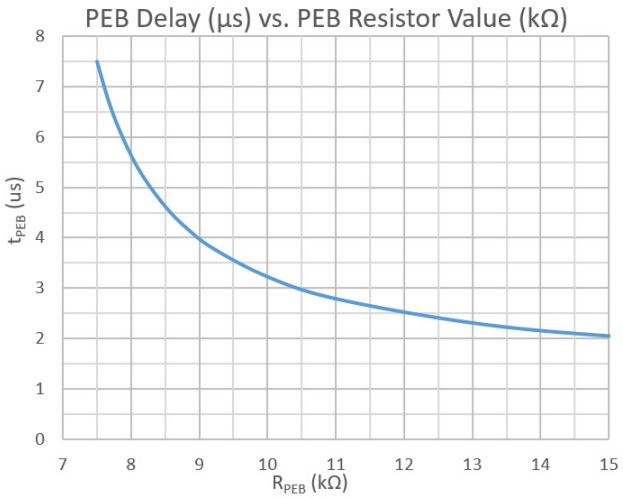


Figure 24: How PEB delay time varies with value of PEB pin resistor to GND.

Ideally, t_{PEB} is equal to the inductor current ramp up time. But the latter is affected by many external parameters, such as switching frequency, inductance, V_{IN} and V_{OUT} ratio, etc. Therefore, some experimentation is required to optimize the PEB delay time. In general for switching frequency at 2 MHz, t_{PEB} = 2 to 4 µs is a good starting point.

The advantage of PEB is that even a non-optimized delay time can significantly reduce the output ripple voltage compared to a conventional LED driver.

Analog Dimming with APWM Pin

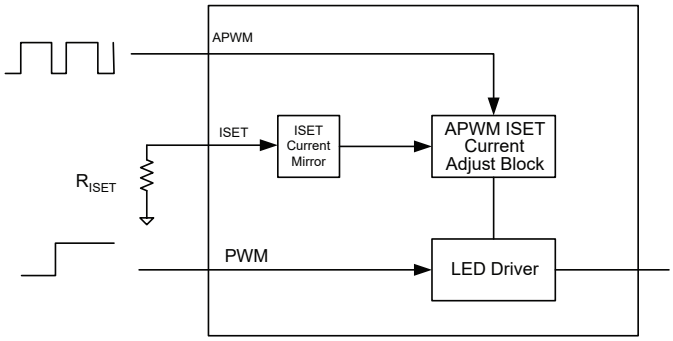


Figure 25: Simplified block diagram of APWM function

The APWM pin is used in conjunction with the ISET pin to achieve analog dimming. This is a digital signal pin that internally adjusts the ISET current. The typical input signal frequency is between 40 kHz and 1 MHz. The duty cycle of this signal is inversely proportional to the percentage of current delivered to the LED. The relationship is shown below:

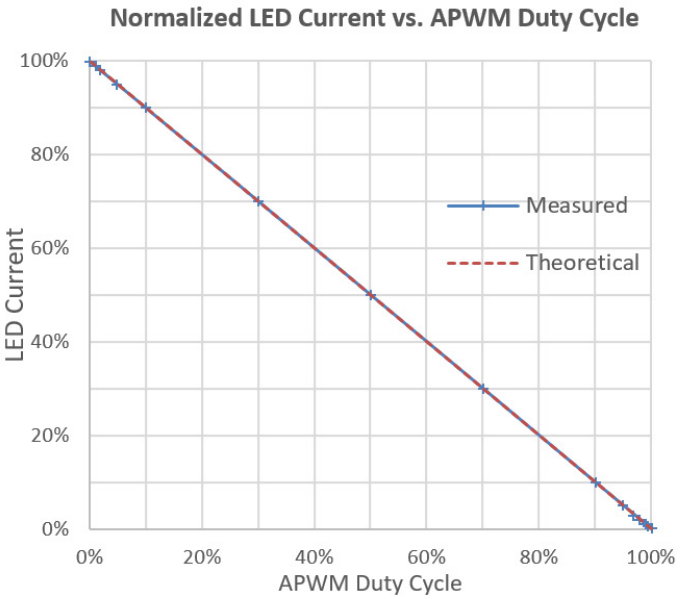


Figure 26: Showing LED current is inversely proportional to the APWM duty cycle. Test conditions: V_{IN} =12 V, V_{OUT} = 25 V (8 × WLED), total LED current = 100 mA × 4, APWM frequency = 100 kHz

As an example, a system that delivers a full LED current of 100 mA per channel would deliver 75 mA when an APWM signal with a duty-cycle of 25% is applied (because analog dimming level is 100% – 25% = 75%). This is demonstrated by the following waveforms.

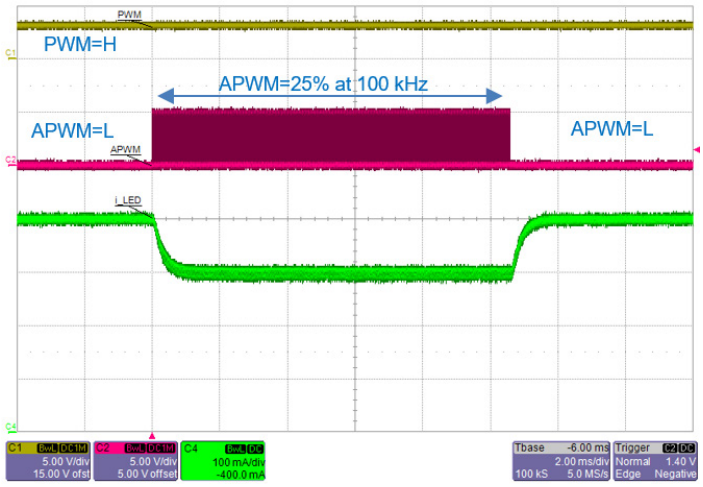


Figure 27: PWM = H. Total LED current drops from 400 mA (4 × 100 mA/ch) to 300 mA when APWM of 25% duty cycle is applied. Note that LED current takes ~0.5 ms to settle after change in APWM.

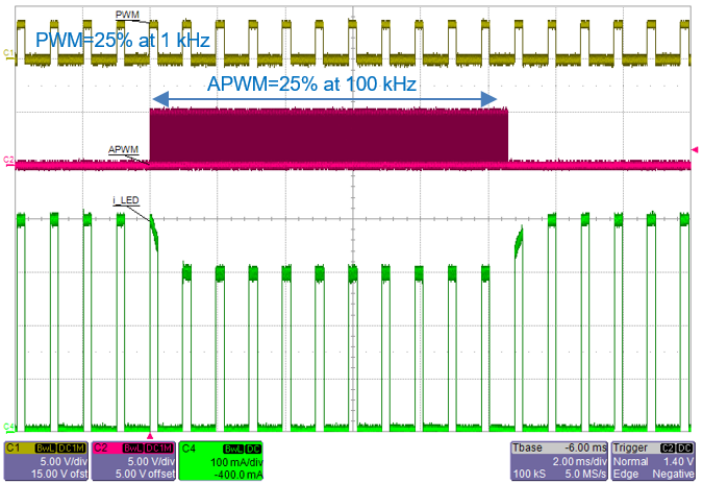


Figure 28: PWM = 25% at 1 kHz. Peak LED current drops from 400 mA (4 × 100 mA/ch) to 300 mA when APWM of 25% duty cycle is applied

One popular application of analog dimming is for LED brightness calibration, commonly known as 'LED Binning'. LEDs from the same manufacturer and series are often grouped into different 'bins' according to their light efficacy (lumens per watt). It is therefore necessary to calibrate the '100% current' for each LED bin, in order to achieve uniform luminosity.

To use APWM pin as a trim function, the user should first set the 100% current based on efficacy of LED from the lowest bin. When using LED with higher efficacy, the required current is then trimmed down to the appropriate level using APWM duty cycle.

As an example, assume that:

- LED from lowest bin has an efficacy of 80 lm/W
- LED highest bin has an efficacy of 120 lm/W

Suppose the maximum LED current was set at 100 mA based LEDs from lowest bin. When using LEDs from highest bin, the current should then be reduces to 67% (80/120). This can be achieved by sending APWM clock with 33% duty cycle.

When analog dimming is not used, APWM pin should be either tied to GND or left floating (there is an internal pull-down resistor to GND).

Extending LED Dimming Ratio

The dynamic range of LED brightness can be further extended, by using a combination of PWM duty cycle, APWM duty cycle, and analog dimming method.

For example, the following approach can be used to achieve a 100,000:1 dimming ratio at 200 Hz:

- Vary PWM duty cycle from 100% down to 0.01% to give 10,000:1 dimming. This requires PWM dimming on-time be reduced down to 0.5 µs.
- With PWM dimming on-time fixed at 0.5µs, vary APWM duty from 0% to 90% to reduce peak LED current from 100% down to 10%. This gives a net effect of 100,000:1 dimming.

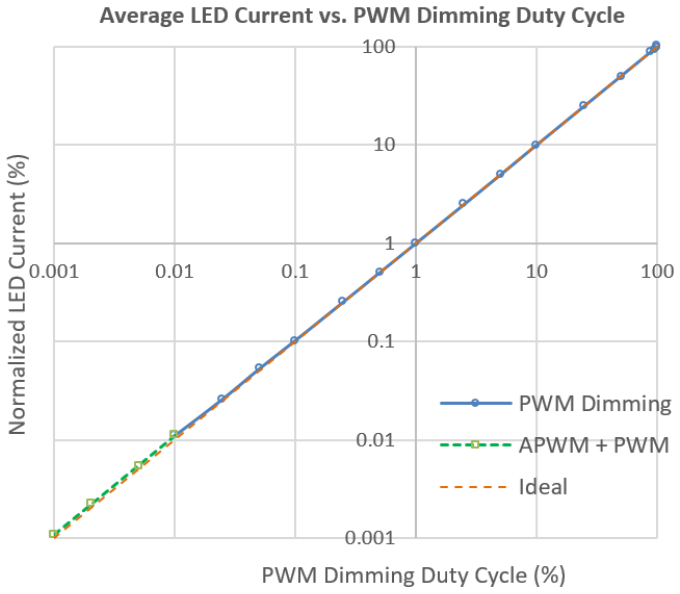


Figure 29: How to achieve 100,000:1 dimming ratio by using both PWM and APWM. Test conditions: V_{IN} = 12 V, V_{OUT} = 25 V (8 × WLED), total LED current = 400 mA, PWM frequency = 200 Hz, APWM frequency = 100 kHz.

Note that the ALT80600 is capable of providing analog dimming range greater than 10:1. By applying APWM with 96% duty cycle, for example, an analog dimming range of 25:1 can be achieved. However, this requires the external APWM signal source to have very fine pulse-width resolution. At 200 kHz APWM frequency, a resolution of 50 ns is required to adjust its duty cycle by 1%.

Analog Dimming with External Voltage

Besides using APWM signal, the LED current can also be reduced by using an external voltage source applied through a resistor to the ISET pin. The dynamic range of this type of dimming is dependent on the ISET pin current. The recommended i_{SET} range is from 20 µA to 125 µA for the ALT80600. Note that the IC will continue to work at i_{SET} below 20 µA, but the relative error in LED current becomes larger at lower dimming level.

Below is a typical application circuit using a DAC (digital-analog converter) to control the LED current. The ISET current (which directly controls the LED current) is normally set as V_{ISET}/R_{ISET}. The DAC voltage can be higher or lower than V_{ISET}, thus adjusting the LED current to a lower or higher value.

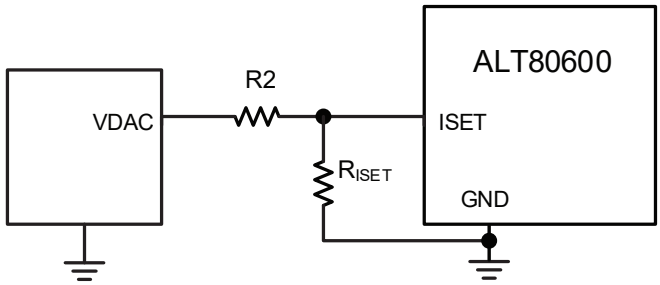


Figure 30: Adjusting LED current with an external voltage source

Equation 5:

$$i_{ISET} = \frac{V_{ISET}}{R_{ISET}} - \left[\frac{VDAC - V_{ISET}}{R2}\right]$$

where V_{ISET} is the ISET pin voltage (typically 1.0 V), and VDAC is the DAC output voltage.

When VDAC is higher than 1.00 V, the LED current is reduced. When VDAC is lower than 1.00 V, the LED current is increased.

Some common applications for the above scheme include:

- LED binning
- Thermal fold-back using external NTC (negative temperature coefficient) thermistor

In the following application example, the thermistor used is NTCS0805E3684JXT (680 kΩ @ 25°C). R1 = 340 kΩ, R2 = 20 kΩ, and R3 = 8.45 kΩ. The LED current per channel is reduced from 97 mA at 25°C to 34 mA at 125°C.

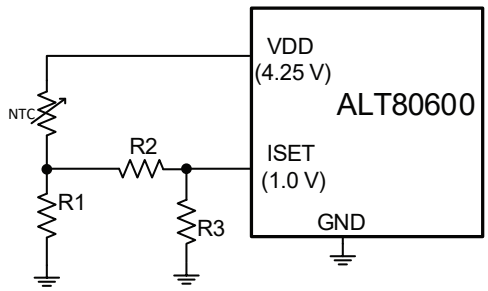


Figure 31: Thermal foldback of LED current using NTC thermistor

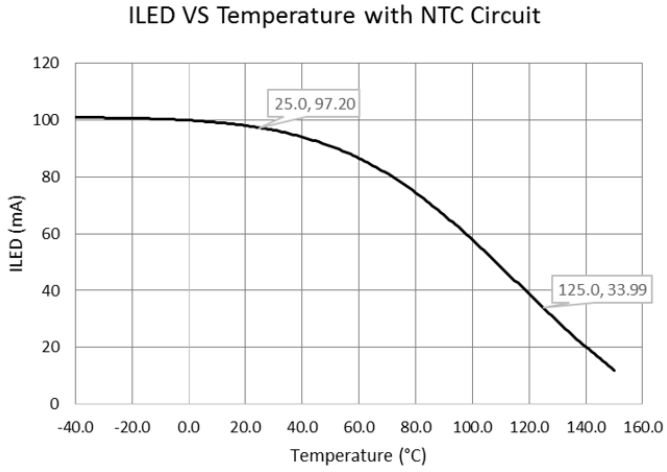


Figure 32: LED current varies with temperature when using thermistor NTCS0805E3684JXT for thermal foldback

VDD

The VDD pin provides regulated bias supply for internal circuits. Connect a C_{VDD} capacitor with a value of 1 µF or greater to this pin. The internal LDO can deliver up to 2 mA of current with a typical VDD voltage of about 4.25 V. This allows it to serve as the pull up voltage for FAULT pin.

Shutdown

If EN pin is pulled low for longer than $t_{EN(OFF)}$ (32k clock cycles), the ALT80600 enters shutdown (sleep mode). As an example, at 2.15 MHz clock frequency, it will take approximately 15.2 ms to completely shut down the IC. The next time EN pin goes high, all internal fault registers are cleared. The IC needs to go through a complete soft start process after PWM goes high.

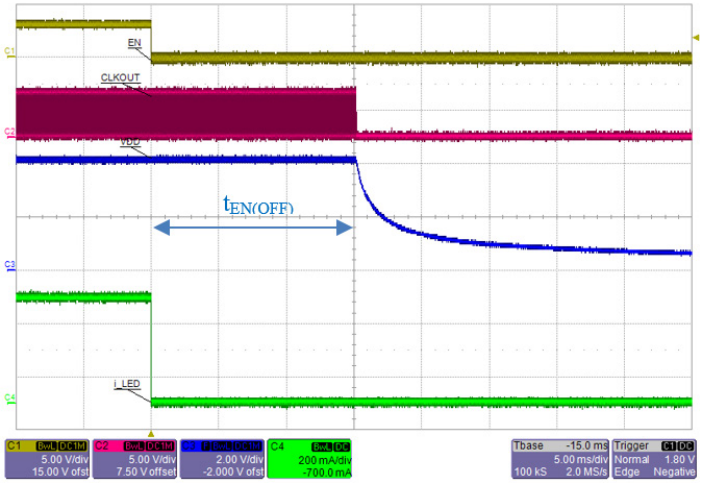


Figure 33: After EN = L for 32k clock cycles (~15 ms at 2.15 MHz), the IC completely shuts down so VDD (Blue) decays.

There is an alternative way to reset the internal fault status registers. By keeping EN = H and PWM = L for longer than 32k clock cycles, the ALT80600 clears all internal fault registers but does not go into sleep mode. The next time PWM pin goes high, the IC will still go through soft start process. The difference is that VDD voltage and CLKOUT signal are always available as long as EN = H.

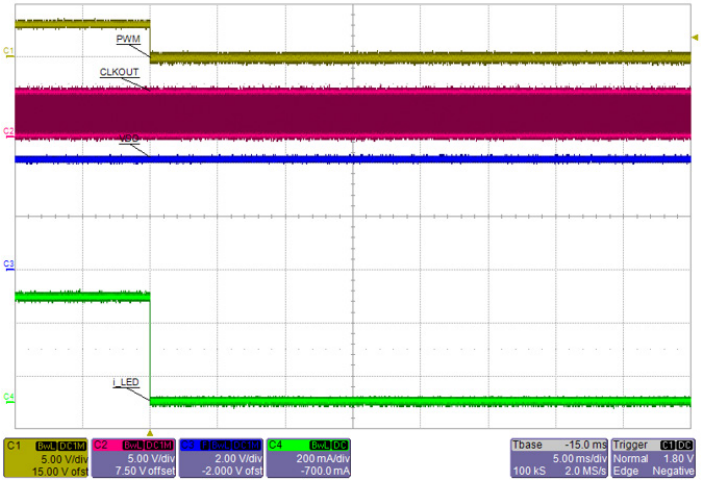


Figure 34: As long as EN = H, the IC does not shut down VDD and CLKOUT. But internal latched faults are cleared by PWM = L for 32k clock cycles.

FAULT DETECTION AND PROTECTION

LED String Partial-Short Detect

All LED current sink pins (LED1 to LED4) are designed to withstand the maximum output voltage, as specified in the AbsMax section. This prevents the IC from being damaged if V_{OUT} is directly applied to an LED pin due to an output connector short.

In case of direct-short or partial-shorted fault in any LED string during operation, the LED pin with voltage exceeding V_{LEDSC} will be removed from regulation. This prevents the IC from dissipating too much power due to large voltage drop across the LED current sink.

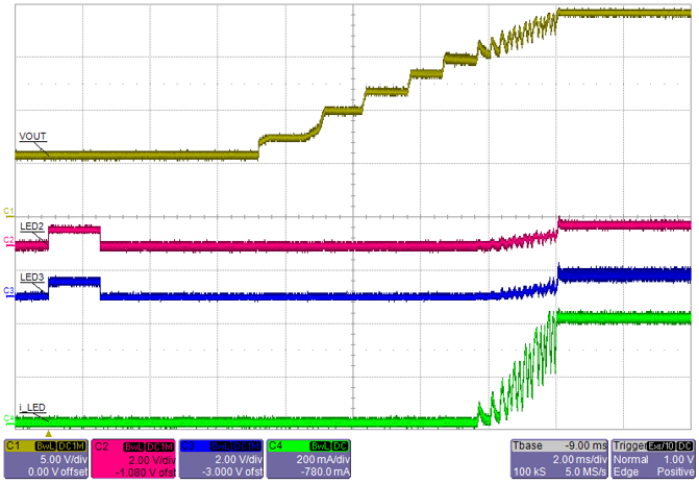


Figure 35: Normal startup sequence showing voltage at LED2 and LED3 pins. V_{IN} = 6 V, output = 6 × WLED in series, current = 4 × 100 mA

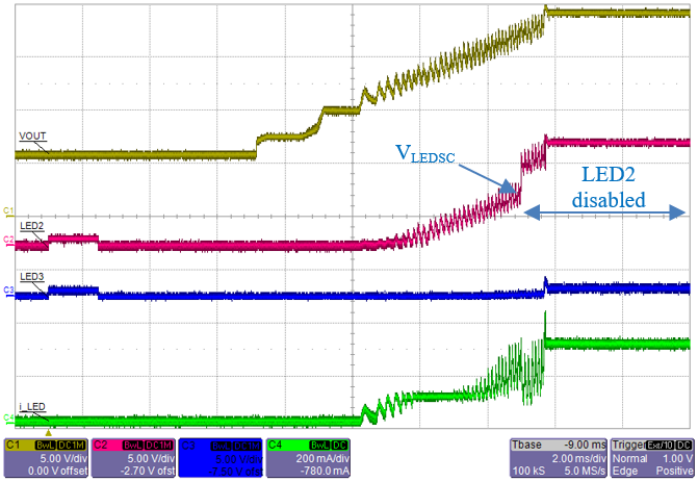


Figure 36: Startup sequence when LED string#2 has a partial-short fault (4 × WLED instead of 6). As soon as LED2 pin rises above V_{LEDSC} (~4.6 V), the channel is disabled. Output is now 300 mA.

While the IC is being PWM dimmed, the IC will recheck the disabled LED every time the PWM signal goes high. This allows for some self-correction in case an intermittent LED pin shorted to VOUT fault is present.

At least one LED pin must be at regulation voltage (below ~1.2 V) for the LED string partial-short detection to activate. In case all of the LED pins are above regulation voltage (this could happen when the input voltage rises too high for the LED strings), they will continue to operate normally.

Overvoltage Protection

The ALT80600 offers a programmable output overvoltage protection (OVP), plus a fixed secondary overvoltage protection (OVP2).

The OVP pin has a threshold level of 2.5 V typical. Overvoltage protection is tripped when current into this pin exceeds ~150 µA. A resistor can be used to set the OVP threshold up to 40 V approximately. This is sufficient for driving 11 white LEDs in series.

The formula for calculating the OVP resistor is shown below:

Equation 6: $$R_{OVP} = (V_{OVP} - V_{OVP(th)}) / i_{OVP(th)}$$

where V_{OVP} is the desired OVP threshold, $V_{OVP(th)}$ = 2.5 V typical, $i_{OVP(th)}$ = 150 µA typical.

To determine the desired OVP threshold, take the maximum LED string voltage at cold and add ~10% margin on top of it.

The OVP event is not a latched fault and, by itself, does not pull the FAULT pin to low. If the OVP condition occurs during a load dump, for example, the IC will stop switching but not shut down.

There are several possibilities of why an OVP condition is encountered during operation. The two most common being an open LED string and a disconnected output connector.

The waveform below shows a typical OVP condition. When one LED string becomes open, current through its LED driver drops to zero. The ALT80600 responses by boosting the output voltage higher. When output reaches OVP threshold, the LED string without current is removed from regulation. The rest of LED strings continue to draw current and drain down V_{OUT}. Once V_{OUT} falls below ~94% OVP, boost will resume switching to power the remaining LED strings.

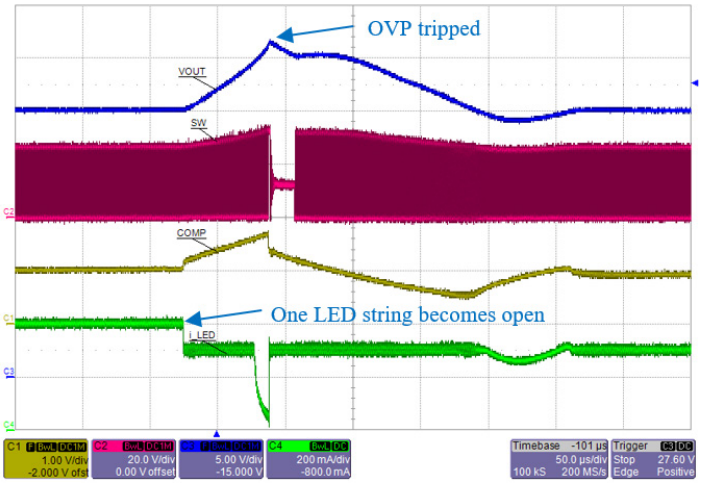


Figure 37: An open-LED string faults causes V_{OUT} to ramp up and trip OVP. The ALT80600 then disables the open LED string and continues with remaining strings.

The ALT80600 also has a fixed secondary overvoltage protection to protect its internal switch. If the boost Schottky diode suddenly becomes open during normal operation, the energy stored in the inductor will force SW node voltage to increase rapidly. Once voltage on the SW pin exceeds OVP2, switching and all LED drivers are disabled. The IC remains latched off until it is reset.

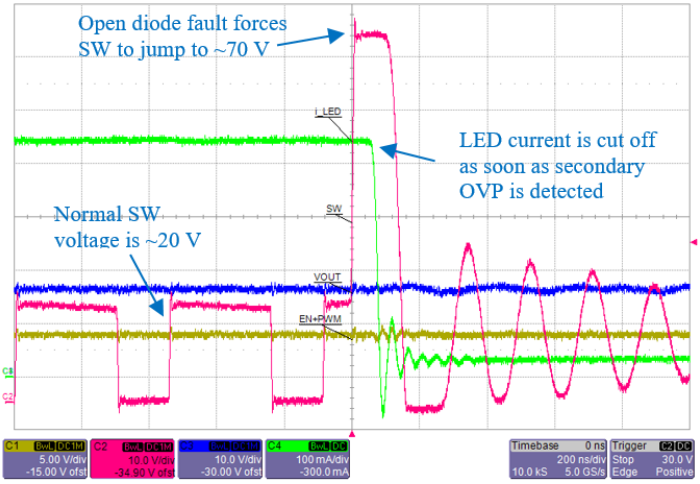


Figure 38: An open-diode fault is introduced during normal operation. SW voltage jumps to ~70 V, causing the MOSFET to self-conduct and dissipate energy in the inductor.

It should be noted that the SW MOSFET in ALT80600 is designed to avalanche and dissipate the excess energy safely in case of open-diode fault. Therefore the IC is not damaged even though SW node rises above AbsMax rating momentarily.

Boost Switch Overcurrent Protection

The boost switch is protected with cycle-by-cycle current limiting set at typical 3.65 A, minimum 3.0 A. The waveform below shows normal switching at V_{IN} = 6 V, V_{OUT} = 25 V, and total LED current 400 mA.

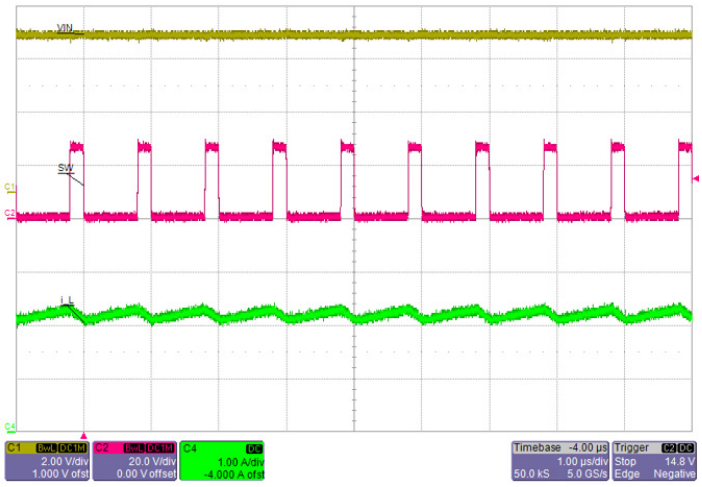


Figure 39: Normal switching waveform showing the SW node voltage and inductor current.

When the input voltage is reduced further, input current increases and peak switch current reaches 3.2 A. SW_OCP is tripped and the IC skips a switching cycle to reduce the current

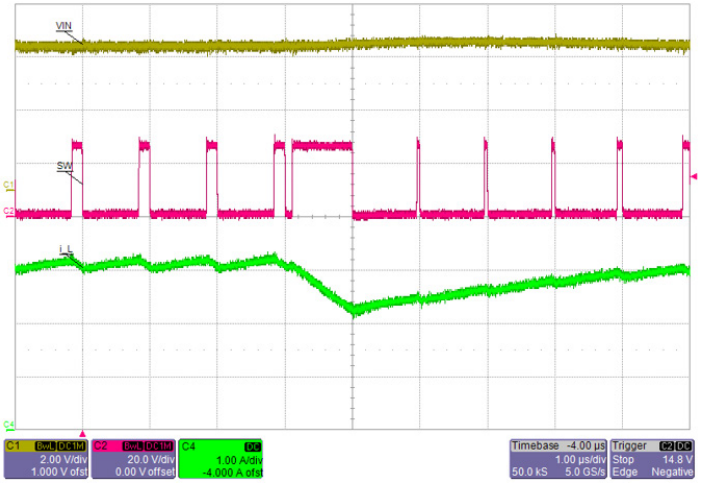
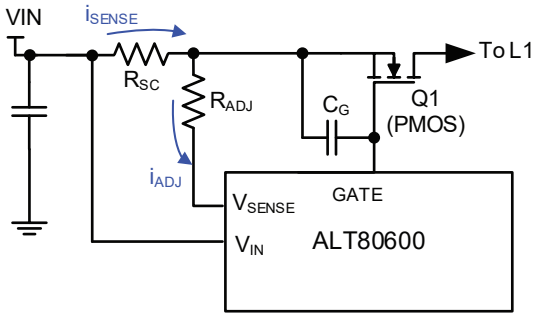


Figure 40: When peak current in SW pin reaches ~3.2 A, overcurrent protection kicks in and the IC skips a switching cycle.

There is also a secondary current limit ($I_{SW(LIM2)}$) that is sensed on the boost switch. This current limit is set at about 33% higher than the cycle-by-cycle current limit. It is to protect the switch

from destructive current spikes in case the boost inductor is shorted. Once this limit is tripped, the ALT80600 will immediately shut down and latch off.

Input Overcurrent Protection and Disconnect Switch



$$V_{IN} - V_{SENSE} = R_{SC} \times i_{SENSE} + R_{ADJ} \times i_{ADJ}$$

Figure 41: Optional input disconnect switch using a PMOSFET

The primary function of the input disconnect switch is to protect the system and the device from catastrophic input currents during a fault condition.

If the input current level goes above the preset current limit threshold, the part will be shut down in less than 3 µs. This is a latched condition. The fault flag is also set to indicate a fault. This feature protects the input from drawing too much current during heavy load. It also prevents catastrophic failure in the system due to a short of the inductor, diode, or output capacitors to GND.

The waveform below illustrates the typical input overcurrent fault condition. As soon as input OCP limit is reached, the part disables the gate of the disconnect switch Q1 and latches off.

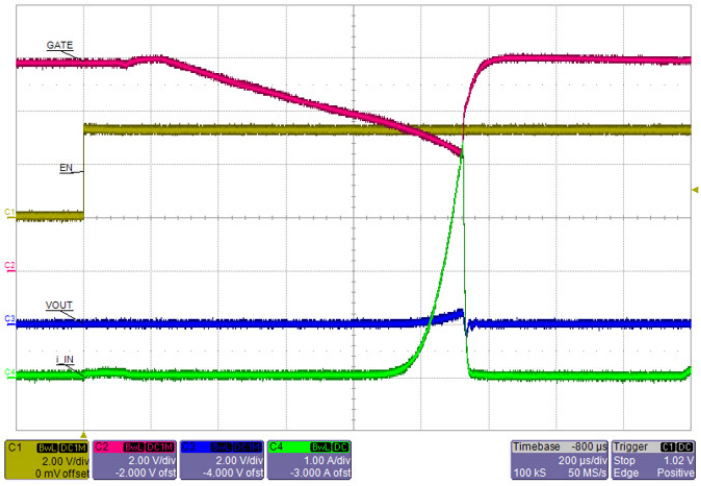


Figure 42: Startup into an output shorted-to-GND fault. Input OCP is tripped when current (Green trace) exceeds 4 A. PMOS Gate (Red) is turned off immediately and IC latches off.

During startup when Q1 first turns on, an inrush current flows through Q1 into the output capacitance. If Q1 turns on too fast (due to its low gate capacitance), the inrush current may trip input OCP limit. In this case, an external gate capacitance CG is added to slow down the turn-on transition. Typical value for CG is around 4.7 to 22 nF. Do not make CG too large, since it also slows down the turn-off transient during a real input OCP fault.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Setting the Current Sense Resistor

The typical threshold for the current sense is 100 mV when R_{ADJ} is 0 Ω. The ALT80600 can have this voltage trimmed using the R_{ADJ} resistor. The typical trip point should be set to at least 3.65 A, which coincides with the cycle-by-cycle current limit typical threshold. A sample calculation is done below for 4.2 A of input current.

When R_{ADJ} is not used:

Equation 7: $$V_{SENSETRIP} = R_{SC} \times i_{SENSE} = 100\ mV$$

The desired sense resistor is R_{SC} = 100 mV / 4.2 A = 23.8 mΩ. But this is not a standard E-24 resistor value. Pick the closest lower value which is 22 mΩ.

When R_{ADJ} is used:

Equation 8: $$V_{SENSETRIP} = R_{SC} \times i_{SENSE} + R_{ADJ} \times i_{ADJ}$$

Therefore

$$R_{ADJ} = [V_{SENSETRIP} - (R_{SC} \times i_{SENSE})] / i_{ADJ}$$
$$= [100\ mV - 92.4\ mV] / 20\ \mu A = 380\ \Omega$$

Input UVLO

When V_{IN} and V_{SENSE} rise above $V_{UVLOrise}$ threshold, the ALT80600 is enabled. The IC is disabled when V_{IN} falls below $V_{UVLOfall}$ threshold for more than 50 µs. This small delay is used to avoid shutting down because of momentary glitches in the input power supply.

Fault Protection During Operation

The ALT80600 constantly monitor the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in the table below. It is important to note that there are several points at which the ALT80600 monitors for faults during operation. The locations are input current, switch current, output voltage, switch voltage, and LED pins. Some of the protection features might not be active during startup to prevent false triggering of fault conditions.

The possible fault conditions that the part can detect include:

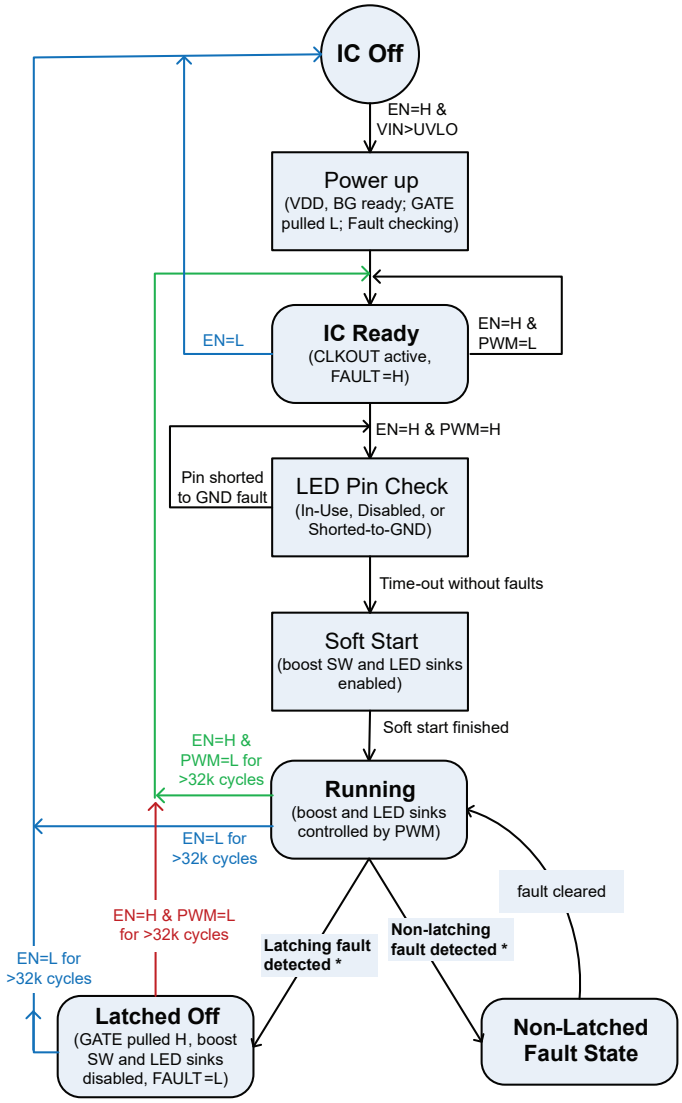
- Open LED Pin or open LED string
- Shorted or partially shorted LED string
- LED pin shorted to GND
- Open or shorted boost diode
- Open or shorted boost inductor
- VOUT short to GND
- SW shorted to GND
- ISET shorted to GND
- FSET shorted to GND
- Input disconnect switch source shorted to GND

Note that some of these faults will not be protected if the input disconnect switch is not being used. An example of this is VOUT short to GND fault.

Table 6: Fault Mode Table

Fault Name	Type	Active	Fault Flag Set	Description	Boost Switch	Disconnect Switch	LED Sink drivers
Primary Switch Overcurrent Protection (Cycle-By-Cycle Current Limit)	Auto-restart	Always	NO	This fault condition is triggered when the SW current exceeds the cycle-by-cycle current limit, $I_{SW(LIM)}$.The present SW on-time is truncated immediately to limit the current. Next switching cycle starts normally.	Off for a single cycle	ON	ON
Secondary Switch Current Limit	Latched	Always	YES	When current through boost switch exceeds secondary SW current limit ($i_{SW(LIM2)}$) the device immediately shuts down the disconnect switch, LED drivers and boost. The Fault flag is set. To reset the fault the EN or PWM pin needs to be pulled low for 32k clock cycles.	OFF	OFF	OFF
Input Disconnect Current Limit	Latched	Always	YES	The device is immediately shut off if the voltage across the input sense resistor is above the VSENSEtrip threshold. To reset the fault the EN or PWM pin must be pulled low for 32k clock cycles.	OFF	OFF	OFF
Secondary OVP	Latched	Always	YES	Secondary overvoltage protection is used for open diode detection. When diode D1 opens, the SW pin voltage will increase until $V_{OVP(SEC)}$ is reached . This fault latches the IC. The input disconnect switch and LED drivers are disabled. To reset the fault the EN or PWM pin needs to be pulled low for 32k clock cycles.	OFF	OFF	OFF
LEDx Pin Shorted to GND	Auto-restart	Startup	NO	If any of the LED pins is determined to be shorted to GND when PWM first goes high, soft-start process is halted. Only when the short is removed, then soft-start is allowed to proceed.	OFF	ON	OFF
LEDx Pin Open	Auto-restart	Normal operation	NO	If an LED string is not getting enough current, the device will first response by increasing the output voltage until OVP is reached. Any LED string that is still not in regulation will be disabled. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level.	ON	ON	OFF for open pins. ON for all others.
ISET Short Protection	Auto-restart	Always	NO	Fault occurs when the ISET current goes above 150% of max current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to regulate to the preset LED current.	OFF	ON	OFF
FSET/SYNC Short Protection	Auto-restart	Always	YES	Fault occurs when the FSET current goes above 150% of max current. The boost will stop switching, Disconnect switch will turn off and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to restart with soft-start.	OFF	OFF	OFF
Overvoltage Protection	Auto-restart	Always	NO	Fault occurs when current into OVP pin exceeds $i_{OVP(th)}$ (typically 150 µA). The IC will immediately stop switching but keep the LED drivers active, to drain down the output voltage. Once the output voltage decreases to ~94% OVP level, the IC will restart switching to regulate the output current.	STOP during OVP event.	ON	ON
Undervoltage Protection	Auto-restart	Always	YES	Device immediately shuts off boost and current sinks if the voltage at VOUT is below $V_{UVP(th)}$. This may happen if VOUT is shorted to GND, or boost diode is open before startup. It will auto-restart once the fault is removed.	OFF	ON	OFF
LED String Partial Short Detection	Auto-restart	Always	NO	Fault occurs if an LED pin voltage exceeds V_{LEDSC} with its current sink in regulation, while at least one other LED pin is below ~1.2 V. This may happen when two or more LEDs are shorted within a string. The LED string exceeding the threshold will then be disabled and removed from operation. Device will re-enable the LED string when its pin voltage falls below threshold, or at the next PWM = H.	ON	ON	OFF for shorted string. ON for all others.
Overtemperature Protection	Auto-restart	Always	YES	Fault occurs when the die temperature exceeds the over-temperature threshold, typically 170°C. IC will restart after temperatures drops lower by T_{SDHYS}	OFF	OFF	OFF
VIN UVLO	Auto-restart	Always	NO	Fault occurs when VIN drops below VUVLO(fall), which is 3.9V max. This fault resets all latched faults.	OFF	OFF	OFF

Fault Recovery Mechanism



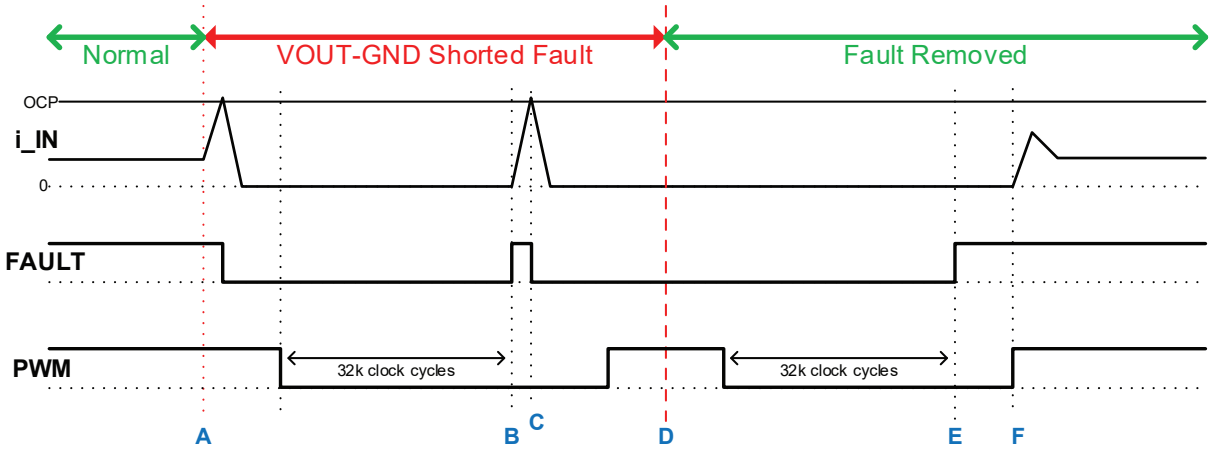
* Note: Fault conditions may be detected in any state or during any state transition. Most faults are non-latching, meaning the IC will auto-restart as soon as the fault is removed. Only the following faults are latching:

Input Disconnect Overcurrent, SW Secondary OCP, and SW Secondary OVP.

Latching faults can only be cleared by:

1. Reset the IC by bring VIN below UVLO,
2. Reset the IC by bring EN=L for >32k cycles, or
3. EN=H and PWM=L for >32k cycles.

The last method has the advantage that it does not interrupt the CLKOUT signal. In case the fault condition (e.g. VOUT shorted to GND) is still present when the latching fault is cleared by PWM=L for >32k cycles, the IC will trip fault once again and stay latched off.



Explanation of events:
A: VOUT-to-GND Short fault introduced. IC trips input OCP which is a latched fault. FAULT is then pulled Low and IC stays in Latched mode (CLKOUT remains available).
B: After PWM=L for 32k cycles, IC clears the latched fault so FAULT goes High
C: Input OCP is tripped again since VOUT is still shorted to GND. So FAULT is pulled Low again and IC returns to Latched mode.
D: PWM=H and VOUT-to-GND Short fault is removed, but IC cannot startup since it is still in Latched mode.
E: After PWM=L for 32k cycles, IC clears the latched fault so FAULT goes High
F: IC restarts at the next PWM=H and resumes normal operation

Figure 43: Timing Diagram to show how to clear Latched Fault with PWM = L

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
Reference Allegro DWG-2871 (Rev. A) or JEDEC MO-220WGGD.
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.

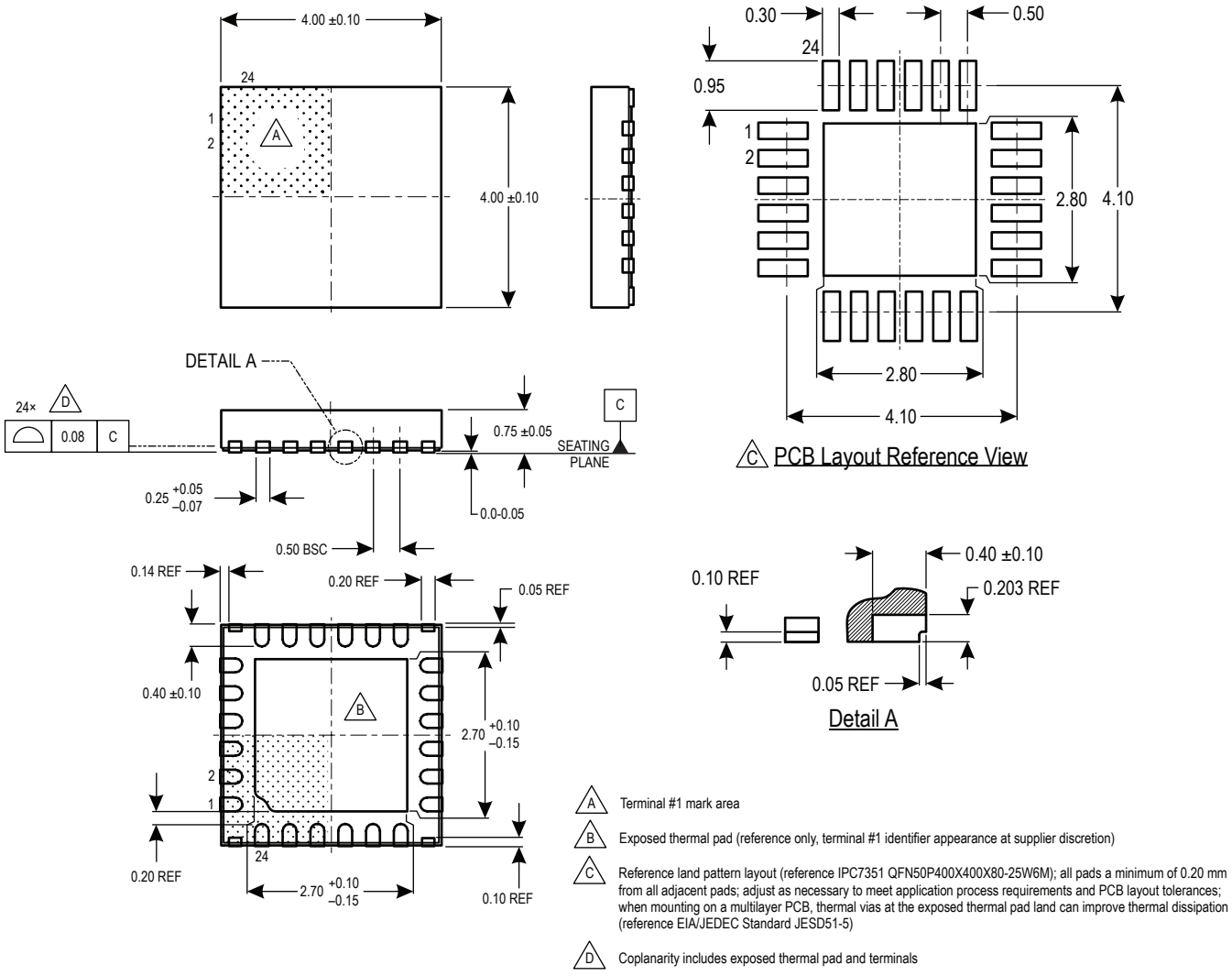


Figure 44: Package ES, 24-Pin 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank

APPENDIX A: DESIGN EXAMPLE

This section provides step-by-step instructions to select component values for an ALT80600 application.

For the purposes of this example, the following operating conditions are assumed:

- V_{IN} = 12 V nominal (6 V min, 18 V max)
- Number of LED channels: nc = 4
- Number of series LEDs per channel: n = 8
- LED current per channel: I_{LED} = 100 mA
- LED forward drop: V_f = 3.2 V max at cold
- Switching frequency: f_{SW} = 2.15 MHz
- Dithering modulation frequency: f_{DITH} = 1 kHz
- Dithering frequency range: Δf_{SW} = ±5%
- Max Ambient temperature: $T_{A(max)}$ = 65°C
- PWM dimming frequency: f_{PWM} = 200 Hz

Step 1: Program the Switching Frequency from equation 1:

$$f_{SW} = 21.5 / (R_{FSET} + 0.2)$$

therefore

$$R_{FSET} - 0.2 = 21.5 / f_{SW}$$

where f_{SW} is in MHz and R_{FSET} is in kΩ.

Substitute f_{SW} = 2.15 MHz to get R_{FSET} = 9.8 kΩ (pick 10 kΩ).

Step 1a: Program the Dithering Modulation Frequency from equation 2:

$$f_{DITH}\,(\text{kHz}) = 25 / C_{DITH}\,(\text{nF})\ .$$

Substitute f_{DITH} = 1 kHz to get C_{DITH} = 25 nF (pick 22 nF).

Step 1b: Select Dithering Range from equation 3:

$$\Delta f_{SW}\ \text{Range}\ (\pm\%) = 20 \times R_{FSET} / R_{DITH}$$

Substitute Δf_{SW} Range = 5 and R_{FSET} = 10 kΩ to get R_{DITH} = 40 kΩ (pick 40.2 kΩ). The switching frequency now linearly sweeps between 2.04 and 2.26 MHz.

Step 2: Determine the LED current set Resistor R_{ISET} from equation 4:

$$R_{ISET} = (V_{ISET} \times A_{ISET}) / I_{LED}\ .$$

Substitute V_{ISET} = 1 V, A_{ISET} = 833, and I_{LED} = 100 mA to get R_{ISET} = 8.33 kΩ (pick 8.25 kΩ).

Step 3: Determining the OVP resistor according to equation 6:

$$R_{OVP} = (V_{OVP} - V_{OVP(th)}) / i_{OVP(th)}\ .$$

The nominal output voltage is:

$$V_{OUT\_nom} = n \times V_f + V_{REG}$$

where V_{REG} is the LED pin regulation voltage. Substitute n = 8, V_f = 3.2 V, and V_{REG} = 0.8 V to get V_{OUT_nom} = 26.4 V.

Set the OVP threshold voltage approximately 10% higher to account for error margin and component tolerances:

$$V_{OVP} = V_{OUT\_nom} \times 1.1 = 29\ \text{V}\ .$$

The OVP resistor is therefore:

$$R_{OVP} = (29\ \text{V} - 2.5\ \text{V}) / 150\ \mu\text{A}$$

$$= 177\ \text{k}\Omega\ (\text{pick}\ 178\ \text{k}\Omega)\ .$$

Step 3a: Check to ensure the maximum boost duty cycle is sufficient to achieve the required conversion ratio.

$$D_{MAX(boost)} = 1 - t_{SW(off)} \times f_{SW(max)}$$

where $t_{SW(off)}$ is the worst-case minimum SW on-time, $f_{SW(max)}$ is the maximum switching frequency with dithering.

Substitute $t_{SW(off)}$ = 85 ns and $f_{SW(max)}$ = 2.26 MHz to get $D_{MAX(boost)}$ = 0.808.

Theoretical maximum output voltage at the lowest input voltage is:

$$V_{OUT(max)} = V_{IN(min)} / (1 - D_{MAX(boost)}) - V_D$$

where V_D is the forward drop of boost Schottky diode.

Substitute $V_{IN(min)}$ = 6 V, $D_{MAX(boost)}$ = 0.808, and V_D = 0.4 V to get $V_{OUT(max)}$ = 30.8 V.

Theoretical $V_{OUT(max)}$ has to be greater than V_{OVP}. If this is not the case, then switching frequency of the boost converter must be reduced to meet the maximum duty cycle requirement.

Step 4: Inductor selection.

The inductor needs to be chosen based on ripple current requirement. In most applications due to stringent EMI requirements, the system also needs to operate in continuous conduction mode (CCM) throughout the whole input voltage range. A simple guideline is to start with 30% peak-to-peak ripple current at nominal input and output voltages.

Step 4a: Determine the Boost Duty Cycle

$$D = 1 - V_{IN} / (V_{OUT} + V_D) .$$

For nominal operation, substitute V_{IN_nom} = 12 V, V_{OUT_nom} = 26.4 V, and V_D = 0.4 V to get D_{nom} = 0.552.

Step 4b: Calculate the nominal Input Current based on estimated efficiency:

$$i_{IN} = V_{OUT} \times i_{OUT} / (V_{IN} \times \eta)$$

where η = efficiency of the converter (typically in the 85-90% range).

For nominal operation, substitute V_{OUT} = 26.4 V, i_{OUT} = 0.4 A, V_{IN} = 12 V, and η = 0.9 to get i_{IN} = 0.98 A.

Step 4c: Select Boost Inductance based on 30% Ripple Current.

For nominal operation, $\Delta i_L = 0.3 \times i_{IN}$ = 0.29 A.

$$\Delta i_L = t_{ON} \times V_{IN} / L = D \times V_{IN} / (f_{SW} \times L)$$

therefore

$$L = D \times V_{IN} / (f_{SW} \times \Delta i_L) .$$

Substitute D_{nom} = 0.552, V_{IN_nom} = 12 V, and f_{SW} = 2.15 MHz to get L = 10.6 µH (pick 10 µH).

STEP 4d: Determine the maximum and minimum input current to the system. The maximum current determines the inductor's saturation current rating. The minimum current determines its critical inductance.

Maximum input current occurs at minimum V_{IN} and maximum V_{OUT} (OVP).

$$i_{IN\_max} = V_{OVP} \times i_{OUT} / (V_{IN\_min} \times \eta) .$$

Substitute V_{OVP} = 29 V, V_{IN_min} = 6 V, and η = 0.85 to get i_{IN_max} = 2.27 A.

Peak inductor current:

$$i_{L\_peak} = i_{IN\_max} + \Delta i_L / 2 .$$

At minimum V_{IN} = 6 V, D = 0.796, Δi_L = 0.22 A, and so i_{L_peak} = 2.27 + 0.22/2 = 2.38 A. Therefore the inductor should have a saturation current of at least 2.5 A.

Minimum input current occurs at maximum V_{IN} and nominal V_{OUT}:

$$i_{IN\_min} = V_{OUT\_nom} \times i_{OUT} / (V_{IN\_max} \times \eta) .$$

Substitute V_{OUT_nom} = 26.4 V, V_{IN_max} = 18 V, and η = 0.9 to get i_{IN_min} = 0.652 A.

At maximum V_{IN} = 18 V, D = 0.328, Δi_L = 0.275 A, and so i_{L_valley} = 0.652 – 0.275/2 = 0.51 A. Therefore, the converter operates in CCM throughout the input voltage range.

Step 5: To verify that there is sufficient slope compensation for the inductor chosen, the ALT80600 generates a variable internal Slope Comp (*SC*) according to f_{SW} and V_{IN}.

- If V_{IN} is between 9 V and 15 V:
  $SC = 3 \times f_{SW} \times V_{IN} / 12$
- If $V_{IN} < 9$ V:
  $SC = 3 \times f_{SW} \times 9 / 12$
- If $V_{IN} > 15$ V:
  $SC = 3 \times f_{SW} \times 15 / 12$

where f_{SW} is in MHz and *SC* is in A/µs.

At f_{SW} = 2.15 MHz and V_{IN} = 6 V, for example, then *SC* = 4.74 A/µs.

The falling slope of inductor current is given as:

$$di_L/dt = -\Delta i_L / t_{OFF} = -\Delta i_L \times f_{SW} / (1 - D)$$

Based on equations from previous section, at V_{IN} = 6 V and $V_{OUT(OVP)}$ = 29 V, then D = 0.796 and Δi_L = 0.22 A.

Therefore $| di_L/dt |$ = 2.32 A/µs, which is slower than the internal slope. That means there is sufficient slope compensation.

In case the negative slope of inductor current is faster than the internal slope comp, a higher inductance value must be used.

Step 6: Select the switching diode.

A Schottky barrier diode (SBD) is typically selected based on its voltage and current ratings:

- The reverse voltage rating must be higher than the maximum voltage stress, which is equal to the OVP threshold in this case.

The average forward current rating must be higher than the total LED current. The peak current through diode is given as:

$$i_{D\_peak} = i_{L\_peak} = i_{IN\_max} + \Delta i_L / 2$$

From previous calculation at minimum V_{IN}, i_{L_peak} = 2.38 A. However, during transient this current could reach cycle-by-cycle SW current limit, $i_{SW(LIM)}$.

Another critical parameter is the diode's reverse leakage current at hot. This is especially important when using PWM dimming.

During PWM off time, the boost converter is not switching, so voltage at output capacitor decays due to leakage current. This increases output ripple voltage, which may generate audible noise from ceramic capacitors.

Make sure to verify the diode's reverse current at hot (such as 125°C) and at the nominal V_{OUT}. As a general guideline, look for a diode with leakage of 100 µA or less. If necessary, consider using a diode with higher voltage rating (such as 100 V instead of 50 V). Doing so can significantly reduce the leakage current at nominal V_{OUT}.

For this design example, a 100 V, 2 A Schottky diode SS2PH9 is selected. It has a very low i_R = 100 µA at T_J = 150°C and V_R = 30 V.

Step 7: Selection of output capacitors.

The use of multilayer ceramic capacitor (MLCC) is recommend. MLCC has extremely low ESR, which is necessary to reduce output switching ripple for boost converter. In addition, the total output capacitance needs to be sufficient to reduce output droop during PWM dimming operation.

The biggest contributing factors for total output capacitance are PWM off-time and leakage current (i_{LK}). This current is mainly due to the reverse current of switching diode, plus a small/negligible leakage current into the OVP pin.

In this design example, the PWM dimming frequency is 200 Hz with minimum duty cycle of 0.01%. So the maximum PWM off-time is essentially t_{OFF} = 5 ms. A typical goal is to keep the output voltage variation at 250 mV or less, so that no audible hum can be heard.

$$\Delta V_{OUT} = t_{OFF} \times i_{LK} / C_{OUT}$$

therefore

$$C_{OUT} = t_{OFF} \times i_{LK} / \Delta V_{OUT} .$$

Substitute t_{OFF} = 5 ms, i_{LK} =110 µA, and ΔV_{OUT} = 0.25 V to get C_{OUT} = 2.2 µF.

A major problem with multilayer ceramic capacitor (MLCC) is that its actual capacitance drops with respect to DC bias. For example, the capacitance of a 4.7 µF, 50 V, 0805 MLCC may be derated by 80% when it is biased at 25 V. That means its real capacity is less than 1 µF in actual application.

MLCC with larger physical size and higher voltage rating typically suffers less derating problem. For example, a 4.7 µF, 50 V, 1210 MLCC may retain 3.3 µF of capacitance at 25 V. This is shown in the table below:

Part#	Package	Rated C at 0 V (µF)	Derating at 25 V	Actual C at 25 V (µF)
GRM21BC71H475KE11	0805	4.7	–80%	0.94
GRM31CR71H475MA12	1206	4.7	–45%	2.59
GRM32ER71H475KA88	1210	4.7	–30%	3.29

Step 8: Selection of input capacitor.

A combination of MLCC and electrolytic capacitor is recommended. The MLCC provides low ESR to reduce input switching ripple. The electrolytic capacitor provides larger capacitance to stabilize input voltage during PWM dimming operation.

A good rule of thumb is to set the input voltage ripple ΔV_{IN} to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows.

$$C_{IN} = \Delta i_L / (8 \times f_{SW} \times \Delta V_{IN}) .$$

Substitute Δi_L = 0.22 A at V_{IN} = 6 V (from step 4b) and f_{SW} = 2.15 MHz to get C_{IN} = 0.21 µF. Due to the DC bias derating, the actual MLCC selected should be rated 1 µF or higher.

A much larger input capacitance is required to provide the inrush current during PWM dimming operation. The exact requirement depends on many external factors, such as length of power cables and response time of the power supply. As a first-order estimate: assuming the power supply takes 25 µs to response, and the input capacitor must keep the V_{IN} drip under 0.2 V while input current ramps up from zero to full load. Therefore the following is needed:

$$C_{IN} = i_{IN} \times t_{PS} / (8 \times \Delta V_{IN}) .$$

Substitute i_{IN} = 2.27 A at V_{IN} = 6 V (from step 4b) and t_{PS} = 25 µs to get C_{IN} = 36 µF. Use an electrolytic capacitor of 33 µF or 47 µF in parallel with the MLCC.

Step 9: Choosing the input disconnect switch components.

Set the input disconnect current limit to 4 A. From equation 7:

$$R_{SC} = V_{SENSETRIP} / i_{SENSE} = 25 \text{ m}\Omega$$

Pick the closest lower resistance value from E-24 series, which is 24 mΩ.

From equation 8:

$$R_{ADJ} = [V_{SENSETRIP} - (R_{SC} \times i_{SENSE})] / i_{ADJ}$$
$$= 200 \ \Omega$$

The following schematic diagram shows calculated values from the design example:

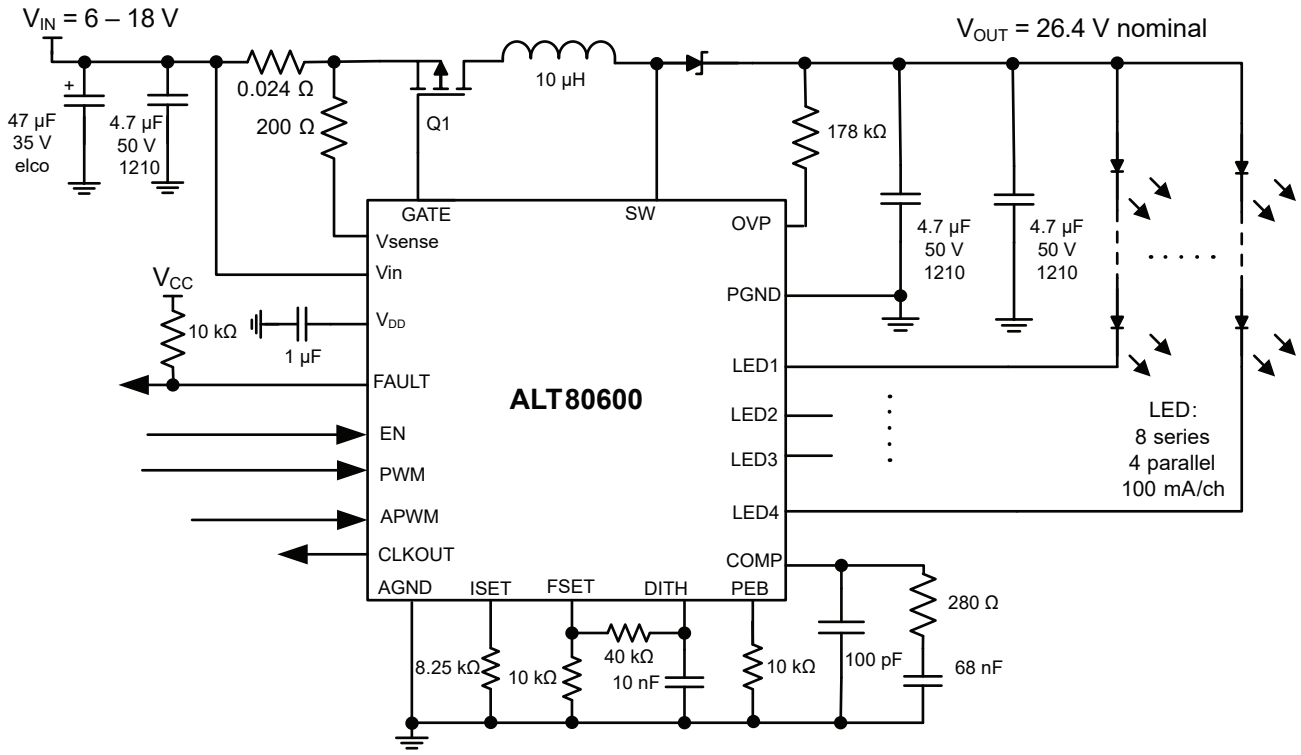


Figure 45: ALT80600 Design Example Schematic

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	March 20, 2018	Initial release
1	November 9, 2018	Corrected reel quantity in Selection Guide (page 2); added Appendix A.
2	March 13, 2019	Updated Synchronization section (page 13)