ATH3100
Product Overview

Desktop Speakerphone IC

"Driving Speakerphone Sound Quality"

Enabled with SoundClear®

PRELIMINARY INFORMATION

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Version 1.0

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1 Features

- Full-Duplex Desktop Speakerphone Controller
- Integrated Dual 16-bit A/Ds-D/As, Sigma-Delta, ADC >80dB SNR, DAC >70dB SNR
- Acoustic Echo Cancellation up to 65dB, 64 ms echo tail
- Noise Cancellation up to 18dB
- Bi-Directional Noise Reduction
- Network Echo Cancellation up to 45dB, 16 ms echo tail
- Sound Enhancement with integrated Bi-Directional 10-band Graphic Equalizers
- Supports Handset & Speakerphone Audio Paths
- Integrated Caller-ID Demodulator – Type I and Type II
- Programmable Polyphonic Ring Tone Generator
- Integrated Programmable DTMF Tone Generation
- Call-State Processor for Talk-Mode Management
- Comfort Noise Generation for natural sounding conversation flow
- Full Featured Analog Audio with Differential Interfaces and Integrated Dual Codecs
  - Programmable Input Amplifiers and Output Drivers with Fully Differential Signaling
  - Two, integrated 20mW 100Ω speaker buffers
  - Multiplexed Dual Microphone Interface with Integrated Pre-Amp
  - Analog Line-In Interface
  - Analog Line-Out Interface – 600Ω differential driver
  - Dynamic Gain Control for Microphone and Line-Inputs
- Close microphone to speaker minimum distance (4cm)
- Independent Digital PCM interface
  - At all four input & output audio ports (4 or 6 wire)
  - Supports time-shared and point-to-point PCM
  - Programmable for IOM-2, SSI, STBus, GCI
- G.711/712 compliant filtering for both Tx/Rx channels ('Telco' filtering)
- Two-wire Serial Microprocessor interface for monitoring, tuning registers, and control
- Easy-to-use eXcho™ GUI for rapid system tuning
- Integrated Power Management Features (suspend, sleep, and coma)
- Single clock or crystal source (8.192MHz)
- Available in 48-pin LQFP or QFN package (green packaging - RoHS)
- Supports Single Voltage Supply Operation VDD = 2.7 to 3.6V
  - Integrated 3.3V to 1.8V low voltage regulator for digital core
- Low power consumption
- -40°C to + 85°C Operating Temperature Range

2 Description

The ATH3100 is Acoustic Technologies new full-duplex speakerphone integrated circuit offering improved voice clarity through the SoundClear® proprietary combination of technologies: Acoustic Echo Cancellation, Noise Cancellation, Sound Enhancement, and Network Echo Cancellation. Device integrates monitoring and control with call-state processors, noise management and equalizers to ensure clear and natural two-way communication. This device builds on our patented core full-duplex echo cancellation, noise cancellation, and sound enhancement technology with added features and enhanced functionality for improving the audio quality and providing phone management capabilities for VoIP, digital PBX, and standard PSTN telephony terminals.

The ATH3100 includes four analog audio interface ports (Line-In, Line-Out, Mic-In, and Speaker-Out), microphone pre-amplification and speaker output drivers. A serial digital PCM interface is additionally available at each of the four audio ports for ease of integration to digital-based telephony system. DTMF and ringer tone generation round out the added features.

Programmable configuration control and system level tuning from a host processor is via a 2-wire serial interface. The ATH3100 utilizes several unique features including call-state processing control, multiple voice activity detection circuits, and network and acoustic digital adaptive echo cancellation filters which combine to cancel echo even during double talk, noise, and changing environments. This integrated combination of techniques results in a highly optimized audio solution that provides natural sounding two-way communications for desktop speakerphone applications.

The on-board programmable gain and performance registers allow the user to tune the performance of the audio system based on customer specific criteria and preferences. Integrated pre-amplification on the line and microphone inputs as well as a line-out driver and low power speaker buffers make the ATH3100 a powerful solution for telephony and loud speaking audio systems. Integrated control processors, noise management and graphic equalizers ensure clear and crisp two-way communication. The ATH3100 supports both handset and speakerphone audio modes and phone management including desktop telephone features such as Caller-ID demodulation, DTMF generation, and ring tone generation.

Target applications for the ATH3100 device include SOHO Speakerphones, Desktop Speakerphones, PBX Phones, and VoIP Speakerphones. For faster time to market, please contact Acoustic Technologies for a mini stitch board evaluation kit including a sample board with the ATH3100, board schematics, tuning tools and coding examples.

3 Package and Pin Description

Figure 1: ATH3100 48-Pin LQFP Package Pin Diagram

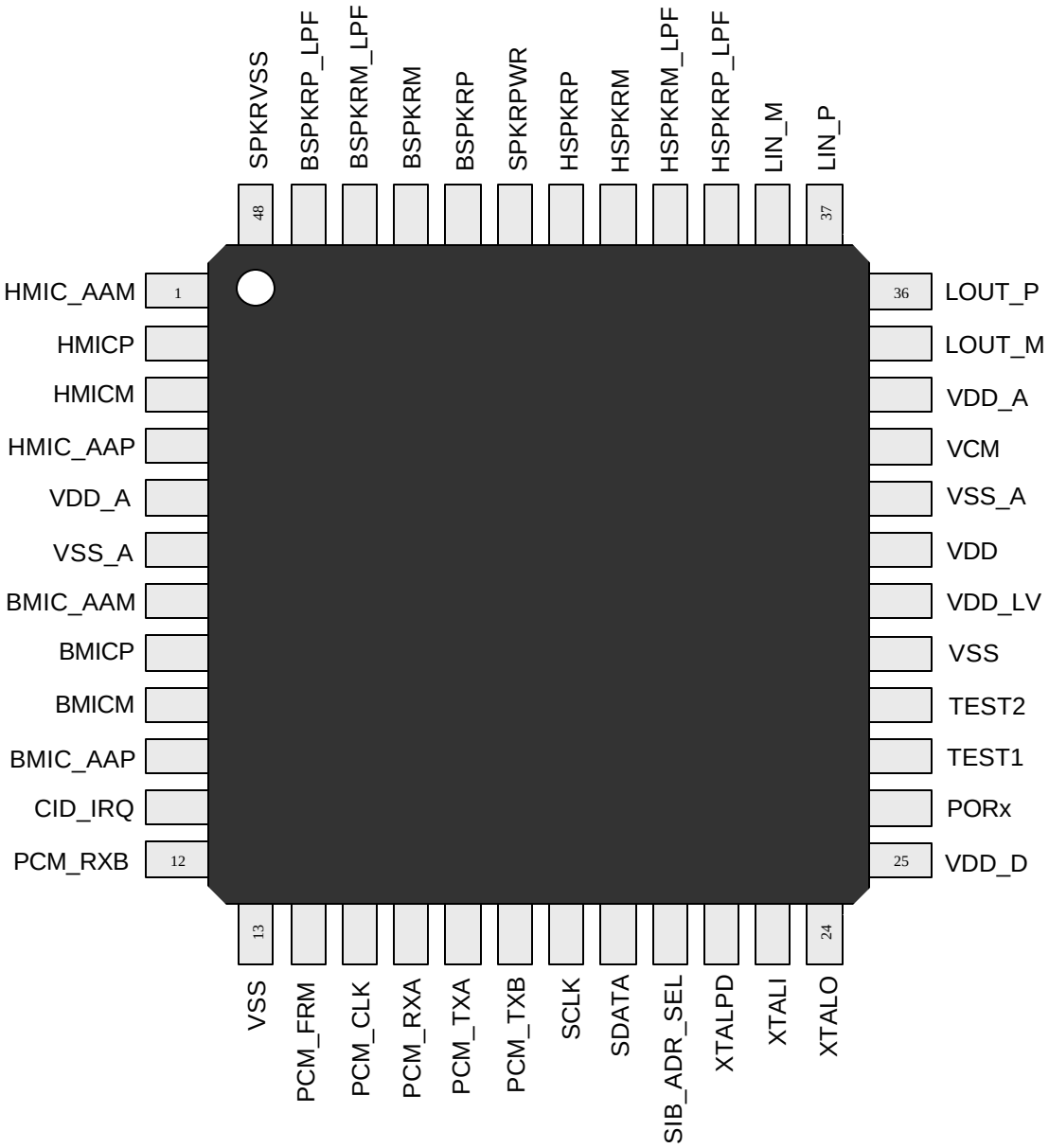
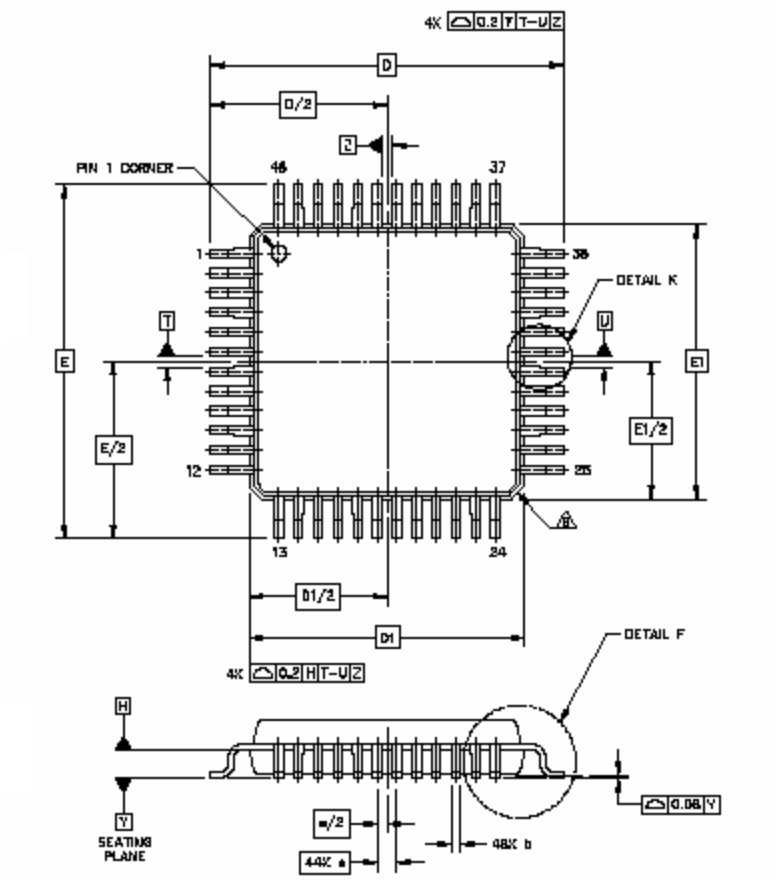
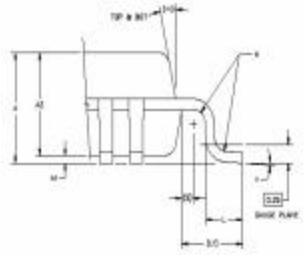


Figure 2: ATH3100 48-Pin LQFP Package Outline Diagram (dimensions are in millimeters)

Top View

Side View





DIM	MIN	MAX	DIM	MIN	MAX
A	1.4	1.6	L1	1 REF	
A1	0.05	0.15	R	0.15	0.25
A2	1.35	1.45	S	0.2 REF	
b	0.17	0.27	θ	1°	5°
b1	0.17	0.23	θ1	12° REF	
c	0.09	0.2			
c1	0.09	0.16			
D	9 BSC				
D1	7 BSC				
e	0.5 BSC				
E	9 BSC				
E1	7 BSC				
L	0.5	0.7			

Table 1: Signal Reference Table

Pin #	Signal Name	Signal Type	Short Signal Description
1	HMIC_AAM	Analog Output	- Output for HS Mic-In 2-pole LPF anti-alias feedback network
2	HMICP	Analog Input	+ Input for HS microphone differential input
3	HMICM	Analog Input	- Input for HS microphone differential input
4	HMIC_AAP	Analog Output	+ Output for HS Mic-In 2-pole LPF anti-alias feedback network
5	VDD_A	Analog PWR	Analog Power Rail = 2.7-3.6V
6	VSS_A	Analog GND	Analog Ground Rail
7	BMIC_AAM	Analog Output	- Output for base Mic-In 2-pole LPF anti-alias feedback network
8	BMICP	Analog Input	+ Input for base microphone differential input
9	BMICM	Analog Input	- Input for base microphone differential input
10	BMIC_AAP	Analog Output	+ Output for base Mic-In 2-pole LPF anti-alias feedback network
11	CID_IRQ	Digital I/O	Caller ID Interrupt Output
12	PCM_RXB	Digital Input	Digital PCM Rx serial receive port B
13	VSS	Digital GND	Digital Ground for I/O
14	PCM_FRM	Digital I/O	8kHz Frame Sync signal for PCM Interface
15	PCM_CLK	Digital I/O	PCM Interface Bit Rate Clock
16	PCM_RXA	Digital Input	Digital PCM Rx serial receive port A
17	PCM_TXA	Digital Output	Digital PCM Tx serial send port A
18	PCM_TXB	Digital Output	Digital PCM Tx serial send port B
19	SCLK	Digital Input	Serial Clock for microprocessor interface
20	SDATA	Digital I/O	Serial Bi-directional data-port for microprocessor interface
21	SIB_ADR_SEL	Digital Input	Serial port ‘slave’ address configuration pin
22	XTALPD	Digital Input	Gates Crystal Oscillator off - invoking lowest power coma mode
23	XTALI	Digital Input	System Clock/Crystal Oscillator input 8.192MHz
24	XTALO	Digital Output	Crystal Oscillator output (N/C if using a clock source on XTALI)
25	VDD_D	Digital PWR	Digital I/O Power Rail = 2.7-3.6V
26	PORx	Digital Input	Chip Reset (active low=0). Hardware full reset (optional use)
27	TEST1	Digital GND	Connect to Digital Ground – Reserved for production test
28	TEST2	Digital GND	Connect to Digital Ground – Reserved for production test
29	VSS	Digital GND	Digital Ground for core and I/O
30	VDD_LV	Digital PWR	LV 1.8V power from on-board regulator, requires decoupling capacitor
31	VDD	Digital PWR	Digital Power Rail and voltage regulator circuits = 2.7-3.6V
32	VSS_A	Analog GND	Analog Ground
33	VCM	Analog	Analog common mode ground reference, requires

		Output	decoupling
34	VDD_A	Analog PWR	Analog Power Rail = 2.7-3.6V
35	LOUT_M	Analog Output	- Output for Line-Out (2.0 Vp-p max into 600Ω)
36	LOUT_P	Analog Output	+ Output for Line-Out (2.0 Vp-p max into 600Ω)
37	LIN_P	Analog Input	+ Input for Line-In input
38	LIN_M	Analog Input	- Input for Line-In input
39	HSPKRP_LPF	Analog Output	+ Output for handset speaker LPF feedback RC network
40	HSPKRM_LPF	Analog Output	- Output for handset speaker LPF feedback RC network
41	HSPKRM	Analog Output	- Output for handset speaker (2.0 Vp-p max into 100Ω)
42	HSPKRP	Analog Output	+ Output for handset speaker (2.0 Vp-p max into 100Ω)
43	SPKRPWR	Analog PWR	Speaker amplifier Power = 2.7-3.6V
44	BSPKRP	Analog Output	+ Output for base speaker (2.0 Vp-p max into 100Ω)
45	BSPKRM	Analog Output	- Output for base speaker (2.0 Vp-p max into 100Ω)
46	BSPKRM_LPF	Analog Output	- Output for base speaker LPF feedback RC network
47	BSPKRP_LPF	Analog Output	+ Output for base speaker LPF feedback RC network
48	SPKRVSS	Analog GND	Speaker amplifier Ground

4 ATH3100 Diagrams

Figure 3: Top Level ATH3100 Block Diagram

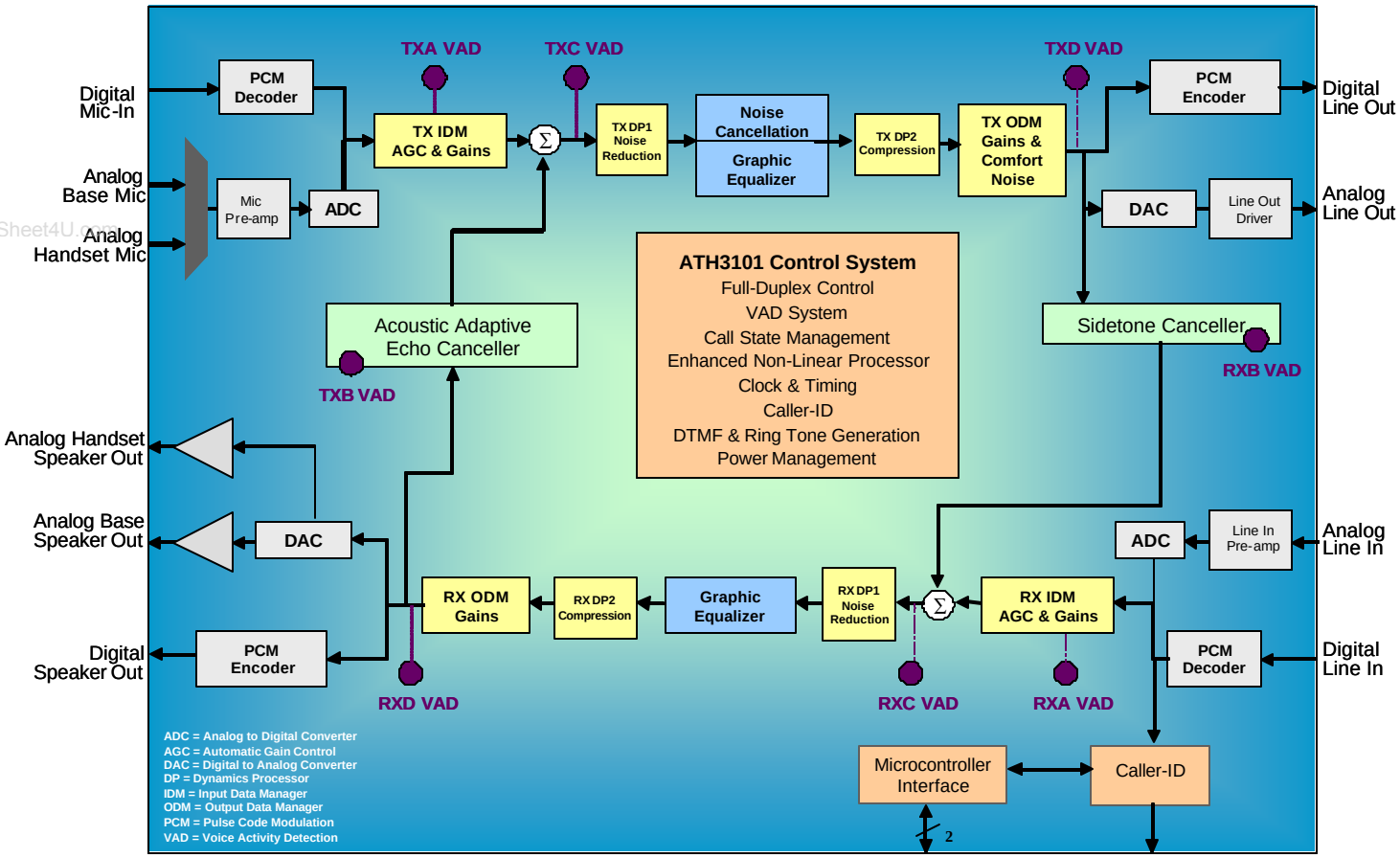


Figure 4: ATH3100 Desktop Speakerphone Application Diagram

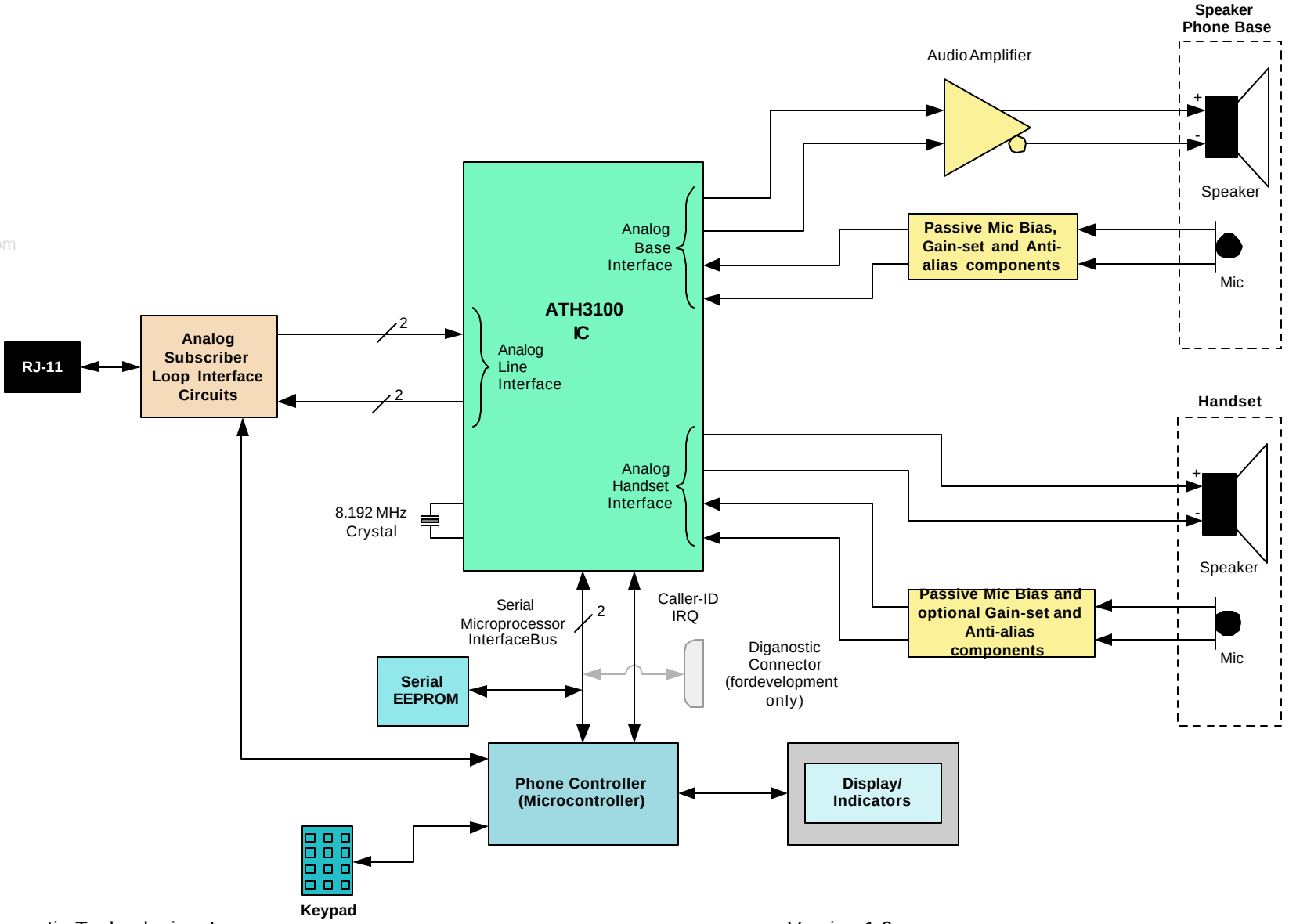
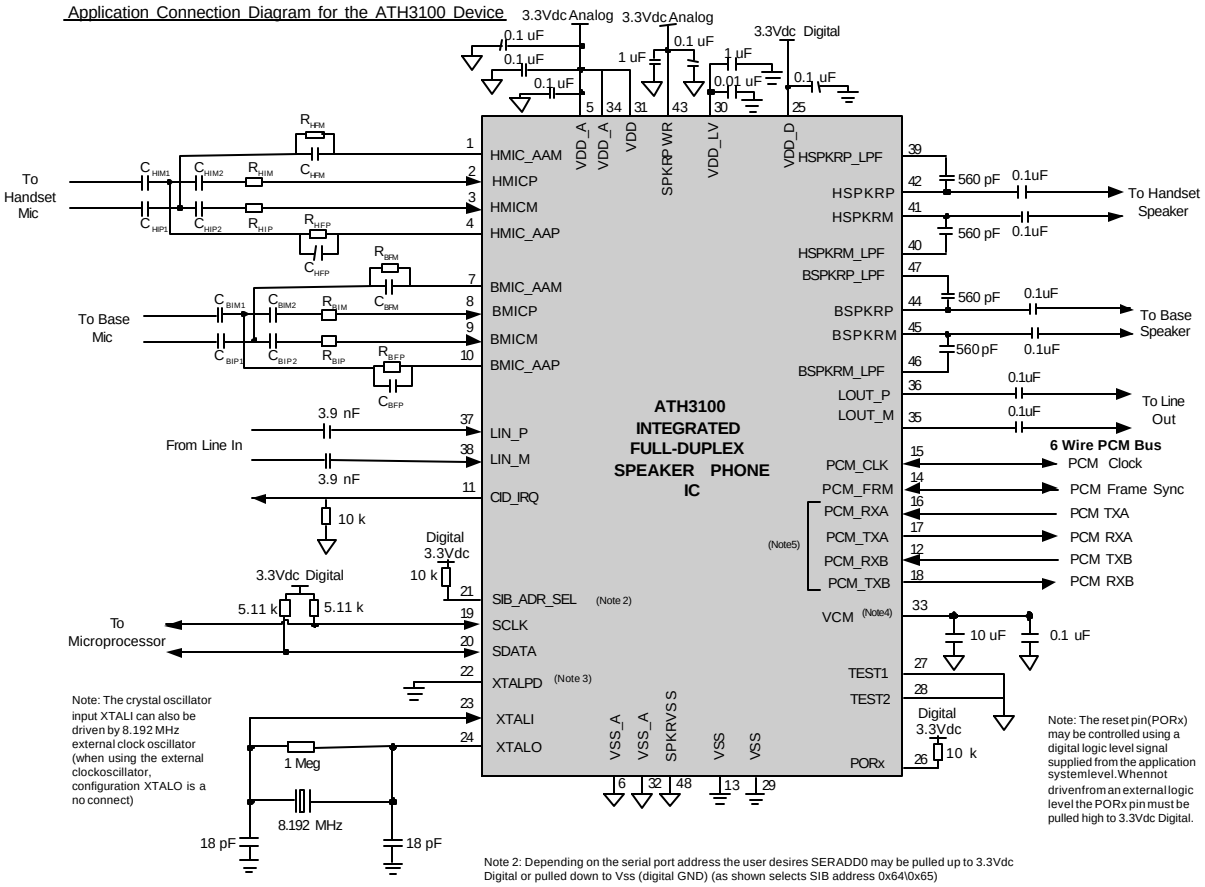


Figure 5: ATH3100 Connection Diagram



Note 2: Depending on the serial port address the user desires SERADD0 may be pulled up to 3.3Vdc Digital or pulled down to Vss (digital GND) (as shown selects SIB address 0x64\0x65)

Note 3: The clock stop pin (XTALPD) may be controlled using a digital logic level signal supplied from the application system. When not using the clock stop feature this pin should be pulled low to Vss (digitalGND).

Note 4: VCM (Voltage, Common Mode) may be buffered and supplied to external circuitry that may need a common mode voltage reference.

Note 5: Add 5.11K resistors to all PCM Tx and Rx pins and pullup to +3.3Vdc Digital.

5 Functional Description

The ATH3100 is an integrated mixed-signal system on a chip (SoC) that incorporates analog and digital interfaces, control logic, and signal processing functions to provide full-duplex voice communication in speakerphone-enabled telephones. The ATH3100 integrates acoustic and network echo reduction, noise cancellation, and several sound enhancement features. Both analog audio connections and a serial digital PCM bus are provided for flexible interfacing to the Line-In, Mic-In, Line-Out, and Speaker-Out signal paths. A programmable serial microprocessor interface is included for system configuration and applications level control.

Acoustic Technologies' full-duplex monitor and control system provides continual on-chip adaptation and adjustment to provide optimal sound quality at all times. The ATH3100's call state processor provides fast and seamless transitions to maintain natural communication and conversation. The ATH3100 also includes integrated call management with speakerphone and handset mode control. Applying the unique SoundClear combination of audio processing techniques results in optimal voice clarity and superior full-duplex speakerphone operation. This highly integrated full-duplex speakerphone IC is provided in a small footprint 48-pin LQFP package and operates with a low power consumption of typical 70mW (including internal regulator and oscillator). The ATH3100 integrates internal regulator circuits to support operation from a single 3.3 volt supply, if desired.

5.1 Top Level Control

The ATH3100 includes sophisticated mode management and control with a call-state processor, multiple Voice Activity Detection (VAD) blocks for continual monitoring of speech and noise levels.

Several Voice Activity Detection (VAD) circuits are used in the audio paths to ensure reliable detection of voice during all operating modes. The VADs continually monitor voice activity and noise levels to decode the call states, and to control the backend suppression control engines, which optimizes the echo canceller performance.

5.2 Analog Interfaces and Processing Blocks

The ATH3100 has integrated analog circuitry for all four audio interfaces (Line-In, Line-Out, Mic-In, and Speaker-Out) as well as a complimentary digital PCM interface applicable for speakerphone and handset telephony applications. The analog interfaces consist of on-chip voice-band ADC/DAC CODECs, anti-aliasing filters, and low noise microphone pre-amplification.

- Line-In Interface
  - Continuous-time Low Noise Amplifier (LNA)
  - Fully differential input port
  - Line level support
  - 256x over-sampled 16-bit Sigma-Delta ADC
  - SNR > 80dB and 13.5 ENOB

- Line-Out Interface
  - 256x over-sampled 16-bit Sigma-Delta DAC
  - DAC accepts a 16-bit 2's complement formatted data-word sampled at 8 kS/s
  - Differential 600Ω capable line driver
  - Driver provides eight user selectable analog gain modes, -21dB to +12dB
  - Line-Out circuits provide analog output signals with > 70 dB SNR and < 0.5% THD

- Microphone Interface
  - Continuous-time, fully differential Low Noise Amplifier (LNA)

- On-chip LPF or externally configurable custom filters and gains with inexpensive passive components
- Microphone level signal support (1mV – 100mV p-p)
- 256x over-sampled 16-bit Sigma-Delta ADC
- Selectable on-chip pre-amplification gain (0dB – 36dB)
- SNR > 80dB and 13.5 ENOB
- Programmable analog sidetone

➢ Speaker-Out Interface
- 256x over-sampled 16-bit Sigma-Delta DAC
- DAC accepts a 16-bit 2's complement formatted data-word sampled at 8 kS/s
- Dual speaker buffers - balanced differential, 20 mW, 100Ω
- DAC/Speaker buffer circuits provide analog output signals with > 70 dB SNR and < 0.5% THD
- Speaker buffer provides eight user selectable output gains from –6dB to +22.9dB

5.3 Power Management Features

The ATH3100 integrates power management features to allow system and application control of the device's power consumption. All of the analog blocks have register control bits for power down mode control if they are not needed by the application. Other top-level power management features are available as register controlled power savings modes – suspend, sleep and coma modes.

5.4 Regulator & References

An on-chip regulator generates the low voltage digital core bias for the ATH3100 allowing for a single 2.7 to 3.6V supply operation. The low voltage regulator pin (30) requires external decoupling. The internal regulator may also be by-passed and a second external voltage supplied for the digital core.

5.5 Clocking Options

The ATH3100 requires a master clock frequency of 8.192 MHz. An external crystal with associated RC network operating at the master clock frequency can be used with the integrated oscillator circuit available on pins XTALI and XTALO. A second option allows supplying an external clock signal directly to the XTALI pin. This option provides a lower power alternative with device power consumption savings.

5.6 Power Consumption

	Internal Oscillator	External Clock
Internal Regulator	70 mW	65 mW
External Regulator	44 mW	39 mW

5.7 Digital Gains

The ATH3100 provides digital gain processing at each of the four internal signal ports (Line-In, Line-Out, Speaker-Out, Mic-In). The digital gain controls can optimize the levels for the maximum dynamic range processing and therefore improve echo cancellation performance.

➢ Input Data Module (IDM)
- Analog to digital dataflow for both Mic-In (Transmit) and Line-In (Receive)
- User programmability of the analog gain elements
- Continuous time gain stage ranging from 0dB to +36dB
- Additional "fine adjustment" in 1.5dB steps ranging from –10.5dB to +12dB

- Dynamic Gain Control function

➢ Output Data Module (ODM)
- Digital to Analog dataflow for both Line-Out (Transmit) and Speaker-Out (Receive)
- ODM controls the various data flow paths and their respective gains
- Continuous time gain stage ranging from 0dB to +18dB
- RX ODM mixes transmit data path to provide optional side tone in handset mode only

5.8 Acoustic and Network Echo Cancellation

Acoustic Technologies' SoundClear Acoustic and Network Echo Cancellation is accomplished using a combination of techniques that include Digital Adaptive Filters and Dynamically Controlled Residual Echo Reduction.

The Adaptive Echo Cancellers (AECs) incorporate Normalized Least Mean Square (NLMS) techniques. The Acoustic AEC cancels echo tails up to 64ms long, ideal for most Business and SOHO offices. The Acoustic AEC provides cancellation while maintaining enhanced robustness to maximize the amount of cancellation.

The Network AEC supplies network echo rejection with a 16ms echo tail, which is required for PSTN speakerphone and handset call implementations using typical line interface electronics.

In addition to the adaptive filters, the device includes residual echo reduction that dynamically attenuates echo signals based on the sophisticated VAD control signals and mode management.

Table 2: ATH3100 Echo Reduction Overview

Total Combined Echo Reduction	
Acoustic	Up to 65 dB
Network	Up to 45 dB

5.9 Comfort Noise Generation and Insertion (CNGI)

Comfort noise generation is a sound enhancement feature used when there is a high level of background noise in conjunction with echo reduction suppression. The residual echo reduction described above has the potential to generate annoying 'pumping' of the background signals. Comfort noise is injected to smooth the talk transitions when call-state changes are detected.

5.10 Noise Cancellation

The ATH3100 includes noise cancellation in the transmit path which is programmable up to 18dB. For quiet background conditions, the noise cancellation can also be disabled if it is not needed. Aggressive noise cancellation may color the voice quality in certain call environments. The noise cancellation is fully programmable to meet the system requirements and customer preferences.

5.11 Dynamics Processor

The ATH3100 includes several blocks called dynamics processors that perform signal compression to minimize peaks and maximize the perceived loudness through the system.

5.12 Graphic Equalizer (GEQ)

The ATH3100 10-band GEQ block functions in both transmit and receive signal paths full-time in speakerphone mode for tuning to specific transducers and product case enclosures. Benefits include

using the GEQ to perform voice enhancement by emphasizing the highs (for voice clarity) and/or lows to improve full duplex speakerphone operation.

5.13 Caller-ID Demodulation

The ATH3100 includes Type I and II Caller-ID demodulation functionality compatible with most telephone systems worldwide. The CID_IRQ pin is a digital interrupt output that will signal the microcontroller to initiate a read sequence of Caller-ID registers within the ATH3100 device.

5.14 DTMF Tone Generation and Ringer Tone Generation

The ATH3100 includes an on-chip digital DTMF Tone Generator and controller. DTMF 'side-tone' mix is available at both the Speaker-Out and Line-Out interfaces. The digital DTMF tone generator allows the user to program and insert comfort tones for PBX based telephony systems as well as implement other user-friendly operations. The levels and durations of the DTMF tones are compliant with ITU recommendations.

The on-chip tone generation processor provides 'ringer' tones for incoming call announcement at the speaker path. A programmable polyphonic tone generator facilitates up to three simultaneous monophonic tones of desired voice-band frequencies. The volume of the individual tones and the mix levels of the composite waveform are programmable, as well as, the 'warble' (i.e. phase and cycle variations) rate between the tones. Eight pre-set tones are available and each is individually programmable and selectable by the user.

5.15 PCM Interface

The ATH3100 supports a four or six-pin serial digital PCM (Pulse Code Modulation) Interface with up to 96 dB Dynamic Range at an 8kHz data rate. The main features of the digital PCM Interface include:

- Dual Tx/Rx PCM Channels
  - Mic-In and Speaker-Out
  - Line-In and Line-Out
- Six pin interface (PCM_TXA, PCM_RXA, PCM_TXB, PCM_RXB, PCM_CLK, PCM_FRM) (i.e. supports both timeshare and point-to-point PCM)
- Programmable expansion/compression including A-law, μ-law, 8-bit linear & 16-bit linear
- The Factory Default mode is GCI (General Communications Interface) μ-law companded
  - PCM_Clk = 2.048 MHz
  - PCM_Frm = 8kHz
- For all other PCM protocols such as SSI, ST-Bus, and IOM-2, please contact the factory for compatibility and register programming information

5.16 Microcontroller Interface

The ATH3100 is equipped with a two-pin read/write Serial Microcontroller Interface. This industry standard slave interface allows an external controller to access the internal registers of the ATH3100, to enable control and monitoring of its operation. This is facilitated by means of a simple protocol performed over the two-wire interface. The features of the Microcontroller Interface include:

- 400kHz Operation
- Two chip I/O pins, SCLK and SDATA
- Compatible with standard interfaces

- Performs reads and writes into the programmable device registers
- Configurable to two addresses in a 7-bit address space based on external Pull-up or Pull-down on the SIB_ADR_SEL pin of the ATH3100 device.

6 Development and Support

Acoustic Technologies has a sample desktop speakerphone design for demonstration. Also, the ATR3100 Evaluation Kit includes a mini stitch board for integrating the device into customer systems for evaluation. In addition, Acoustic provides a ATR3100DT Development Kit which includes documentation and tools needed to finish integration and tuning of the device in end telephony products.

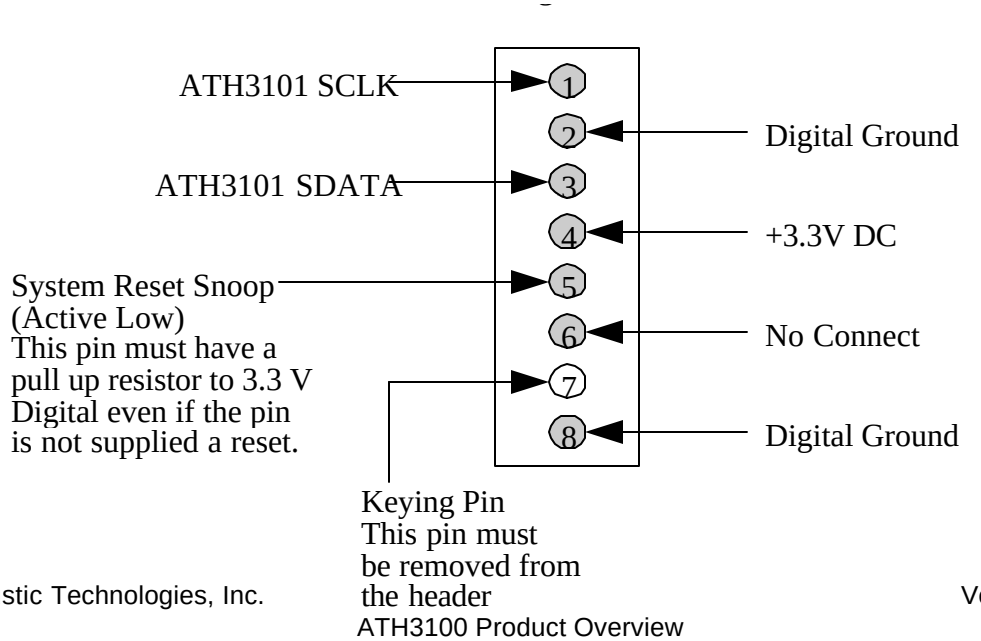
The mini stitch board includes all the components needed in a high quality desktop speakerphone design including a low-cost microcontroller and memory for boot configuration and control. Component count and system cost are minimized with the ATH3100 device's integrated CODECs, telephone management, and advanced I/O ports.

A development and debug port is wired internally to the ATH3100 for connection to Acoustic Technologies' eXcho™ tuning GUI that makes it easy to customize features such as the graphic equalizer, noise cancellation levels, and flexible tuning for customer plastics and transducers.

6.1 Header Required on Boards

To use the eXcho software tools with a customer designed PCB, it is necessary to add an SIB header to the board. The SIB communication interface is described below. This header is an 8 pin 1.25mm mini-connector or a connector with pins spaced 0.100" apart. An example of a header that could be used is the Sullins Electronics Corporation part number PZC08SFBN or equivalent. The header must include connections to the SCLK and SDATA pins of the ATH3101. The header will also need to source +3.3 V DC in order to power the SIB-232 dongle used to communicate between eXcho on the PC and the PCB. A system reset should also be included on the header so eXcho can snoop the reset line. The reset of the SIB-232 dongle is active low and therefore should have a pull up resistor on the line. If reset is not supplied to the header pin, then the pin still must be pulled up with a resistor in order to avoid false reset detections. The SIB-232 dongle header is used for development but is not required for production.

Figure 4: SIB-232 Dongle Header Pin Out



7 Electrical Characteristics

Table 3: Absolute Maximum Ratings

Parameter	*Symbol*	*Min*	*Max*
Analog Power Supply	V_{DD_A}	-0.5V	4.0V
Digital Power Supply	V_{DD}	-0.5V	4.0V
Speaker Buffer Power Supply	$V_{SPKRPWR}$	-0.5V	4.0V
Low Voltage Digital Power Supply	V_{DDLV}	-0.5V	2.2V
Input Voltage – 5V Tolerant Digital I/O (All Except XTALI & RESERVED pins)	V_{IN}	-0.5V	5.5V
Input Voltage – 3V Tolerant for XTALI & RESERVED pins	V_{IN}	-0.5V	4.0V
Output Voltage	V_{OUT}	-0.5V	V_{DD} +0.5V
Output Current	I_O		100mA
Case Temperature Under Bias	T_C	-55ºC	+125ºC
Storage Temperature	T_{STG}	-65ºC	+150ºC

*WARNING: Exceeding these values may cause permanent damage to the device.

The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Operation at these extremes is not recommended or guaranteed.

Table 4: Recommended Operating Conditions

Parameter	*Symbol*	*Min*	*Typ*	*Max*
3v Analog & Regulator Supply Voltage	V_{DD_A} V_{DD_P}	2.7V	3.3V	3.6V
Analog & Regulator Ramp Time (NOTE 1)	t_{PS}			10 ms
3v Digital Supply Voltage	V_{DD_D}	2.7V	3.3V	3.6V
3v Speaker Buffer Supply Voltage	$V_{SPKRPWR}$	2.7V	3.3V	3.6V
Operating Temperature Range (Ambient)	T_{OP}	-40°C		+85°C
ESD	HBM		2000v	
ESD	MM		200v	

NOTE 1: Analog & regulator power pins (VDD_A and VDD_P) must be tied together and must ramp from 10% to 90% within 10 ms. This is subject to change with final characterization of silicon.

8 GLOSSARY

Acoustic Echo: Echo created by signal propagation from a loudspeaker to a microphone

AAEC: Adaptive Acoustic Echo Canceller

ADC: Analog to Digital Converter

ALEC: Adaptive Line Echo Cancller (same as Network Echo Canceller)

CNGI: Comfort Noise Generation and Insertion

DAC: Digital to Analog Converter

DP: Dynamics Processor

Double-talk: The state when both people (on separate phones) are speaking at the same time

DTMF: Dual Tone Multiple Frequency

Echo: Echo is a delayed signal that returns to its place of origin

ENLP: Enhanced Non-Linear Processor

ERL: Echo Return Loss

ERLE: Echo Return Loss Enhancement

Full-Duplex: Simultaneous transmit and receive paths are active in a communications system for natural flow

Gain: Change in signal amplitude after passing through an amplifier or other circuit

GCI: General Circuit Interface (PCM)

GEQ: Graphic Equalizer functionality for Sound Enhancement

Howling: An annoying squealing noise created from feedback when the coupling between the speaker and microphone is strong enough to increase the system closed loop gain past the condition for oscillation

Hybrid: A hybrid is a converter between two-wire to four-wire transmissions

IDM: Input Data Manager, refers to the digital audio signal mixing, multiplexing and gain blocks immediately downstream from the microphone and line-in ADCs

LI: Line-In

LNA: Low-Noise Amplifier

LO: Line-Out

NC: Noise Cancellation

Network Echo: Echo from an impedance mismatch in a hybrid within the phone or from the hybrid on the other end of the call

ODM: Output Data Manager, refers to the digital audio signal mixing, multiplexing and gain blocks immediately upstream of the speaker and line-out DACs

PCM: Pulse Code Modulation

RES: Residual Echo Suppression

RX: Receive Path

Single-talk: The state when there is speech on only one end of the connection of a phone when one person is speaking and the other is listening

TX: Transmit Path

VAD: Voice Activity Detection helps determine the state of operation: double talk, single talk, or quiet and also distinguishes between conversation and background noise to ensure the proper state of operation

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