ISL94202

Series Charge/Discharge Path 3-to-8 Cell Li-Ion Battery Pack Monitor

FN8889
Rev.2.00
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1. Overview

The ISL94202 is a Li-ion battery monitor IC that supports from three to eight series connected cells. It provides complete battery monitoring and pack control. The ISL94202 provides automatic shutdown and recovery from out-of-bounds conditions and automatically controls pack cell balancing.

The ISL94202 is highly configurable as a stand-alone unit, but can be used with an external microcontroller, which communicates to the IC through an I^2C interface.

1.1 Features

- Eight cell voltage monitors support Li-ion CoO_2, Li-ion Mn_2O_4, and Li-ion $FePO_4$ chemistries
- Stand-alone pack control - no microcontroller needed
- Multiple voltage protection options (each programmable to 4.8V; 12-bit digital value) and selectable overcurrent protection levels
- Programmable detection/recovery times for overvoltage, undervoltage, overcurrent, and short-circuit conditions
- Configuration/calibration registers maintained in EEPROM
- Open battery connect detection
- Integrated charge/discharge FET drive circuitry with built-in charge pump supports high-side N-channel FETs
- Cell balancing uses external FETs with internal state machine or external microcontroller
- Enters low power states after periods of inactivity
  - Charge or discharge current detection resumes normal scan rates

1.2 Applications

- Power tools
- Battery back-up systems
- Light electric vehicles
- Portable equipment
- Energy storage systems
- Solar farms
- Medical equipment
- Hospital beds
- Monitoring equipment
- Ventilators

1.3 Related Literature

- For a full list of related documents, visit our website
  - ISL94202 product page

1.4 Typical Application Diagram

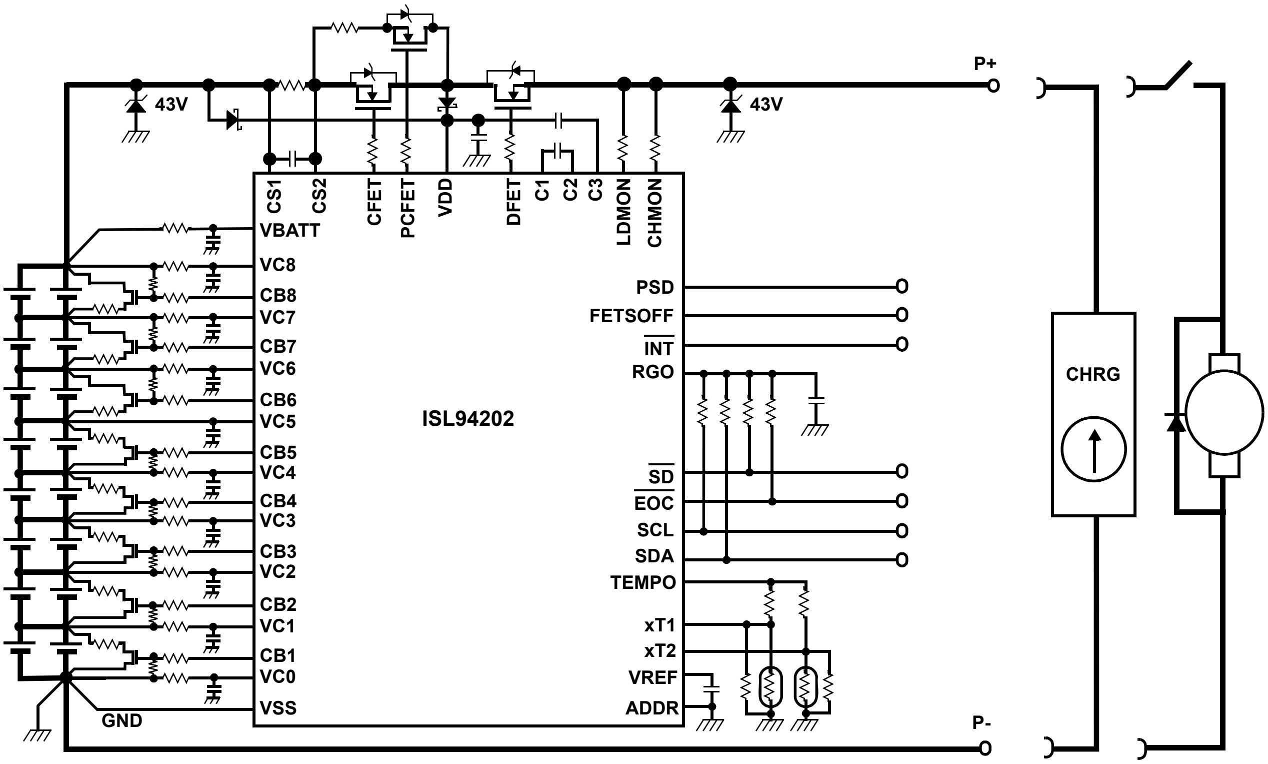


Figure 1.1 Typical Application Diagram

1.5 Block Diagram

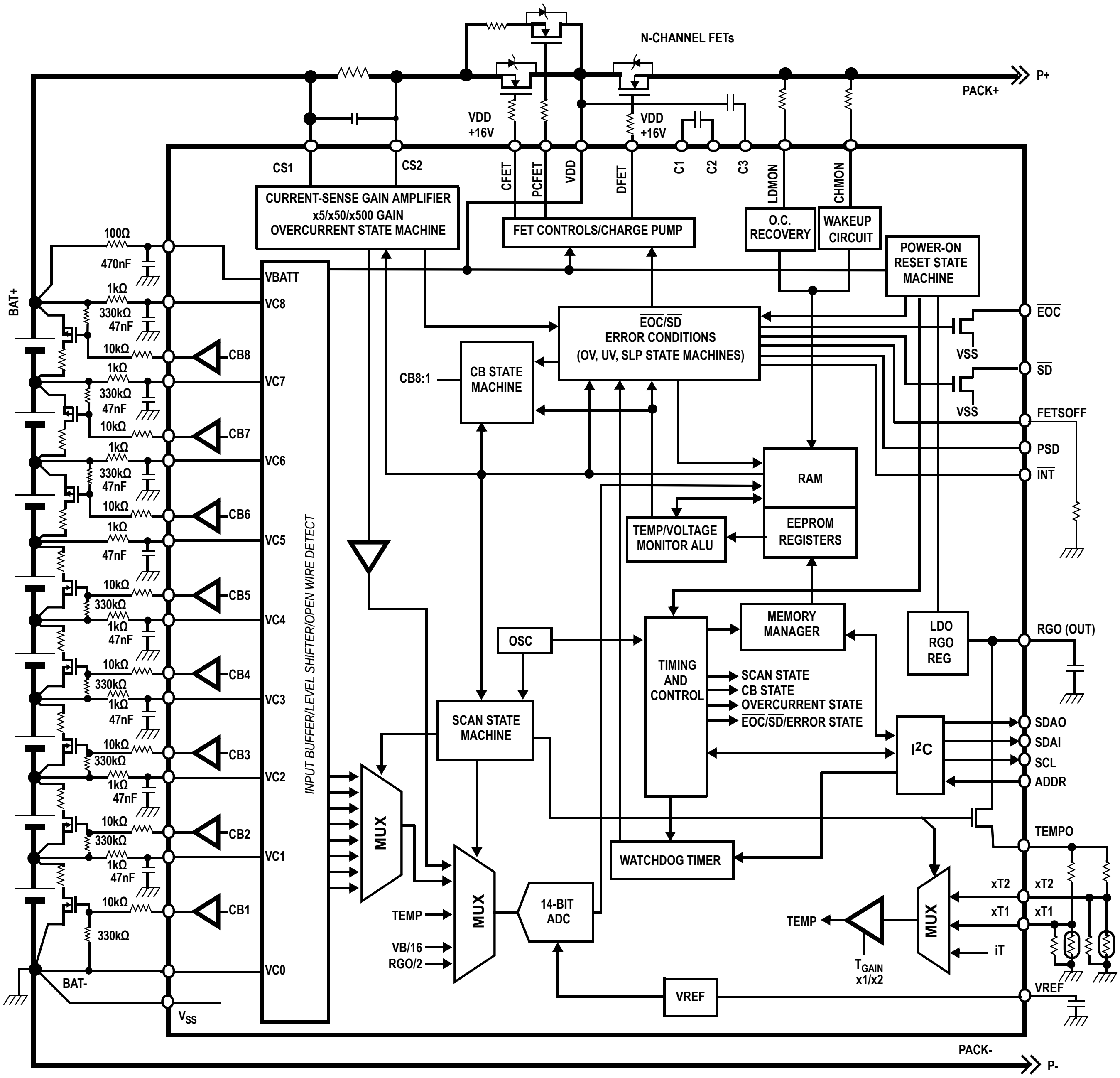


Figure 1.2 Block Diagram

1.6 Ordering Information

Part Number (Notes 1 2, 3)	Part Marking	Temp. Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL94202IRTZ	94202 IRTZ	-40 to +85	48 Ld TQFN	L48.6x6
ISL94202EVKIT1Z	Evaluation Kit			

Notes:

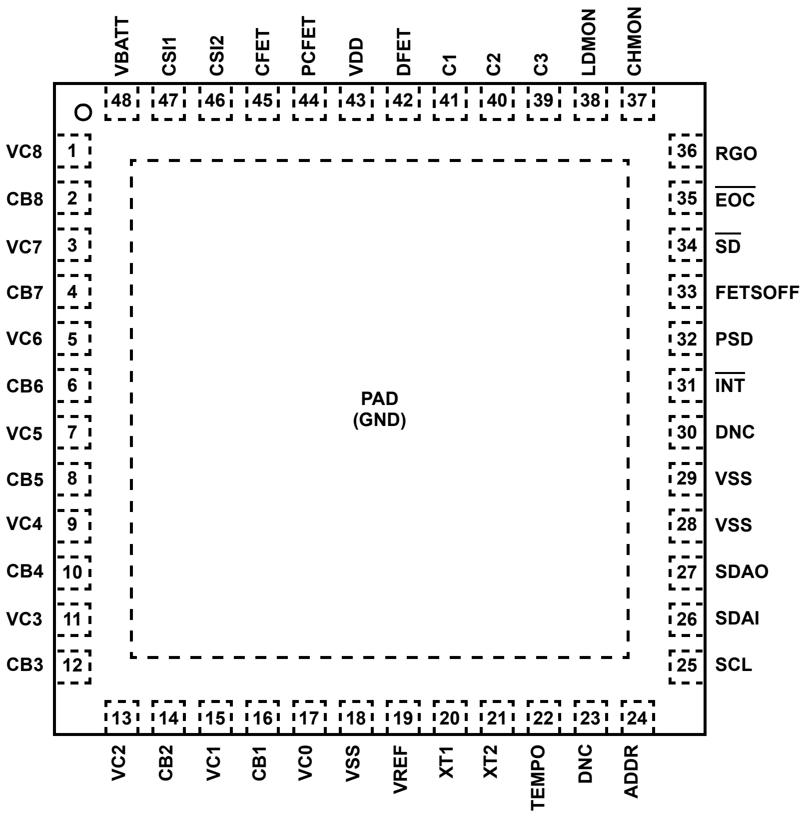
1. Add “-T” suffix for 4k unit, “-T7” for 1k unit, or “-T7A” suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for ISL94202. For more information on MSL, see tech brief TB363.

Table 1.1 Key Differences Between Family of Parts

Part #	Cells Supported		Pack Voltage (Op)		Cell Balance	Current Sense	Charge/Discharge FET			Supply Current (Typ)		Stand-Alone Capable	Internal ADC	Daisy Chain
	Min	Max	Min (V)	Max (V)			Control	Arrangement	Location	Normal	Sleep			
ISL94202	3	8	4	36	External	High Side	Yes	One Path	High Side	348µA	13µA	Yes	Yes	No
ISL94203	3	8	4	36	External	High Side	Yes	Two Path	High Side	348µA	13µA	Yes	Yes	No
ISL94208	4	6	8	26.4	Internal	Low Side	Yes	Both	Low Side	850µA	2µA	No	No	No
ISL94212	6	12	6	60	External	No	No	N/A	N/A	3.31mA	12µA	No	Yes	Yes

1.7 Pin Configuration

ISL94202
(48 LD TQFN)
TOP VIEW



1.8 Pin Descriptions

Pin Number	Symbol	Description
1, 3, 5, 7, 9, 11, 13, 15, 17	VC[8:0]	**Battery cell n voltage input.** This pin is used to monitor the voltage of this battery cell. The voltage is level shifted to a ground reference and is monitored internally by an ADC converter. VCn connects to the positive terminal of a battery cell (CELLN) and VC(n-1) the negative terminal of CELLN (VSS connects with the negative terminal of CELL1).
2, 4, 6, 8, 10, 12, 14, 16	CB[8:1]	**Cell balancing FET control output n.** This internal drive circuit controls an external FET used to divert a portion of the current around a cell while the cell is being charged or adds to the current pulled from a cell during discharge in order to perform a cell voltage balancing operation. This function is generally used to reduce the voltage on an individual cell relative to other cells in the pack. The cell balancing FETs are turned on or off by an internal cell balance state machine or an external controller.
18, 28, 29	VSS	**Ground**. This pin connects to the most negative terminal in the battery string.
19	VREF	**Voltage Reference Output.** This output provides a 1.8V reference voltage for the internal circuitry and for the external microcontroller.
20	XT1	**Temperature monitor inputs.** These pins input the voltage across two external thermistors used to determine the temperature of the cells and or the power FET. When this input drops below the threshold, an external over-temperature condition exists.
21	XT2	
22	TEMPO	**Temperature Monitor Output Control.** This pin outputs a voltage to be used in a divider that consists of a fixed resistor and a thermistor. The thermistor is located in close proximity to the cells or the power FET. The TEMPO output is connected internally to the VREF voltage through a PMOS switch only during a measurement of the temperature, otherwise the TEMPO output is off.
23, 30	DNC	Do not connect
24	ADDR	**Serial Address.** This is an address input for an I^{2}C communication link to allow for two devices on one bus.
25	SCL	**Serial Clock.** This is the clock input for an I^{2}C communication link.
26	SDAI	**Serial Data.** These are the data lines for an I^{2}C interface. When connected together, they form the standard bidirectional interface for the I^{2}C bus (recommended). When separated, they can use separate level shifters for two-device operation (not supported).
27	SDAO	
31	INT	**Interrupt.** This pin goes active low when there is an external µC connected to the ISL94202 and µC communication fails to send a slave byte within a watchdog timer period. This is a CMOS type output.
32	PSD	**Pack Shutdown.** This pin goes active high when any cell voltage reaches the OVLO threshold (OVLO flag). Optionally, PSD is also set if there is a voltage differential between any two cells that is greater than a specified limit (CELLF flag) or if there is an open-wire condition. This pin can be used for blowing a fuse in the pack or as an interrupt to an external µC.
33	FETSOFF	**FETSOFF.** This input allows an external microcontroller to turn off both Power FET and CB outputs. This pin should be pulled low when inactive.
34	SD	**Shutdown.** This output indicates that the ISL94202 detected any failure condition that would result in the DFET turning off. This could be undervoltage, overcurrent, over-temperature, under-temperature, etc. The $\overline{\text{SD}}$ pin also goes active if there is any charge overcurrent condition. This is an open-drain output.
35	EOC	**End-of-Charge.** This output indicates that the ISL94202 detected a fully charged condition. This is defined by any cell voltage exceeding an EOC voltage (as defined by an EOC value in EEPROM).
36	RGO	**Regulator Output.** This is the 2.5V regulator output.
37	CHMON	**Charge Monitor.** This input monitors the charger connection. When the IC is in the Sleep mode, connecting this pin to the charger wakes up the device. When the IC recovers from a charge overcurrent condition, this pin is used to monitor that the charger is removed prior to turning on the power FETs. In a single-path configuration, this pin and the LDMON pin connect together.
38	LDMON	**Load Monitor.** This pin monitors the load connection. When the IC is in the Sleep mode, connecting this pin to a load wakes up the device. When the IC recovers from a discharge overcurrent or short-circuit condition, this pin is used to monitor that the load is removed prior to turning on the power FETs. In a single path configuration, this pin and the CHMON pin connect together.
39, 40, 41	C[3:1]	**Charge Pump Capacitor Pins.** These external capacitors are used for the charge pump driving the power FETs.
42	DFET	**Discharge FET Control.** The ISL94202 controls the gate of a discharge FET through this pin. The power FET is an N-channel device. The FET is turned on by the ISL94202 if all conditions are acceptable. The ISL94202 will turn off the FET in the event of an out-of-bounds condition. The FET can be turned off by an external microcontroller by writing to the CFET control bit. The CFET output is also turned off by the FETSOFF pin. The FET output cannot be turned on by an external microcontroller if there are any out-of-bounds conditions.
43	VDD	**IC Supply Pin.** This pin provides the operating voltage for the IC circuitry.

Pin Number	Symbol	Description
44	PCFET	**Precharge FET Control.** The ISL94202 controls the gate of a precharge FET through this pin. The power FET is an N-channel device. The FET is turned on by the ISL94202 if all conditions are acceptable. The ISL94202 will turn off the FET in the event of an out-of-bounds condition. The FET can be turned off by an external microcontroller by writing to the PCFET control bit. The PCFET output is also turned off by the FETSOFF pin. The FET output cannot be turned on by an external microcontroller if there are any out-of-bounds conditions. Either the PCFET or the CFET turn on, but not both.
45	CFET	**Charge FET Control.** The ISL94202 controls the gate of a charge FET through this pin. The power FET is an N-channel device. The FET is turned on by the ISL94202 if all conditions are acceptable. The ISL94202 will turn off the FET in the event of an out-of-bounds condition. The FET can be turned off by an external microcontroller by writing to the CFET control bit. The CFET output is also turned off by the FETSOFF pin. The FET output cannot be turned on by an external microcontroller if there are any out-of-bounds conditions. Either the PCFET or the CFET turn on, but not both.
46	CSI2	**Current-Sense Inputs.** These pins connect to the ISL94202 current-sense circuit. There is an external resistance across which the circuit operates. The sense resistor is typically in the range of 0.2mΩ to 5mΩ.
47	CSI1	
48	VBATT	**Input Level Shifter Supply and Battery Pack Voltage Input.** This pin powers the input level shifters and is also used to monitor the voltage of the battery stack. The voltage is internally divided by 32 and connected to an ADC converter through a MUX.
PAD	GND	**Thermal Pad.** This pad should connect to ground.

Contents

3. Specifications

3.1 Absolute Maximum Ratings

(Note 1)

Parameter	Minimum	Maximum (Note 1)	Unit
Power Supply Voltage, VDD	VSS - 0.5	VSS+ 45.0	V
Cell Voltage (VC, VBATT)			
VCn	-0.5	VBATT + 0.5	V
VCn - VSS (n = 8)	-0.5	45.0	V
VCn - VSS (n = 6, 7)	-0.5	36.0	V
VCn - VSS (n = 4, 5)	-0.5	27.0	V
VCn - VSS (n = 2, 3)	-0.5	17.0	V
VCn - VSS (n = 1)	-0.5	7.0	V
VCn - VSS (n = 0)	-0.5	3.0	V
VCn - VC(n-1) (n = 2 to 12)	-3.0	7.0	V
VC1 - VC0	-0.5	7.0	V
Cell Balance Pin Voltages (VCB)			
VCBn - VC(n-1), n = 1 to 5	-0.5	7.0	V
VCn - VCBn, n = 6 to 8	-0.5	7.0	V
Terminal Voltage			
ADDR, xT1, xT2, FETSOFF, PSD, $\overline{\text{INT}}$	-0.5	VRGO +0.5	V
SCL, SDAI, SDAO, $\overline{\text{EOC}}$, $\overline{\text{SD}}$	-0.5	5.5	V
CFET, PCFET, C1, C2, C3	VDD - 0.5	VDD + 15.5 (60V max)	V
DFET, CHMON, LDMON	-0.5	VDD + 15.0 (60V max)	V
Terminal Current			
RGO		25	mA
Current-Sense Voltage			
VBATT, CS1, CS2	-0.5	VDD +1.0	V
VBATT - CS1, VBATT - CS2	-0.5	+0.5	V
CS1 - CS2	-0.5	+0.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	1.5		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

Note:

1. Devices are characterized, but not production tested, at Absolute Maximum Voltages.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN Package (Notes 2, 3)	28	0.75

Notes:

2. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Continuous Package Power Dissipation		400	mW
Maximum Junction Temperature		+125	°C
Storage Temperature Range	-55	+125	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-40	+85	°C
Operating Voltage			
VDD	4V	36	V
VCn-VC(n-1) Specified Range	2.0	4.3	V
VCn-VC(n-1) Extended Range	1.0	4.4	V
VCn-VC(n-1) Maximum Range (any cell)	0.5	4.8	V

3.4 Electrical Specification

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C.**

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Power-Up Condition – Threshold Rising (Device becomes operational)	V_{PORR1}	V_{DD} minimum voltage at which device operation begins (CFET turns on; CHMON = V_{DD})		6.0		V
	V_{PORR2}	CHMON minimum voltage at which device operation begins (CFET turns on; V_{DD} > 6.0V)		V_{DD}		V
Power-Down Condition – Threshold Falling	V_{PORF}	V_{DD} minimum voltage device remains operational (RGO turns off)		3.0		V
2.5V Regulated Voltage	V_{RGO}	I_{RGO} = 3mA	**2.4**	2.5	**2.6**	V
1.8V Reference Voltage	V_{REF}		**1.79**	1.8	**1.81**	V
VBATT Input Current - V_{BATT}	I_{VBATT}	Input current; Normal/Idle/Doze modes V_{DD} = 33.6V		38	**45**	μA
		Input current; Sleep/Power-Down modes V_{DD} = 33.6V			**1**	μA
V_{DD} Supply Current	I_{VDD1}	Device active (Normal mode) (No error conditions) CFET, PCFET, DFET = OFF; V_{DD} = 33.6V		310	**370**	μA
	I_{VDD2}	Device active (Idle mode) (No error conditions) Idle = 1 CFET, PCFET, DFET = OFF; V_{DD} = 33.6V		215	**275**	μA
	I_{VDD3}	Device active (Doze mode) (No error conditions) Doze = 1 CFET, PCFET, DFET = OFF; V_{DD} = 33.6V		210	**265**	μA
	I_{VDD4}	FET drive current (I_{VDD} increase when FETs are on - Normal/Idle/Doze modes); V_{DD} = 33.6V		215		μA
	I_{VDD5}	Device active (Sleep mode); Sleep = 1; V_{DD} = 33.6V 0°C to +60°C		13	30	μA
		-40°C to +85°C			**50**	μA
	I_{VDD6}	Power-down PDWN = 1; V_{DD} = 33.6V			**1**	μA
Input Bias Current	ICS1	V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (Normal, idle, doze)		10	**15**	μA
		V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (Sleep, Power-Down) 0°C to +60°C			1	μA
		-40°C to +85°C			**3**	μA
	ICS2	V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (Normal, Idle, Doze)		10	**15**	μA
		V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (Sleep, Power-Down) 0°C to +60°C			1	μA
		-40°C to +85°C			**3**	μA
VCn Input Current	I_{VCN}	Cell input leakage current AO2:AO0 = 0000H (Normal/Idle/Doze; not sampling cells)	**-1**		**1**	μA
CBn Input Current	I_{CBN}	Cell Balance pin leakage current (no balance active)	**-1**		**1**	μA

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Temperature Monitor Specifications						
External Temperature Accuracy	V_{XT1}	External temperature monitoring error. ADC voltage error when monitoring xT1 input. TGain = 0; (xTn = 0.2V to 0.737V)	**-25**		**15**	mV
Internal Temperature Monitor Output (See "Temperature Monitoring/Response" on page 49)	T_{INT25}	[iTB:iT0]$_{10}$*1.8/4095/GAIN GAIN = 2 (TGain bit = 0) Temperature = +25°C		0.276		V
	V_{INTMON}	Change in [iTB:iT0]$_{10}$*1.8/4095/GAIN GAIN = 2 (TGain bit = 0) Temperature = -40°C to +85°C		1.0		mV/°C
Cell Voltage Monitor Specifications						
Cell Monitor Voltage Accuracy (Relative)	V_{ADCR}	Relative cell measurement error (Maximum absolute cell measurement error - Minimum absolute cell measurement error) VCn - VC(n-1) = 2.4V to 4.2V; 0°C to +60°C		3	10	mV
		VCn - VC(n-1) = 0.1V to 4.7V; 0°C to +60°C			15	mV
		VCn - VC(n-1) = 0.1V to 4.7V; -40°C to +85°C			**30**	mV
Cell Monitor Voltage Accuracy (Absolute)	V_{ADC}	Absolute cell measurement error (Cell measurement error compared with voltage at the cell) VCn - VC(n-1) = 2.4V to 4.2V; 0°C to +60°C	-15		15	mV
		VCn - VC(n-1) = 0.1V to 4.7V; 0°C to +60°C	-20		20	mV
		VCn - VC(n-1) = 0.1V to 4.7V; -40°C to +85°C	**-30**		**30**	mV
V_{BATT} Voltage Accuracy	V_{BATT}	V_{BATT} - [VBB:VB0]$_{10}$*32*1.8/4095; 0°C to +60°C	-200		200	mV
		-40°C to +85°C	**-270**		**270**	mV
Current-Sense Amplifier Specifications						
Charge Current Threshold	VCCTH	VCS1-VCS2, CHING indicates charge current VCS1 = 26.4V		-100		µV
Discharge Current Threshold	VDCTH	VCS1-VCS2, DCHING indicates discharge current; VCS1 = 26.4V		100		µV

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Current-Sense Accuracy	VIA1	V_{IA1} = ([ISNSB:ISNS0]$_{10}$*1.8/4095)/5; CHING bit set; Gain = 5 VCS1 = 26.4V, VCS2 - VCS1 = + 100mV	**97**	102	**107**	mV
	VIA2	V_{IA2} = ([ISNSB:ISNS0]$_{10}$*1.8/4095)/5; DCHING bit set; Gain = 5 VCS1 = 26.4V, VCS2 - VCS1 = - 100mV	**-107**	-102	**-97**	mV
	VIA3	V_{IA3} = ([ISNSB:ISNS0]$_{10}$*1.8/4095)/50; CHING bit set; Gain = 50 VCS1 = 26.4V, VCS2 - VCS1 = + 10mV	**8.0**	10.0	**12.0**	mV
	VIA4	V_{IA4} = ([ISNSB:ISNS0]$_{10}$*1.8/4095)/50; DCHING bit set; Gain = 50 VCS1 = 26.4V, VCS2 - VCS1 = - 10mV	**-12.0**	-10.0	**-8.0**	mV
	VIA5	V_{IA3} = ([ISNSB:ISNS0]$_{10}$*1.8/4095)/500; CHING bit set; Gain = 500 VCS1 = 26.4V, VCS2 - VCS1 = + 1mV 0°C to +60°C	0.5	1.0	1.5	mV
		-40°C to +85°C	**0.4**		**1.6**	mV
	VIA6	V_{IA4} = ([ISNSB:ISNS0]$_{10}$*1.8/4095)/500; DCHING bit set; Gain = 500 VCS1 = 26.4V, VCS2 - VCS1 = - 1mV 0°C to +60°C	-1.5	-1.0	-0.5	mV
		-40°C to +85°C	**-1.6**		**-0.4**	mV
Overcurrent/Short-Circuit Protection Specifications						
Discharge Overcurrent Detection Threshold	V_{OCD}	V_{OCD} = 4mV [OCD2:0] = 0,0,0	**2.6**	4.0	**5.4**	mV
		V_{OCD} = 8mV [OCD2:0] = 0,0,1	**6.4**	8.0	**9.6**	mV
		V_{OCD} = 16mV [OCD2:0] = 0,1,0	**12.8**	16.0	**19.2**	mV
		V_{OCD} = 24mV [OCD2:0] = 0,1,1	**20**	25	**30**	mV
		V_{OCD} = 32mV [OCD2:0] = 1,0,0 (default)	**26.4**	33.0	**39.6**	mV
		V_{OCD} = 48mV [OCD2:0] = 1,0,1	**42.5**	50.0	**57.5**	mV
		V_{OCD} = 64mV [OCD2:0] = 1,1,0	**60.3**	67.0	**73.7**	mV
		V_{OCD} = 96mV [OCD2:0] = 1,1,1	**90**	100	**110**	mV
Discharge Overcurrent Detection Time	t_{OCDT}	[OCDTA:OCDT0] = 0A0H (160ms) (default) Range: 0ms to 1023ms 1ms/step 0s to 1023s; 1s/step		160		ms
Short-Circuit Detection Threshold	V_{SCD}	V_{SCD} = 16mV [SCD2:0] = 0,0,0	**10.4**	16.0	**21.6**	mV
		V_{SCD} = 24mV [SCD2:0] = 0,0,1	**18**	24	**30**	mV
		V_{SCD} = 32mV [SCD2:0] = 0,1,0	**26**	33	**40**	mV
		V_{SCD} = 48mV [SCD2:0] = 0,1,1	**42**	49	**56**	mV
		V_{SCD} = 64mV [SCD2:0] = 1,0,0	**60**	67	**74**	mV
		V_{SCD} = 96mV [SCD2:0] = 1,0,1 (default)	**90**	100	**110**	mV
		V_{SCD} = 128mV [SCD2:0] = 1,1,0	**127**	134	**141**	mV
		V_{SCD} = 256mV [SCD2:0] = 1,1,1	**249**	262	**275**	mV
Short-Circuit Current Detection Time	t_{SCT}	[SCTA:SCT0] = 0C8H (200µs) (default) Range: 0µs to 1023µs; 1µs/step 0ms to 1023ms 1ms/step		200		µs

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C.** **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Charge Overcurrent Detection Threshold	V_{OCC}	V_{OCC} = 1mV [OCC2:0] = 0,0,0	**0.2**	1.0	**2.1**	mV
		V_{OCC} = 2mV [OCC2:0] = 0,0,1	**0.7**	2.0	**3.3**	mV
		V_{OCC} = 4mV [OCC2:0] = 0,1,0	**2.8**	4.0	**5.2**	mV
		V_{OCC} = 6mV [OCC2:0] = 0,1,1	**4.5**	6.0	**7.5**	mV
		V_{OCC} = 8mV [OCC2:0] = 1,0,0 (default)	**6.6**	8.0	**9.8**	mV
		V_{OCC} = 12mV [OCC2:0] = 1,0,1	**9.6**	12.0	**14.4**	mV
		V_{OCC} = 16mV [OCC2:0] = 1,1,0	**14.5**	17.0	**19.6**	mV
		V_{OCC} = 24mV [OCC2:0] = 1,1,1	**22.5**	25.0	**27.5**	mV
Overcurrent Charge Detection Time	t_{OCCT}	[OCCTA:OCCT0] = 0A0H (160ms) (default) Range: 0ms to 1023ms 1ms/step 0s to 1023s; 1s per step		160		ms
Charge Monitor Input Threshold (Falling Edge)	V_{CHMON}	µCCMON bit = 1; CMON_EN bit = 1	**8.2**	8.9	**9.8**	V
Load Monitor Input Threshold (Rising Edge)	V_{LDMON}	µCLMON bit = 1; LMON_EN bit = 1	**0.45**	0.60	**0.75**	V
Load Monitor Output Current	I_{LDMON}	µCLMON bit = 1; LMON_EN bit = 1		62		µA
Voltage Protection Specifications						
Overvoltage Lockout Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{OVLO}	[OVLOB:OVLO0] = 0E80H (4.35V) (default) Range: 12-bit value (0V to 4.8V)		4.35		V
Overvoltage Lockout Recovery Threshold - All Cells	V_{OVLOR}	Falling edge		V_{OVR}		V
Undervoltage Lockout Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{UVLO}	[UVLOB:UVLO0] = 0600H (1.8V) (default) Range: 12-bit value (0V to 4.8V)		1.8		V
Undervoltage Lockout Recovery Threshold - All Cells	V_{UVLOR}	Rising edge		V_{UVR}		V
Overvoltage Lockout Detection Time	t_{OVLO}	Normal operating mode 5 consecutive samples over the limit (minimum = 160ms, maximum = 192ms)		176		ms
Undervoltage Lockout Detection Time	t_{UVLO}	Normal operating mode 5 consecutive samples under the limit (minimum = 160ms, maximum = 192ms)		176		ms
Overvoltage Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{OV}	[OVLB:OVL0] = 0E2AH (4.25V) (default) Range: 12-bit value (0V to 4.8V)		4.25		V
Overvoltage Recovery Voltage (Falling Edge - All Cells) [VCn-VC(n-1)]	V_{OVR}	[OVRB:OVR0] = 0DD5H (4.15V) (default) Range: 12-bit value (0V to 4.8V)		4.15		V
Overvoltage Detection/Release Time	t_{OVT}	[OVTA:OVT0] = 201H (1s) (default) Range: 0ms to 1023ms; 1ms/step 0s to 1023s; 1s/step		1		s
Undervoltage Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{UV}	[UVLB:UVL0] = 0900H (2.7V) (default) Range: 12-bit value (0V to 4.8V)		2.7		V
Undervoltage Recovery Voltage (Rising Edge - All Cells) [VCn-VC(n-1)]	V_{UVR}	[UVRB:UVR0] = 0A00H (3.0V) (default) Range: 12-bit value (0V to 4.8V)		3.0		V
Undervoltage Detection Time	t_{UVT}	[UVTA:UVT0] = 201H (1s) (default) Range: 0ms to 1023ms; 1ms/step 0s to 1023s; 1s/step		1		s

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Undervoltage Release Time	t_{UVTR}	[UVTA:UVT0] = 201H (1s) + 3s (default) Range: (0ms to 1023ms) + 3s; 1ms/step (0s to 1023s) + 3s; 1s/step		3		s
Sleep Voltage Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{SLL}	[SLLB:SLL0] = 06AAH (2.0V) (default) Range: 12-bit value (0V to 4.8V)		2.0		V
Sleep Detection Time	t_{SLT}	[SLTA:SLT0] = 201H (1s) (default) Range: 0ms to 1023ms; 1ms/step 0s to 1023s; 1s/step		1		s
Low Voltage Charge Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{LVCH}	[LVCHB:LVCH0] = 07AAH (2.3V) (default) Range: 12-bit value (0V to 4.8V) Precharge if any cell is below this voltage		2.3		V
Low Voltage Charge Threshold Hysteresis	V_{LVCHH}			117		mV
End-of-Charge Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{EOC}	[EOCSB:EOCS0] = 0E00H (4.2V) (default) Range: 12-bit value (0V to 4.8V)		4.2		V
End-of-Charge Threshold Hysteresis	V_{EOCH}			117		mV
Sleep Mode Timer	t_{SMT}	[MOD7:MOD0] = 0DH (off) (default) Range: 0s to 255 minutes		90		min
Watchdog Timer	t_{WDT}	[WDT4:WDT0] = 1FH (31s) (default) Range: 0s to 31s		31		s
Temperature Protection Specifications						
Internal Temperature Shutdown Threshold	T_{ITSD}	[IOTSB:IOTS0] = 02D8H		115		°C
Internal Temperature Recovery	T_{ITRCV}	[IOTRB:IOTR0] = 027DH		95		°C
External Temperature Output Voltage	V_{TEMPO}	Voltage output at TEMPO pin (during temperature scan); I_{TEMPO} = 1mA	**2.30**	2.45	**2.60**	V
External Temperature Limit Threshold (Hot) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 3.1)	T_{XTH}	xTn Hot threshold. Voltage at V_{TEMPI}, xT1 or xT2 = 04B6H TGain = 0 ~+55°C; thermistor = 3.535k Detected by COT, DOT, CBOT bits = 1		0.265		V
External Temperature Recovery Threshold (Hot) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 3.1)	T_{XTHR}	xTn Hot recovery voltage at V_{TEMPI} xT1 or xT2 = 053EH TGain = 0 (~+50°C; thermistor = 4.161k) Detected by COT, DOT, CBOT bits = 0		0.295		V
External Temperature Limit Threshold (Cold) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 3.1)	T_{XTC}	xTn Cold threshold. Voltage at V_{TEMPI} xT1 or xT2 = 0BF2H TGain = 0 (~ -10°C; thermistor = 42.5k) Detected by CUT, DUT, CBUT bits		0.672		V
External Temperature Recovery Threshold (Cold) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 3.1)	T_{XTCH}	xTn Cold recovery voltage at V_{TEMPI}. xT1 or xT2 = 0A93H TGain = 0 (~5°C; thermistor = 22.02k) Detected by CUT, DUT, CBUT bits		0.595		V
Cell Balance Specifications						
Cell Balance FET Gate Drive Current		VC1 to VC5 (current out of pin)	**15**	25	**35**	µA
		VC6 to VC8 (current into pin)	**15**	25	**35**	µA

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C.** **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Cell Balance Maximum Voltage Threshold (Rising Edge - Any cell) [VCMAX]	V_{CBMX}	[CBVUB:CBVU0] = 0E00H (4.2V) (default) Range: 12-bit value (0V to 4.8V)		4.2		V
Cell Balance Maximum Threshold Hysteresis	V_{CBMXH}			117		mV
Cell Balance Minimum Voltage Threshold (Falling Edge - Any cell) [VCMIN]	V_{CBMN}	[CBVLB:CBVL0] = 0A00H (3.0V) (default) Range: 12-bit value (0V to 4.8V)		3.0		V
Cell Balance Minimum Threshold Hysteresis	V_{CBMNH}			117		mV
Cell Balance Maximum Voltage Delta Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{CBDU}	[CBDUB:CBD0] = 06AAH (2.0V) (default) Range: 12-bit value (0V to 4.8V)		2.0		V
Cell Balance Maximum Voltage Delta Threshold Hysteresis	V_{CBDUH}			117		mV
Wake-Up Specifications						
Device CHMON Pin Voltage Threshold (Wake on Charge) (Rising Edge)	V_{WKUP1}	CHMON pin rising edge Device wakes up and sets Sleep flag LOW	**7.0**	8.0	**9.0**	V
Device LDMON Pin Voltage Threshold (Wake on Load) (Falling Edge)	V_{WKUP2}	LDMON pin falling edge Device wakes up and sets Sleep flag LOW	**0.15**	0.40	**0.70**	V
Open-Wire Specifications						
Open-Wire Current	I_{OW}			1.0		mA
Open-Wire Detection Threshold	V_{OW1}	VCn-VC(n-1); VCn is open. (n = 2, 3, 4, 5, 6, 7, 8). Open-wire detection active on the VCn input.		-0.3		V
	V_{OW2}	VC1-VC0; VC1 is open. Open-wire detection active on the VC1 input.		0.4		V
	V_{OW3}	VC0-VSS; VC0 is open. Open-wire detection active on the VC0 input.		1.25		V
FET Control Specifications						
DFET Gate Voltage	V_{DFET1}	(ON) 100µA load; V_{DD} = 36V	**47**	52	**57**	V
	V_{DFET2}	(ON) 100µA load; V_{DD} = 6V	**8**	9	**10**	V
	V_{DFET3}	(OFF)		0		V
CFET Gate Voltage (ON)	V_{CFET1}	(ON) 100µA load; V_{DD} = 36V	**47**	52	**57**	V
	V_{CFET2}	(ON) 100µA load; V_{DD} = 6V	**8**	9	**10**	V
	V_{CFET3}	(OFF)		V_{DD}		V
PCFET Gate Voltage (ON)	V_{PFET1}	(ON) 100µA load; V_{DD} = 36V	**47**	52	**57**	V
	V_{PFET2}	(ON) 100µA load; V_{DD} = 6V	**8**	9	**10**	V
	V_{PFET3}	(OFF)		V_{DD}		V
FET Turn-Off Current (DFET)	$I_{DF(OFF)}$		**14**	15	**16**	mA
FET Turn-Off Current (CFET)	$I_{CF(OFF)}$		**9**	13	**17**	mA
FET Turn-Off Current (PCFET)	$I_{PF(OFF)}$		**9**	13	**17**	mA
FETSOFF Rising Edge Threshold	$V_{FO(IH)}$	FETSOFF rising edge threshold. Turn off FETs		1.8		V
FETSOFF Falling Edge Threshold	$V_{FO(IL)}$	FETSOFF falling edge threshold. Turn on FETs		1.2		V
Serial Interface Characteristics (Note 5)						
Input Buffer Low Voltage (SCL, SDA)	V_{IL}	Voltage relative to V_{SS} of the device	**-0.3**		**V_{RGO} x 0.3**	V
Input Buffer High Voltage (SCL, SDAI, SDAO)	V_{IH}	Voltage relative to V_{SS} of the device	**V_{RGO} x 0.7**		**V_{RGO} + 0.1**	V

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C.** **(Continued)**

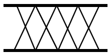
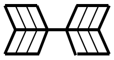
Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Output Buffer Low Voltage (SDA)	V_{OL}	I_{OL} = 1mA			**0.4**	V
SDA and SCL Input Buffer Hysteresis	I^2CHYST	Sleep bit = 0	**0.05 x V_{RGO}**			V
SCL Clock Frequency	f_{SCL}				**400**	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the maximum spec is suppressed.			**50**	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	From SCL falling crossing V_{IH} (minimum), until SDA exits the V_{IL} (maximum) to V_{IH} (minimum) window			**0.9**	µs
Time the Bus Must Be Free Before Start of New Transmission	t_{BUF}	SDA crossing V_{IH} (minimum) during a STOP condition to SDA crossing V_{IH} (minimum) during the following START condition	**1.3**			µs
Clock Low Time	t_{LOW}	Measured at the V_{IL} (maximum) crossing	**1.3**			µs
Clock High Time	t_{HIGH}	Measured at the V_{IH} (minimum) crossing	**0.6**			µs
Start Condition Set-Up Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge, both crossing the V_{IH} (minimum) level	**0.6**			µs
Start Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing V_{IL} (maximum) to SCL falling edge crossing V_{IH} (minimum)	**0.6**			µs
Input Data Set-Up Time	$t_{SU:DAT}$	From SDA exiting the V_{IL} (maximum) to V_{IH} (minimum) window to SCL rising edge crossing V_{IL} (minimum)	**100**			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing V_{IH} (minimum) to SDA entering the V_{IL} (maximum) to V_{IH} (minimum) window	**0**		**0.9**	µs
Stop Condition Set-Up Time	$t_{SU:STO}$	From SCL rising edge crossing V_{IH} (minimum) to SDA rising edge crossing V_{IL} (maximum)	**0.6**			µs
Stop Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing V_{IH} (minimum)	**0.6**			µs
Data Output Hold Time	t_{DH}	From SCL falling edge crossing V_{IL} (maximum) until SDA enters the V_{IL} (maximum) to V_{IH} (minimum) window	**0**			ns
SDA and SCL Rise Time	t_R	From V_{IL} (maximum) to V_{IH} (minimum)			**300**	ns
SDA and SCL Fall Time	t_F	From V_{IH} (minimum) to V_{IL} (maximum)			**300**	ns
SDA and SCL Bus Pull-Up Resistor Off-Chip	R_{OUT}	Maximum is determined by t_R and t_F For C_B = 400pF, maximum is 2kΩ ~ 2.5kΩ For C_B = 40pF, maximum is 15kΩ ~ 20kΩ	**1**			kΩ
Input Leakage (SCL, SDA)	I_{LI}		**-10**		**10**	µA
EEPROM Write Cycle Time	t_{WR}	+25°C			30	ms

Notes:

4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Device MIN and/or MAX values are based on temperature limits established by characterization and are not production tested.
5. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

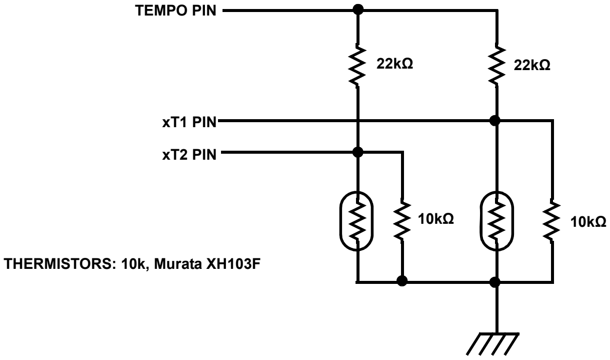
3.5 Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM LOW TO HIGH	WILL CHANGE FROM LOW TO HIGH
	MAY CHANGE FROM HIGH TO LOW	WILL CHANGE FROM HIGH TO LOW

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGES ALLOWED	CHANGING: STATE NOT KNOWN
	N/A	CENTER LINE IS HIGH IMPEDANCE

3.6 Timing Diagrams

3.6.1 External Temperature Configuration



DIGITAL TEMPERATURE VOLTAGE READING =
xTn * 2 (TGAIN BIT = 0)
xTn * 1 (TGAIN BIT = 1)

Figure 3.1 External Temperature Configuration

3.6.2 Wake-Up Timing

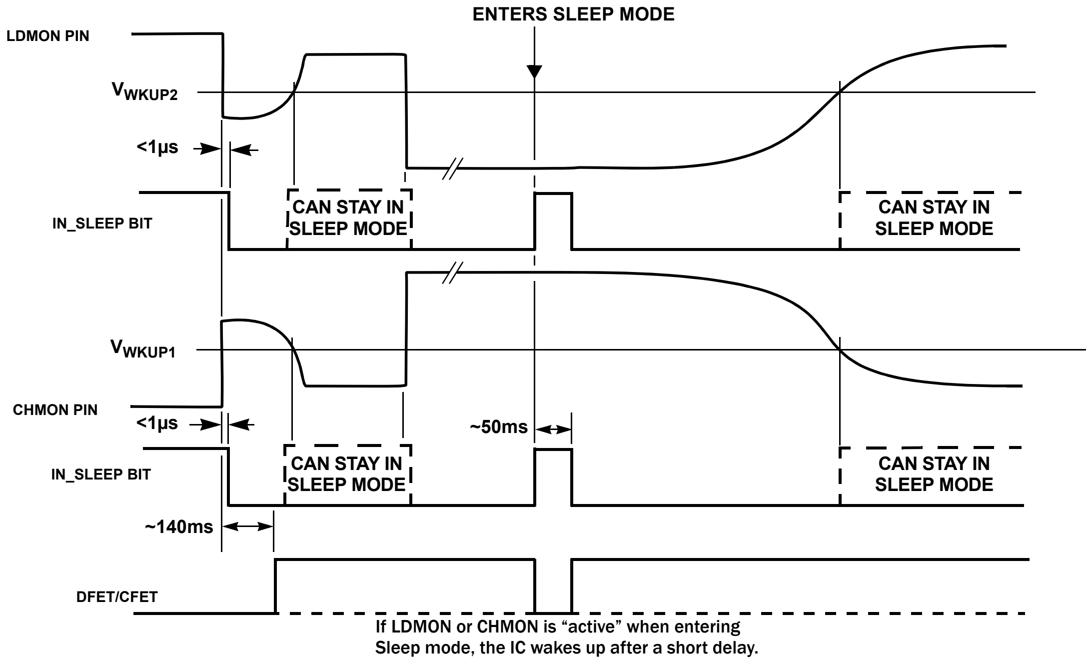


Figure 3.2 Wake-Up Timing (from Sleep)

3.6.3 Power-Up Timing

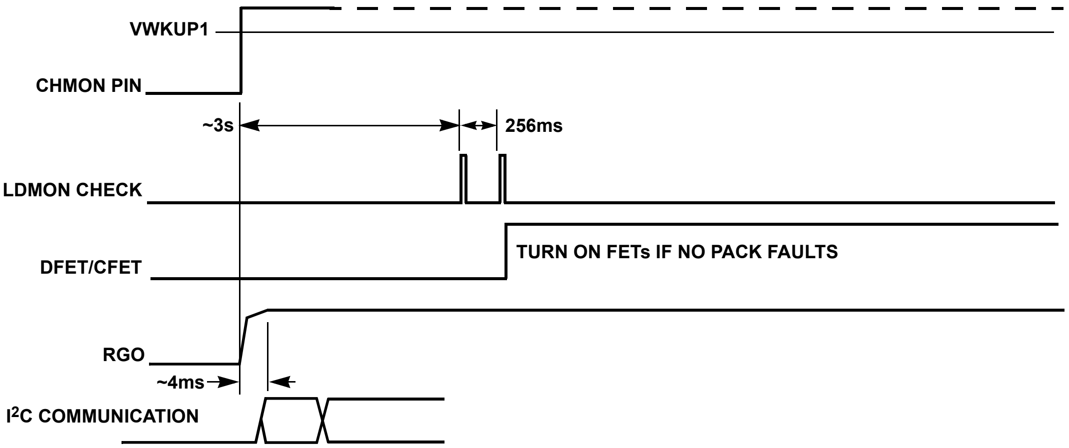


Figure 3.3 Power-Up Timing (from Power-Up/Shutdown)

3.6.4 Change in FET Control

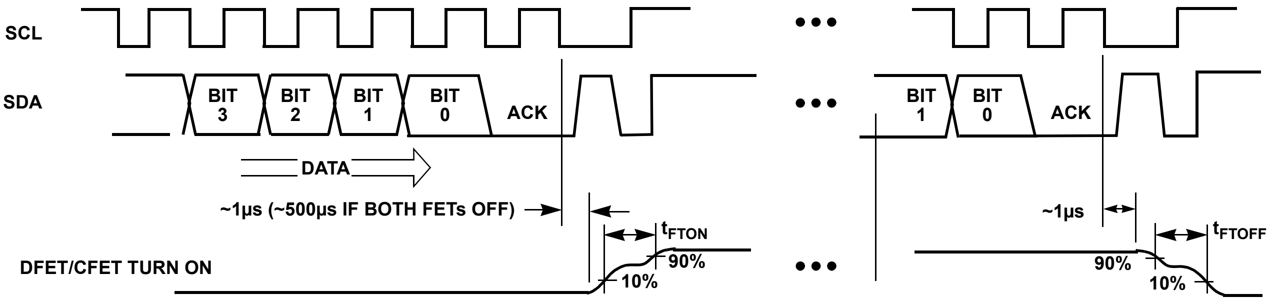


Figure 3.4 I²C FET Control Timing

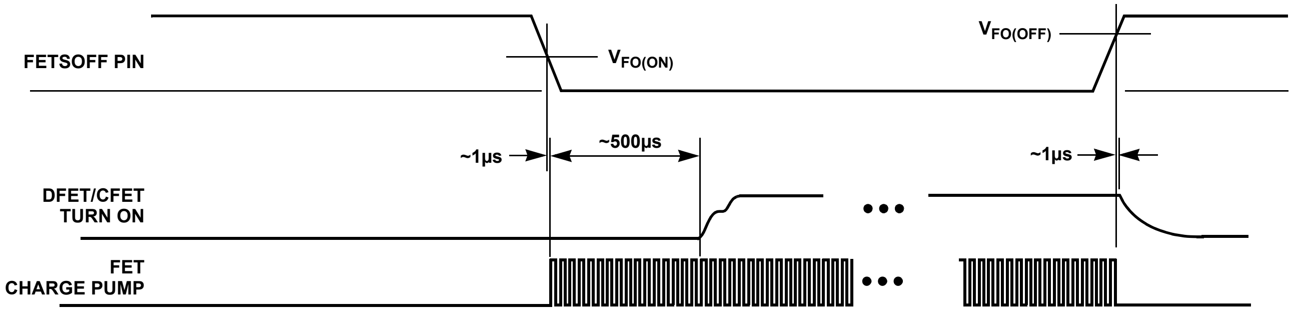
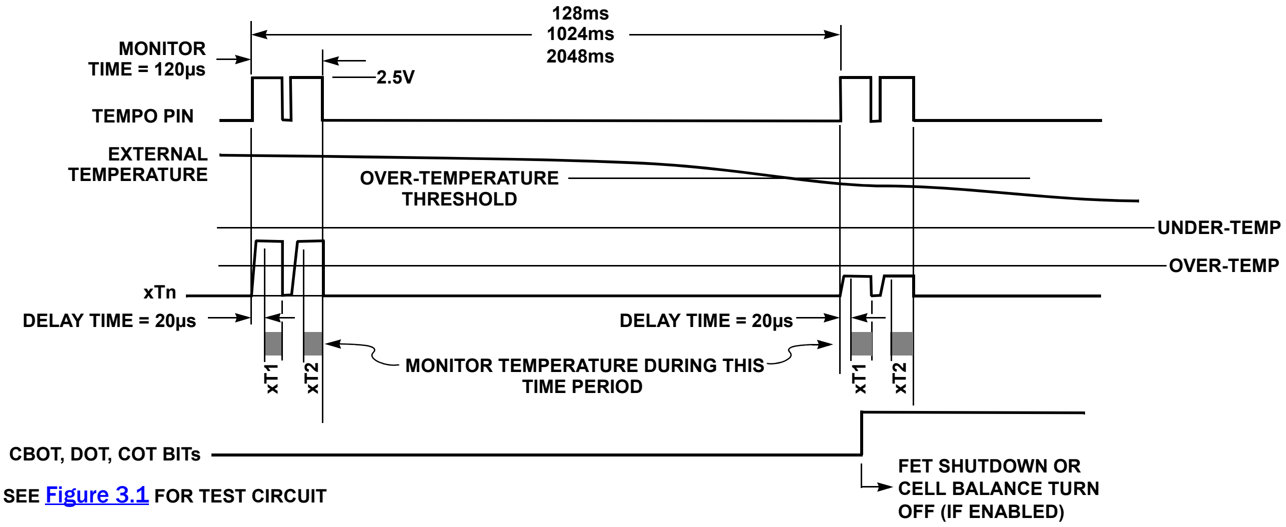


Figure 3.5 FETSOFF FET Control Timing

3.6.5 Automatic Temperature Scan



SEE Figure 3.1 FOR TEST CIRCUIT

Figure 3.6 Automatic Temperature Scan

3.6.6 Serial Interface Timing Diagrams

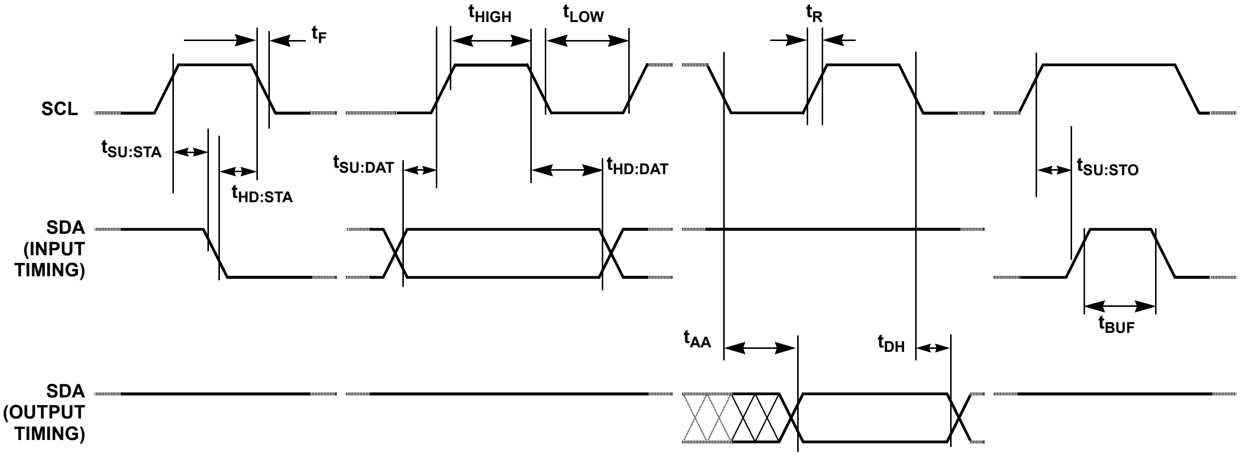


Figure 3.7 Serial Interface Bus Timing

3.6.7 Discharge Overcurrent/Short-Circuit Monitor

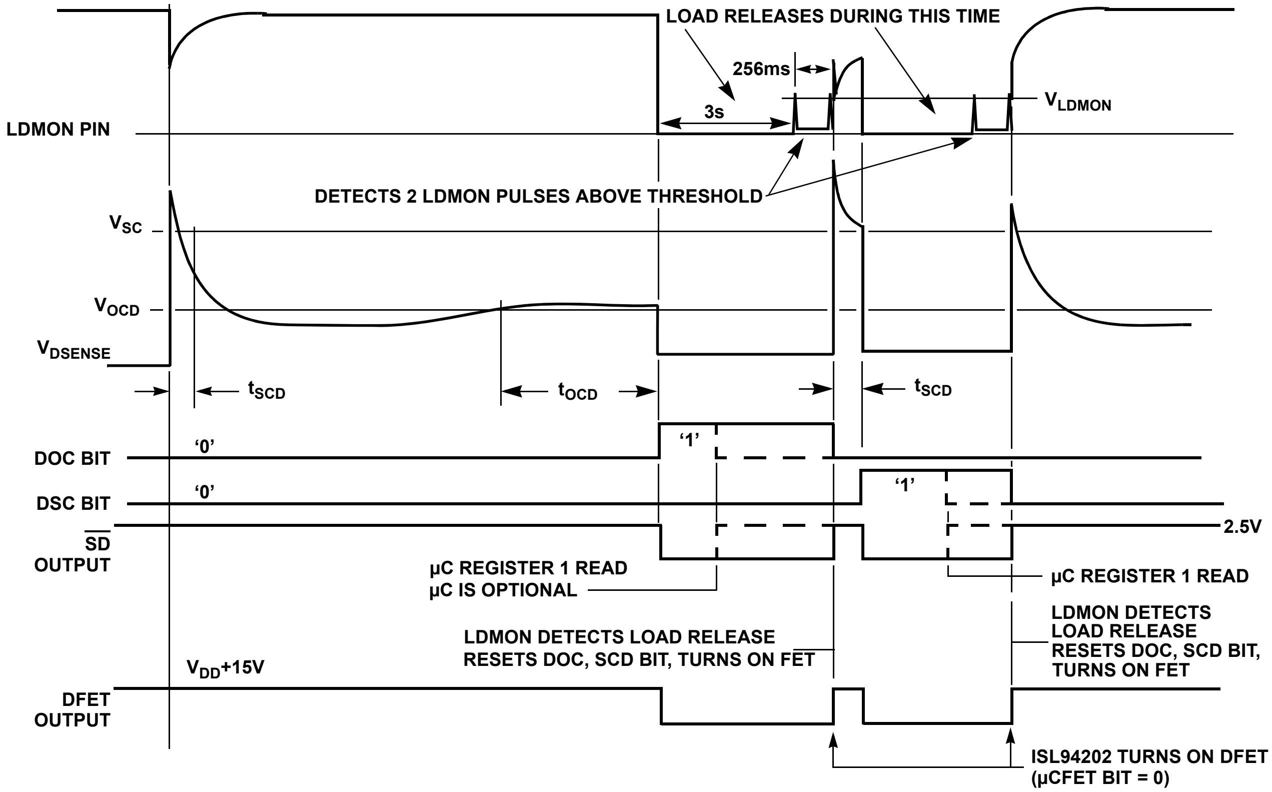


Figure 3.8 Discharge/Short-Circuit Monitor

3.6.8 Charge Overcurrent Monitor

(Assumes NO_OCCR bit is '0')

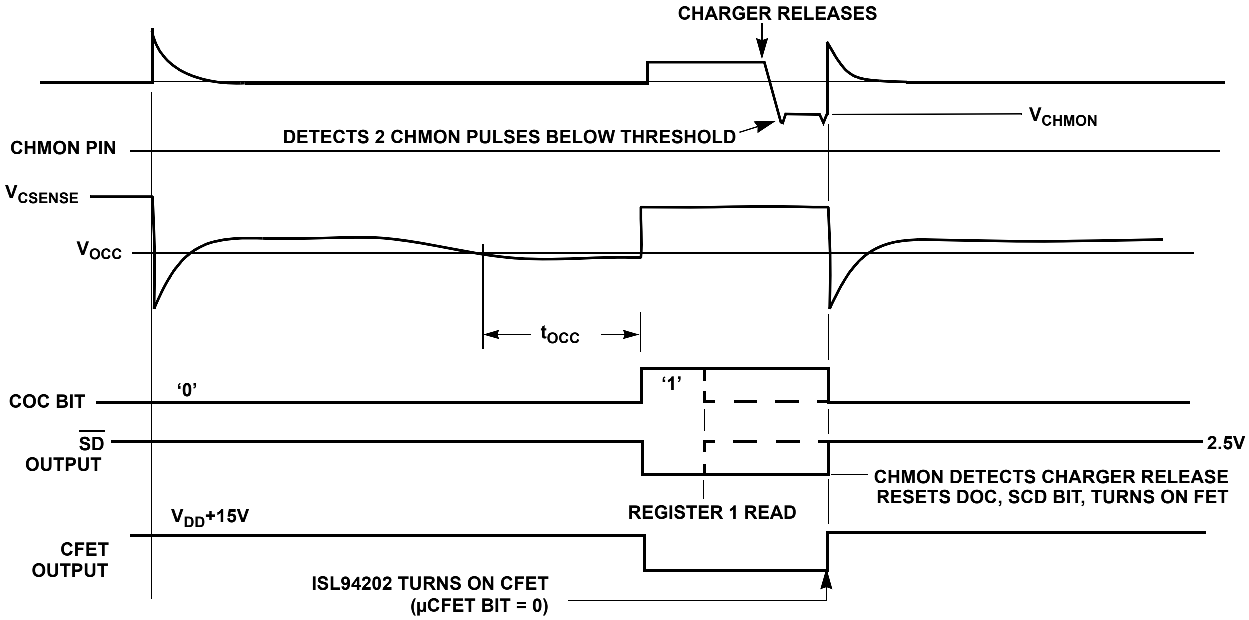


Figure 3.9 Charge Overcurrent Monitor

4. Functional Description

This IC is intended to be a stand-alone battery pack monitor, so it provides monitor and protection functions without requiring an external microcontroller.

The part operates power control FETs on the high side with a built-in charge pump for driving N-channel FETs. The current-sense function is also on the high side.

To extend battery life, power is minimized in all areas with parts of the circuit powered down a majority of the time. The RGO output stays on so that any connected microcontroller can remain on most of the time.

The ISL94202 includes:

- Input level shifter to enable monitoring of battery stack voltages
- 14-bit ADC converter, with voltage readings trimmed and saved as 12-bit results
- 1.8V voltage reference (0.8% accurate)
- 2.5V regulator, with the voltage maintained during sleep
- Automatic scan of the cell voltages; overvoltage, undervoltage, and sleep voltage monitoring
- Selectable overcurrent detection settings
    - Eight discharge overcurrent thresholds
    - Eight charge overcurrent thresholds
    - Eight short-circuit thresholds
    - 12-bit programmable discharge overcurrent delay time
    - 12-bit programmable charge overcurrent delay time
    - 12-bit programmable short-circuit delay time
- Current-sense monitor with gain that provides the ability to read the current-sense voltage
- Second external temperature sensor for use in monitoring the pack or power FET temperatures
- EEPROM for storing operating parameters and a user area for general purpose pack information

5. Battery Connections

5.1 Power Path

Figure 5.1 shows the main power path connections for a single charge/discharge path.

These figures show Schottky diodes on the VDD pin. These are to maintain the voltage on the VDD pin during high current conditions or when the Charge FET is OFF. These are not needed if V_{DD} can be maintained within 0.5V of V_{BATT}.

The CHMON pin connects to the pack pin that receives the charge and the LDMON pin connects to the pack pin that drives the load. For the single path application, these pins can tie together.

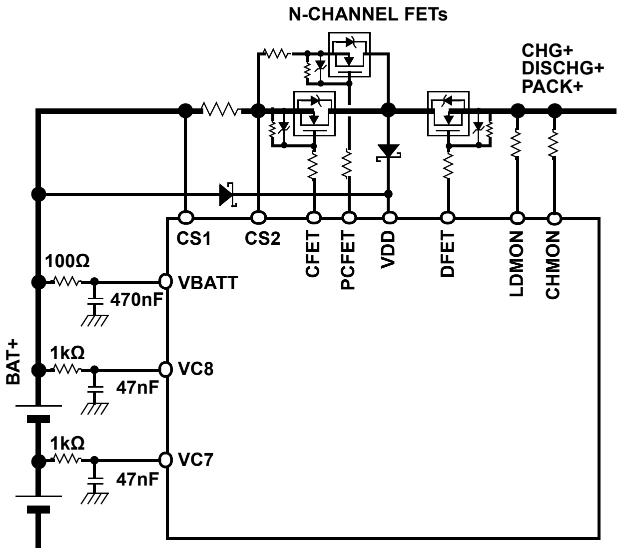


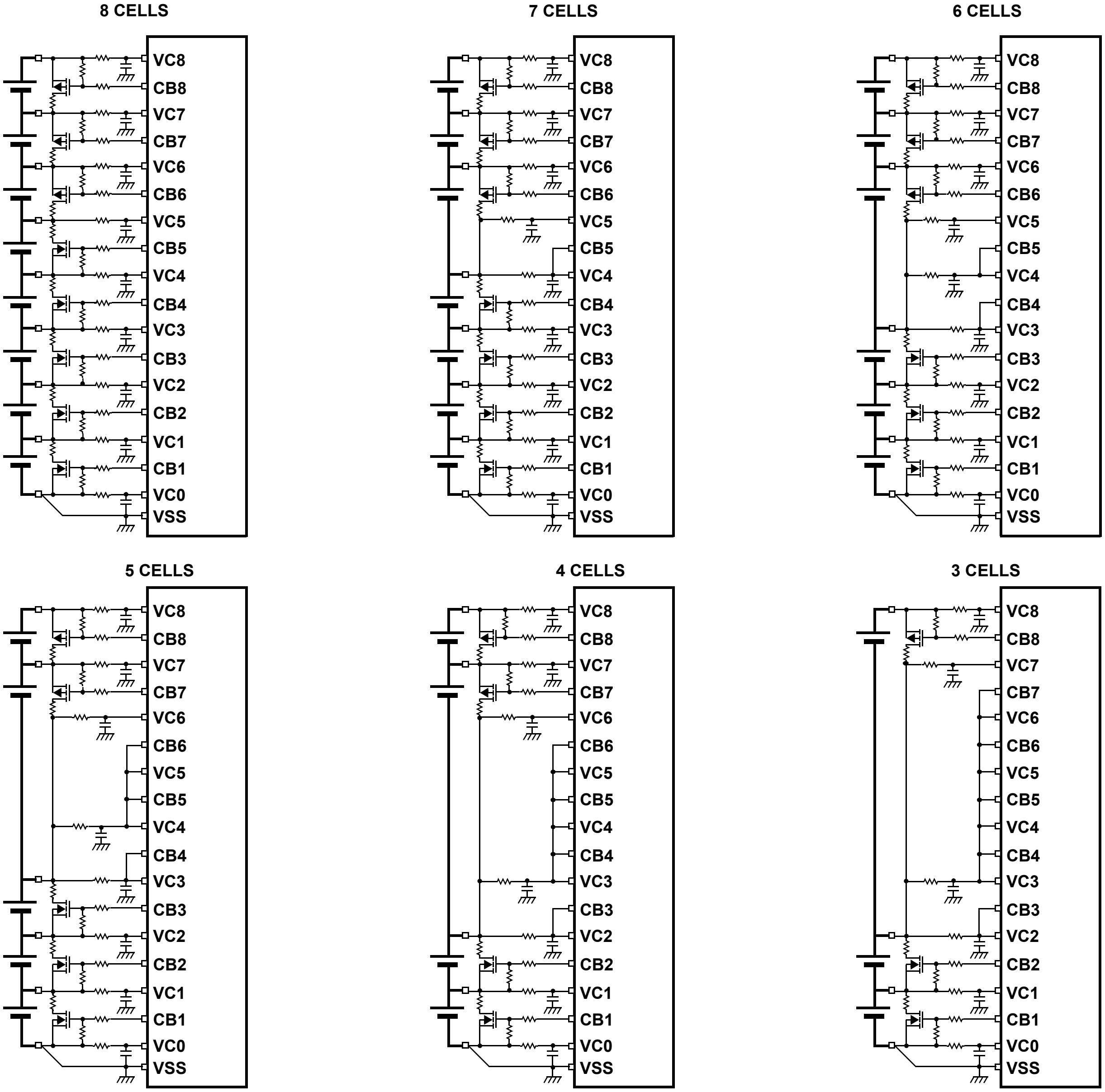
Figure 5.1 Single Path FET Drive/Power Supply Detail

5.2 Pack Configuration

A register in EEPROM (CELLS) identifies the number of cells that are supposed to be present, so the ISL94202 only scans these cells. This register is also used for the cell balance operation. The register contents are a 1:1 representation of the cells connected to the pack. For example, in a 6-cell pack, the value in CELLS is ‘11100111’ (CFH), which indicates that Cells 1, 2, 3, 6, 7, and 8 are connected. Also see Figure 5.2.

5.3 Battery Cell Connections

Suggested connections for pack configurations varying from three cells to eight cells are shown in Figure 5.2.



NOTE: MULTIPLE CELLS CAN BE CONNECTED IN PARALLEL

Figure 5.2 Battery Connection Options

6. Operating Modes

6.1 Power-Up Operation

When the ISL94202 first connects to the battery pack, it is unknown which pins connect first or in what order. When the VDD and VSS pins connect, the device enters the power-down state. It remains in this state until a charger is connected. The device will also power up if the CHMON pin is connected to the VDD pin through an outside resistor to simplify the PCB manufacture. It is possible that the pack powers up automatically when the battery stack is connected due to momentary conduction through the power FET G-S and G-D capacitors.

Once the charger connects (or CHMON connects), the internal power supply turns on. This powers up all internal supplies and starts the state machine. If some cells are not connected, the state machine recognizes this, either through the open-wire test (see “Typical Operating Conditions” on page 32) or because the monitored cell voltage reads zero when the “CELLS” register indicates that there should be a voltage at that pin. If the cell voltages do not read correctly, then the ISL94202 remains in the POR loop until conditions are valid for power-up. (It is for this reason that the factory default for the device is three cells. When manufacturing the application board, Cells 1, 2, and 8 must be connected to power up. If other cells are connected it is OK, but for the other cells to be monitored, the CELLS register needs to be changed.)

If the inputs all read “good” during this sequence, then the state machine enters the normal monitor state. In the normal state, if all cell voltages read “good” and there are no overcurrent or temperature issues and there is no load, the FETs turn on. To determine if there is a load, the device does a load check. This operation waits for about three seconds and then must see no load for two successive load monitor cycles (256ms apart).

During the POR operation, the RAM registers are all reset to default conditions from values saved in the EEPROM.

When the cell voltages drop, the ISL94202 remains on if the V_{DD} voltage remains above 1V and the VRGO voltage is above 2.25V. This is to maintain operation of the device in the event of a short drop in cell voltage due to a pack short-circuit condition. In the event of a longer battery stack voltage drop, the device will return to a power-down condition if V_{DD} drops below a POR threshold of about 3.5V when V_{RGO} is below 2.25V (see Figures 6.14 and 6.15).

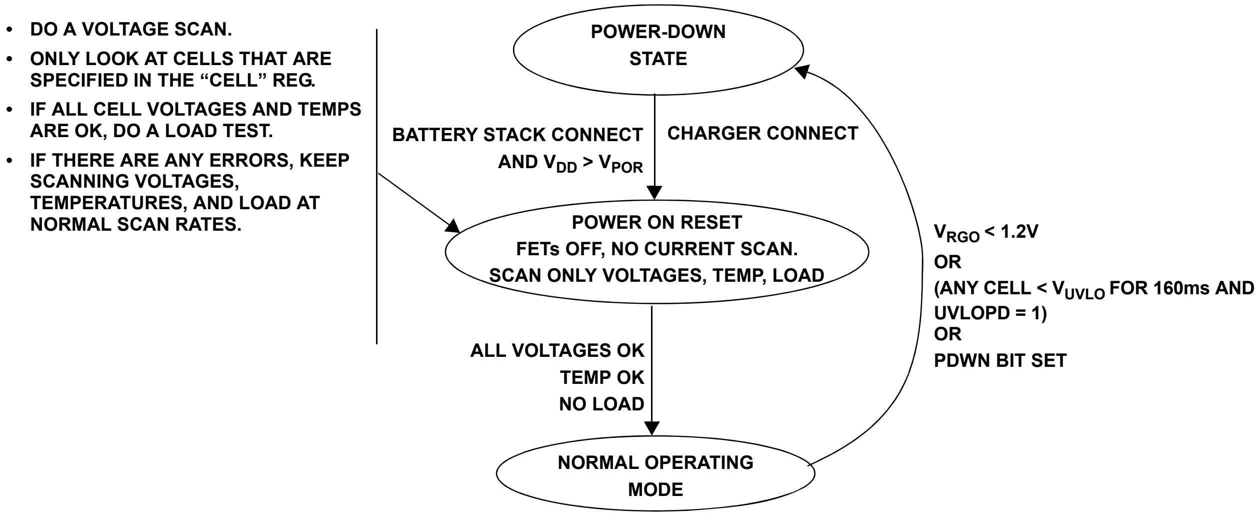


Figure 6.14 Power-On Reset State Machine

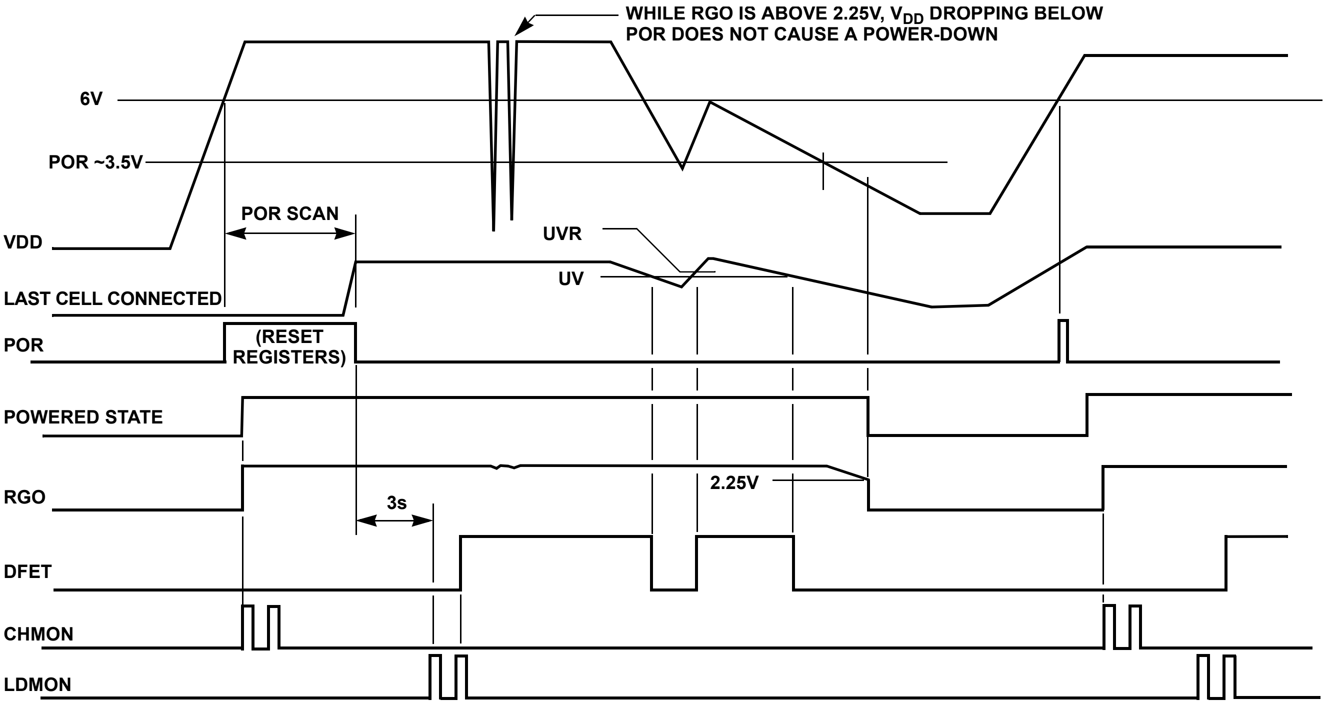


Figure 6.15 Power-Up/Power-Down Low Voltage Waveforms

6.2 Wake-Up Circuit

When in Sleep mode, the wake-up circuit detects that the output pin is pulled low (as might be the case when a load is attached to the pack and the FETs are off) or pulled high (as might be the case when the charger is connected and the FETs are off).

The wake-up circuit does not draw significant continuous current from the battery.

6.3 Low Power States

In order to minimize power consumption, most circuits are kept off when not being used and items are sampled when possible.

There are five power states in the device (see Figure 6.16).

6.3.1 Normal mode

This is the normal monitoring/scan mode. In this mode, the device monitors the current continuously and scans the voltages every 32ms. If balancing is called for, then the device activates external balancing components. All necessary circuits are on and unnecessary circuits are off.

During the scan, the ISL94202 draws more current as it activates the input level shifter, the ADC, and data processing. Between scans, circuits turn off to minimize power consumption.

6.3.2 Idle mode

If there is no current flowing for 0 to 15 minutes (set in the MOD register), then the device enters the Idle mode. In this mode, voltage scanning slows to every 256ms per scan. The FETs and the LDO remain on. In this mode, the device consumes less current, because there is more time between scans.

When the ISL94202 detects any charge or discharge current, the device exits the Idle mode and returns to the Normal mode of operation.

The device does not automatically enter the Idle mode if the µCSCAN bit is set to “1”, because the microcontroller is in charge of performing the scan and controlling the operation.

Setting the Idle bit to “1” forces the device to enter Idle mode, regardless of current flow. When a µC sets the Idle bit, the device remains in Idle, regardless of the timer or the current. Setting the mode control bits to “0” allows the device to control the mode.

6.3.3 Doze Mode

While in Idle mode, if there is no current flowing for another 0 to 16 minutes (same value as the idle timer), the device enters the Doze mode, where cell voltage sampling occurs every 512ms. The FETs and the LDO remain on. In this mode, the device consumes less current than in Idle mode, because there is more time between scans.

When the ISL94202 detects any charge or discharge current, the device exits Doze mode and returns to the Normal mode.

The device does not automatically enter the Idle mode if the µCSCAN bit is set to “1”, because the microcontroller is in charge of performing the scan and controlling the operation.

Setting the Doze bit forces the device to enter the Doze mode, regardless of the current flow. When a microcontroller sets the Doze bit, the device remains in Doze mode regardless of the timer or the current. Setting the mode control bits to “0” allows the device to control the mode.

Note: Setting the Idle/Doze timer to 0 immediately forces the device into the Doze mode when there is no current.

6.3.4 Sleep Mode

The ISL94202 enters the Sleep mode when the voltage on the cells drops below the sleep voltage threshold for a period of time, specified by the sleep delay timer. To prevent the device from entering the Sleep mode by a low voltage on the cells, the Sleep Voltage Level (SLL) register can be set to “0”.

The device can also enter the Sleep mode from the Doze mode if there has been no detected current for more than the duration of the Sleep mode timer (set in the MOD register). In this case, the device remains in Doze mode until there has been no current for 0 to 240 minutes (with 16 minute steps).

The external microcontroller forces the ISL94202 to enter Sleep mode by writing to the Sleep bit (Register 88H). Setting the Sleep bit forces the Sleep mode, regardless of the current flow.

Note: If both Idle/Doze and Sleep timers are set to "0", the device immediately goes to sleep. To recover from this condition, apply current to the device or hold the LDMON pin low (or CHMON pin high) and write non-zero values to the registers.

While in the Sleep mode, everything is off except for the 2.5V regulator and the wake up circuits. The device can be waken by LDMON connection to a load or CHMON connection to a charger.

6.3.5 Power-Down Mode

This mode occurs when the voltage on the pack is too low for proper operation. This occurs when:

- V_{DD} is less than the POR threshold and RGO < 2.25V. This condition occurs if cells discharge over a long period of time.
- V_{DD} is less than 1V and RGO > 2.25V. This condition can occur during a short-circuit with minimum capacity cells. The V_{DD} drops out, but the RGO cap maintains the logic supply.
- Any cell voltage is less than the UVLO threshold for more than about 160ms (and UVLOPD = 1).
- Commanded by an external µC.

Recovering out of any low power state brings the ISL94202 into the Normal operating mode.

6.3.6 Exceptions

There is one exception to the normal sequence of mode management. When the microcontroller sets the µCSCAN bit, the internal scan stops. This means that the device no longer looks for the conditions required for sleep. The external microcontroller needs to manage the modes of operation.

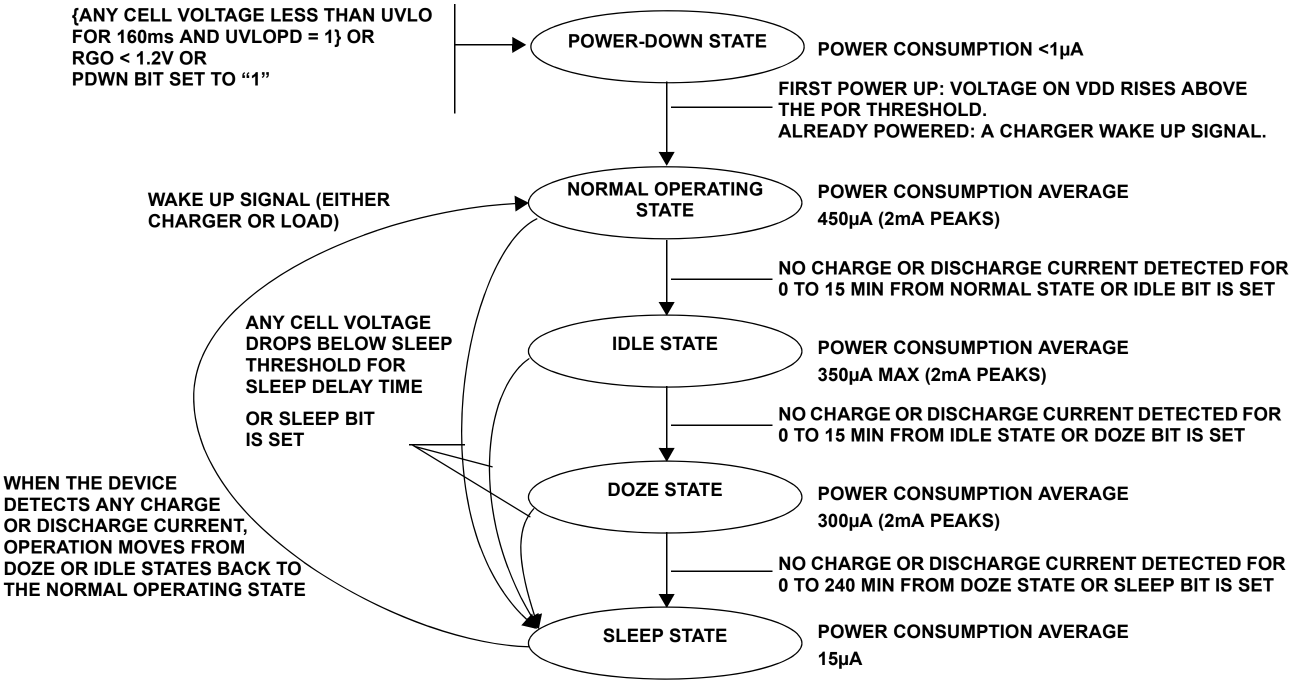


Figure 6.16 ISL94202 Power States

7. Typical Operating Conditions

Table 7.2 shows some typical device operating parameters.

Table 7.2 Typical Operating Conditions

Function	Typical	Unit
ADC Resolution	14	Bits
ADC Results Saved (and calibrated)	12	Bits
ADC Conversion Time	10	µs
Overcurrent/Short-Circuit Scan Time	Continuous	
Voltage Scan Time (Time per Cell) Includes Settling Time	125	µs
Voltage Protection Scan Rate (Time between scans) Normal Mode; Idle Mode Doze Mode	32 256 512	ms
Internal Over-temperature Turn-on/Turn-off Delay Time	128	ms
External Temperature Autoscan On Time; TEMPO = 2.5V	0.2	ms
External Temperature Autoscan Off Time; TEMPO = 0V Normal Mode Idle Mode Doze Mode	128 1024 2048	ms
Wake-Up Delay from Sleep. Time to Turn On Power FETs Following Load or Charger Connection. All Pack Conditions OK.	140	ms
Wake-Up Delay from Shutdown or Initial Power-Up. Time to Turn On Power FETs Following Charger Connection. All Pack Conditions OK.	3	sec
Default Idle/Doze Mode Delay Times	10	min
Default Sleep Mode Delay Time	90	min

8. Cell Fail Detection

The Cell Fail (CELLF) condition indicates that the difference between the highest voltage cell and the lowest voltage cell exceeds a programmed threshold (as specified in the CBDU register). Once detected, the CELLF condition turns off the cell balance FETs and the power FETs, but only if the µCFET bit = “0.” Setting the µCFET bit = 1 prevents the power FETs from turning off during a CELLF condition. The microcontroller is then responsible for the power FET control.

An EEPROM bit, CFPSD, when set to “1”, enables the PSD activation when the ISL94202 detects a Cell Fail condition. When CELLF = 1 and CFPSD = 1, the power FETs and cell balance FETs turn off, PLUS the PSD output goes active. The pack designer can use the PSD pin output to deactivate the pack by blowing a fuse.

The CELLF function can be disabled by setting the CBDU value to FFFH. In this case, the voltage differential can never exceed the limit. However, disabling the cell fail condition also disables the open-wire detection (see “Open-Wire Detection” on page 34).

9. Open-Wire Detection

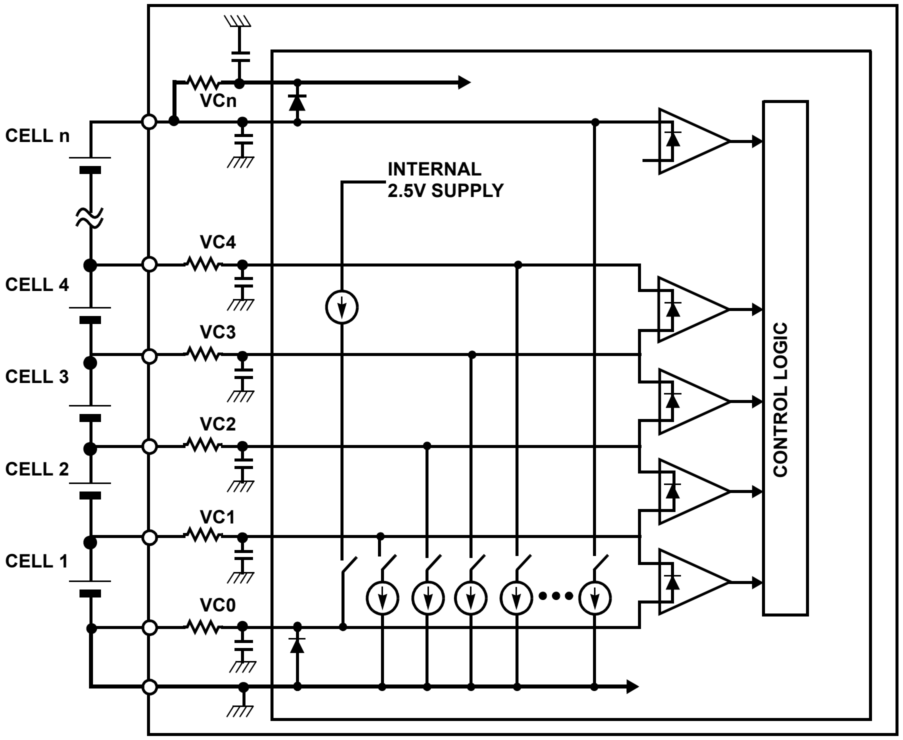
The ISL94202 device has a special, open-battery wire detection function that prevents the cells from being excessively charged or discharged by turning off the power FETs if there is an open wire. Additionally, the open-wire detection function prevents the operation of cell balancing when there is an open wire. Cell balancing with an open wire should be avoided for two reasons. First, an open wire compromises cell balancing. Second, excessive voltage may appear on the ISL94202 VCn input pins if the cell balance turns on the external balancing FET when there is an open wire. Internal clamps and input series resistors prevent damage as a result of short term exposure to higher input voltages.

The open-wire feature uses built in circuits to force short pulses of current into or out of the input capacitors (see Figure 9.17). When there is no open wire, the battery cell itself changes little in response to the open-wire test.

The open-wire operation is disabled by setting a control bit (DOWD) to “1”. When enabled (DOWD = 0), the ISL94202 performs an open-wire test when the CELLF condition exists and then once every 32 voltage scans as long as the CELLF condition remains. A CELLF condition is the first indication that there might be an open wire.

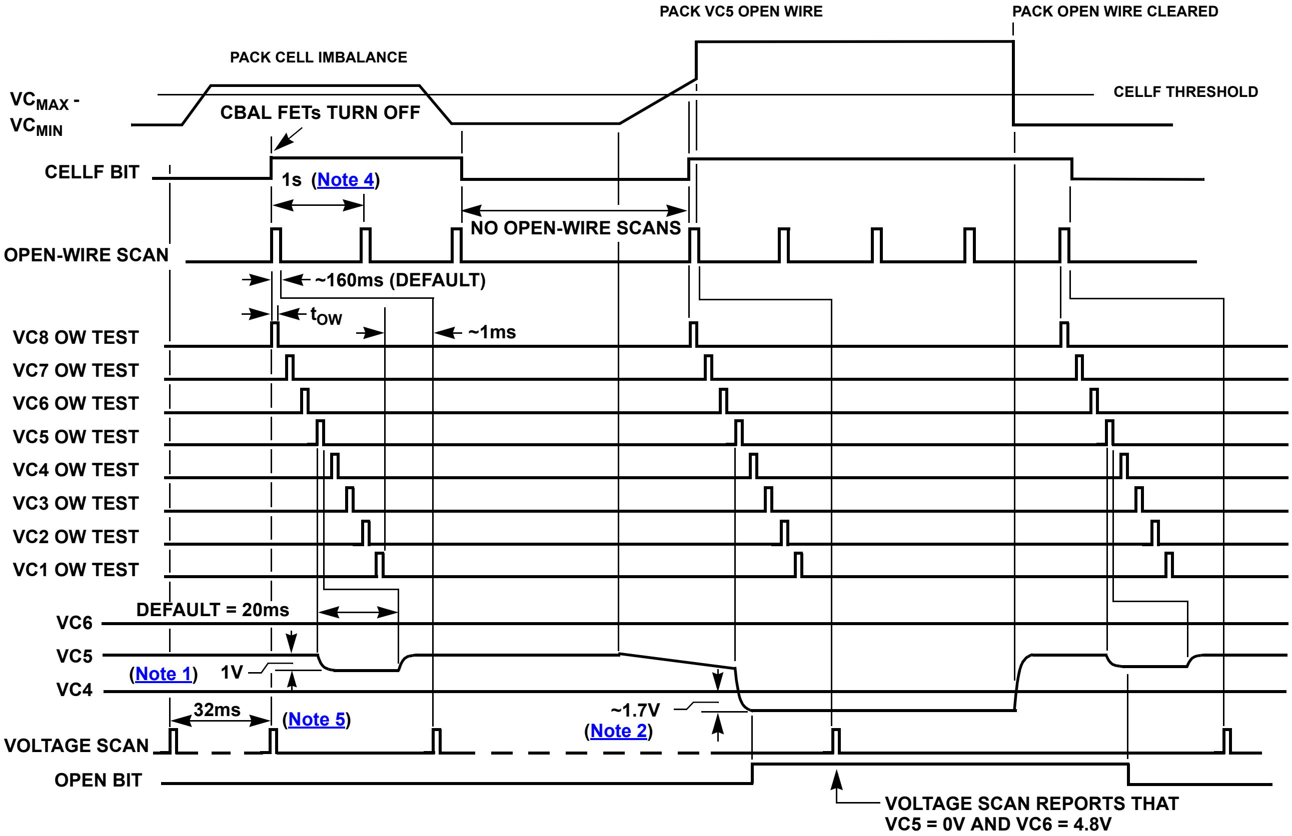
In operation, the open-wire circuit pulls (or pushes) 1mA of current sequentially on each VCn input for a period of time. The open-wire on-time is programmable by a value in the OWT register. The pulse duration is programmable between 1µs and 512ms. The default values for current and time are 1mA current and 1ms duration. Note that, in the absence of a battery cell, 1mA input current, along with an external capacitor of 4.7nF, changes the voltage of the input to the open-wire threshold of -1.4V (relative to the adjacent cell) within 30µs. With the cell present, the voltage will have a negligible change.

Each input has a comparator that detects if the voltage on an input drops more than 1.4V below the voltage of the cell below. Exceptions are VC1 and VC0. For VC1, the circuit looks to see if the voltage drops below 1V. For VC0, the circuit looks to see if the voltage exceeds 1.4V. If any comparator trips, then the device sets an OPEN error flag indicating an open-wire failure and disables cell balancing. See Figure 9.18 on page 35 for sample timing.



NOTE: THE OPEN-WIRE TEST IS RUN ONLY IF THE DEVICE DETECTS THE CELLF CONDITION AND THEN ONCE EVERY 32 VOLTAGE SCANS WHILE A CELLF CONDITION EXISTS. EACH CURRENT SOURCE IS TURNED ON SEQUENTIALLY.

Figure 9.17 Open-Wire Detection



Notes:
1. Voltage drop = 1mA * 1kΩ = 1V.
2. Voltage = V_F of CB5 Balance FET body diode + (1mA * 1kΩ).
3. OWPSD bit = 0.
4. This time is 8s in Idle and 16s in Doze.
5. This 32ms scan rate increases to 256ms in Idle and 512ms in Doze.

Figure 9.18 Open-Wire Test Timing

With the open-wire setting of 1mA, input resistors of 1kΩ create a voltage drop of 1V. This voltage drop, combined with the body diode clamp of the cell balance FET, provides the -1.4V needed to detect an open wire. For this reason and for the increased protection, it is not recommended that smaller input series resistors be used. For example, with a 100Ω input resistor, the voltage across the input resistor drops only 0.1V. This will not allow the input open-wire detection hardware to trigger (although the digital detection of an open wire still works, the hardware detection automatically turns off the open-wire current).

Input resistors larger than 1kΩ may be desired to increase the input filtering. This is allowed in the open-wire test, by providing an increase in the detection time (by changing the OWT value.) However, increasing the input resistors can significantly affect measurement accuracy. The ISL94202 has up to 2µA variation in the input measurement current. This amounts to about 2mV measurement error with 1k resistors (this error has been factory calibrated out). However, 10kΩ resistors can result in up to 20mV measurement errors. To increase the input filtering, the preferred method is to increase the size of the capacitors.

Depending on the selection of the input filter components, the internal open-wire comparators may not detect an open-wire condition. This might happen if the input resistor is small. In this case, the body diode of the cell balance FET may clamp the input before it reaches the open-wire detection threshold. To overcome this limitation and provide a redundant open-wire detection, at the end of the open-wire scan, all input voltages are converted to digital values. If any digital value equals 0V (minimum) or 4.8V (maximum), the device sets an OPEN error flag indicating an open-wire failure.

When an open-wire condition occurs and the “Open-Wire Power Shutdown” (OWPSD) bit is equal to “0”, the ISL94202 turns off all power FETs and the cell balance FETs, but does not set the PSD output. While in this condition, the device continues to operate normally in all other ways (i.e., the cells are scanned and the current monitored. As time passes, the device drops into lower power modes).

When an open-wire condition occurs and OWPSD = 1, the OPEN flag is set, the ISL94202 turns off all power FETs, and the cell balance FETs and the ISL94202 sets the PSD output port active.

The device can automatically recover from an open-wire condition, because the open-wire test is still functional, unless the OWPSD bit equals 1 and the PSD pin blows a fuse in the pack. If the open-wire test finds that the open wire has been cleared, then OPEN bit is reset and other tests determine whether conditions allow the power FETs to turn back on.

The open-wire test hardware has two limitations. First, it depends on the CELLF indicator. If the Cell Balance Maximum Voltage Delta (CBDU) value is set to high (FFFh for example), then the device may never detect a CELLF condition. The second limitation is that the open-wire test does not happen immediately. First, a scan must detect a CELLF condition. CELLF detection happens in a maximum of 32ms (Normal mode) or in a maximum of 256ms (Doze mode). Once CELLF is detected, the open-wire test occurs on the next scan, 32ms to 256ms later.

10. Current and Voltage Monitoring

There are two main automatic processes in the ISL94202. The first are the current monitor and overcurrent shutdown circuits. The second are the voltage, temperature, and current analog-to-digital scan circuits.

10.1 Current Monitor

The current monitor is an analog detection circuit that tracks the charge and discharge current and current direction. The current monitor circuit is on all the time, except in Sleep and Power-Down modes.

The current monitor compares the voltage across the sense resistor to several different thresholds. These are short-circuit (discharge), overcurrent (discharge), and overcurrent (charge). If the measured voltage exceeds the specified limit, for a specified duration of time, the ISL94202 acts to protect the system, as described in the following section.

The current monitor also tracks the direction of the current. This is a low-level detection and indicates the presence of a charge or discharge current. If either condition is detected, the ISL94202 sets an appropriate flag.

10.2 Current Sense

The current-sense element is on the high-side of the battery pack.

The current-sense circuit has a gain x5, x50, or x500. The sense amplifier allows a very wide range of currents to be monitored. The gain settings allow a sense resistor in the range of 0.3mΩ to 5mΩ. A diagram of the current-sense circuit is shown in Figure 10.19.

There are two parts of the current-sense circuit. The first part is a digital current monitor circuit. This circuit allows the current to be tracked by an external microcontroller or computer. The current-sense amplifier gain in this current measurement is set by the [CG1:CG0] bits. The 14-bit offset adjusted ADC result of the conversion of the voltage across the current-sense resistor is saved to RAM, as well as a 12-bit value that is used for threshold comparisons. The offset adjustment is based on a “factory calibration” value saved in EEPROM.

The digital readouts cover the input voltage ranges shown in Table 10.3.

Table 10.3 Maximum Current Measurement Range

Gain Setting	Voltage Range (mV)	Current Range (RSENSE = 1mΩ)
5x	-250 to 250	-250A to 250A
50x	-25 to 25	-25A to 25A
500x	-2.5 to 2.5	-2.5A to 2.5A

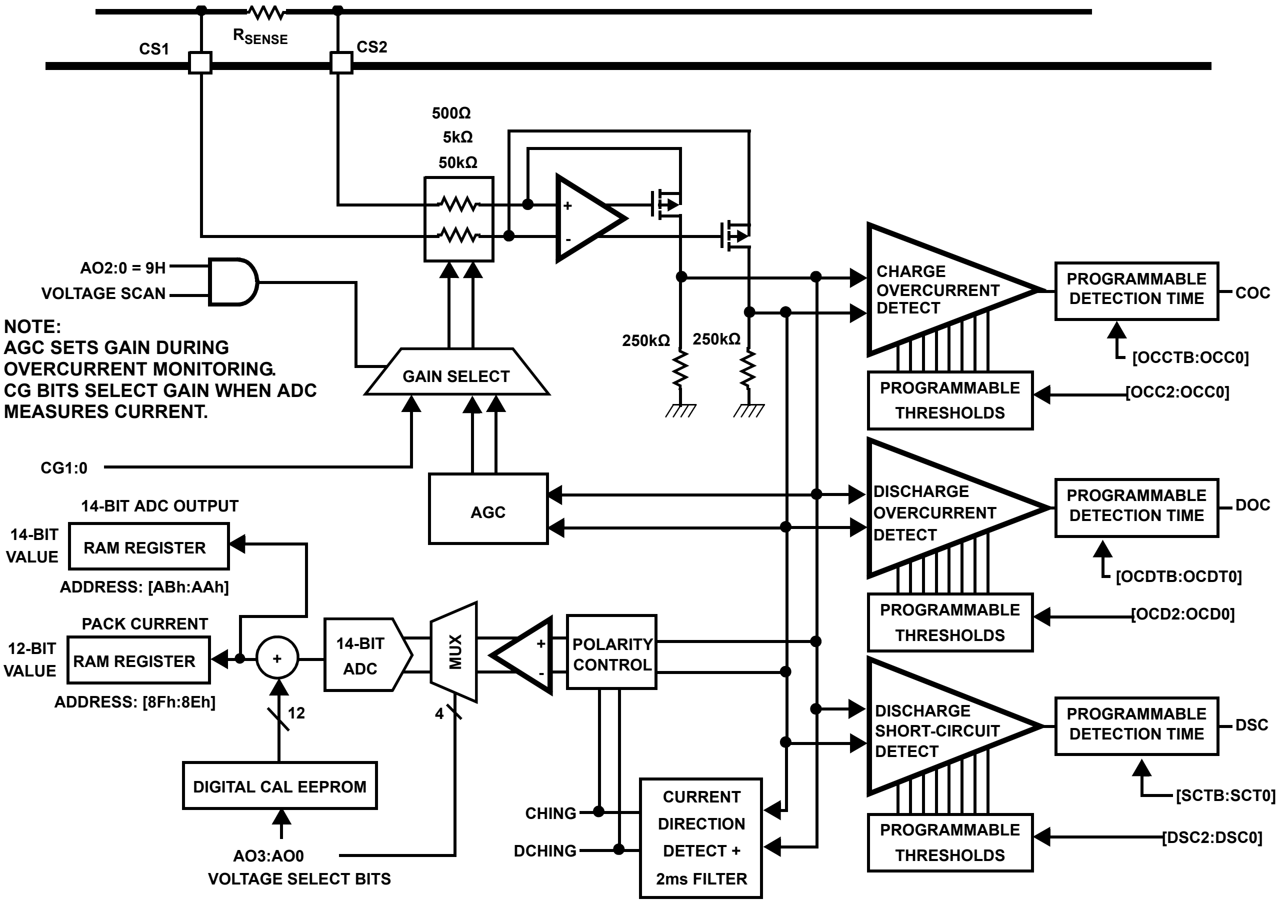


Figure 10.19 Block Diagram for Overcurrent Detect and Current Monitoring

The second part is the analog current direction, overcurrent, and short-circuit detect mechanisms. This circuit is on all the time. During the operation of the overcurrent detection circuit, the sense amplifier gain is automatically controlled.

For current direction detection, there is a 2ms digital delay for getting into or out of either direction condition. This means that charge current detection circuit needs to detect an uninterrupted flow of current out of the pack for more than 2ms to indicate a discharge condition. Then, the current detector needs to identify that there is a charge current or no current for a continuous 2ms to remove the discharge condition.

The overvoltage and short-circuit detection thresholds are programmable using values in the EEPROM. The discharge overcurrent thresholds are shown in Table 10.4. The charge overcurrent thresholds are shown in Table 10.5. The discharge short-circuit thresholds are shown in Table 10.6.

Table 10.4 Discharge Overcurrent Threshold Voltages

OCD SETTING	Threshold (mV)	Equivalent Current (A)				
		0.3mΩ	0.5mΩ	1mΩ	2mΩ	5mΩ
000	4	13.3	8	4	2	0.8
001	8	26.6	16	8	4	1.6
010	16	53.3	32	16	8	3.2
011	24	80	48	24	12	4.8
100	32	106.7	64	32	16	6.4
101	48	(Note 1)	96	48	24	9.6
110	64	(Note 1)	(Note 1)	64	32	12.8
111	96	(Note 1)	(Note 1)	(Note 1)	48	19.2

Note:

1. These selections may not be reasonable due to sense resistor power dissipation.

Table 10.5 Charge Overcurrent Threshold Voltages

OCC Setting	Threshold (mV)	Equivalent Current (A)				
		0.3mΩ	0.5mΩ	1mΩ	2mΩ	5mΩ
000	1	3.3	2	1	0.5	0.2
001	2	6.7	4	2	1	0.4
010	4	13.3	8	4	2	0.8
011	6	20	12	6	3	1.2
100	8	26.6	16	8	4	1.6
101	12	40	24	12	6	2.4
110	16	53.3	32	16	8	3.2
111	24	80	48	24	12	4.8

Table 10.6 Discharge Short-Circuit Current Threshold Voltages

DSC Setting	Threshold (mV)	Equivalent Current (A)				
		0.3mΩ	0.5mΩ	1mΩ	2mΩ	5mΩ
000	16	53.3	32	16	8	3.2
001	24	80	48	24	12	4.8
010	32	106.7	64	32	16	6.4
011	48	160	96	48	24	9.6
100	64	213.3	128	64	32	12.8
101	96	(Note 1)	192	96	48	19.2
110	128	(Note 1)	(Note 1)	128	64	25.6
111	256	(Note 1)	(Note 1)	Note	128	51.2

Note:

1. These selections may not be reasonable due to sense resistor power dissipation. Assumes short-circuit FET turn off in 10ms or less.

The charge and discharge overcurrent conditions and the discharge short-circuit condition need to be continuous for a period of time before an overcurrent condition is detected. These times are set by individual 12-bit timers. The timers consist of a 10-bit timer value and a 2-bit scale value (see Table 10.7).

Table 10.7 Charge/Discharge Overcurrent/Short-Circuit Delay Times

[OCCTB:A] [OCDTB:A] [SCTB:A] Scale Value	[OCCT9:0] [OCDT9:0] [SCT9:0] Delay (10-bit Value)
00	0 to 1024µs
01	0 to 1024ms
10	0 to 1024s
11	0 to 1024 minutes

10.3 Overcurrent and Short-Circuit Detection

The ISL94202 continually monitors current by mirroring the current across a current-sense resistor (between the CS1 and CS2 pins) to a resistor to ground.

- A discharge overcurrent condition exists when the voltage across the external sense resistor exceeds the discharge overcurrent threshold, set by the discharge overcurrent threshold bits [OCD2:OCD0], for an overcurrent time delay, set by the discharge overcurrent timeout bits [OCDTB:OCDT0]. This condition sets the DOC bit high. The LD_PRSNT bit is also set high at this time. If the µCFET bit is 0, then the power FETs turn off automatically. If the µCFET bit is 1, then the external µC must control the power FETs.
- A charge overcurrent condition exists when the voltage across the external sense resistor exceeds the charge overcurrent threshold, set by the charge overcurrent threshold bits [OCC2:OCC0], for an overcurrent time delay, set by the discharge overcurrent timeout bits [OCCTB:OCCT0]. This condition sets the COC bit high. The CH_PRSNT bit is also set high at this time. If the µCFET bit is 0, then the power FETs turn off automatically. If the µCFET bit is 1, then the external µC must control the power FETs.
- A discharge short-circuit condition exists when the voltage across the external sense resistor exceeds the discharge short-circuit threshold, set by the discharge short-circuit threshold bits [SCD2:SCD0], for an overcurrent time delay, set by the discharge short-circuit timeout bits [SCDTB:SCDT0]. This condition sets the DSC bit high. The LD_PRSNT bit is also set high at this time. The power FETs turn off automatically in a short-circuit condition, regardless of the condition of the µCFET bit.

10.4 Overcurrent and Short-Circuit Response (Discharge)

Once the ISL94202 enters the discharge overcurrent protection or short-circuit protection mode, the ISL94202 begins a load monitor state. In the load monitor state, the ISL94202 waits three seconds and then periodically checks the load by turning on the LDMON output for 0 to 15ms every 256ms. Program the pulse duration with the [LPW3:LPW0] bits in EEPROM.

When turned on, the recovery circuit outputs a small current (~60µA) to flow from the device and into the load. With a load present, the voltage on the LDMON pin is low and the LD_PRSNT bit remains set to “1”. When the load rises to a sufficiently high resistance, the voltage on the LDMON pin rises above the LDMON threshold and the LD_PRSNT bit is reset. When the load has been released for a sufficiently long period of time (two successive load sample periods) the ISL94202 recognizes that the conditions are OK and resets the DOC or DSC bits.

If the µCFET bit is 0, then the device automatically re-enables the power FETs by setting the DFET and CFET (or PCFET) bits to “1” (assuming all other conditions are within normal ranges). If the µCFET bit is 1, then the µC must turn on the power FETs.

An external microcontroller can override the automatic load monitoring of the device. It does this by taking control of the load monitor circuit (set the µCLMON bit = 1) and periodically pulsing the LMON_EN bit. When the microcontroller detects that LD_PRSNT = 0, the µC sets the CLR_LERR bit to “1” (to clear the error condition and reset the DOC or DSC bit) and sets the DFET and CFET (or PCFET) bits to “1” to turn on the power FETs.

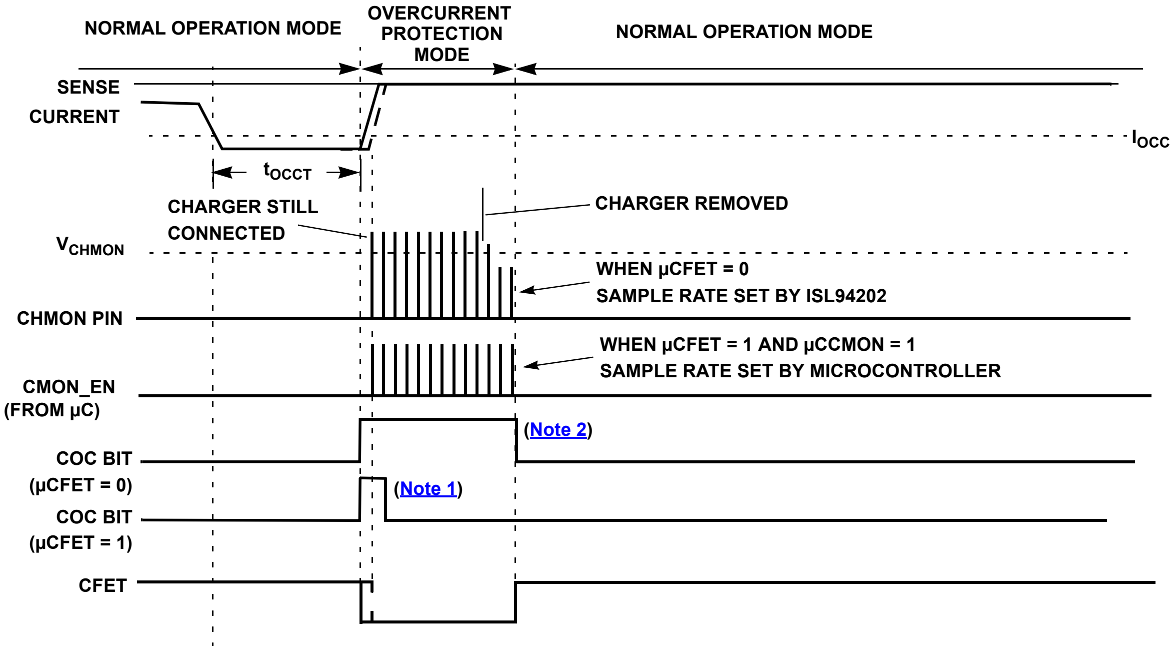
10.5 Overcurrent Response (Charge)

Once the ISL94202 enters the charge Overcurrent Protection mode, the ISL94202 begins a charger monitor state. In the charger monitor state, the ISL94202 periodically checks the charger connection by turning on the CHMON output for 0ms to 15ms every 256ms. Program the use duration with the [CPW3:CP0] bits in EEPROM.

When turned on, the recovery circuit checks the voltage on the CHMON pin. With a charger present, the voltage on the CHMON pin is high (>9V) and the CH_PRSNT bit remains set to “1”. When the charger connection is removed, the voltage on the CHMON pin falls below the CHMON threshold and the CH_PRSNT bit is reset. When the charger has been released for a sufficiently long period of time (two successive sample periods), the ISL94202 recognizes that the conditions are OK and clears the COC bit.

If the µCFET bit is 0, the device automatically re-enables the power FETs by setting the DFET and CFET (or PCFET) bits to “1” (assuming all other conditions are within normal ranges). If the µCFET bit is 1, then the µC must turn on the power FETs.

An external microcontroller can override the automatic charger monitoring of the device. It does this by taking control of the load monitor circuit (set the µCCMON bit = 1) and periodically pulsing the CMON_EN bit. When the microcontroller detects that CH_PRSNT = 0, the µC sets the CLR_CERR bit to “1” (to clear the error condition and reset the COC bit) and sets the DFET and CFET (or PCFET) bits to “1” to turn on the power FETs.



Notes:

1. When µCFET = 1, COC bit is reset when the CLR_CERR is set to “1”.
2. When µCFET = 0, COC is reset by the ISL94202 when the condition is released

Figure 10.20 Charge Overcurrent Protection Mode - Event Diagram

10.6 Microcontroller Overcurrent FET Control Protection

If any of the microcontroller override bits (µCSCAN, µCFET, µCLMON, µCCMON, or µCBAL) are set to “1” and the microcontroller does not send a valid slave byte to the ISL94202 within the watchdog timeout period, then the microcontroller control bits are all reset, the device turns off the power FETs and the balance FETs, and the $\overline{INT}$ output provides a 1µs pulse one time per second.

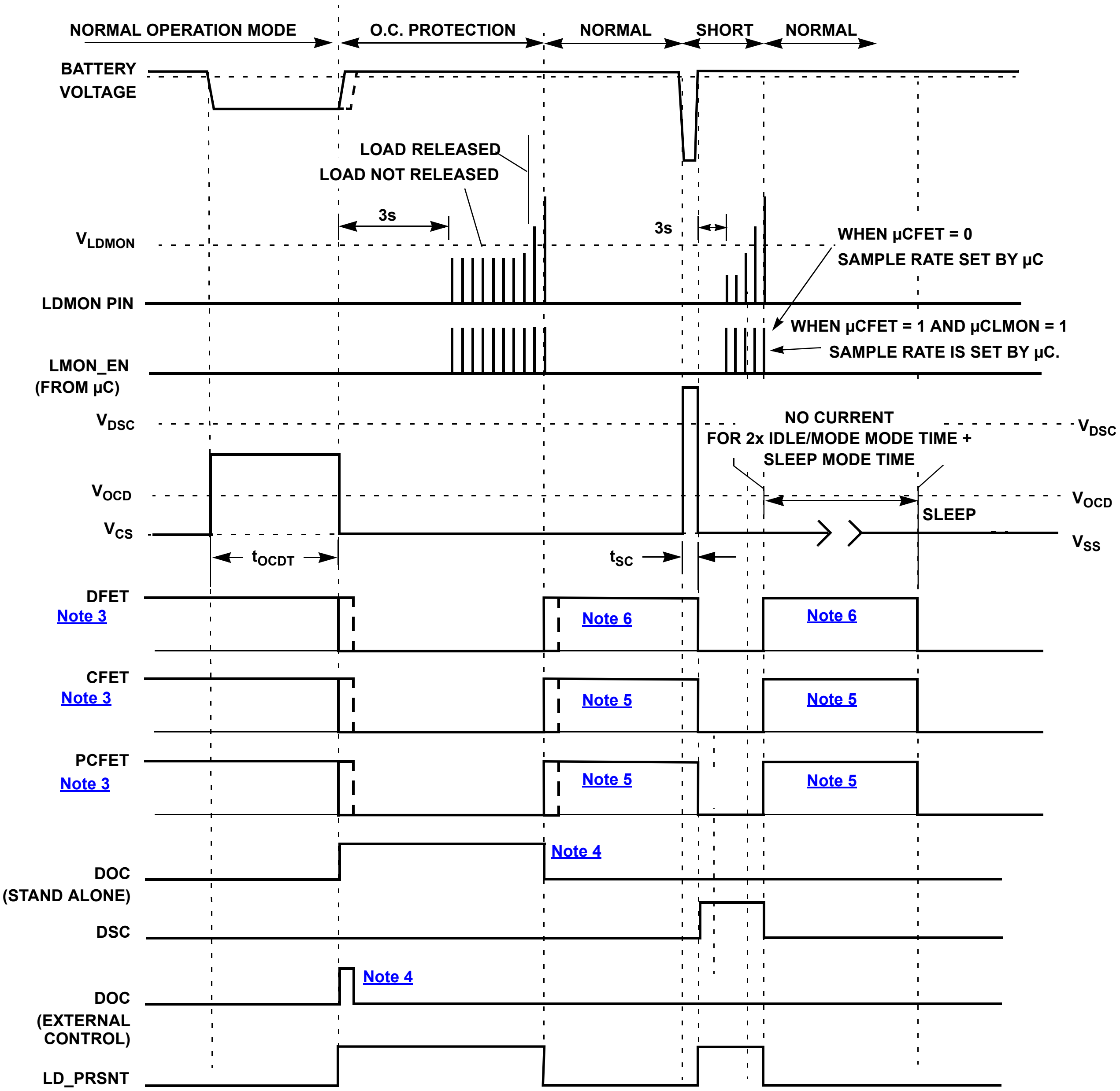


Figure 10.21 Discharge Overcurrent Protection Mode - Event Diagram

Notes:

3. When µCFET = 1, CFET, DFET and PCFET are controlled by external µC.
   When µCFET = 0, CFET, DFET and PCFET are controlled automatically by the ISL94202.
4. When µCFET = 1, DOC and DSC bits are reset by setting the CLR_LERR bit.
   When µCFET = 0, DOC and DSC are reset by the ISL94202 when the condition is released.
5. PCFET turns on if any cell voltage is less than LVCHG threshold. Otherwise CFET turns on.
6. DFET does not turn on if any cell is less than the UV threshold, unless the DFODUV bit is set.

10.7 Voltage, Temperature, and Current Scan

The voltage scan consists of the monitoring of the digital representation of the current, cell voltages, temperatures, pack voltage, and regulator voltage. This scan occurs once every 32ms, 256ms, or 512ms (depending on the mode of operation, see Figure 10.22). The temperature, pack voltage, and regulator voltage are scanned only every fourth scan. The open wire is scanned every 32nd scan as long as the CELLF condition exists.

After each measurement scan, the ISL94202 performs an offset adjustment and stores the values in RAM. After the values are stored, the state machine executes compare operations that determine if the pack is operating within limits. See Figure 10.22 for details on the scan sequence.

During manufacture, Intersil provides calibration values in the EEPROM for each cell voltage reading. When there is a new conversion for a particular voltage, the calibration is applied to the conversion.

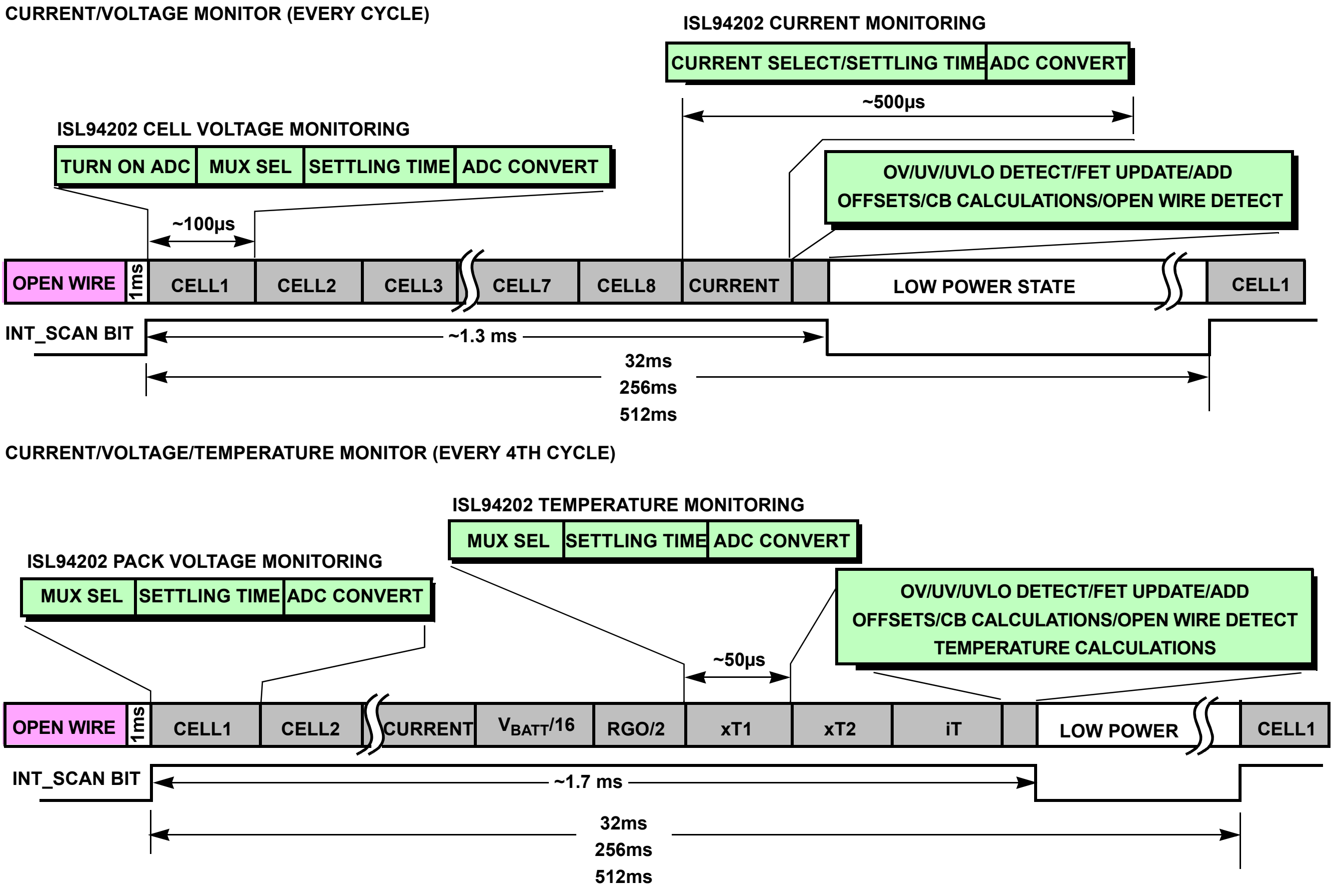


Figure 10.22 Cell Voltage, Current, Temperature Scanning

Notes:

7. The open-wire test performed every 32 voltage scans, if CELLF = 1, just prior to the scan.
8. FETs turn off immediately if there is an error, but they do not turn on until the end of the voltage scan (at "FET update" if everything else is OK). An exception to this is when a device wakes up when connected to a load. In this case, the FETs turn on immediately on wake-up, then a scan begins.
9. The voltage scan can be turned off by an external microcontroller by setting the µCSCAN bit. This bit is monitored by the watchdog timer, so if an external microcontroller stops communicating with the ISL94202 for more than the WDT period, this bit is automatically reset and the scan resumes.

10.8 Cell Voltage Monitoring

The circuit that monitors the input cell voltage multiplies the cell voltage by 3/8. The ADC converts this voltage to a digital value, using a 1.8V internal reference. The ADC produces a calibrated 14-bit value, but only 12 bits are stored in the cell registers (see Figure 10.23.)

In manufacturing, each cell voltage is calibrated at 3.6V per cell and at +25°C. This calibrated value is used for all subsequent voltage threshold comparisons.

The ISL94202 has two different overvoltage and undervoltage level comparisons, OVLO/UVLO and OV/UV. While both use the ADC converter output values and a digital comparator, the responses are different. The OVLO and UVLO levels are meant to be secondary thresholds above and below the OV and UV thresholds.

10.8.1 UVLO and OVLO

Because they provide a secondary safety condition, OVLO and UVLO can cause the pack to shut down, either permanently, as in the case of an OVLO when the PSD pin connects to an external fuse; or severely, as in the case of an UVLO when the device powers down and requires connection to a charger to recover.

The OVLO condition can be overridden by setting the OVLO threshold to FFFH or by an external µC setting the µCSCAN bit to override the internal automatic scan, then turning on the CFET. However, if the µC takes permanent control of the scan, the µC needs to take over the scan for all cells and all control functions, including comparisons of the cell voltage to OV and UV thresholds, managing time delays, and controlling all cell balance functions.

The UVLO response can be overridden by setting the UVLO threshold to 0V. The device can respond to the UVLO condition by entering the Power-Down mode (set UVLOPD in EEPROM to “1”) or by turning off the FETs and setting the UVLO bit (UVLOPD = “0”).

When the UVLOPD bit is set to “1” (indicating that the ISL94202 should power down during a UVLO condition) and the µCFET bit is set to “1” (indicating that the µC is in control of the FETs), the automatic UVLO control forces a power-down condition, overriding the µC FET control.

The UVLO and OVLO detection both have delays of 5 sample cycles (typically 160ms) to prevent noise generated entry into the mode.

The OVLO and UVLO values are each set by 12-bit values in EEPROM.

The OVLO has a recovery threshold of OVR and UVLO has a recovery threshold of UVR (if the response overrides have been set). If the response overrides are not set, then the recovery thresholds are usually irrelevant; for example, when the UVLO forces the device into a power-down condition or the OVLO condition caused a PSD controlled fuse to blow.

10.8.2 UV, OV, and Sleep

UV, OV, and SLP thresholds are set by individual 12-bit values.

UV and OV recovery thresholds are set by individual 12-bit values.

The voltage protection scan occurs once every 32ms in normal operation. If there has been no activity (no charge or discharge current) detected in a programmable period of 1 to 16 minutes, then the scan occurs every 256ms (Idle mode). If no charge or discharge condition has been detected in Idle mode for the programmable period, then the scan occurs every 512ms.

If an overvoltage, undervoltage, or sleep condition is detected and is pending, the scan rate remains unchanged. It can take longer to detect the fault condition in Idle or Doze modes. The scan rate is determined by the mode of operation and the mode of operation is determined solely by the time since pack charge/discharge current was detected.

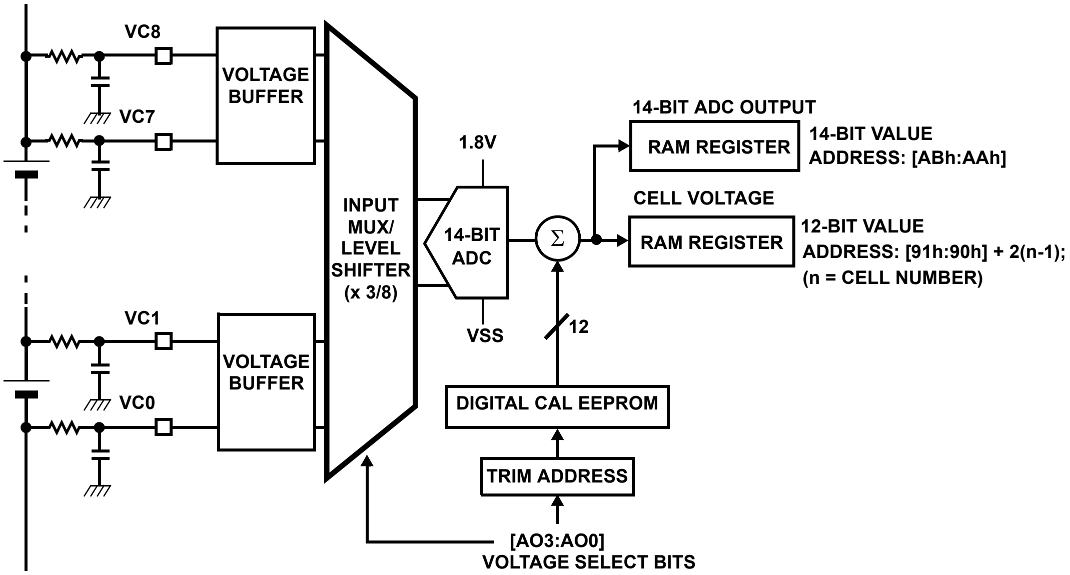


Figure 10.23 Block Diagram of Cell Voltage Capture

During a scan, each cell is monitored for overvoltage, undervoltage, and sleep voltage. The voltage will also be converted to an ADC value and be stored in memory.

If, during the scan, a voltage is outside the set limit, then a timer starts. There is one timer for all of the cells. If the condition remains on any cell or combination of cells for the duration of the time period, an error condition exists. This sets the appropriate flag and notifies the protection circuitry to take action (if automatic action is enabled).

The timeout delays for OV, UV, and Sleep are each 12-bit values stored in EEPROM (see Table 10.8).

Table 10.8 OV, UV, Sleep Delay Times

Scale Value	Delay (10-Bit Value)
00	0 to 1024µs
01	0 to 1024ms
10	0 to 1024s
11	0 to 1024min

The control logic for overvoltage, undervoltage, and sleep conditions is shown in Table 10.8, Figure 10.24 and Figure 10.25 on page 48.

10.9 Overvoltage Detection/Response

The device needs to monitor the voltage on each battery cell (V_{Cn}). If for any cell, $[V_{Cn\ -\ VC(n-1)}] > V_{OV}$ for a time exceeding t_{OV}, the device sets an OV flag. Then (if µCFET = 0), the ISL94202 turns the charge FET OFF, by setting the CFET bit to "0". Once the OV flag is set the pack has entered Overcharge Protection mode. The status of the discharge FET remains unaffected.

The charge FET remains off until the voltage on the overcharged cell drops back below a recovery level, V_{OVR}, for a recovery time period, t_{OVR}. The t_{OVR} time equals the t_{OV} time.

The detection timer and recovery timer are asynchronous to the voltage threshold. As a result, a setting of 1s can result in a delay time of 1s to 2s, depending on when the OV/OVR is detected. For a setting of 1000ms, the detection time will be within 1ms.

The device further continues to monitor the battery cell voltages and is released from overcharge protection mode when $[V_{Cn\ -\ VC(n-1)}] < V_{OVR}$ for more than the overcharge release time, for all cells.

When the device is released from overcharge protection mode, the charge FET is automatically switched ON (if µCFET = 0). When the device returns from Overcharge Protection mode, the status of the discharge FET remains unaffected.

During charge, if the voltage on any cell exceeds an End-Of-Charge threshold (EOCS), then an EOCHG bit is set and the $\overline{\text{EOC}}$ output is pulled low. The EOCHG bit and the $\overline{\text{EOC}}$ output resume normal conditions when the voltage on all cells drops back below the [EOCS - 117mV] threshold.

There is also an overvoltage lockout. When this level is reached, an OVLO bit is set, the PSD output is set, and the charge FET or precharge FET is immediately turned off (by setting the CFET or PCFET bit to "0"). The PSD output can be used to blow a fuse to protect the cells in the pack.

If, during an OV condition, the µCFET bit is set to "1", the microcontroller must control both turn off and turn on of the charge and precharge power FETs. This does not apply to the OVLO condition.

The device includes an option to turn the charge FET back on in an overvoltage condition, if there is discharge current flowing out of the pack. This option is set by the CFODOV (CFET ON During Overvoltage) Flag stored in EEPROM. Then, if the discharge current stops and there is still an overcharge condition on the cell, the device again disables the charge FET.

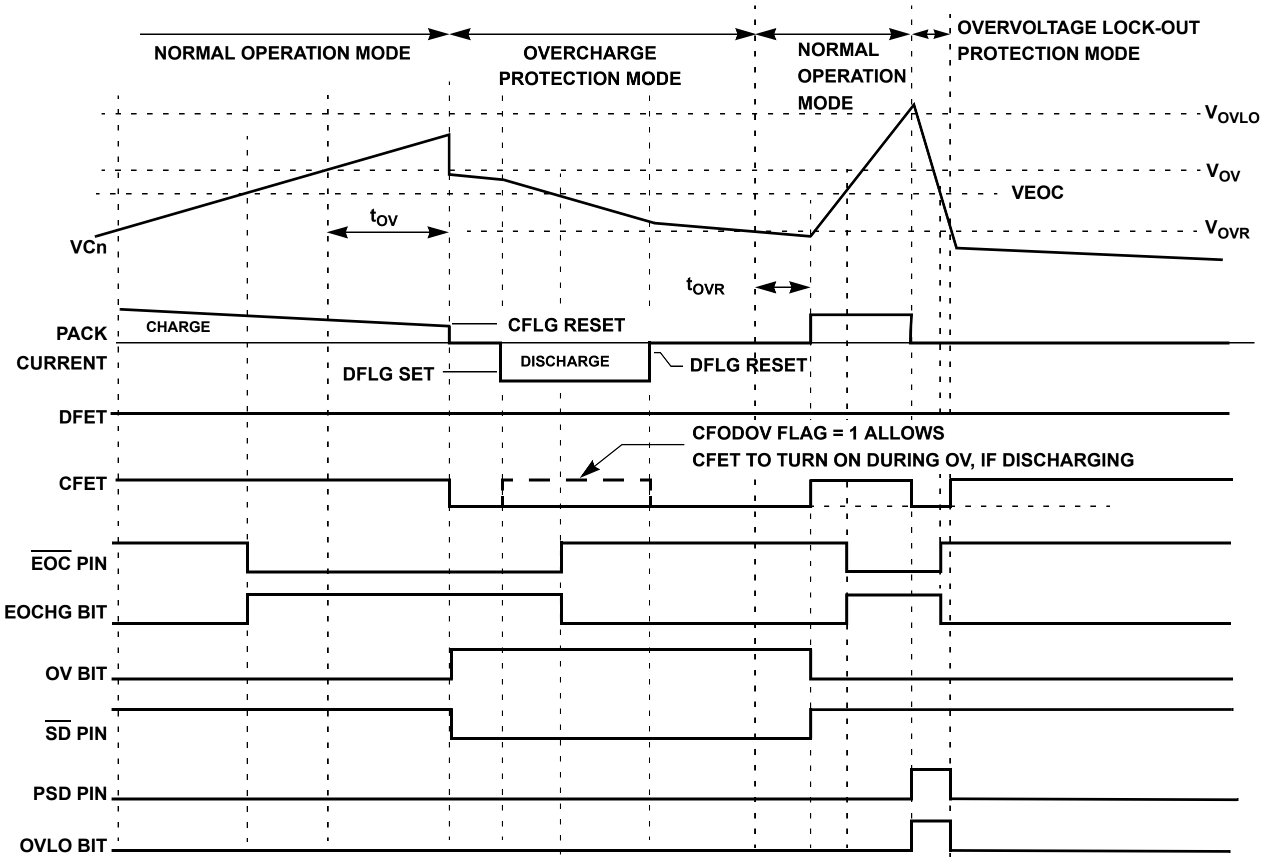


Figure 10.24 Overvoltage Protection Mode-Event Diagram

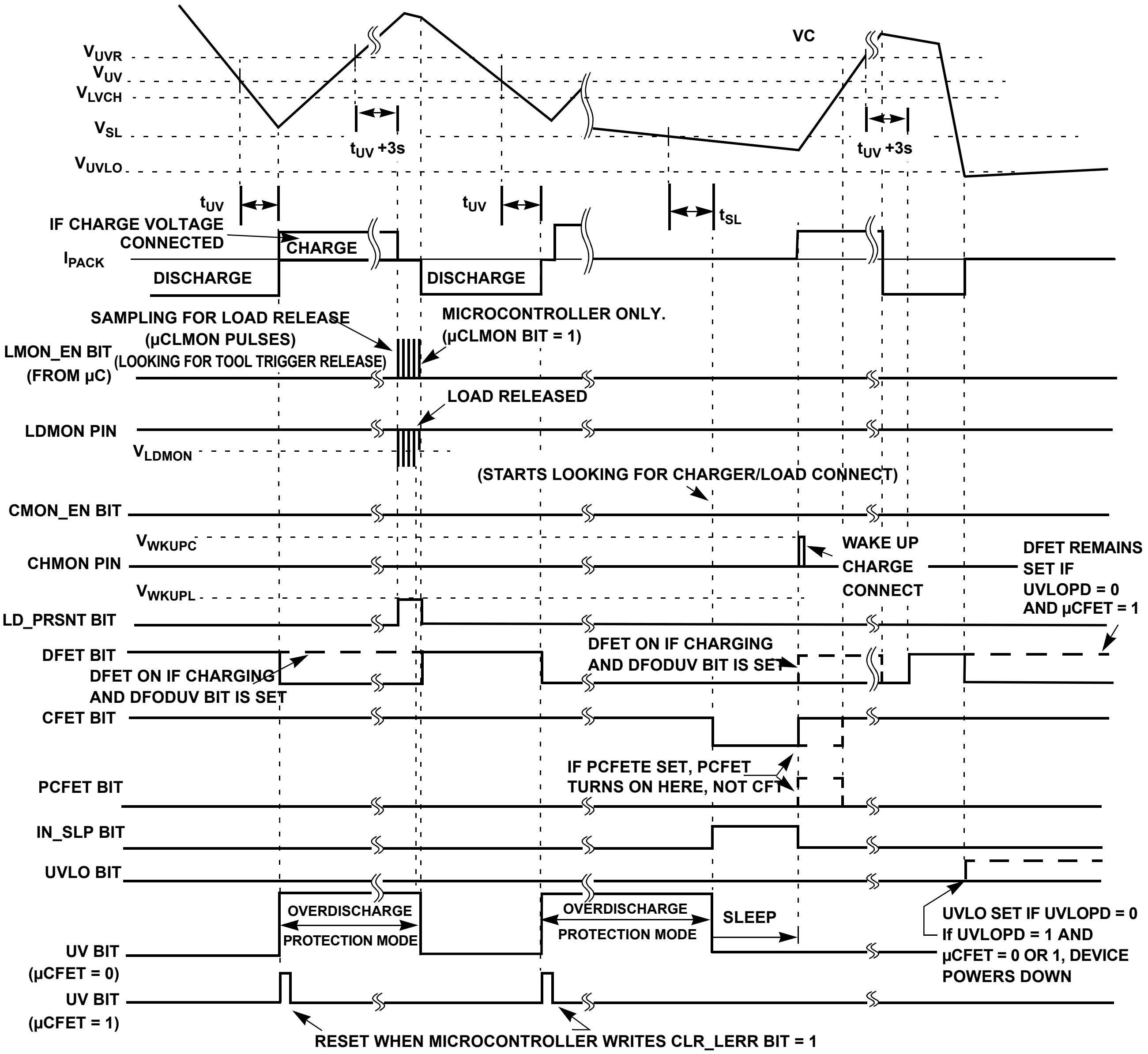


Figure 10.25 Undervoltage Protection Mode-Event Diagram

10.10 Undervoltage Detection/Response

If $V_{Cn} < V_{UV}$, for a time exceeding t_{UVT}, the cells are said to be in an overdischarge (undervoltage) state. In this condition, the ISL94202 sets a UV bit. If the µCFET bit is set to “0”, the ISL94202 also switches the discharge FET OFF (by setting the DFET bit = 0).

While any cell voltage is less than a low voltage charge threshold, and if the PCFETE bit is set, the PCFET output is turned on instead of the CFET output. This enables a precharge condition to limit the charge current to undervoltage cells.

From the undervoltage mode, if the cells recover to above a V_{UVR} level for a time exceeding t_{UVT} plus three seconds, the ISL94202 pulses the LDMON output once every 256ms and looks for the absence of a load. The pulses are of programmable duration (0ms to 15ms) using the [LPW3:LPW0] bits. During the pulse period, a small current (~60µA) is output into the load. If there is no load, then the LDMON voltage will be higher than the recovery threshold of 0.6V. When the load has been removed and the cells are above the undervoltage recovery level, the ISL94202 clears the UV bit and, if µCFET = 0, turns on the discharge FET and resumes normal operation.

Note, the t_{UV} detection timer and t_{UVR} recovery timer are asynchronous to the voltage threshold. As a result, a setting of 1s can result in a delay time of 1s to 2s (and a recovery time of 3s to 4s), depending on when the UV/UVR is detected. For a setting of 1000ms, the detection time will be within 1ms.

If any of the cells drop below a sleep threshold ($VCn < V_{SLP}$) for a period of time (t_{SLT}), the device sets the Sleep bit and (if µCFET = 0), the ISL94202 turns off both FETs (DFET and CFET = 0) and puts the pack into a Sleep mode by setting the Sleep bit to “1”. If the µCFET bit is set, the device does not go to sleep.

There is also an undervoltage lockout condition. This is detected by comparing the cell voltages to a programmable UVLO threshold. When any cell voltage drops below the UVLO threshold and remains below the threshold for five voltage scan periods (~160ms), a UVLO bit is set and the $\overline{SD}$ output pin goes active. If UVLOPD = 0 and µCFET = 0, the DFET is also turned off. If UVLOPD = 1, then the ISL94202 goes into a power-down state.

If the µCFET bit is set to “1”, the microcontroller must both turn off and turn on the discharge power FETs and control the sleep and power-down conditions.

The device includes an option to turn the discharge FET back on in an undervoltage condition, if there is a charge current flowing into the pack. This option is set by the DFODUV (DFET ON During Undervoltage) Flag stored in EEPROM. Then, if the charge current stops and there is still an undervoltage condition on the cell, the device again disables the discharge FET.

10.11 Temperature Monitoring/Response

As part of the normal voltage scan, the ISL94202 monitors both the temperature of the device and the temperature of two external temperature sensors. External Temperature 2 can be used to monitor the temperature of the FETs, instead of the cells, by setting the xT2M bit to “1”.

The temperature voltages have two gain settings (the same gain for all temperature inputs). For external temperatures, a TGain bit = 0, sets the gain to 2x (full scale input voltage = 0.9V). A TGain bit = 1 and sets the gain to 1x (full scale input voltage = 1.8V). See Figure 10.26.

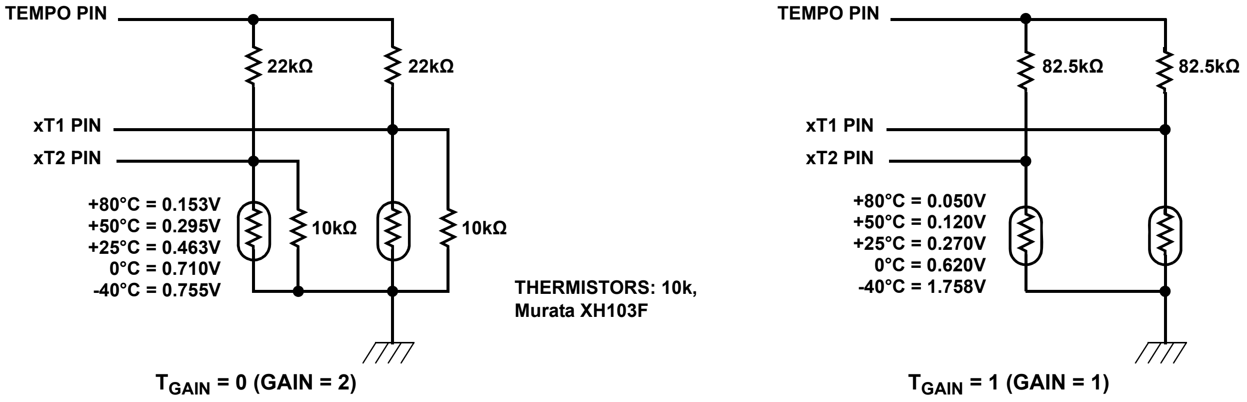
The default temperature gain setting is x2, so the temperature monitoring circuit of $T_{GAIN} = 0$ (GAIN = 2) is preferred. This configuration has other advantages. The temperature response is more linear and covers a wider temperature range before nearing the limits of the ADC reading.

The internal temperature reading converts from voltage to temperature using (EQ. 1) and (EQ. 2):

$$\text{TGain} = 1 \qquad \frac{\text{intTemp(mV)} \times 1000}{0.92635} - 273.15 = \text{ICTemp}(°\text{C}) \tag{EQ. 1}$$

$$\text{TGain} = 0 \qquad \frac{\text{intTemp(mV)} \times 1000}{1.8527} - 273.15 = \text{ICTemp}(°\text{C}) \tag{EQ. 2}$$

If the temperature of the IC (Internal Temp) goes above a programmed over-temperature threshold, then the ISL94202 sets an over-temperature flag (IOT), prevents cell balancing and turns off the FETs.



$T_{GAIN} = 0$ (GAIN = 2) $T_{GAIN} = 1$ (GAIN = 1)

Figure 10.26 External Temperature Circuits

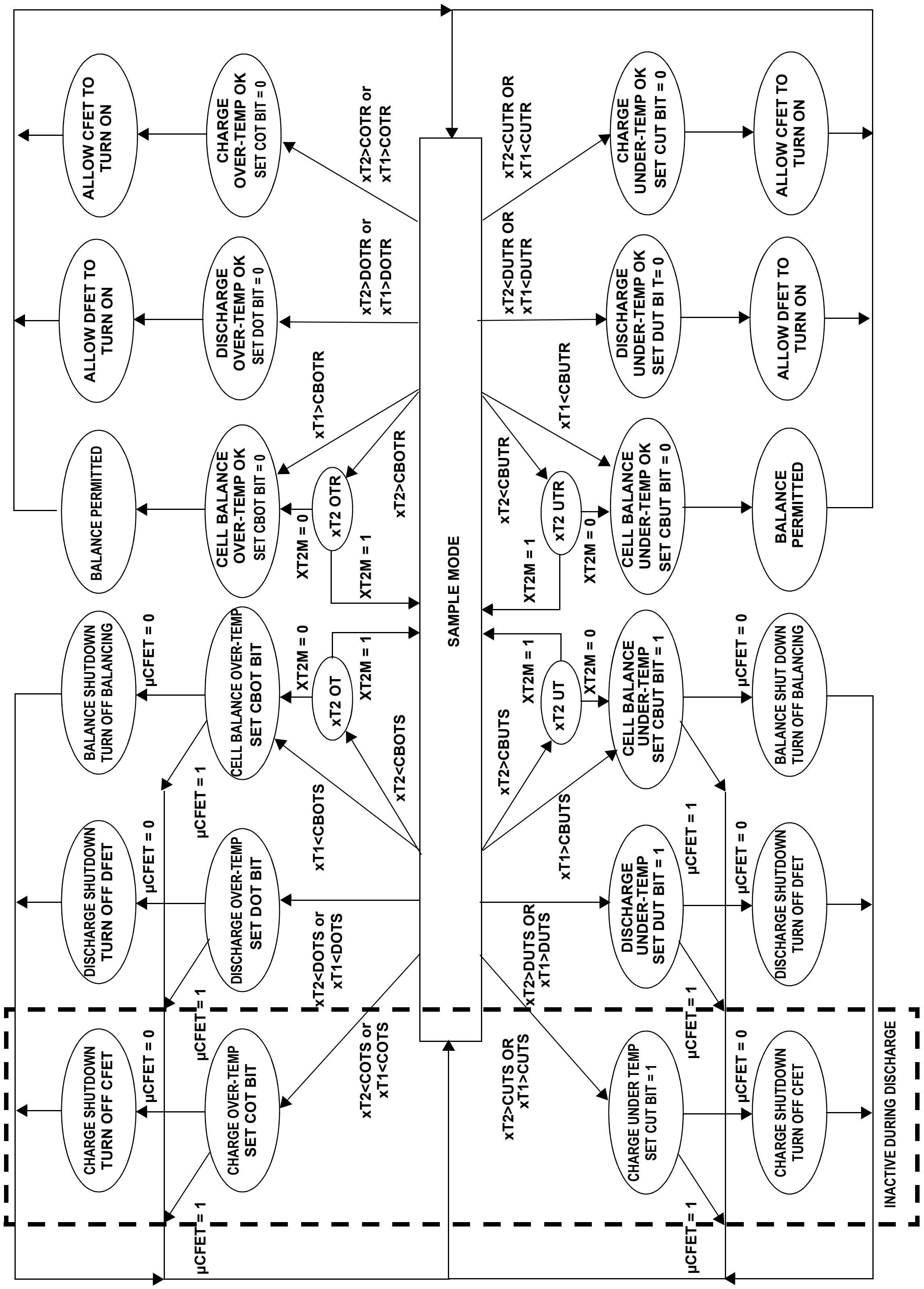


Figure 10.27 Temperature Management State Machine

10.11.1 Over-Temperature

If the temperature of either of the external temperature sensors (xT1 or xT2), as determined by an external resistor and thermistor, goes below any of the thresholds (charge, discharge, and cell balance as set by internal EEPROM values), indicating an over-temperature condition, the ISL94202 sets the corresponding over-temp flag.

If the automatic responses are enabled (µCFET = 0), the Charge Over-Temperature (COT) or Discharge Over-Temperature (DOT) flag is set and the corresponding charge or discharge FET is turned off. For series FET applications, COT will not shut off CFET during discharge regardless of µCFET setting. If the Cell Balance Over-Temperature (CBOT) flag is set, the device turns off the balancing outputs and prevents cell balancing while the condition exists.

If the automatic responses are disabled (µCFET = 1), then the ISL94202 only sets the flags and an external microcontroller responds to the condition.

An exception to the above occurs if the xT2 sensor is configured as a FET temperature indicator (XT2M = 1). In this case, the xT2 is not compared to the cell balance temperature thresholds, it is used only for power FET control.

10.11.2 Under-Temperature

If the temperature of either of the external temperature sensors (xT1 or xT2), as determined by an external resistor and thermistor, goes above any of the thresholds (charge, discharge, and cell balance as set by internal EEPROM values), indicating an under-temperature condition, the ISL94202 sets the corresponding under-temperature flag.

If the xT1 automatic responses are enabled (µCFET = 0), then the Charge Under-Temperature (CUT) or Discharge Under-Temperature (DUT) flag is set the corresponding charge or discharge FET is turned off. For series FET applications, CUT will not shut off CFET during discharge regardless of µCFET setting. If the Cell Balance Under-Temperature (CBUT) flag is set, the device turns off cell balancing outputs and prevents cell balancing.

If the xT2 automatic responses are disabled (µCFET = 1) then the ISL94202 only sets the flags and an external microcontroller responds to the condition.

An exception to the above occurs if the xT2 sensor is configured as a FET temperature indicator (XT2M = 1). In this case, the xT2 is not compared to the cell balance temperature thresholds. It is used only for power FET control).

For both xT1 and xT2, when the temperature drops back within a normal operating range, the over or under-temperature condition is reset.

10.12 Microcontroller Read of Voltages

An external microcontroller can read the value of any of the internally monitored voltages independently of the normal voltage scan. To do this requires that the µC first set the µCSCAN bit. This stops the internal scan and starts the watchdog timer. If the µC maintains this state, then communication must continue and the µC must manage all voltage and current pack control operations as well as implement the cell balance algorithms. However, if the µCSCAN bit remains set for a short period of time, the device continues to monitor voltages and control the pack operation.

Once the µCSCAN bit is set, the external µC writes to register 85H to select the desired voltage and to start the ADC conversion (set the ADCSTRT bit to "1" to start an ADC conversion). Once the conversion is complete, the results are read from the ADC registers [ADCD:ADC0]. The result is a 14-bit value. The ADC conversion takes about 100µs or the µC can poll the I^2C link waiting for an ACK to indicate that the ADC conversion is complete.

If the µCSCAN bit is set when the ISL94202 internal scan is scheduled, then the internal scan pauses until the µCSCAN bit is cleared and the internal scan occurs immediately.

Reading an ADC value from the µC requires the following sequence (and time) to complete:

Table 10.9 µC Controlled Measurement of Individual Voltages

Step	Operation	Number I^2CCycles	Time at 400kHz I^2C CLK (ea.) (µs)	Time (Cumulative) (µs)
1	Set µCSCAN bit	29	72.5	72.5
2	Set voltage and start ADC	29	72.5	145
3	Wait for ADC complete	N/A	110	255
4	Read register AB	29	72.5	327.5
5	Read register AA	29	72.5	410
6	Clear µCSCAN bit	29	100	472.5

To sample more than one time (for averaging), repeat Steps 2 through 5 as many times as desired. However, if this is a continuous operation, care must be taken to monitor other pack functions or to pause long enough for the ISL94202 internal operations to collect data to control the pack. A burst of five measurements takes about 1.8ms.

10.13 Voltage Conversions

To convert from the digital value stored in the register to a “real world” voltage, the following conversion equations should be used.

The term “HEXvalue_{10}” means the Binary to Decimal conversion of the register value.

10.13.1 Cell Voltages

$$\text{Cell Voltage} = \frac{\text{HEXvalue}_{10} \times 1.8 \times 8}{4095 \times 3} \qquad \text{(EQ. 3)}$$

The cell voltage conversion equation is also used to set the voltage thresholds.

10.13.2 Pack Current

$$\text{Pack Current} = \frac{\text{HEXvalue}_{10} \times 1.8}{4095 \times \text{Gain} \times \text{SenseR}} \qquad \text{(EQ. 4)}$$

Gain is the gain setting in register 85H, set by the [CG1:CG0] bits.

SenseR is the sense resistor value in Ohms.

This pack current reading is valid only when the current direction indicators show that there is a charge or discharge current. If the current is too low for the indicators to show current flowing, then use the 14-bit value to estimate the current. See “14-bit Register” on page 53.

10.13.3 Temperature

$$\text{Temperature} = \frac{\text{HEXvalue}_{10} \times 1.8}{4095} \qquad \text{(EQ. 5)}$$

Equation 5 converts the register value to a voltage, but the temperature then is converted to a temperature depending on the external arrangement of thermistor and resistors. See “Temperature Monitoring/Response” on page 49.

10.13.4 14-bit Register

If HEXvalue_{10} is greater than or equal to 8191, then:

$$\text{14-bit value} = \frac{(\text{HEXvalue}_{10} - 16384) \times 1.8}{8191} \qquad \text{(EQ. 6)}$$

If HEXvalue_{10} is less than 8191, then:

$$\text{14-bit value} = \frac{\text{HEXvalue}_{10} \times 1.8}{8191} \qquad \text{(EQ. 7)}$$

Once the voltage value is obtained, if the measurement is a cell voltage, then the value should be multiplied by 8/3. A temperature value is used “as-is”, but the voltage value is converted to temperature by including the external temperature circuits into the conversion.

To determine pack current from this 14-bit value requires the following computations.

First, if both current direction flags show zero current, then the external controller must apply an offset. Measure the 14-bit voltage when there is a pack current of 0. Then subtract this offset from the 14-bit current-sense measurement value and take the absolute value of the result. If either of the current direction flags indicate a current, then do not subtract the offset value, but use the 14-bit value directly. In either case, divide the 14-bit voltage value by the current-sense gain and the current-sense resistor to arrive at the pack current.

11. Microcontroller FET Control

The external microcontroller can override the device control of the FETs. With the µCFET bit set to "1", the external microcontroller can turn the FETs on or off under all conditions except the following:

- If there is a discharge short-circuit condition, the device turns the FETs off. The external microcontroller is responsible for turning the FETs back on once the short-circuit condition clears.
- If there is an internal over-temperature condition, the device turns the FETs off. The external microcontroller is responsible for turning the FETs back on once the temperature returns to within normal operating limits.
- If there is an overvoltage lockout condition, the device turns the charge or precharge FETs off. The external microcontroller is responsible for turning the FETs back on, once the OVLO condition clears. This assumes that the PSD output has not blown a fuse to disable the pack.
- If there is an open-wire detection, the device turns the FETs off. The external microcontroller is responsible for turning the FET back on. This assumes that the open wire did not cause the PSD output to blow a fuse to disable the pack.
- If the FETSOFF input is HIGH, the FETs turn off and remain off. The external µC is responsible for turning the FETs on once the FETSOFF condition clears.
- If there is a sleep condition, the device turns the FETs off. On wake up, the microcontroller is responsible for turning on the FETs.

The microcontroller can also control the FETs by setting the µCSCAN bit. However, this also stops the scan, requiring the microcontroller to manage the scan, voltage comparisons, FET control, and cell balance. While the µCSCAN bit is set to "1", the only operations controlled by the device are:

- Discharge short-circuit FET control. The external µC cannot override the turn off of the FETs during the short-circuit.
- FETSOFF external control. The FETSOFF pin has priority on control of the FETs, even when the microcontroller is managing the scan.
- In all other cases, the microcontroller must manage the FET control, because it is also managing the voltage scan and all comparisons.

12. Cell Balance

At the same rate as the scan of the cell voltages, if cell balancing is on, the system checks for proper cell balance conditions. The ISL94202 prevents cell balancing if proper temperature, current, and voltage conditions are not met. The cells only balance during a CBON time period. When the CBOFF timer is running, the cell balance is off. Three additional bits determine whether the balancing happens only during charge, only during discharge, during both charge and discharge, during the end of charge condition, or not at any time.

- The cell balance circuit depends on the 14-bit ADC converter built into the device and the results of the cell voltage scan (after calibration).
- The ADC converter loads a set of registers with each cell voltage during every cell voltage measurement.
- At the end of the cell voltage measurement scan, the ISL94202 updates the minimum (CELMIN) and maximum (CELMAX) cell voltages.
- After calculating the CELMIN and CELMAX values, all of the cell voltages are compared with the CELMIN value. When any of the cells exceed CELMIN by CBDL (the minimum CB delta voltage), a flag is set in RAM indicating that the cell needs balancing (this is the CBnON bit).
- If any of the cells exceed the lowest cell by CBDU (maximum CB delta voltage) then a flag is set indicating that a Cell voltage failure occurred (CELLF).
- When the CELLF flag indicates that there is too great a cell to cell differential, the balancing is turned off.
- If CELMAX is below CBMIN (all the cell voltages are too low for balancing) then the CBUV bit is set and there will be no cell balancing. Cell balance does not start again until the CBMIN value rises above (CBMIN + 117mV). When this happens, the ISL94202 clears the CBUV bit.
- If the CELMIN voltage is greater than the CBMAX voltage (all the cell voltages are too high for balancing) then the CBOV bit is set and there will be no cell balancing. Cell balancing does not start again until the CBMAX value drops below (CBMAX - 117mV). When this happens, the ISL94202 clears the CBOV bit.
- A register in EEPROM (CELLS) identifies the number of cells that are supposed to be present so only the cells present are used for the cell balance operation. Note: This is also used in the cell voltage scan and open-wire detect operation.
- There are no limits to the number of cells that can be balanced at any one time, because the balancing is done external to the device.
- The cell balance block updates at the start of the cell balance ON period to determine if balancing is needed and that the right cells are being balanced. The cells selected at this time will be balanced for the duration of the cell balance period.
- The cell balance is disabled if any external temperature is out of a programmed range set by CBUTS (cell balance under temperature) and CBOTS (cell balance over-temperature).
- The cell balance operation can be disabled by setting the Cell Balance During Charge (CBDC), the Cell Balance During Discharge (CBDD), and the Cell Balance During End-of-Charge (CB_EOC) bits to zero. See Table 12.10 on page 56.
- Cell balancing turns off when set to balance in the charge mode and there is no charging current detected (see CB_EOC exception below).
- Cell balancing turns off when set to balance in the discharge mode and there is no discharge current detected (see CB_EOC exception below).
- If cell balancing is set to operate during both charge and discharge, then ISL94202 balances while there is charge current or discharge current, but does not balance when no current flow is detected (all other limiting factors continue to apply). See CB_EOC exception in the following.
- The CB_EOC bit provides an exception to the cell balance current direction limit. When the CB_EOC bit is set, balancing occurs while an end of charge condition exists (EOC bit = 1), regardless of current flow. This allows the ISL94202 to “drain” high voltage cells when the charge is complete. This speeds the balancing of the pack, especially when there is a large capacity differential between cells. Once the end of charge condition clears, the cell balance operation returns to normal programming.
- Balance is disabled by asserting the FETSOFF external pin.

- The cell balance outputs are on only while the cell balance on timer is counting down. This is a 12-bit timer. The cell balance outputs are all off while the cell balance off timer is counting down. This is also a 12-bit timer. The timer values are set as in Table 12.11.

Table 12.10 Cell Balance Truth Table (see Figure 12.28)

CB_EOC Bit	EOC Pin	CBDC	CHING	CBDD	DCHING	Enable
0 1	x 1	0	0	0	0	0
0 1	x 1	0	0	0	1	0
0 1	x 1	0	0	1	0	0
0 1	x 1	0	0	1	1	1
0 1	x 1	0	1	0	0	0
0 1	x 1	0	1	0	1	0
0 1	x 1	0	1	1	0	0
0 1	x 1	0	1	1	1	0
0 1	x 1	1	0	0	0	0
0 1	x 1	1	0	0	1	0
0 1	x 1	1	0	1	0	0
0 1	x 1	1	0	1	1	1
0 1	x 1	1	1	0	0	1
0 1	x 1	1	1	0	1	0
0 1	x 1	1	1	1	0	1
0 1	x 1	1	1	1	1	0
1	0	x	x	x	x	1

Table 12.11 CBON and CBOFF Times

Scale Value	Time (10-Bit Value)
00	0 to 1024µs
01	0 to 1024ms
10	0 to 1024s
11	0 to 1024min

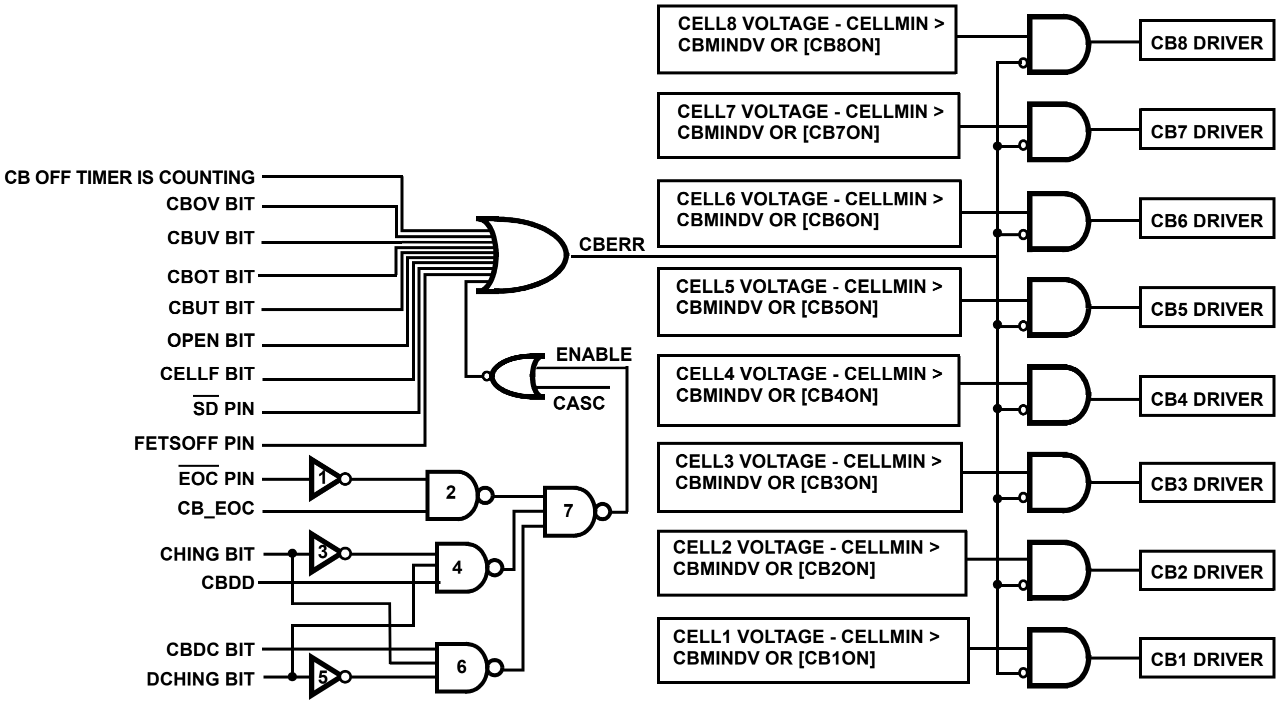


Figure 12.28 Cell Balance Operation

12.1 µC Control of Cell Balance FETs

To control the cell balance FETs, the external microcontroller first needs to set the µCCBAL bit to turn off the automatic cell balance operation.

To turn on a cell balance FET, the µC needs to turn on the cell balance output FET using the Cell Balance Control Register 84H. In this register, each bit corresponds to a specific cell balance output.

With the cell balance outputs specified, the microcontroller sets the CBAL_ON bit. This turns on the cell balance output control circuit.

12.2 Cell Balance FET Drive

The cell balance FETs are driven by a current source or sink of 25µA. The gate voltage on the externals FET is set by the gate to source resistor. This resistor should be set such that the gate voltage does not exceed 9V. An external 9V zener diode across the gate to source resistor can help to prevent overvoltage conditions on the cell balance pin.

The cell balance circuit connection is shown in Figure 12.29 on page 58.

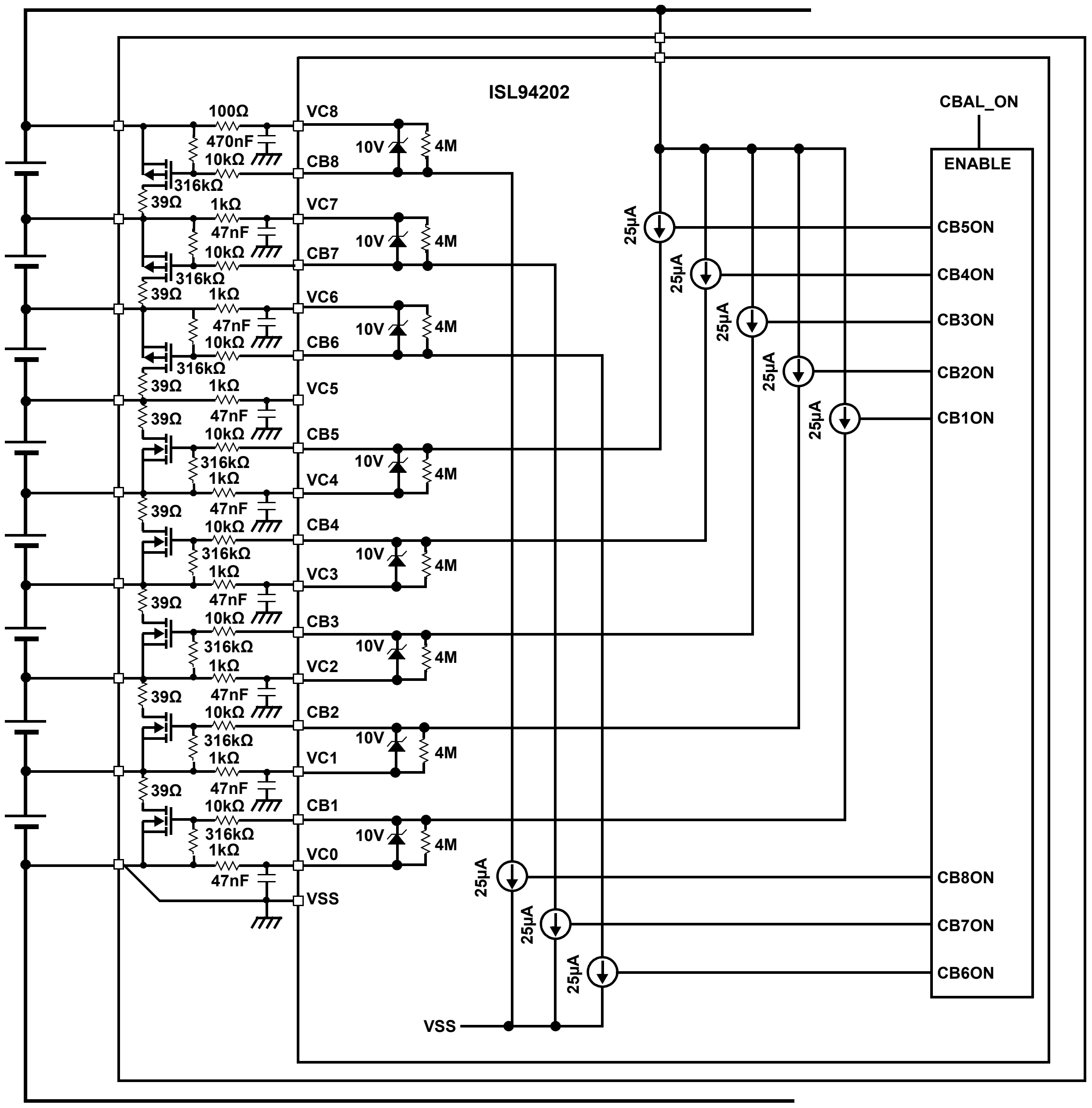


Figure 12.29 Cell Balance Drive Circuits and Cell Connection Options

13. Watchdog Timer

The I^2C watchdog timer prevents an external microcontroller from initiating an action that it cannot undo through the I^2C port, which can result in poor or unexpected operation of the pack.

The watchdog timer is normally inactive when operating the device in a stand-alone operation. When the pack is expected to have a µC along with the ISL94202, the WDT is activated by setting any of the following bits: µCSCAN, µCCMON, µCLMON, µCCBAL, µCFET, EEEN.

When active (an external µC is assumed to be connected), the absence of I^2C communications for the watchdog timeout period causes a timeout event. The ISL94202 needs to see a start bit and a valid slave byte to restart the timer.

The watchdog timeout signal turns off the cell balance and power FET outputs, resets the serial interface, and pulses the $\overline{\text{INT}}$ output once per second in an attempt to get the microcontroller to respond. If the $\overline{\text{INT}}$ is unsuccessful in restarting the communication interface, the part operates normally, except the power FETs and cell balance FETs are forced off. The ISL94202 remains in this condition until I^2C communications resumes.

When I^2C communication resumes, the µCSCAN, µCCMON, µCLMON, µCFET, and EEEN bits are automatically cleared and the µCCBAL bit remains set. The power FETs and cell balance FETs turn on, if conditions allow.

14. Power FET Drive

The ISL94202 drives the power FETs gates with a voltage higher than the supply voltage by using external capacitors as part of a charge pump. The capacitors connect (as shown in Figure 1.2 on page 3) and are nominally 4.7nF. The charge pump applies approximately (V_{DD} * 2) voltage to the gate, although the voltage is clamped at V_{DD} + 16V.

The power FET turn-on times are limited by the capacitance of the power FET and the current supplied by the charge pump. The power FET turn-off times are limited by the capacitance of the power FET and the pull-down current of the ISL94202. The ISL94202 provides a pull-down current for up to 300µs. This should be long enough to discharge any FET capacitance.

Table 14.12 shows typical turn-on and turn-off times for the ISL94202 under specific conditions.

Table 14.12 Power Fet Gate Control (Typical)

Parameter	Conditions	Typical
Power FET Gate Turn-On Current	DFET, CFET, PCFET Charge pump caps = 4.7nF	32kHz 5mA, pulses, 50% duty cycle
Power FET Gate Turn-On Time	10% to 90% of final voltage V_{DD} = 28V; DFET, CFET = IRF1404 PCFET = FDD8451	160µs 160µs
Power FET Gate Turn-Off Current	CFET, CFET, PCFET	13mA (CFET, PCFET) 15mA (DFET)
Power FET Gate Turn-Off Pulse Width	Pulse duration	300µs
Power FET Gate Fall Time	90% to 10% of final voltage V_{DD} = 28V; DFET: IRF1404 CFET: IRF1404 PCFET: FDD8451	6µs 6µs 2µs

15. General I/Os

There is an open-drain output ($\overline{\text{SD}}$) that is pulled up to RGO (using an external resistor) and indicates if there are any error conditions, such as overvoltage, undervoltage, over-temperature, open input, and overcurrent. The output goes active (LOW) when there is any cell or pack failure condition. The output returns HIGH when all error conditions clear.

There is an open-drain output ($\overline{\text{EOC}}$) that is pulled up to RGO (using an external resistor) and indicates that the cells have reached an end of charge state. The output goes active (LOW) when all cell voltages are above a threshold specified by a 12-bit value in EEPROM. The output returns HIGH, when all cells are below the EOC threshold.

Factory programmable options offer inverse polarity of $\overline{\text{SD}}$ or $\overline{\text{EOC}}$. Please contact Automotive Marketing if there is interest in either of these options.

The PSD pin goes active high, when any cell voltage reaches the OVLO threshold (OVLO flag). Optionally, PSD also goes high if there is a voltage differential between any two cells that is greater than a specified limit (CELLF flag) or if there is an open-wire condition. This pin can be used for blowing a fuse in the pack or as an interrupt to an external µC.

An input pin (FETSOFF), when pulled high, turns off the power FETs and the cell balance FETs, regardless of any other condition.

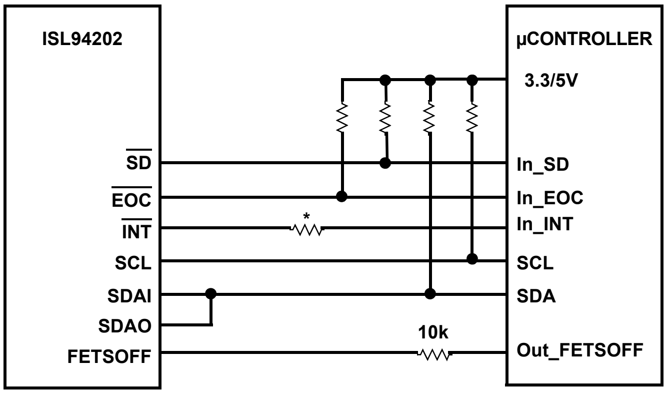
16. Higher Voltage Microcontrollers

When using a microcontroller powered by 3.3V or 5V, the design can include pull-up resistors to the microcontroller supply on the communication link and the open-drain $\overline{\text{SD}}$ and $\overline{\text{EOC}}$ pins (instead of pull-up resistors to RGO.)

The $\overline{\text{INT}}$ pin is a CMOS output with a maximum voltage of RGO+0.5V. It is OK to connect this directly to a microcontroller as long as the microcontroller pin does not have a pull up to the 3.3/5V supply. If it does, then a series resistor is recommended.

The FETSOFF input on the ISL94202 is also limited to RGO+0.5V. This is limited by an input ESD structure that clamps the voltage. The connection from the µC to this pin should include a series resistor to limit any current resulting from the clamp.

An example of this connection is shown in Figure 16.30.



* Resistor needed only if µC has a pull-up on the In_INT pin

Figure 16.30 Connection of Higher Voltage Microcontroller

17. Packs with Fewer than Eight Cells

See “Pack Configuration” on page 27 for help when using fewer than eight cells. This section presents options for minimum number of components. However, when using the ISL94202EVAL1Z evaluation board with fewer than eight cells, it is not necessary to remove components from the PCB. Simply tie the unused connections together, as shown in Figure 17.31. This normally requires only a different cable.

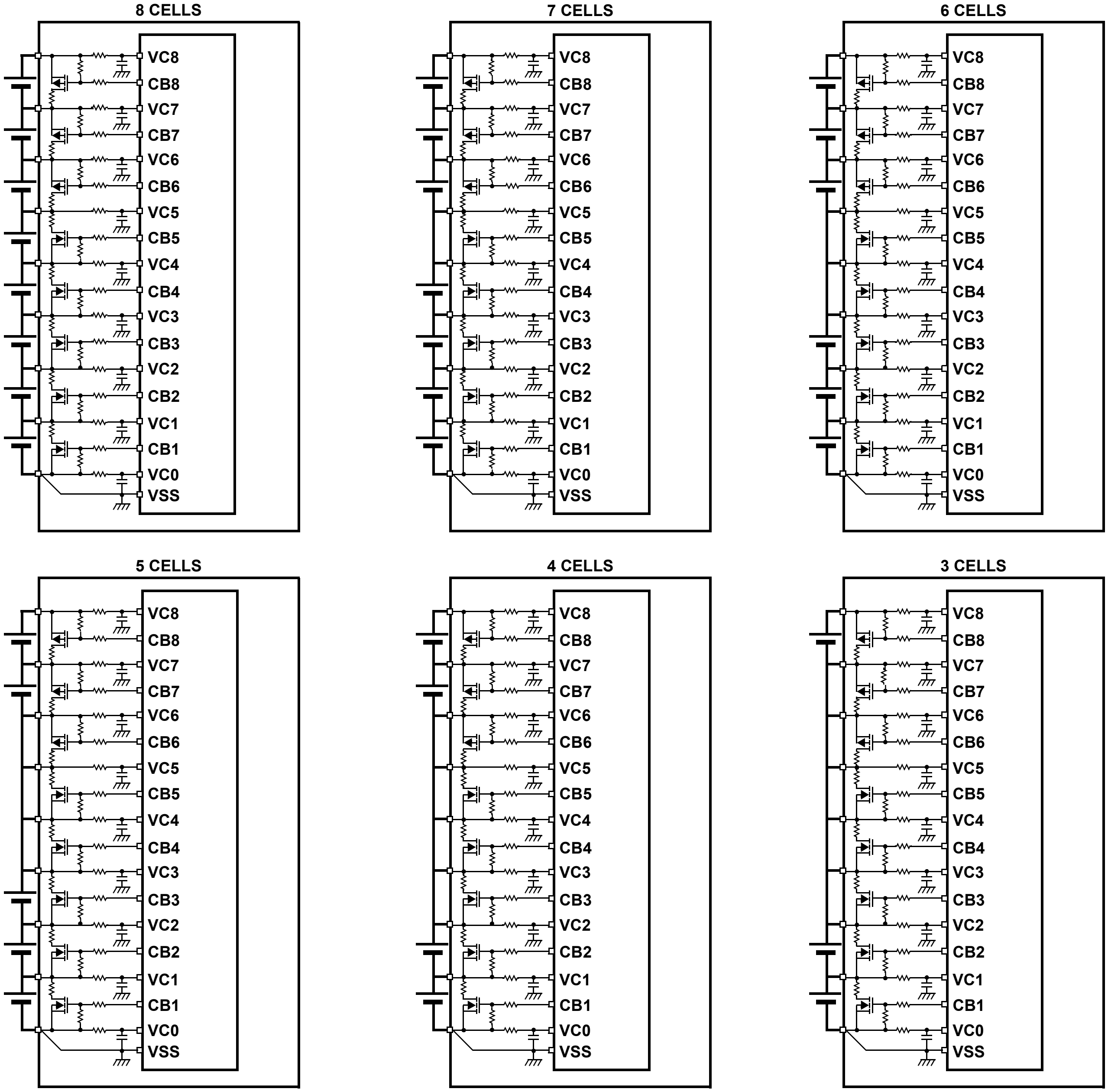


Figure 17.31 Battery Connection Options Using the ISL94202EVAL1Z Board

18. PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high performance from your PC board.

- The use of low inductance components, such as chip resistors and chip capacitors, is strongly recommended.
- Minimize signal trace lengths. This is especially true for the CS1, CS2, and VC0-VC8 inputs. Trace inductance and capacitance can easily affect circuit performance. Vias in the signal lines add inductance at high frequency and should be avoided.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This is especially true for the CS1 and CS2 lines, since their inputs are normally very low voltage.
- Maximize use of AC decoupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e., no split planes or ground plane gaps under these lines). Avoid vias in the signal I/O lines.
- VDD bypass and charge pump capacitors should use wide temperature and high frequency dielectric (X7R or better) with capacitors rated at 2X the maximum operating voltage.
- The charge pump and VDD bypass capacitors should be located close to the ISL94202 pins and VDD should have a good ground connection.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- An example PCB layout is shown in Figure 18.32. This figure shows placement of the VDD bypass capacitor close to the VDD pin and with a good ground connection. The charge pump capacitors are also close to the IC. The current-sense lines are shielded by ground plane as much as possible. The ground plane under the IC is shown as an "island". The intent of this layout was to minimize voltages induced by EMI on the ground plane in the vicinity of the IC. This example assumes a 4-layer board with most signals on the inner layers.

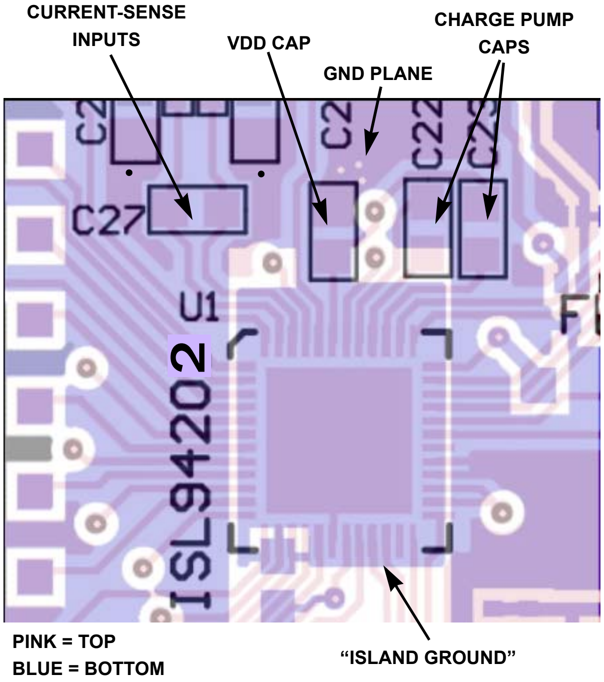


Figure 18.32 Example 4-Layer PCB Layout for VDD Bypass, Charge Pump, and Current Sense

18.1 QFN Package

The QFN package requires additional PCB layout rules for the thermal pad. The thermal pad is electrically connected to VSS supply through the high-resistance IC substrate. The thermal pad provides heat sinking for the IC. In normal operation, the device should generate little heat, so thermal pad design and layout are not too important. However, if the design uses the RGO pin to supply power to external components, then the IC can experience some internal power dissipation. In this case, careful layout of the thermal pad and the use of thermal vias to direct the heat away from the IC is an important consideration. Besides heat dissipation, the thermal pad also provides noise reduction by providing a ground plane under the IC.

18.2 Circuit Diagrams

The “Block Diagram” on page 3 shows a simple application diagram with eight cells in series and two cells in parallel (8S2P).

19. EEPROM

The ISL94202 contains an EEPROM array for storing the device configuration parameters, the device calibration values, and some user available registers. Access to the EEPROM is through the I^2C port of the device. Memory is organized in a memory map as described in:

- "Registers: Summary (EEPROM)" on page 74
- "Registers: Summary (RAM)" on page 75
- "Registers: Detailed (EEPROM)" on page 76
- "Registers: Detailed (RAM)" on page 82.

When the device powers up, the ISL94202 transfers the contents of the configuration EEPROM memory areas to RAM. (Note that the user EEPROM has no associated RAM). An external microcontroller can read the contents of the Configuration RAM or the contents of the EEPROM. Prior to reading the EEPROM, set the EEEN bit to "1". This enables access to the EEPROM area. If EEEN is "0", then a read or write occurs in the shadow RAM area.

The content of the Shadow Ram determines the operation of the device.

Reading from the RAM or EEPROM can be done using a byte or page read. See:

- "Current Address Read" on page 70
- "Random Read" on page 70
- "Sequential Read" on page 71
- "EEPROM Access" on page 72
- "Register Protection" on page 73

Writing to the Configuration or User EEPROM must use a Page Write operation. Each Page is four bytes in length and pages begin at Address 0.

See:

- "Page Write" on page 69
- "Register Protection" on page 73

The EEPROM contains an error detection and correction mechanism. When reading a value from the EEPROM, the device checks the data value for an error.

If there are no errors, then the EEPROM value is valid and the ECC_USED and ECC_FAIL bits are set to "0". If there is a 1-bit error, the ISL94202 corrects the error and sets the ECC_USED bit. This is a valid operation and value read from the EEPROM is correct. During an EEPROM read, if there is an error consisting of two or more bits, the ISL94202 sets the ECC_FAIL bit (ECC_USED = 0). This read contains invalid data.

The error correction is also active during the initial power-on recall of the EEPROM values to the shadow RAM. The circuit corrects for any one-bit errors. Two-bit errors are not corrected and the contents of the shadow RAM maintain the previous value.

Internally, the power-on recall circuit uses the ECC_USED and ECC_FAIL bits to determine there is a proper recall before allowing the device operation to start. However, an external µC cannot use these bits to detect the validity of the shadow RAM on power-up or determine the use of the error correction mechanism, because the bits automatically reset on the next valid read.

20. Serial Interface

- The ISL94202 uses a standard I^{2}C interface, except the design separates the SDA input and output (SDAI and SDAO)
- Separate SDAI and SDAO lines can be tied together and operate as a typical I^{2}C bus
- Interface speed is 400kHz, maximum

20.1 Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL94202 devices operate as slaves in all applications.

When sending or receiving data, the convention with the most significant bit (MSB) is sent first. Therefore, the first address bit sent is Bit 7.

20.2 Clock and Data

Data states on the SDA line can change only while SCL is LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (see Figure 20.33).

20.3 Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met (see Figure 20.34).

20.4 Stop Condition

All communications must be terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition is only issued after the transmitting device has released the bus (see Figure 20.34).

20.5 Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge that it received the eight bits of data (see Figure 20.35).

The device responds with an acknowledge after recognition of a start condition and the correct slave byte. If a write operation is selected, the device responds with an acknowledge after the receipt of each subsequent eight bits. The device acknowledges all incoming data and address bytes, except for the slave byte when the contents do not match the device's internal slave address.

In the read mode, the device transmits eight bits of data, releases the SDA line, then monitors the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device terminates further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

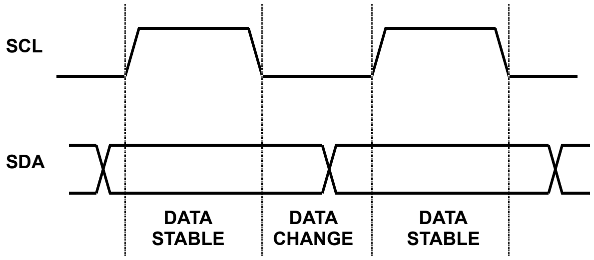


Figure 20.33 Valid Data Changes On I²C Bus

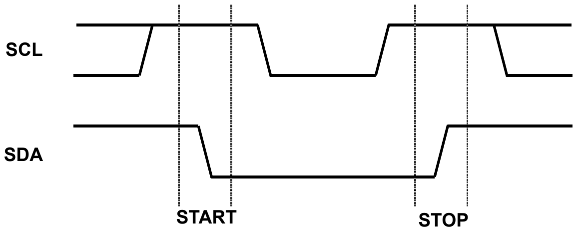


Figure 20.34 I²C Start and Stop Bits

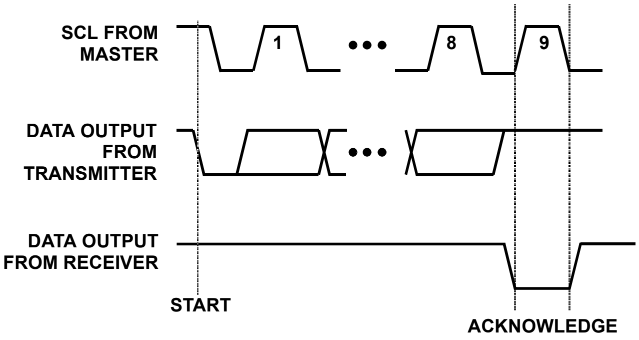


Figure 20.35 Acknowledge Response From Receiver

20.6 Write Operations

20.6.1 Byte Write

For a byte write operation, the device requires the Slave Address Byte and a Word Address Byte. This gives the master access to any one of the words in the array. After receipt of the Word Address Byte, the device responds with an acknowledge and awaits the next eight bits of data. After receiving the eight bits of the Data Byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 20.36.

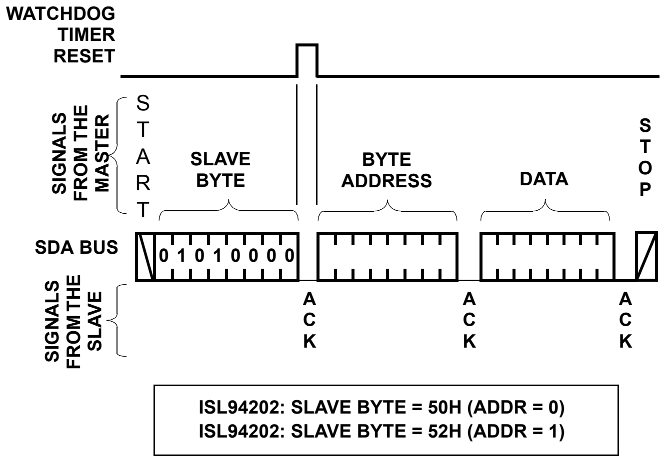


Figure 20.36 Byte Write Sequence

A write to a protected block of memory suppresses the acknowledge bit.

When writing to the EEPROM, write to all addresses of a page without an intermediate read operation or use a page write command. Each page is four bytes long, starting at Address 0.

20.6.2 Page Write

A page write operation is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it "rolls over" and goes back to '0' on the same page. This means that the master can write four bytes to the page starting at any location on that page. If the master begins writing at Location 2 and loads four bytes, then the first two bytes are written to Locations 2 and 3 and the last two bytes are written to Locations 0 and 1. Afterwards, the address counter would point to Location 2 of the page that was just written. If the master supplies more than four bytes of data, then new data overwrites the previous data, one byte at a time. See Figure 20.37.

Do not write to addresses 58H through 7FH or locations higher than address ABH, since these addresses access registers that are reserved. Writing to these locations can result in unexpected device operation.

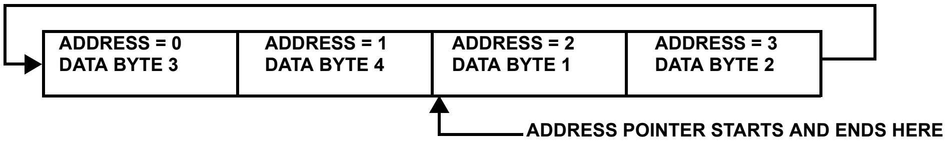


Figure 20.37 Writing 4 Bytes to A 4-Byte Page Starting at Location 2

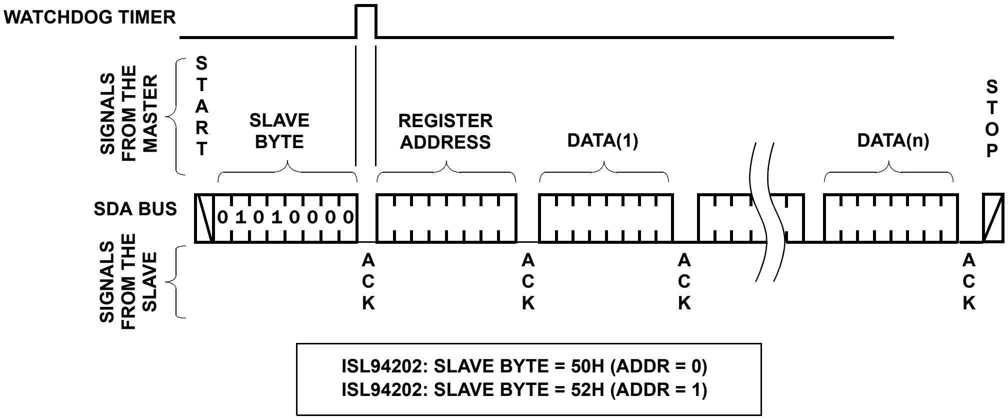


Figure 20.38 Page Write Sequence

20.7 Read Operations

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

20.7.1 Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the address of the address counter is undefined, requiring a read or write operation for initialization. See Figure 20.39 on page 71.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

20.7.2 Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition (see Figure 20.40)

20.7.3 Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first Data Byte is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition

The data output is sequential, with the data from address n followed by the data from address n+1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to address 0000H and the device continues to output data for each acknowledge received. See Figure 20.41 for the acknowledge and data transfer sequence.

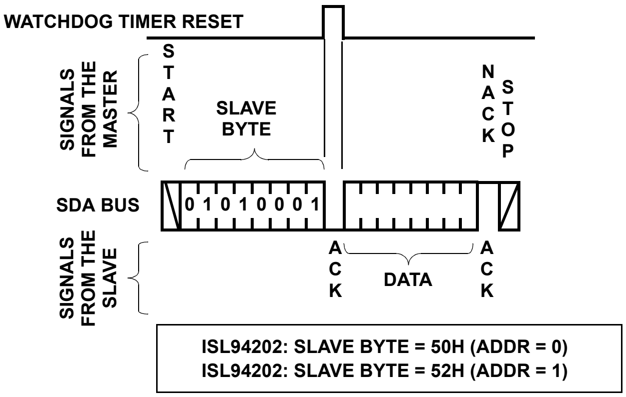


Figure 20.39 Current Address Read Sequence

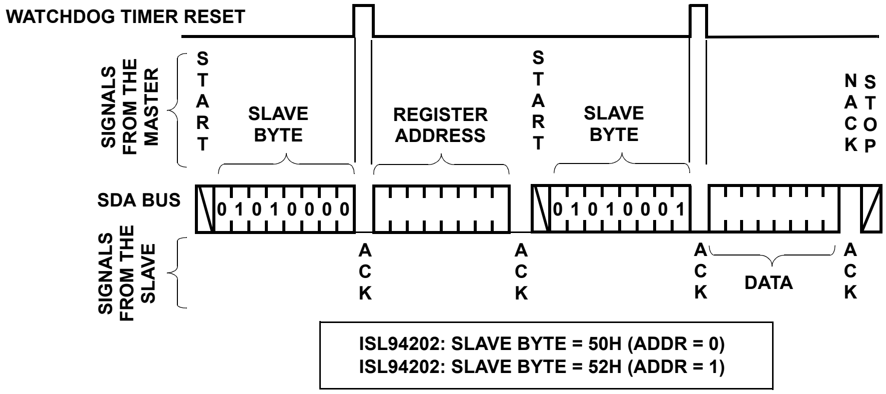


Figure 20.40 Random Read Sequence

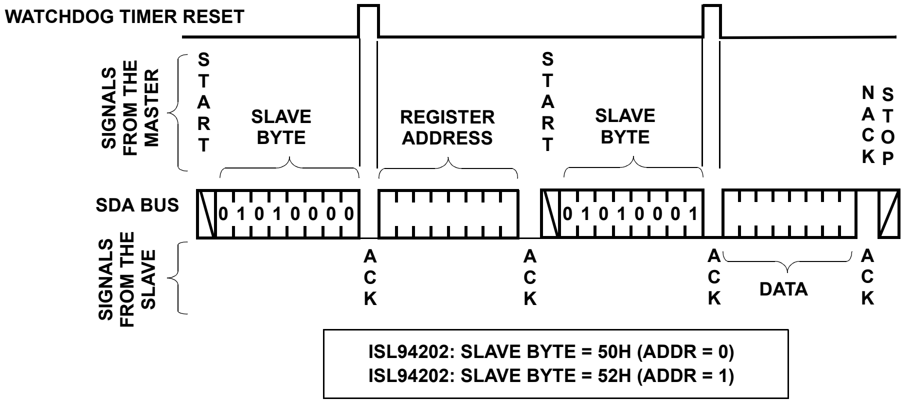


Figure 20.41 Sequential Read Sequence

20.7.4 EEPROM Access

The user is advised not to use page transfers when reading or writing to EEPROM. Only single byte I^2C transactions should be used. In addition, “Write” transactions should be separated with a 30ms delay to enable each byte write operation to complete.

20.7.5 EEPROM Read

The ISL94202 has a special requirement when reading the EEPROM. An EEPROM read operation from the first byte of a four byte page (locations 0H, 4H, 8H, etc.) initiates a recall of the EEPROM page. This recall takes more than 200µs, so the first byte may not be ready in time for a standard I^2C response. It is necessary to read this first byte of every page two times.

20.7.6 EEPROM Write

The ISL94202 also has a special requirement when writing the EEPROM. An EEPROM write operation to the first byte of a four byte page (locations 0H, 4H, 8H, etc.) initiates a recall of the EEPROM page. This recall takes more than 200µs, so the first byte may not be ready in time for a standard I^2C response. It is necessary to write this first byte of every page two times. These “duplicate” writes should be separated with a 30ms delay and followed with a 30ms delay. Again, only single byte transactions should be used with a 30ms delay between each write operation.

20.8 Synchronizing Microcontroller Operations with Internal Scan

Internal scans occur every 32ms in Normal mode, 256ms in Idle mode and 512ms in Doze mode. The internal scan normally takes about 1.3ms, with every fourth scan taking about 1.7ms. While the percentage of time taken by the scan is small, it is long enough that random communications from the microcontroller can coincide with the internal scan. When the two scans happen at the same time, errors can occur in the recorded values.

To avoid errors in the recorded values, the goal is to synchronize external I^2C transactions so that they only occur during the device’s Low Power State (see Figure 10.22 on page 43.) To assist in the synchronization, the microcontroller can use the INT_SCAN bit. This bit is “0” during the internal scan and “1” during the “Low Power State”.

The microcontroller software should look for the INT_SCAN bit to go from a “0” to a “1” to allow the maximum time to complete read or write operations. This insures that the results reported to the µC are from a single scan and changes made do not interfere with state machine detection and timing.

21. Register Protection

The entire EEPROM memory is write protected on initial power-up and during normal operation. An enable byte allows writing to various areas of the memory array.

The enable byte is encoded, so that a value of ‘0’ in the EEPROM Enable register (89H) enables access to the shadow memory (RAM), a value of ‘1’ allows access to the EEPROM.

After a read or write of the EEPROM, the microcontroller should reset the EEPROM Enable register value back to zero to prevent inadvertent writes to the EEPROM and to turn off the EEPROM block to reduce current consumption. If the microcontroller fails to reset the EEPROM bit and communications to the chip stops, then the Watchdog timer will reset the EEPROM select bit.

22. Registers: Summary (EEPROM)

Table 22.13 EEPROM Register Summary

EEPROM (Configured as 32 4-Byte Pages)							
Page	**ADDR**	**0x**	**1x**	**2x**	**3x**	**4x**	**5x**
0	0	Overvoltage Level	Overvoltage Delay Timer	Minimum CB Delta	Charge Over-Temperature Level	Internal Over-Temperature Level	User EEPROM
	1						
	2	Overvoltage recovery	Undervoltage Delay Timer	Maximum CB Delta	Charge Over-Temp Recovery	Internal Over-Temperature Recovery	
	3						
1	4	Undervoltage Level	Open Wire Timing	Cell Balance On time	Charge Under-Temperature Level	Sleep Voltage	
	5						
	6	Undervoltage Recovery	Discharge Overcurrent Timeout Settings, Discharge Setting	Cell Balance Off Time	Charge Under-Temperature Recovery	Sleep Delay Timer/ Watchdog Timer	
	7						
2	8	OVLO Threshold	Charge overcurrent Timeout Settings, Charge overcurrent Setting	Minimum CB Temperature Level	Discharge Over-Temperature Level	Sleep Mode Timer	Reserved
	9					CELLS Config	
	A	UVLO Threshold	Short-Circuit Timeout Settings/ Recovery Settings, Short-Circuit Setting	Minimum CB Temperature Recovery	Discharge Over-Temperature Recovery	Features 1	
	B					Features 2	
3	C	EOC Voltage Level	Minimum CB Volts	Maximum CB Temperature Level	Discharge Under-Temperature Level	Reserved	
	D						
	E	Low Voltage Charge Level	Maximum CB Volts	Maximum CB Temperature Recovery	Discharge Under-Temperature Recovery		
	F						

23. Registers: Summary (RAM)

Table 23.14 RAM Register Summary

RAM				
Page	**ADDR**	**8x**	**9x**	**Ax**
0	0	Status1	CELL1 Voltage	iT Voltage
	1	Status2		
	2	Status3	CELL2 Voltage	xT1 Voltage
	3	Status4		
1	4	Cell Balance	CELL3 Voltage	xT2 Voltage
	5	Analog Out		
	6	FET Cntl/Override Control Bits	CELL4 Voltage	VBATT/16 Voltage
	7	Override Control Bits		
2	8	Force Ops	CELL5 Voltage	VRGO/2 Voltage
	9	EE Write Enable		
	A	CELLMIN Voltage	CELL6 Voltage	14-bit ADC Voltage
	B			
3	C	CELLMAX Voltage	CELL7 Voltage	Reserved
	D			
	E	ISense Voltage	CELL8 Voltage	
	F			

24. Registers: Detailed (EEPROM)

Table 24.15 EEPROM Register Detail

Bit/ ADDR	F 7	E 6	D 5	C 4	B 3	A 2	9 1	8 0	7	6	5	4	3	2	1	0
00 01	**Overvoltage Threshold** If any cell voltage is above this threshold voltage for an overvoltage delay time, the charge FET is turned off.									Default (Hex):			1E2A	(V):		4.25
	Charge Detect Pulse Width These bits set the duration of the charger monitor pulse width.				OVLB	OVLA	OVL9	OVL8	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
	CPW3	CPW2	CPW1	CPW0	$\text{Threshold} = \dfrac{\text{HEXvalue}_{10} \times 1.8 \times 8}{4095 \times 3}$											
	0000 = 0ms to 1111 = 15ms; Default = 1ms															
02 03	**Overvoltage Recovery** If all cells fall below this overvoltage recovery level, the charge FET is turned on.									Default (Hex):			0DD4	(V):		4.15
	Reserved				OVRB	OVRA	OVR9	OVR8	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
04 05	**Undervoltage Threshold** If any cell voltage is below this threshold voltage for an undervoltage delay time, the discharge FET is turned off.									Default (Hex):			18FF	(V):		2.7
	Load Detect Pulse Width These bits set the duration of the charger monitor pulse width.				UVLB	UVLA	UVL9	UVL8	UVL7	UVL6	UVL5	UVL4	UVL3	UVL2	UVL1	UVL0
	LPW3	LPW2	LPW1	LPW0	$\text{Threshold} = \dfrac{\text{HEXvalue}_{10} \times 1.8 \times 8}{4095 \times 3}$											
	0000 = 0 ms to 1111 = 15ms; Default = 1ms															
06 07	**Undervoltage Recovery** If all cells rise above this overvoltage recovery level (and there is no load), the discharge FET is turned on.									Default (Hex):			09FF	(V):		3.0
	Reserved				UVRB	UVRA	UVR9	UVR8	UVR7	UVR6	UVR5	UVR4	UVR3	UVR2	UVR1	UVR0
08 09	**Overvoltage Lockout Threshold** If any cell voltage is above this threshold for five successive scans, then the device is in an overvoltage lockout condition. In this condition, the Charge FET is turned off, the cell balance FETs are turned off, the OVLO bit is set, and the PSD output is set to active.									Default (Hex):			0E7F	(V):		4.35
	Reserved				OVLO B	OVLO A	OVLO 9	OVLO 8	OVLO 7	OVLO 6	OVLO 5	OVLO 4	OVLO 3	OVLO 2	OVLO 1	OVLO 0
0A 0B	**Undervoltage Lockout Threshold** If any cell voltage is below this threshold for five successive scans, then the device is in an undervoltage lockout condition. In this condition, the Discharge FET is turned off and the UVLO bit is set. The device also powers down (unless overridden).									Default (Hex):			0600	(V):		1.8
	Reserved				UVLO B	UVLO A	UVLO 9	UVLO 8	UVLO 7	UVLO 6	UVLO 5	UVLO 4	UVLO 3	UVLO 2	UVLO 1	UVLO 0
0C 0D	**End-of-Charge (EOC) Threshold** If any cell exceeds this level, then the EOC output and the EOC bit are set.									Default (Hex):			0DFF	(V):		4.2
	Reserved				EOCB	EOCA	EOC9	EOC8	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
0E 0F	**Low Voltage Charge Level** If the voltage on any cell is less than this level, then the PCFET output turns on instead of the PC output. To disable this function, set the value to zero or set the PCFETE bit to 0.									Default (Hex):			07AA	(V):		2.3
	Reserved				LVCH B	LVCH A	LVCH9	LVCH8	LVCH7	LVCH6	LVCH5	LVCH4	LVCH3	LVCH2	LVCH1	LVCH0
10 11	**Overvoltage Delay Time Out** This value sets the time that is required for any cell to be above the overvoltage threshold before an overvoltage condition is detected.									Default (Hex):			0801	(s):		1
	Reserved				OVDT B	OVDT A	OVDT 9	OVDT 8	OVDT 7	OVDT 6	OVDT 5	OVDT 4	OVDT 3	OVDT 2	OVDT 1	OVDT 0
					00 = µs 01 = ms 10 = s 11 = min		0 to 1024									

Table 24.15 EEPROM Register Detail (Continued)

Bit/ ADDR	F 7	E 6	D 5	C 4	B 3	A 2	9 1	8 0	7	6	5	4	3	2	1	0
12 13	**Undervoltage Delay Time Out** This value sets the time that is required for any cell to be below the undervoltage threshold before an undervoltage condition is detected.								Default (Hex):				0801	(s):		1
	Reserved				UVDT B	UVDT A	UVDT 9	UVDT 8	UVDT 7	UVDT 6	UVDT 5	UVDT 4	UVDT 3	UVDT 2	UVDT 1	UVDT 0
					00 = μs 01 = ms 10 = s 11 = min		0 to 1024									
14 15	**Open-Wire Timing (OWT)** This value sets the width of the open-wire test pulse for each cell input.								Default (Hex):				0214	(ms):		20
	Reserved						OWT 9	OWT 8	OWT 7	OWT 6	OWT 5	OWT 4	OWT 3	OWT 2	OWT 1	OWT 0
							0 = μs 1 = ms	0 to 512								
16 17	Discharge Overcurrent Time Out/Threshold **Time Out** A discharge overcurrent needs to remain for this time period prior to entering a discharge overcurrent condition. This is a 12-bit value: Lower 10 bits set the time. Upper bits set the time base.								Default (Hex):				44A0	(ms): (mV):		160 32
	Threshold This value sets the voltage across current-sense resistor that creates a discharge overcurrent condition.															
		OCD2	OCD1	OCD0	OCDT B	OCDT A	OCDT 9	OCDT 8	OCDT 7	OCDT 6	OCDT 5	OCDT 4	OCDT 3	OCDT 2	OCDT 1	OCDT 0
		000 = 4mV 001 = 8mV 010 = 16mV 011 = 24mV 100 = 32mV 101 = 48mV 110 = 64mV 111 = 96mV			00 = μs 01 = ms 10 = s 11 = min		0 to 1024									
18 19	Charge Overcurrent Time Out/Threshold **Time Out** A charge overcurrent needs to remain for this time period prior to entering a charge overcurrent condition. This is a 12-bit value: Lower 10 bits set the time. Upper bits set the time base.								Default (Hex):				44A0	(ms): (mV):		160 8
	Threshold This value sets the voltage across current-sense resistor that creates a charge overcurrent condition															
		OCC2	OCC1	OCC0	OCCT B	OCCT A	OCCT 9	OCCT 8	OCCT 7	OCCT 6	OCCT 5	OCCT 4	OCCT 3	OCCT 2	OCCT 1	OCCT 0
		000 = 1mV 001 = 2mV 010 = 4mV 011 = 6mV 100 = 8mV 101 = 12mV 110 = 16mV 111 = 24mV			00 = μs 01 = ms 10 = s 11 = min		0 to 1024									
1A 1B	Discharge Short-Circuit Time Out/Threshold **Time Out** A short-circuit current needs to remain for this time period prior to entering a short-circuit condition. This is a 12 bit value: Lower 10 bits set the time. Upper bits set the time base								Default (Hex):				60C8	(μs): (mV):		200 128
	Threshold This value sets the voltage across current-sense resistor that creates a short-circuit condition															
		SCD2	SCD1	SCD0	SCTB	SCTA	SCT9	SCT8	SCT7	SCT6	SCT5	SCT4	SCT3	SCT2	SCT1	SCT0
		000 = 16mV 001 = 24mV 010 = 32mV 011 = 48mV 100 = 64mV 101 = 96mV 110 = 128mV 111 = 256mV			00 = μs 01 = ms 10 = s 11 = min		0 to 1024									

Table 24.15 EEPROM Register Detail (Continued)

Bit/ ADDR	F 7	E 6	D 5	C 4	B 3	A 2	9 1	8 0	7	6	5	4	3	2	1	0
1C 1D	**Cell Balance Minimum Voltage (CBMIN)** If all cell voltages are less than this voltage, then cell balance stops.									Default (Hex):			0A55		(V):	3.1
	Reserved				CBVLB	CBVLA	CBVL9	CBVL8	CBVL7	CBVL6	CBVL5	CBVL4	CBVL3	CBVL2	CBVL1	CBVL0
1E 1F	**Cell Balance Maximum Voltage (CBMAX)** If all cell voltages are greater than this voltage, then cell balance stops.									Default (Hex):			0D70		(V):	4.0
	Reserved				CBVUB	CBVUA	CBVU9	CBVU8	CBVU7	CBVU6	CBVU5	CBVU4	CBVU3	CBVU2	CBVU1	CBVU0
20 21	**Cell Balance Minimum Differential Voltage (CBMINDV)** If the difference between the voltage on CELLN and the lowest voltage cell is less than this voltage, then cell balance for CELLN stops.									Default (Hex):			0010	(mV):		20
	Reserved				CBDLB	CBDLA	CBDL9	CBDL8	CBDL7	CBDL6	CBDL5	CBDL4	CBDL3	CBDL2	CBDL1	CBDL0
22 23	**Cell Balance Maximum Differential Voltage (CBMAXDV)** If the difference between the voltage on CELLN and the lowest voltage cell is greater than this voltage, then cell balance for CELLN stops and the CELLF flag is set.									Default (Hex):			01AB	(mV):		500
	Reserved				CBDUB	CBDUA	CBDU9	CBDU8	CBDU7	CBDU6	CBDU5	CBDU4	CBDU3	CBDU2	CBDU1	CBDU0
24 25	**Cell Balance On Time (CBON)** Cell balance is on for this set amount of time, unless another condition indicates that there should be no cell balance. This is a 12-bit value: Lower 10 bits set the time. Upper 2 bits set the time base.									Default (Hex):			0802	(s):		2
	Reserved				CBONTB	CBONTA	CBONT9	CBONT8	CBONT7	CBONT6	CBONT5	CBONT4	CBONT3	CBONT2	CBONT1	CBONT0
					00 = µs 01 = ms 10 = s 11 = min		0 to 1024									
26 27	**Cell Balance Off Time (CBOFF)** Cell balance is off for the set amount of time. This is a 12-bit value: Lower 10 bits set the time. Upper 2 bits set the time base.									Default (Hex):			0802	(s):		2
	Reserved				CBOFTB	CBOFTA	CBOFT9	CBOFT8	CBOFT7	CBOFT6	CBOFT5	CBOFT4	CBOFT3	CBOFT2	CBOFT1	CBOFT0
					00 = µs 01 = ms 10 = s 11 = min		0 to 1024									
28 29	**Cell Balance Minimum Temperature Limit (CBUTS)** If the External Temperature 1 or the External Temperature 2 (XT2M = 0) is greater than this voltage, then cell balance stops. The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			0BF2		(V): (°C):	1.344 -10
	Reserved				CBUTSB	CBUTSA	CBUTS9	CBUTS8	CBUTS7	CBUTS6	CBUTS5	CBUTS4	CBUTS3	CBUTS2	CBUTS1	CBUTS0
2A 2B	**Cell Balance Minimum Temperature Recovery Level (CBUTR)** If the External Temperature 1 and the External Temperature 2 (XT2M = 0) all recover and fall below this voltage, then cell balance can resume (all other conditions OK). The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			0A93		(V): (°C):	1.19 +5
	Reserved				CBUTRB	CBUTRA	CBUTR9	CBUTR8	CBUTR7	CBUTR6	CBUTR5	CBUTR4	CBUTR3	CBUTR2	CBUTR1	CBUTR0
2C 2D	**Cell Balance Maximum Temperature Limit (CBOTS)** If the External Temperature 1 or the External Temperature 2 (XT2M = 0) is less than this voltage, then cell balance stops. The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			04B6		(V): (°C):	0.530 +55
	Reserved				CBOTSB	CBOTSA	CBOTS9	CBOTS8	CBOTS7	CBOTS6	CBOTS5	CBOTS4	CBOTS3	CBOTS2	CBOTS1	CBOTS0
2E 2F	**Cell Balance Maximum Temperature Recovery Level (CBOTR)** If the External Temperature 1 and the External Temperature 2 temperature (XT2M = 0) all recover and rise above this voltage, then cell balance can resume (all other conditions OK). The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			053E		(V): (°C):	0.590 +50
	Reserved				CBOTRB	CBOTRA	CBOTR9	CBOTR8	CBOTR7	CBOTR6	CBOTR5	CBOTR4	CBOTR3	CBOTR2	CBOTR1	CBOTR0
	For All Temperature Limits, TGain bit = 0, Temperature Gain = 2															

Table 24.15 EEPROM Register Detail (Continued)

Bit/ ADDR	F 7	E 6	D 5	C 4	B 3	A 2	9 1	8 0	7	6	5	4	3	2	1	0
30 31	**Charge Over-Temperature Voltage** If External Temperature 1 or the External Temperature 2 is less than this voltage, then the charge FET is turned off and the COT bit is set. The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			04B6	(V): (°C):		0.530 +55
	Reserved				COTS B	COTS A	COTS 9	COTS 8	COTS 7	COTS 6	COTS 5	COTS 4	COTS 3	COTS 2	COTS 1	COTS 0
32 33	**Charge Over-Temperature Recovery Voltage** If External Temperature 1 or the External Temperature 2 rise above this setting, then the charge FET is turned on and the COT bit is reset (unless overrides are in place). The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			053E	(V): (°C):		0.590 +50
	Reserved				COTR B	COTR A	COTR 9	COTR 8	COTR 7	COTR 6	COTR 5	COTR 4	COTR 3	COTR 2	COTR 1	COTR 0
34 35	**Charge Under-Temperature Voltage** If External Temperature 1 or the External Temperature 2 is greater than this voltage, then the charge FET is turned off and the CUT bit is set. The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			0BF2	(V): (°C):		1.344 -10
	Reserved				CUTS B	CUTS A	CUTS 9	CUTS 8	CUTS 7	CUTS 6	CUTS 5	CUTS 4	CUTS 3	CUTS 2	CUTS 1	CUTS 0
36 37	**Charge Under-Temperature Recovery Voltage** If External Temperature 1 or the External Temperature 2 fall below this setting, then the charge FET is turned on and the CUT bit is reset (unless overrides are in place). The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			0A93	(V): (°C):		1.190 +5
	Reserved				CUTR B	CUTR A	CUTR 9	CUTR 8	CUTR 7	CUTR 6	CUTR 5	CUTR 4	CUTR 3	CUTR 2	CUTR 1	CUTR 0
38 39	**Discharge Over-Temperature Voltage** If External Temperature 1 or the External Temperature 2 is less than this voltage, then the discharge FET is turned off and the DOT bit is set. The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			4B6	(V): (°C):		0.530 +55
	Reserved				DOTS B	DOTS A	DOTS 9	DOTS 8	DOTS 7	DOTS 6	DOTS 5	DOTS 4	DOTS 3	DOTS 2	DOTS 1	DOTS 0
3A 3B	**Discharge Over-Temperature Recovery Voltage** If External Temperature 1 or the External Temperature 2 rise above this setting, then the discharge FET is turned on and the DOT bit is reset (unless overrides are in place). The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			053E	(V): (°C):		0.590 +50
	Reserved				DOTR B	DOTR A	DOTR 9	DOTR 8	DOTR 7	DOTR 6	DOTR 5	DOTR 4	DOTR 3	DOTR 2	DOTR 1	DOTR 0
3C 3D	**Discharge Under-Temperature Voltage** If External Temperature 1 or the External Temperature 2 is greater than this voltage, then the discharge FET is turned off and the DUT bit is set. The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			0BF2	(V): (°C):		1.344 -10
	Reserved				DUTS B	DUTS A	DUTS 9	DUTS 8	DUTS 7	DUTS 6	DUTS 5	DUTS 4	DUTS 3	DUTS 2	DUTS 1	DUTS 0
3E 3F	**Discharge Under-Temperature Recovery Voltage** If External Temperature 1 or the External Temperature 2 fall below this setting, then the discharge FET is turned on and the DUT bit is reset (unless overrides are in place). The voltage is based on recommended external components (see Figure 10.26 on page 50).									Default (Hex):			0A93	(V): (°C):		1.190 +5
	Reserved				DUTR B	DUTR A	DUTR 9	DUTR 8	DUTR 7	DUTR 6	DUTR 5	DUTR 4	DUTR 3	DUTR 2	DUTR 1	DUTR 0
40 41	**Internal Over-Temperature Voltage** If the internal temperature is greater than this voltage, then all FETs are turned off and the IOT bit is set.									Default (Hex):			67CH	(V): (°C):		0.73 +115
	Reserved				IOTS B	IOTS A	IOTS 9	IOTS 8	IOTS 7	IOTS 6	IOTS 5	IOTS 4	IOTS 3	IOTS 2	IOTS 1	IOTS 0
42 43	**Internal Over-Temperature Recovery Voltage** When the internal temperature voltage drops below this level, then the FETs can be turned on again and the IOT bit is reset on the next µC read.									Default (Hex):			621H	(V): (°C):		0.69 +95
	Reserved				IOTR B	IOTR A	IOTR 9	IOTR 8	IOTR 7	IOTR 6	IOTR 5	IOTR 4	IOTR 3	IOTR 2	IOTR 1	IOTR 0
44 45	**Sleep Level Voltage** If any cell voltage is below this threshold voltage for a sleep delay time, the device goes into the Sleep mode.									Default (Hex):			06AA	(V):		2.0
	Reserved				SLLB	SLLA	SLL 9	SLL 8	SLL 7	SLL 6	SLL 5	SLL 4	SLL 3	SLL 2	SLL 1	SLL 0

Table 24.15 EEPROM Register Detail (Continued)

Bit/ ADDR	F 7	E 6	D 5	C 4	B 3	A 2	9 1	8 0	7	6	5	4	3	2	1	0
46 47	Sleep Delay Timer/Watchdog Timer **Sleep Delay** This value sets the time that is required for any cell to be below the sleep voltage threshold before the device enters the Sleep mode. Lower 10 bits set the time. Upper 1 bit sets the time base.									Default (Hex):			FC0F	Sleep WDT	(s) (s)	1 31
	Watchdog Timer (WDT) Time allowed the microcontroller between I²C slave byte writes to the ISL94202 after setting any override bit.															
	WDT4	WDT3	WDT2	WDT1	WDT0	SLTA	SLT9	SLT8	SLT7	SLT6	SLT5	SLT4	SLT3	SLT2	SLT1	SLT0
	0 to 31 seconds					00 = µs 01 = ms 10 = s 11 = min		0 to 511								
48 49	Sleep Mode Timer/Cell Configuration **Mode Timer** Time required to enter Sleep mode from the Doze mode when no current is detected.									Default (Hex):			83FF	Idle/ Doze: Sleep Mode	(min) (min) Cells	15 240 3
	Cell Configuration Only these combinations are acceptable. Any other combination will prevent any FET from turning on.															
	CELL8	CELL7	CELL6	CELL5	CELL4	CELL3	CELL2	CELL1	MOD7	MOD6	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0
	8 7 6 5 4 3 2 1				NUMBER OF CELLS				Idle and Doze Mode: [MOD3:0] = 0 to 15 Minutes Sleep Mode [MOD7:4] = 0 to 240 Minutes Example: Value = 0101 1010 Idle/Doze = 10 minutes Sleep = 80 minutes							
	1 0 0 0 0 0 1 1				3 Cells connected											
	1 1 0 0 0 0 1 1				4 Cells connected											
	1 1 0 0 0 1 1 1				5 Cells connected											
	1 1 1 0 0 1 1 1				6 Cells connected											
	1 1 1 0 1 1 1 1				7 Cells connected											
	1 1 1 1 1 1 1 1				8 Cells connected											

Table 24.16 EEPROM Register Detail (Feature Controls)

Bit/ ADDR	7	6	5	4	3	2	1	0
4A	CFPSD CELLF PSD 1 = Activates PSD output when a “Cell Fail” condition occurs. 0 = Does NOT activate PSD output when a cell fails condition occurs.	Reserved	XT2M xTemp 2 Mode Control 1 = xT2 monitors FET temp. Cell balance outputs are not shut off when xT2 temperature exceeds Cell Balance limits 0 = xT2 monitors cell temp. (Normal operation.)	TGain External Temp Gain 1 = Gain of iT, xT1 and xT2 inputs is 1x. 0 = Gain of iT, xT1 and xT2 inputs is 2x.	Reserved, this bit must be 0.	**PCFETE** Precharge FET Enable 1 = Precharge FET output turns on instead of the CFET output when any of the cell voltages are below the under the LVCHG threshold. 0 = Precharge FET is not used	**DOWD** Disable Open-Wire Scan 1 = Disable the input open-wire detection scan 0 = Enable the input open-wire detection scan	**OWPSD** Open-Wire PSD 1 = Responds automatically to the input Open Wire condition AND sets PSD. 0 = Responds automatically to the input Open Wire condition and DOES NOT set PSD.
4B	CBDD CB during Discharge 1 = Do balance during discharge 0 = No balance during discharge When both CBDD and CBDC equal “0”, cell balance is turned off.	CBDC CB during Charge 1 = Do balance during charge 0 = No balance during charge When both CBDD and CBDC equal “0”, cell balance is turned off.	DFODUV DFET on during UV (Charging) 1 = Keep DFET on while the pack is charging, regardless of the cell voltage. This minimizes DFET power dissipation during UV, when the pack is charging 0 = Normal DFET operation.	CFODOV CFET on during OV (Discharging) 1 = Keep CFET on while the pack is discharging, regardless of the cell voltage. This minimizes CFET power dissipation during OV, when the pack is discharging 0 = Normal CFET operation.	UVLOPD Enable UVLO Power-Down 1 = The device powers down when detecting an UVLO condition. 0 = When a UVLO condition is detected, the device remains powered.	Reserved	Reserved	CB_EOC Enable CBAL during EOC 1 = Cell balance occurs during EOC condition regardless of current direction. 0 = Cell balance turns off during EOC if there is no current flowing.
4C 4F	Reserved							
50 57	User EEPROM Available to the user (Note: There is no shadow memory associated with these registers).							

25. Registers: Detailed (RAM)

Table 25.17 RAM Register Detail (Status and Control)

Bit/ ADDR	7	6	5	4	3	2	1	0
80 (Read only) These bits are set and reset by the device.	CUT Charge Under-Temp An external thermistor shows the temp is lower than the minimum charge temp limit.	COT Charge Over-Temp An external thermistor shows the temp is higher than the maximum charge temp limit.	DUT Discharge Under-Temp An external thermistor shows the temp is lower than the minimum discharge temp limit.	DOT Discharge Over-Temp An external thermistor shows the temp is higher than the maximum discharge temp limit.	UVLO Undervoltage Lockout At least one cell is below the undervoltage lockout threshold.	**UV** Undervoltage At least one cell has an undervoltage condition.	**OVLO** Overvoltage Lockout At least one cell is above the overvoltage lockout threshold.	**OV** Overvoltage At least one cell has an overvoltage condition.
81 (Read only) These bits are set and reset by the device	EOCHG End of charge End of charge voltage reached.	Reserved	OPEN Open wire An open input circuit is detected.	CELLF Cell Fail Indicates that there is more than the maximum allowable voltage difference between cells.	DSC Discharge Short-Circuit Short-circuit current detected.	DOC Discharge Overcurrent Excessive Discharge current detected.	COC Charge Overcurrent Excessive Charge current detected.	IOT Internal Over-Temp The internal sensor indicates an over-temp condition.
82 (Read only) These bits are set and reset by the device	LVCHG Low Voltage Charge At least one cell voltage < LVCHG threshold. If set, PCFET turns on instead of CFET.	**INT_SCAN** Internal Scan In-Progress When this bit is "0" for the duration of the internal scan.	**ECC_FAIL** EEPROM Error Correct Fail EEPROM error correction failed. Two bits failed, error not corrected. Previous value retained.	ECC_USED EEPROM Error Correct EEPROM error correction used. One bit failed, bit error corrected.	DCHING Discharging Indicates that a discharge current is detected. Charge current is flowing out of the pack.	CHING Charging Indicates that a charge current is detected. Charge current is flowing into the pack.	CH_PRSNT Chrgr Present Set to "1" during COC, while charger is attached. (CHMON > threshold.) If µCLMON = 0, bit resets automatically. If µCLMON = 1, bit resets by µC read of register.	LD_PRSNT Load Present Set to "1" during DOC or DSC, while load attached. (LDMON < threshold.) If µCCMON = 0, bit resets automatically. If µCCMON = 1, bit resets by µC read of register.
83 (Read only) These bits are set and reset by the device	Reserved	IN_SLEEP In Sleep Mode No scans. RGO remains on, VREF off. Monitors for a charger or load connection.	IN_DOZE In Doze mode Scans every 512ms	IN_IDLE In Idle Mode Scans every 256ms	CBUV Cell Balance Undervoltage All cell voltages < the minimum allowable cell balance voltage threshold.	CBOV Cell Balance Overvoltage All cell voltages > the maximum allowable cell balance voltage threshold.	CBUT Cell Balance Under-Temp xT1 or xT2 indicates temp < allowable cell balance low temperature threshold	CBOT Cell Balance Over-Temp xT1 or xT2 indicates temp > allowable cell balance high temperature threshold
84 (R/$\overline{W}$)	Cell balance FET control bits These bits control the cell balance when the external controller overrides the internal cell balance operation.							
	CB8ON	CB7ON	CB6ON	CB5ON	CB4ON	CB3ON	CB2ON	CB1ON
	If µCCBAL = 1, CBAL_ON = 1 and CBnON bit = 1 the cell balance FET is on. If µCCBAL = 0, CBAL_ON = 0 or CBnON bit = 0 the cell balance FET is off.							

Table 25.17 RAM Register Detail (Status and Control) (Continued)

Bit/ ADDR	7	6	5	4	3	2	1	0
85 (R/$\overline{\text{W}}$)	Analog MUX control bits Voltage monitored by ADC when microcontroller overrides the internal scan operation.							
	Current Gain Setting Current gain set when current is monitored by ADC. Only used when microcontroller overrides the internal scan.							
	ADC Conversion Start							
	Reserved	ADCSTRT	CG1	CG0	AO3	AO2	AO1	AO0
		Ext µC sets this bit to 1 to start a conversion	**CG1 0** 0 0 0 1 1 0 1 1	**Gain** x50 x5 x500 x500	**AO3 2 1 0** 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1	OFF VC1 VC2 VC3 VC4 VC5 VC6 VC7	**AO3 2 1 0** 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	VC8 Pack current VBAT/16 RGO/2 xT1 xT2 iT OFF
86 (R/$\overline{\text{W}}$)	CLR_LERR Clear load error 1 = Resets load monitor error condition. This bit is automatically cleared. Only active when µCCMON = 1	LMON_EN Load monitor enable 1 = Load monitor on 0 = Load monitor off Only active when µCLMON = 1	CLR_ERR Clear charge error 1 = Resets charge monitor error condition. This bit is automatically cleared. Only active when µCCMON = 1	CMON_EN Charge monitor enable 1 = Charger monitor on 0 = Charger monitor off. Only active when µCCMON = 1	PSD Pack shut down 1 = PSD on 0 = PSD off	PCFET Pre-charge FET 1 = PCFET on 0 = PCFET off Bit = 0 if DOC or DSC, unless the automatic response is disabled by µCFET bit. (4)	CFET Charge FET 1 = CFET on 0 = CFET off Bit = 0 if COC, unless the automatic response is disabled by µCFET bit. (4)	DFET Discharge FET 1 = DFET on 0 = DFET off Bit = 0 if DOC or DSC unless the automatic response is disabled by µCFET bit. (4)
87 (R/$\overline{\text{W}}$)	Reserved	µCFET µC does FET control 1 = FETs controlled by external µC. 0 = Norm automatic FET control (7), (10)	µCCBAL µC does cell balance 1 = Internal balance disabled. µC manages cell balance 0 = internal balance enabled. (7)	µCLMON µC does load monitor 1 = Load monitor on 0 = Load monitor off (7)	µCCMON µC does charger mon 1 = Charge monitor on 0 = Charge monitor off (7)	µCSCAN µC does scan 1 = No auto scan. System controlled by µC. 0 = Normal scan (7), (99)	OW_STRT Open wire start 1 = Does one open-wire scan (bit auto reset to 0) 0 = No scan Only active if DOWD = 1 or µCSCAN = 1	CBAL_ON Cell balance On 1 = (CBnON =1) outputs ON 0 = Cell bal outputs OFF Only active if µCCBAL= 1.
88 (R/$\overline{\text{W}}$)	Reserved	Reserved	Reserved	Reserved	PDWN Power-Down 1 = Power-down the device. 0 = Normal operation	SLEEP Set Sleep 1 = Put device into Sleep mode. 0 = Normal operation	DOZE Set Doze 1 = Put device into Doze mode. 0 = Normal operation	IDLE Set Idle 1 = Put device into Idle mode 0 = Normal operation.
89 (R/$\overline{\text{W}}$)	EEPROM Enable							
								EEEN
	Reserved. These bits should be zero.							0 = RAM access 1 = EEPROM access

Table 25.18 RAM Register Detail (Monitored Voltages)

Bit/ ADDR	F 7	E 6	D 5	C 4	B 3	A 2	9 1	8 0	7	6	5	4	3	2	1	0
8A 8B	**Cell Minimum Voltage** This is the voltage of the cell with the minimum voltage.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELLMINB	CELLMINA	CELLMIN9	CELLMIN8	CELLMIN7	CELLMIN6	CELLMIN5	CELLMIN4	CELLMIN3	CELLMIN2	CELLMIN1	CELLMIN0
8C 8D	**Cell Maximum Voltage** This is the voltage of the cell with the maximum voltage.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELLMAXB	CELLMAXA	CELLMAX9	CELLMAX8	CELLMAX7	CELLMAX6	CELLMAX5	CELLMAX4	CELLMAX3	CELLMAX2	CELLMAX1	CELLMAX0
8E 8F	**Pack Current** This is the current flowing into or out of the pack.									$\frac{HEXvalue_{10} \times 1.8}{4095 \times Gain \times SenseR}$ Polarity identified by CHING and DCHING bits.						
	Reserved				ISNSB	ISNSA	ISNS9	ISNS8	ISNS7	ISNS6	ISNS5	ISNS4	ISNS3	ISNS2	ISNS1	ISNS0
90 91	**Cell 1 Voltage** This is the voltage of CELL1.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL1B	CELL1A	CELL19	CELL18	CELL17	CELL16	CELL15	CELL14	CELL13	CELL12	CELL11	CELL10
92 93	**Cell 2 Voltage** This is the voltage of CELL2.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL2B	CELL2A	CELL29	CELL28	CELL27	CELL26	CELL25	CELL24	CELL23	CELL22	CELL21	CELL20
94 95	**Cell 3 Voltage** This is the voltage of CELL3.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL3B	CELL3A	CELL39	CELL38	CELL37	CELL36	CELL35	CELL34	CELL33	CELL32	CELL31	CELL30
96 97	**Cell 4 Voltage** This is the voltage of CELL4.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL4B	CELL4A	CELL49	CELL48	CELL47	CELL46	CELL45	CELL44	CELL43	CELL42	CELL41	CELL40
98 99	**Cell 5 Voltage** This is the voltage of CELL5.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL5B	CELL5A	CELL59	CELL58	CELL57	CELL56	CELL55	CELL54	CELL53	CELL52	CELL51	CELL50
9A 9B	**Cell 6 Voltage** This is the voltage of CELL6.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL6B	CELL6A	CELL69	CELL68	CELL67	CELL66	CELL65	CELL64	CELL63	CELL62	CELL61	CELL60
9C 9D	**Cell 7 Voltage** This is the voltage of CELL7.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL7B	CELL7A	CELL79	CELL78	CELL77	CELL76	CELL75	CELL74	CELL73	CELL72	CELL71	CELL70

Table 25.18 RAM Register Detail (Monitored Voltages)(Continued)

Bit/ ADDR	F 7	E 6	D 5	C 4	B 3	A 2	9 1	8 0	7	6	5	4	3	2	1	0
9E 9F	**Cell 8 Voltage** This is the voltage of CELL8.									$\frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$						
	Reserved				CELL8B	CELL8A	CELL89	CELL88	CELL87	CELL86	CELL85	CELL84	CELL83	CELL82	CELL81	CELL80
A0 A1	**Internal Temperature** This is the voltage reported by the ISL94202 internal temperature sensor.									$\frac{HEXvalue_{10} \times 1.8}{4095}$						
	Reserved				iTB	iTA	iT9	iT8	iT7	iT6	iT5	iT4	iT3	iT2	iT1	iT0
A2 A3	**External Temperature 1** This is the voltage reported by an external thermistor divider on the xT1 pin.									$\frac{HEXvalue_{10} \times 1.8}{4095}$						
	Reserved				xT1B	xT1A	xT19	xT18	xT17	xT16	xT15	xT14	xT13	xT12	xT11	xT10
A4 A5	**External Temperature 2** This is the voltage reported by an external thermistor divider on the xT2 pin.									$\frac{HEXvalue_{10} \times 1.8}{4095}$						
	Reserved				xT2B	xT2A	xT29	xT28	xT27	xT26	xT25	xT24	xT23	xT22	xT21	xT20
A6 A7	**VBATT Voltage** This is the voltage of Pack.									$\frac{HEXvalue_{10} \times 1.8 \times 32}{4095}$						
	Reserved				VBB	VBA	VB9	VB8	VB7	VB6	VB5	VB4	VB3	VB2	VB1	VB0
A8 A9	**VRGO Voltage** This is the voltage of ISL94202 2.5V regulator.									$\frac{HEXvalue_{10} \times 1.8 \times 2}{4095}$						
	Reserved				RGOB	RGOA	RGO 9	RGO 8	RGO 7	RGO 6	RGO 5	RGO 4	RGO 3	RGO 2	RGO 1	RGO 0

Table 25.18 RAM Register Detail (Monitored Voltages)(Continued)

<table>
<tr><th>Bit/
ADDR</th><th>F
7</th><th>E
6</th><th>D
5</th><th>C
4</th><th>B
3</th><th>A
2</th><th>9
1</th><th>8
0</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="2">AA
AB</td><td colspan="8">**14-Bit ADC Voltage**
This is the calibrated voltage out of the ISL94202 ADC. In normal scan mode, this value is not usable, because it cannot be associated with a specific monitored voltage. However, when the µC takes over the scan operations, this value can be useful. This is a 2’s complement number.</td><td colspan="8">$\text{if..HEXvalue}_{10} \geq 8191 \rightarrow \frac{(\text{HEXvalue}_{10} - 16384) \times 1.8}{8191}$
$\text{else} \rightarrow \frac{\text{HEXvalue}_{10} \times 1.8}{8191}$</td></tr>
<tr><td colspan="2">Reserved</td><td>ADC
D</td><td>ADC
C</td><td>ADC
B</td><td>ADC
A</td><td>ADC
9</td><td>ADC
8</td><td>ADC
7</td><td>ADC
6</td><td>ADC
5</td><td>ADC
4</td><td>ADC
3</td><td>ADC
2</td><td>ADC
1</td><td>ADC
0</td></tr>
</table>

Notes:

1. A “1” written to a control or configuration bit causes the action to be taken. A “1” read from a status bit indicates that the condition exists.
2. “Reserved” indicates that the bit or register is reserved for future expansion. When writing to RAM addresses, write a reserved bit with the value “0”. Do not write to reserved registers at addresses 4CH through 4FH, 58H through 7FH, or ACH through FFH. Ignore reserved bits that are returned in a read operation.
3. The IN_SLEEP bit is cleared on initial power up, by the CHMON pin going high or by the LDMON pin going low.
4. When the automatic responses are enabled, these bits are automatically set and reset by hardware when any conditions indicate. When automatic responses are over-ridden, an external microcontroller I^2C write operation controls the respective FET and a read of the register returns the current state of the FET drive output circuit (though not the actual voltage at the output pin).
5. Setting EEEN to 0 prior to a read or write to the EEPROM area results in a read or write to the shadow memory. Setting EEEN to “1” prior to a read or write from the EEPROM area results in a read or write from the non-volatile array locations.
6. Writes to EEPROM registers require that the EEEN bit be set to “1” and all other bits in EEPROM enable register set to “0” prior to the write operation.
7. This bit is reset when the Watchdog timer is active and expires.
8. The memory is configured as eight pages of 16 bytes. The I^2C can perform a “page write” to write all values on one page in a single cycle.
9. Setting this bit to “1” disables all internal voltage and temperature scans. When set to “1”, the external µC needs to process all overvoltage, undervoltage, over-temp, under temp and all cell balance operations.
10. Short-Circuit, Open-Wire, Internal Over Temperature, OVLO and UVLO faults, plus Sleep, and FETSOFF conditions override the µCFET control bit and automatically force the appropriate power FETs off.

26. Revision History

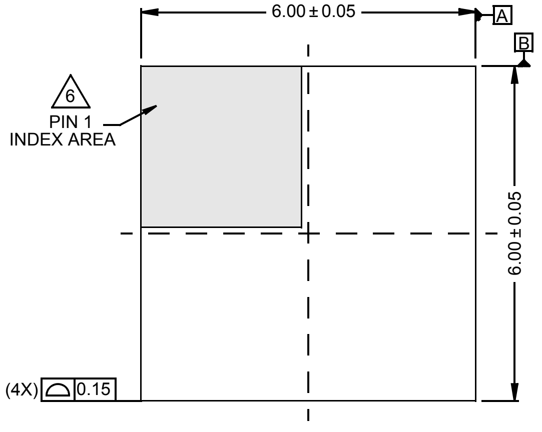
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

Date	Revision	Change
Mar 7, 2017	FN8889.2	Updated entire datasheet to new standards. Updated Applications section on page 1 Added Table #1.1 on page 4.
Dec 12, 2016	FN8889.1	Ordering Information table on page 4, updated Note 1 to include tape and reel options and quantities. ESD Rating on page 8, Human Body Model (Tested per JESD22-A114F) changed from: 2kV to: 1.5kV
Oct 24, 2016	FN8889.0	Initial Release.

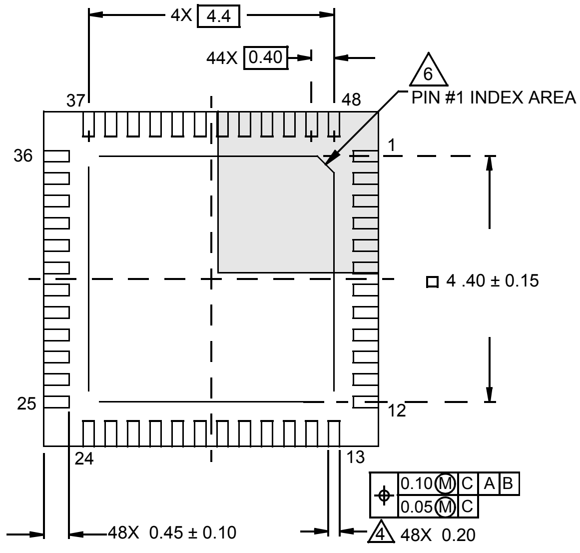
27. Package Outline Drawing

For the most recent package outline drawing, see L48.6x6

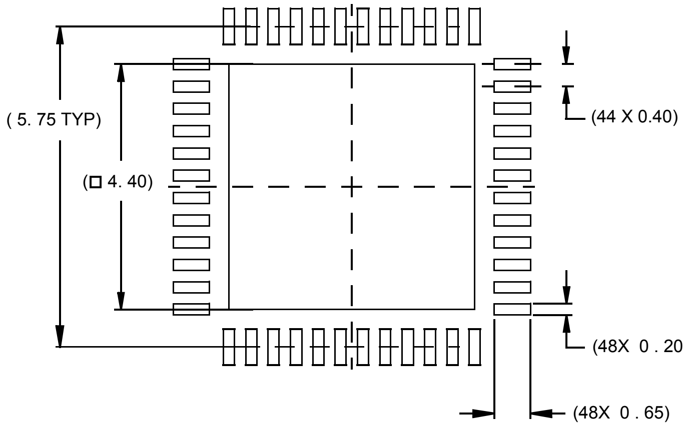
L48.6x6
48 Lead Thin Quad Flat No-Lead Plastic Package
Rev 2, 7/14



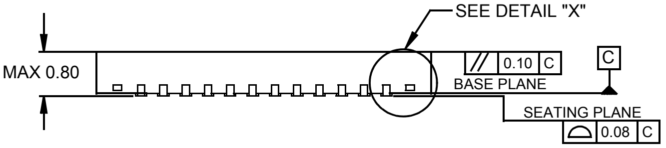
TOP VIEW



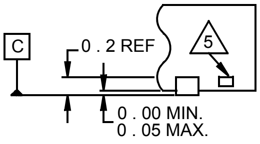
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

28. About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

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