ADS7142 Nanopower, Dual-Channel, Programmable Sensor Monitor

1 Features

- Standalone, Nanopower Sensor Monitor for Cost-sensitive Designs
- Small Package Size: 1.5 mm x 2 mm
- Efficient Host Sleep and Wake-up
  - Autonomous Monitoring at 900 nW
  - Windowed Comparator for Event-triggered Host Wake-up
  - Data Buffering during Host Sleep
- Independent Sensor Configuration and Calibration
  - Dual-Channel, Pseudo-Differential, or Ground-Sense Input Configuration
  - Programmable Thresholds for Calibration
  - Internal Calibration improves Offset and Drift
- False Trigger Prevention
  - Programmable Thresholds per Channel
  - Programmable Hysteresis for Noise Immunity
  - Event Counter for Transient Rejection
- Deep Data Analysis
  - Data Buffer for Fault Diagnostics
  - High Precision Mode for 16-bit Accuracy
  - One-Shot Mode for Fast Data Capture
- I^2C™ Interface
  - Compatible from 1.65 V to 3.6 V
  - 8 Configurable Addresses
  - Up to 3.4 MHz (High Speed)
- Wide Operating Range
  - Analog Supply: 1.65 V to 3.6 V
  - Temperature Range: –40°C to 125°C

2 Applications

- Sensor Nodes for Internet of Things (IoT)
- Gas, Heat, PIR Motion and Smoke Detectors
- Preventive Maintenance for Elevators, Escalators, HVAC, Industrial Equipment, and so forth
- Wearable Electronics
- Zero Cross Detection for Fault Indicators
- Supervisory Functions
- Comparator with Programmable Reference
- Sensors for Deep Learning Artificial Intelligence

3 Description

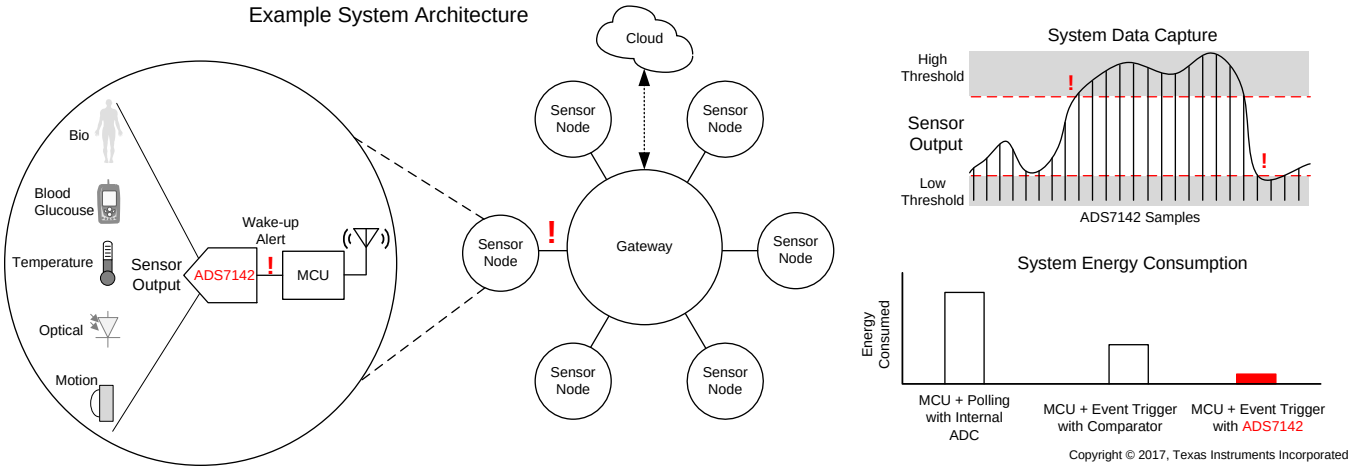
The ADS7142 autonomously monitors signals while optimizing system power, reliability, and performance. It implements event-triggered interrupts per channel using a digital windowed comparator with programmable high and low thresholds, hysteresis, and event counter. The device includes a dual-channel analog multiplexer in front of a successive approximation register analog-to-digital converter (SAR ADC) followed by an internal data buffer for converting and capturing data from sensors.

The ADS7142 is available in 10-pin QFN package and consumes only 900 nW of power. The small form-factor and low power consumption make this device suitable for space-constrained and/or battery-powered applications.

Device Information(1)

PART NAME	PACKAGE	BODY SIZE (NOM)
ADS7142	X2QFN (10)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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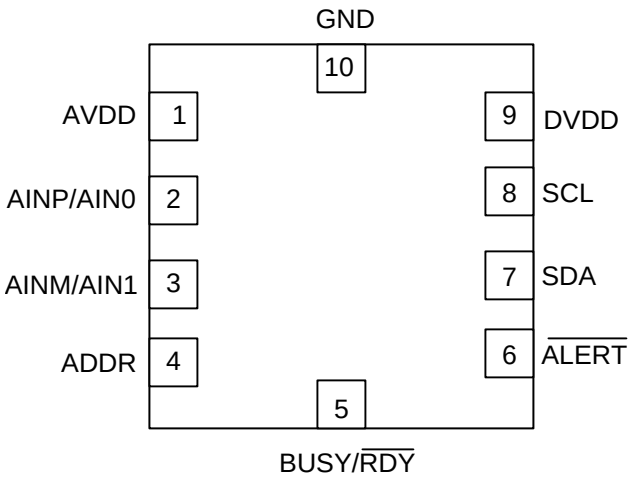
4 Revision History

Changes from Original (September 2017) to Revision A **Page**

- Changed the device status from *Advance Information* to *Production Data* ... 1

5 Pin Configuration and Functions

RUG PACKAGE
10-Pin X2QFN
TOP VIEW



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	1	Supply	Analog supply input, also used as the reference voltage for analog-to-digital conversion.
AINP/AIN0	2	Analog input	Single-Channel operation: Positive analog signal input Two-Channel operation: Analog signal input, Channel 0
AINM/AIN1	3	Analog input	Single-Channel operation: Negative analog signal input Two-Channel operation: Analog signal input, Channel 1
ADDR	4	Analog Input	Input for selecting I^2C address of the device. The device address can be selected from one of the eight values by connecting resistors on this pin. Refer Table 2 for details
BUSY/$\overline{RDY}$	5	Digital output	The device pulls this pin high when it is scanning through channels in a sequence and brings this pin low when sequence is completed or aborted.
$\overline{ALERT}$	6	Digital output	Active low, open drain output. Status of this pin is controlled by Digital window comparator block. Connect a pull-up resistor from DVDD to this pin
SDA	7	Digital input/output	Serial data in/out for I^2C interface. Connect a pull-up resistor from DVDD to this pin
SCL	8	Digital input	Serial clock for I^2C interface. Connect a pull-up resistor from DVDD to this pin
DVDD	9	Supply	Digital I/O supply voltage
GND	10	Supply	Ground for power supply, all analog and digital signals are referred to this pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
ADDR to GND	–0.3	AVDD + 0.3	V
AVDD to GND	–0.3	3.9	V
DVDD to GND	–0.3	3.9	V
AINP/AIN0 to GND	–0.3	AVDD + 0.3	V
AINM/AIN1 to GND	–0.3	AVDD + 0.3	V
Input current on any pin except supply pins	-10	10	mA
Digital Input to GND	–0.3	DVDD + 0.3	V
Storage Temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog Supply Voltage Range	1.65		3.6	V
DVDD	Digital Voltage Supply Voltage Range	1.65		3.6	A
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–60		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS7142 RUG 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics - All Modes

At TA = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT - Two-Channel Single-Ended Configuration						
	Full-scale input voltage span(1)	AINP/AIN0 to GND or AINM/AIN1 to GND	0		AVDD	V
	Absoulte Input voltage range	AINP/AIN0 to GND or AINM/AIN1 to GND	–0.1		AVDD + 0.1	V
ANALOG INPUT - Single-Channel Single-Ended Configuration (with Remote Ground Sense)						
	Full-scale input voltage span(1)	AINP/AIN0 to GND or AINM/AIN1 to GND	0		AVDD	V
	Absoulte Input voltage range	AINP/AIN0 to GND	–0.1		AVDD + 0.1	V
		AINM/AIN1 to GND	–0.1		0.1	V
ANALOG INPUT - Single-Channel Pseudo-Differential Configuration						
	Full-scale input voltage span(1)	AINP/AIN0 to GND or AINM/AIN1 to GND	–AVDD/2		AVDD/2	V
	Absoulte Input voltage range	AINP/AIN0 to GND	–0.1		AVDD + 0.1	V
		AINM/AIN1 to GND	AVDD/2–0.1		AVDD/2+0.1	V
Internal Oscillator						
t_{HSO}	Time Period for High Speed Oscillator			50	110	ns
t_{LPO}	Time Period for Low Power Oscillator			95.2	300	µs
Digital Input/Output (SCL, SDA)						
V_{IH}	High Level input Voltage		0.7 × DVDD		DVDD	V
V_{IL}	Low Level input Voltage		0		0.3 × DVDD	V
V_{OL}	Low Level output Voltage	With 3 mA Sink Current and DVDD > 2 V	0		0.4	V
		With 3 mA Sink Current and 1.65 V < DVDD < 2 V	0		0.2 × DVDD	V
I_{OL}	Low Level Output Current (Sink)	V_{OL} = 0.4 V for Standard and Fast Mode (100, 400 kHz)	3			mA
		V_{OL} = 0.6 V for Fast Mode (400 kHz)	6			
		V_{OL} = 0.4 V Fast Mode Plus (1 MHz)	20			
I_{OL}	Low Level Output Current (Sink)	V_{OL}= 0.4 V High Speed (1.7 MHz, 3.4 MHz)	25			mA
I_I	Input Current on Pin				10	µA
C_I	Input Capacitance on Pin				10	pF
Digital Output (BUSY/$\overline{\text{RDY}}$)						
V_{OH}	High Level Output Voltage	I_{source} = 2 mA	0.7 × DVDD		DVDD	V
V_{OL}	High Level Output Voltage	I_{sink} = 2 mA	0		0.3 × DVDD	V
Digital Output ($\overline{\text{ALERT}}$)						
I_{OL}	Low Level Output Current	V_{OL} < 0.25 V		5		mA
V_{OL}	Low Level Output Voltage	I_{sink} = 5 mA	0		0.25	V
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog Supply Voltage		1.65		3.6	V
DVDD	Digital I/O Suplly Voltage		1.65		3.6	V

(1) Ideal Input span, does not include gain or offset error.

6.6 Electrical Characteristics - Manual Mode

At TA = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sampling Dynamics						
t_{conv}	Conversion Time	AVDD = 1.65 to 3.6V			1.8	µs
t_{acq}	Acquistion Time	AVDD = 1.65 to 3.6V		18		T_{SCL}
t_{cycle}	Cycle Time	AVDD = 1.65 to 3.6V		(t_{conv} + t_{acq})		µs
DC Specifications						
	Resolution			12		Bits
NMC	No Missing Codes	AVDD = 1.65 to 3.6V	12			Bits
DNL	Differential nonlinerity	AVDD = 1.65 to 3.6V	–0.99	±0.3	1	LSB(1)
INL	Integral nonlinearity		–2.75	±0.5	2.75	LSB
E_O	Offset Error	Post Offset Calibration	–2.9	±0.5	2.9	LSB
dV_{OS}/dT	Offset Drift with Temperature	Post Offset Calibration		5		ppm/°C
E_G	Gain Error		–0.1	±0.03	0.1	%FSR
	Gain Error Drift with Temperature			5		ppm/°C
AC Specifications						
SNR(2)	Signal-to-Noise Ratio	f_{in} = 2 kHz, AVDD = 3 V, f_{sample} =140 kSPS	68.75	71.4		dB
		f_{in} = 2 kHz, AVDD = 1.8 V, f_{sample} =140 kSPS		69.2		dB
THD(2) (3)	Total Harmonic Distortion	f_{in} = 2 kHz, AVDD = 3 V, f_{sample} =140 kSPS		–87.0		dB
		f_{in} = 2 kHz, AVDD = 1.8 V, f_{sample} =140 kSPS		–84.0		dB
SINAD(2)	Signal-to-Noise and distortion	f_{in} = 2 kHz, AVDD = 3 V, f_{sample} =140 kSPS	68.5	71.2		dB
		f_{in} = 2 kHz, AVDD = 1.8 V, f_{sample} =140 kSPS		69.0		dB
SFDR(2)	Spurious Free dynamic range	f_{in} = 2 kHz, AVDD = 3 V, f_{sample} =140 kSPS		91.0		dB
BW	-3dB Small Signal Bandwidth			25.0		MHz
Power Consumption						
I_{AVDD}	Analog Supply Current	f_{sample} =140 kSPS, SCL = 3.4 MHz		265	300	µA
		f_{sample} =5.5 kSPS, SCL = 100 kHz		8		µA
		f_{sample} =140 kSPS, SCL = 3.4 MHz, AVDD = 1.8 V		160		µA
		f_{sample} =5.5 kSPS, SCL = 100 kHz, AVDD = 1.8 V		5		µA
I_{DVDD}	Digital Supply Current	f_{sample} =140 kSPS, SCL = 3.4 MHz, SDA = AAA0h		25		µA
		f_{sample} =5.5 kSPS, SCL = 100 kHz, AVDD = 1.8 V, SDA = AAA0h		1.5		µA
I_{AVDD}	Static Analog Supply Current	No Activity on SCL and SDA, BUSY/$\overline{RDY}$ Low		6		nA
I_{DVDD}	Static Analog Supply Current	No Activity on SCL and SDA, BUSY/$\overline{RDY}$ Low		2		nA

(1) LSB means least significant byte. Refer to ADC Transfer Function for details.
(2) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(3) Calculated on the first nine harmonics of the input frequency.

6.7 Electrical Characteristics - Autonomous Modes

At T_A = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sampling Dynamics						
t_{conv}	Conversion Time	High Speed Oscillator		14		t_{HSO}
		Low Power Oscillator		14		t_{LPO}
t_{acq}	Acquistion Time	High Speed Oscillator	7			t_{HSO}
		Low Power Oscillator	4			t_{LPO}
t_{cycle}	Cycle Time	High Speed Oscillator		nCLK		t_{HSO}
		Low Power Oscillator		nCLK		t_{LPO}
DC Specifications						
	Resolution			12		Bits
E_O	Offset Error	Post Offset Calibration		±0.5		LSB
E_G	Gain Error			±0.03		%FSR
Power Consumption						
I_{AVDD}	Analog Supply Current	With Low Power Oscillator, nCLK =18		0.75		µA
		With Low Power Oscillator, AVDD = 1.8 V, nCLK =18		0.45		µA
		With Low Power Oscillator, nCLK = 250		0.5		µA
		With High Speed Oscillator, nCLK =21		940		µA
I_{DVDD}	Digital Supply Current	With Low Power Oscillator, nCLK =18, DVDD =3.3 V		0.15		µA
I_{AVDD}	Static Analog Supply Current	No Activity on SCL and SDA, BUSY/$\overline{RDY}$ Low		5		nA
I_{DVDD}	Static Analog Supply Current	No Activity on SCL and SDA, BUSY/$\overline{RDY}$ Low		0.6		nA

6.8 Electrical Characteristics - High Precision Mode

At T_A = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Specifications						
	Resolution(2)			16		Bits
ENOB	Effective number of bits	With DC Input of AVDD/2(3)		15.4		
E_O	Offset Error	Post Offset Calibration		±10		LSB
E_G	Gain Error			±0.03		%FSR
Power Consumption						
I_{AVDD}	Analog Supply Current	With Low Power Oscillator, nCLK =18		0.6		µA
		With Low Power Oscillator, AVDD = 1.8 V, nCLK =18		0.3		µA
		With Low Power Oscillator, nCLK = 250		0.5		µA
		With High Speed Oscillator, nCLK =21		980		µA
I_{DVDD}	Digital Supply Current	With Low Power Oscillator, nCLK =21, DVDD =3.3 V		0.2		µA
I_{AVDD}	Static Analog Supply Current	No Activity on SCL and SDA, BUSY/$\overline{RDY}$ Low		5		nA
I_{DVDD}	Static Analog Supply Current	No Activity on SCL and SDA, BUSY/$\overline{RDY}$ Low		0.7		nA

(1) Sampling Dynamics for High Precision Mode are same as for Autonomous modes.
(2) Refer to Equation 5
(3) For DC Input, ENOB = Ln[FSR/Standard deviation of Codes]/Ln[2]. Refer to Figure 34

6.9 Timing Requirements

At T_A = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted.(1)

PARAMETER		Test Conditions	MIN	MAX	UNIT
Standard-mode (100 kHz) Figure 1					
f_{SCL}	SCL clock frequency		0	100	kHz
t_{HD-STA}	Hold time (repeated) START condition	After this period, the first clock pulse generated.	4		µs
t_{LOW}	Low period of SCL		4.7		µs
t_{HIGH}	High period of SCL		4		µs
t_{SU-STA}	set-up time for a repeated start condition		4.7		µs
t_{HD-DAT} (2) (3)	data hold time	For I^2C Bus devices	0		µs
t_{SU-DAT}	data setup time		250		ns
t_{SU-STO}	setup-up time for STOP condition		4		µs
t_{BUF}	bus free time between a STOP and START condition		4.7		µs
C_b	capacitive load on each line			400	pF
Fast-mode (400 kHz) Figure 1					
f_{SCL}	SCL clock frequency		0	400	kHz
t_{HD-STA}	Hold time (repeated) START condition		0.6		µs
t_{LOW}	Low period of SCL		1.3		µs
t_{HIGH}	High period of SCL		0.6		µs
t_{SU-STA}	set-up time for a repeated start condition		0.6		µs
t_{HD-DAT}	data hold time		0		µs
t_{SU-DAT}	data setup time		100		ns
t_{SU-STO}	setup-up time for STOP condition		0.6		µs
t_{BUF}	bus free time between a STOP and START condition		1.3		µs
C_b	capacitive load on each line			400	pF
Fast-mode Plus (1000 kHz) Figure 1					
f_{SCL}	SCL clock frequency		0	1000	kHz
t_{HD-STA}	Hold time (repeated) START condition		0.26		µs
t_{LOW}	Low period of SCL		0.5		µs
t_{HIGH}	High period of SCL		0.26		µs
t_{SU-STA}	set-up time for a repeated start condition		0.26		µs
t_{HD-DAT}	data hold time		0		µs
t_{SU-DAT}	data setup time		50		ns
t_{SU-STO}	setup-up time for STOP condition		0.26		µs
t_{BUF}	bus free time between a STOP and START condition		0.5		µs
C_b	capacitive load on each line			550	pF
High Speed mode (1.7 MHz) C_b = 400 pF (Max) Figure 2					
f_{SCLH}	SCLH clock frequency		0	1.7	MHz
t_{HD-STA}	Hold time (repeated) START condition		160		ns
t_{LOW}	Low period of SCL		320		ns
t_{HIGH}	High period of SCL		120		ns
t_{SU-STA}	set-up time for a repeated start condition		160		ns
t_{HD-DAT}	data hold time		0	150	ns

(1) All values referred to $V_{IH(min)}$ (0.7 DVDD) and $V_{IL(max)}$ (0.3 DVDD)
(2) t_{HD-DAT} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(3) The maximum t_{HD-DAT} could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD-DAT} or t_{VD-ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock is streched, the data must be valid by the set-up time before it releases.

Timing Requirements (continued)

At T_A = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted.(1)

PARAMETER		Test Conditions	MIN	MAX	UNIT
t_{SU-DAT}	data setup time		10		ns
t_{SU-STO}	setup-up time for STOP condition		160		ns
C_b	capacitive load on each line			400	pF
High Speed mode (3.4 MHz) C_b = 100 pF (Max) Figure 2					
f_{SCLH}	SCLH clock frequency		0	3.4	MHz
t_{HD-STA}	Hold time (repeated) START condition		160		ns
t_{LOW}	Low period of SCL		160		ns
t_{HIGH}	High period of SCL		60		ns
t_{SU-STA}	set-up time for a repeated start condition		160		ns
t_{HD-DAT}	data hold time		0	70	ns
t_{SU-DAT}	data setup time		10		ns
t_{SU-STO}	setup-up time for STOP condition		160		ns
C_b	capacitive load on each line			100	pF

6.10 Switching Characteristics

At T_A = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted.(1)

PARAMETER		Test Conditions	MIN	MAX	UNIT
Standard-mode (100 kHz) Figure 1					
t_{rCL}	Rise time of SCL			1000	ns
t_{rDA}	Rise time of SDA			1000	ns
t_{fCL}	Fall time of SCL			300	ns
t_{fDA}	Fall time of SDA			300	ns
t_{VD-DAT} (2)	data valid time			3.45	µs
t_{VD-ACK} (2)	data hold time			3.45	µs
Fast-mode (400 kHz) Figure 1					
t_{rCL}	Rise time of SCL		20	300	ns
t_{rDA}	Rise time of SDA		20	300	ns
t_{fCL}	Fall time of SCL		20 × DVDD/3.6	300	ns
t_{fDA}	Fall time of SDA		20 × DVDD/3.6	300	ns
t_{VD-DAT}	data valid time			0.9	µs
t_{VD-ACK}	data hold time			0.9	µs
t_{SP} (3)	pulse width of spikes suppressed by the input filter		0	50	ns
Fast-mode Pus (1000 kHz) Figure 1					
t_{rCL}	Rise time of SCL			120	ns
t_{rDA}	Rise time of SDA			120	ns
t_{fCL}	Fall time of SCL		20 × DVDD/3.6	120	ns
t_{fDA}	Fall time of SDA		20 × DVDD/3.6	120	ns
t_{VD-DAT}	data valid time			0.45	µs
t_{VD-ACK}	data hold time			0.45	µs
t_{SP}	pulse width of spikes suppressed by the input filter		0	50	ns
High Speed mode (1.7 MHz) C_b = 400 pF (Max) Figure 2					
t_{rCL}	Rise time of SCLH		20	80	ns

(1) All values referred to $V_{IH(min)}$ (0.7 DVDD) and $V_{IL(max)}$ (0.3 DVDD)
(2) t_{VD-DAT} = time for data signal from SCL LOW to SDA output.
(3) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

Switching Characteristics (continued)

At T_A = -40°C to 125°C, AVDD = 3V, DVDD = 1.65 to 3.6V, All Channel Configurations, unless otherwise noted.(1)

PARAMETER		Test Conditions	MIN	MAX	UNIT
t_{rCL1}	Rise time of SCLH after a repeated start condition and after an acknowledge bit		20	160	ns
t_{rDA}	Rise time of SDAH		20	160	ns
t_{fCL}	Fall time of SCLH		20	80	ns
t_{fDA}	Fall time of SDAH		20	160	ns
t_{SP}	pulse width of spikes suppressed by the input filter		0	10	ns
High Speed mode (3.4 MHz) C_b = 100 pF (Max) Figure 2					
t_{rCL}	Rise time of SCLH		10	40	ns
t_{rCL1}	Rise time of SCLH after a repeated start condition and after an acknowledge bit		10	80	ns
t_{rDA}	Rise time of SDAH		10	80	ns
t_{fCL}	Fall time of SCLH		10	40	ns
t_{fDA}	Fall time of SDAH		10	80	ns
t_{SP}	pulse width of spikes suppressed by the input filter		0	10	ns

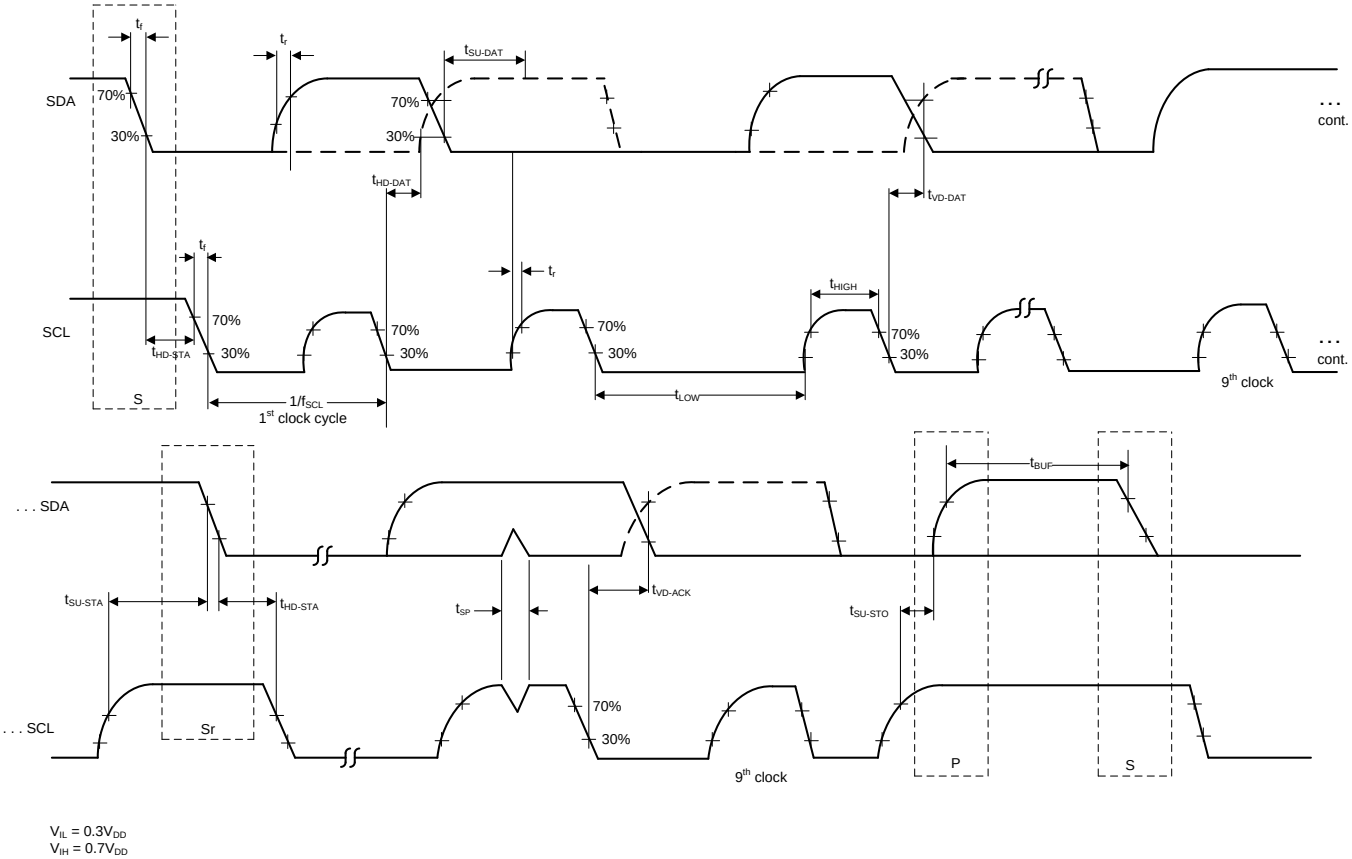
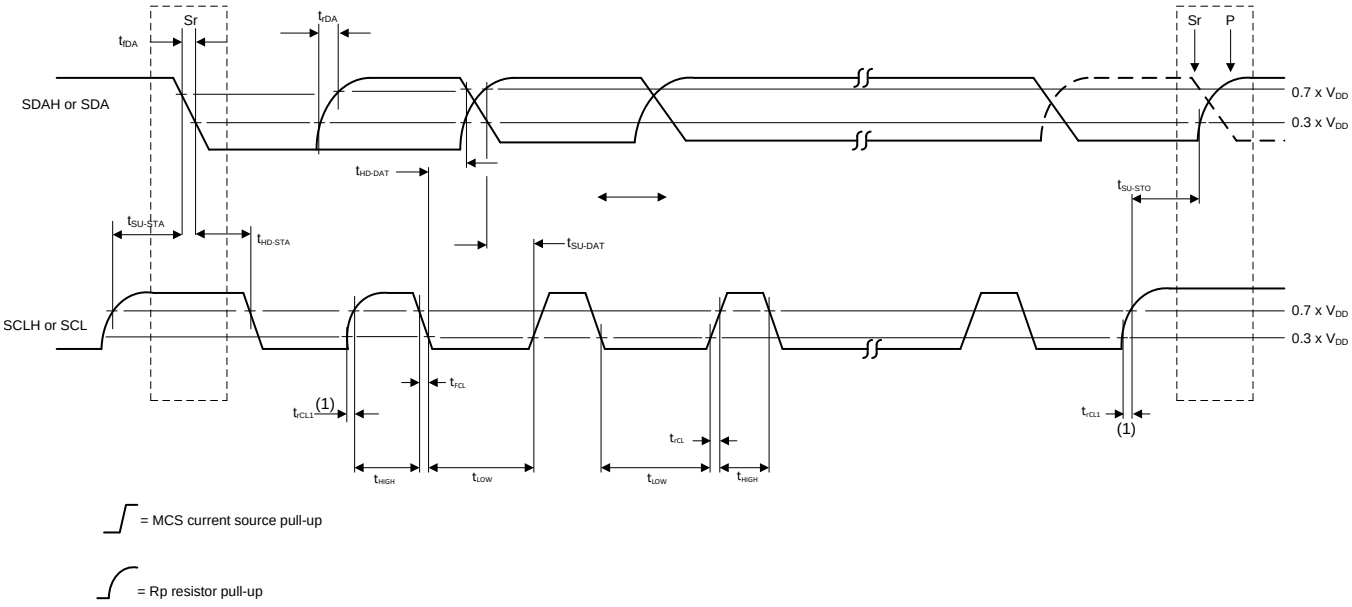


Figure 1. Timing Diagram for Standard-mode, Fast-mode and Fast-mode Plus



(1) First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 2. Timing Diagram for High Speed Mode

6.11 Typical Characteristics for All Modes

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.

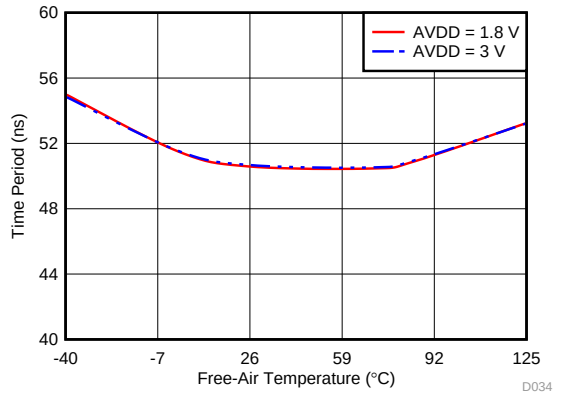


Figure 3. High Speed Oscillator Time Period with Temperature

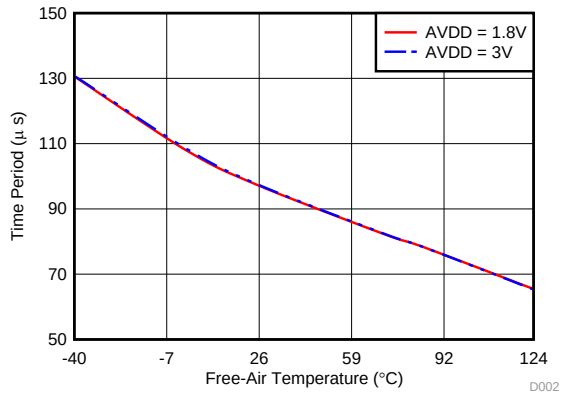
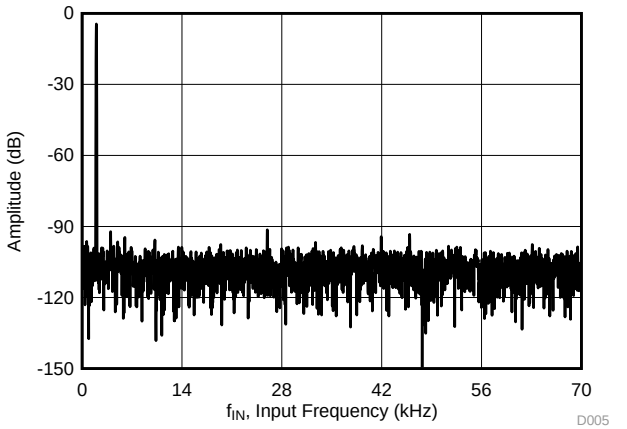


Figure 4. Low Power Oscillator Time Period with Temperature

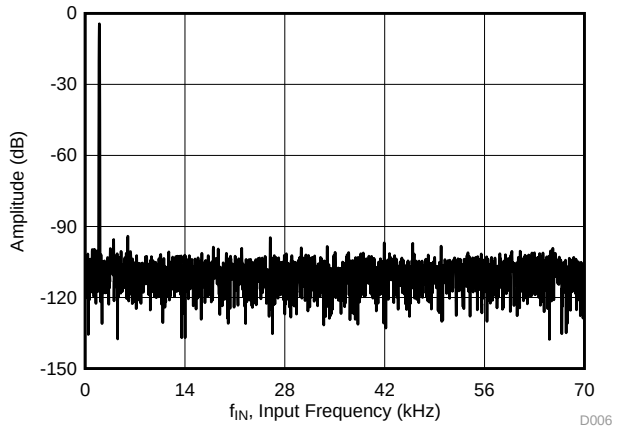
6.12 Typical Characteristics for Manual Mode

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.



SNR = 69.6 dB | THD = -82.9 dB | ENOB = 11.2
f_{sample} = 140 kSPS | SFDR = 87.2 dB | AVDD = 1.8 V

Figure 5. Typical FFT in Manual Mode

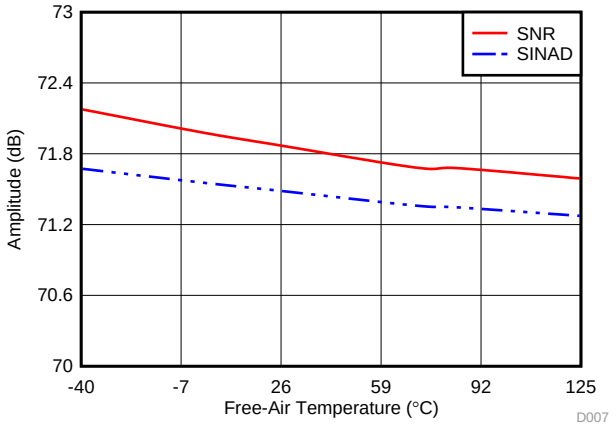


SNR = 71.7 dB | THD = -85 dB | ENOB = 11.5
f_{sample} = 140 kSPS | SFDR = 89.2 dB | AVDD = 3 V

Figure 6. Typical FFT in Manual Mode

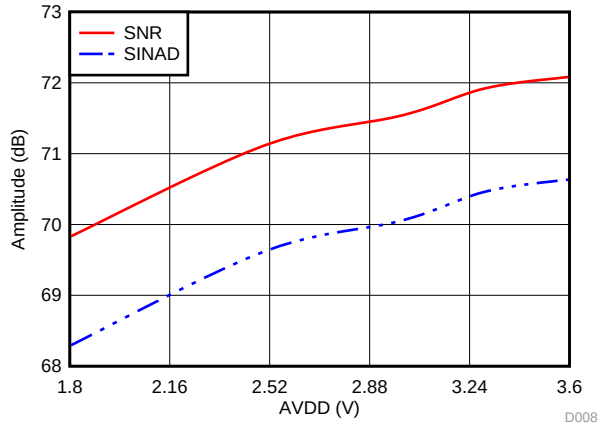
Typical Characteristics for Manual Mode (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.



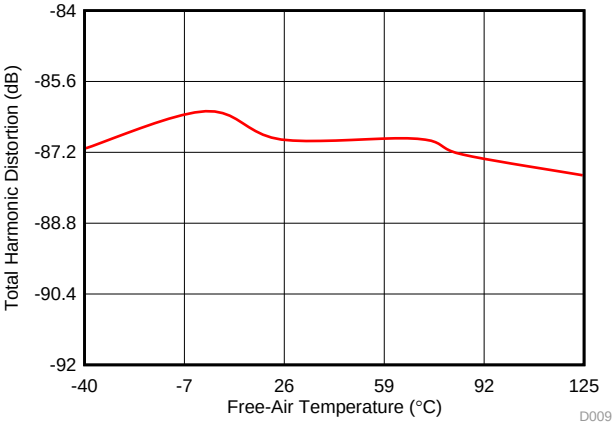
f_{sample} = 140 kSPS

Figure 7. SNR and SINAD in Manual Mode with Temperature



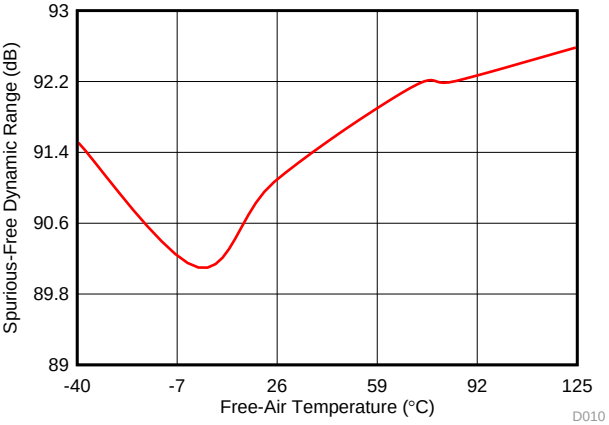
f_{sample} = 140 kSPS

Figure 8. SNR and SINAD in Manual Mode with AVDD



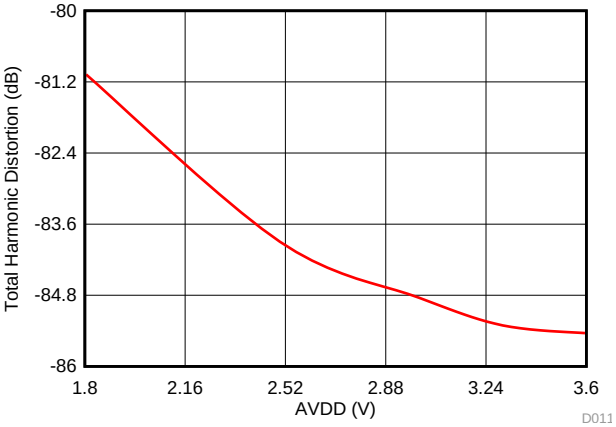
f_{sample} = 140 kSPS

Figure 9. THD in Manual Mode with Temperature



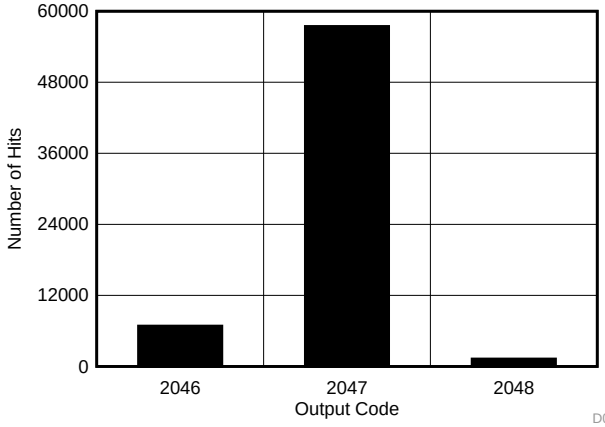
f_{sample} = 140 kSPS

Figure 10. SFDR in Manual Mode with Temperature



f_{sample} = 140 kSPS S

Figure 11. THD in Manual Mode with AVDD



Mean code = 2046.9 Standard Deviation = 0.34

Figure 12. Typical DC Code Spread in Manual Mode

Typical Characteristics for Manual Mode (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.

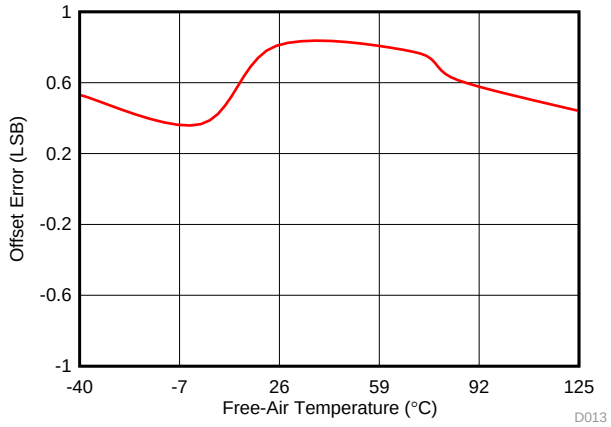


Figure 13. Offset Error in Manual Mode with Temperature

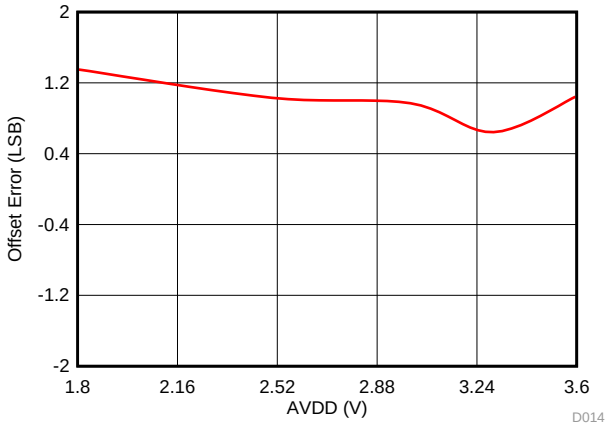


Figure 14. Offset Error in Manual Mode with AVDD

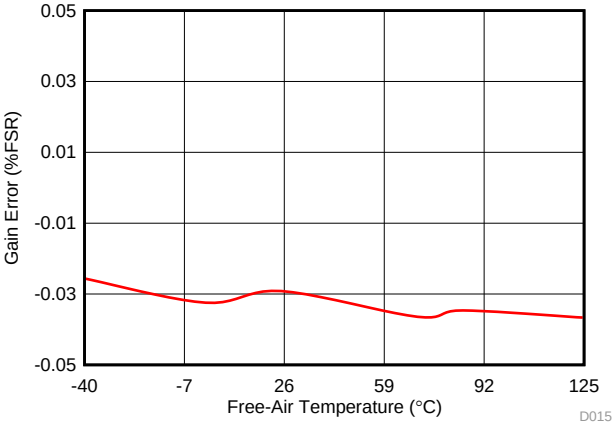


Figure 15. Gain Error in Manual Mode with Free-Air Temperature

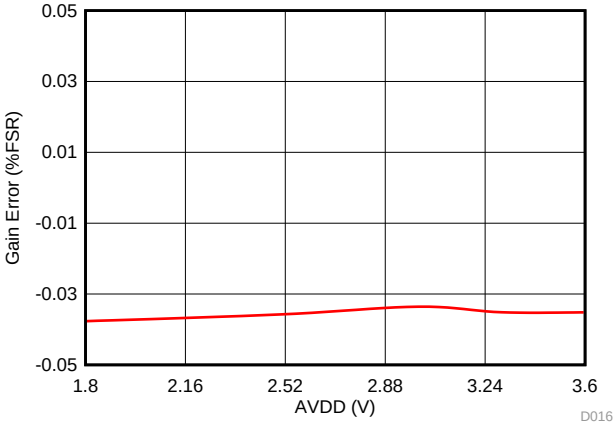


Figure 16. Gain Error in Manual Mode with AVDD

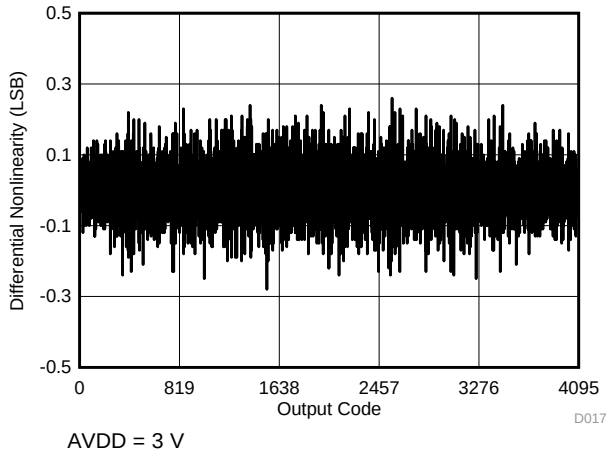


Figure 17. Typical DNL in Manual Mode

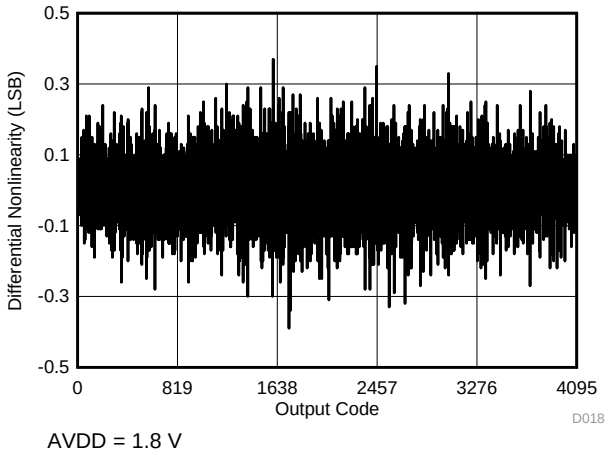
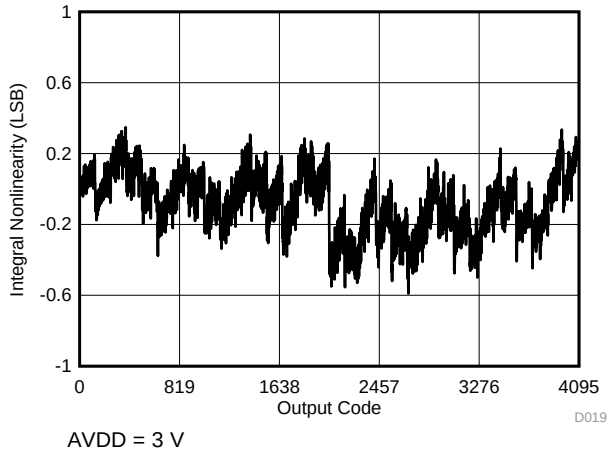


Figure 18. Typical DNL in Manual Mode

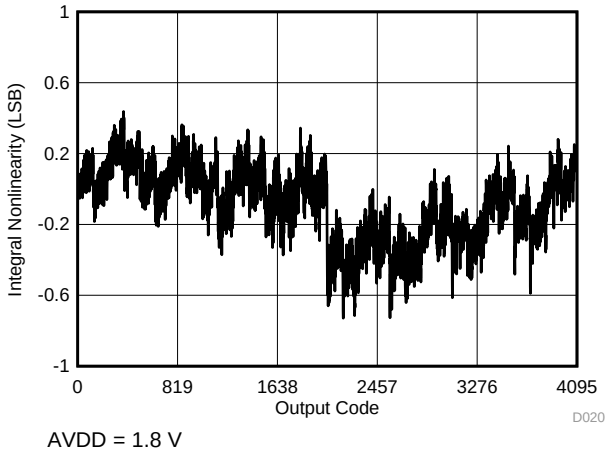
Typical Characteristics for Manual Mode (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.



AVDD = 3 V

Figure 19. Typical INL in Manual Mode



AVDD = 1.8 V

Figure 20. Typical INL in Manual Mode

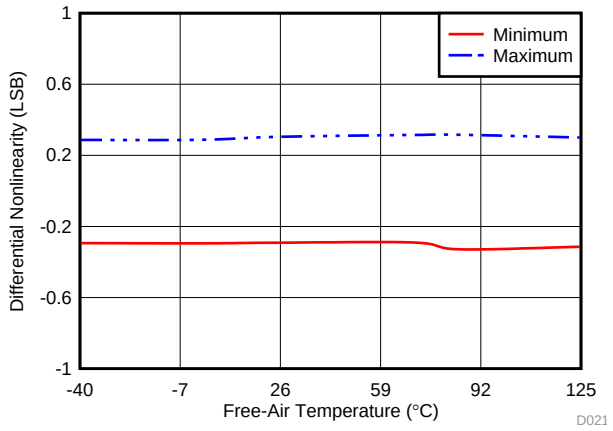


Figure 21. DNL in Manual Mode with Temperature

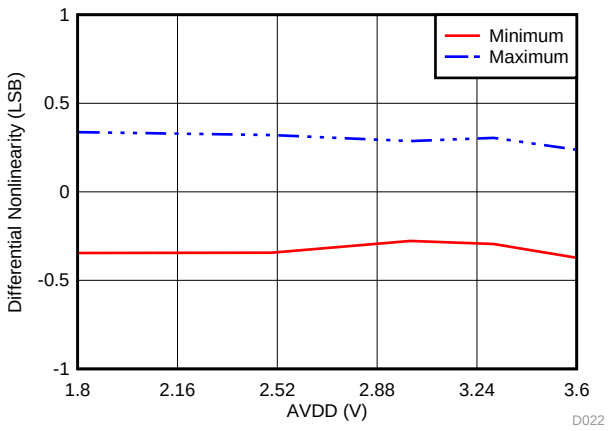


Figure 22. DNL in Manual Mode with AVDD

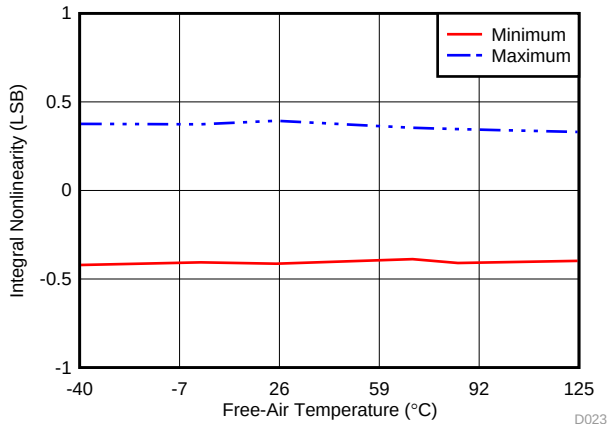


Figure 23. INL in Manual Mode with Temperature

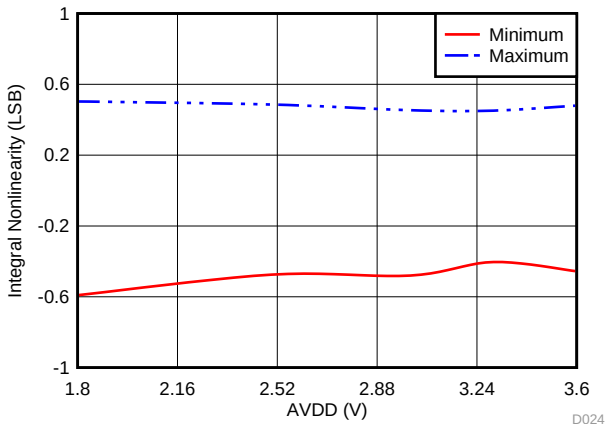
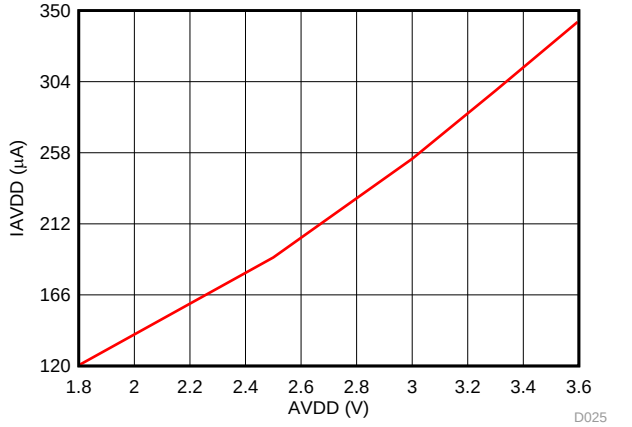


Figure 24. INL in Manual Mode with AVDD

Typical Characteristics for Manual Mode (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.



f_{Sample} = 140 kSPS SCL = 3.4 MHz

Figure 25. I_{AVDD} in Manual Mode with AVDD

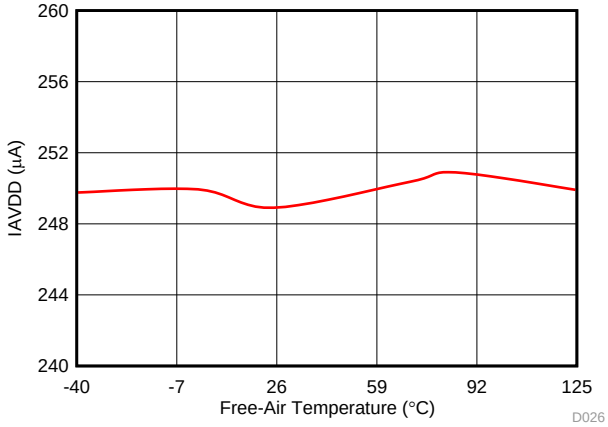
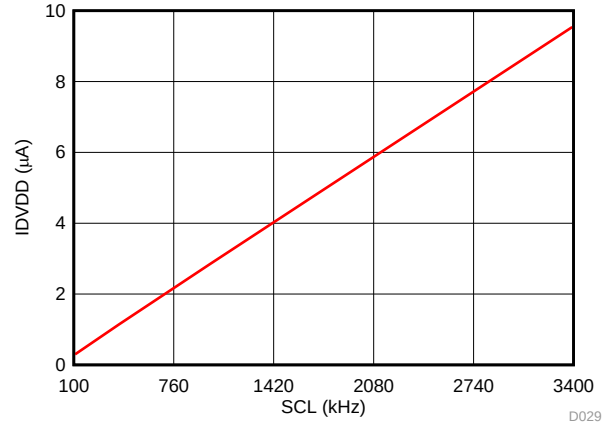
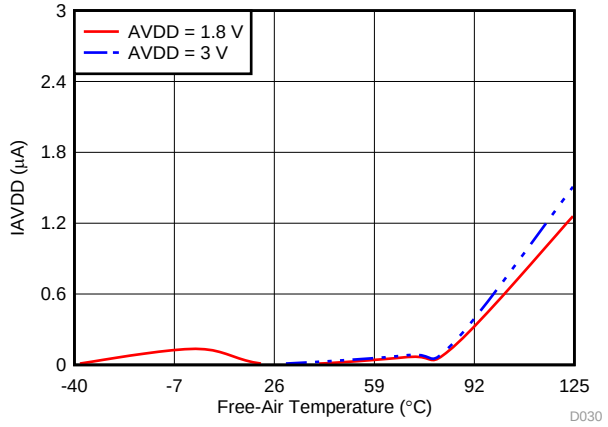


Figure 26. I_{AVDD} in Manual Mode with Temperature



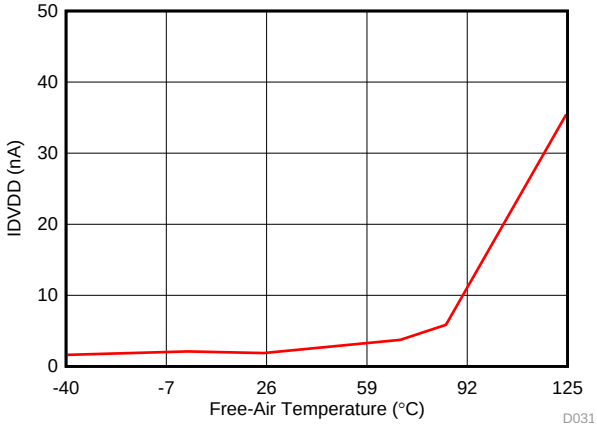
DVDD = 1.8 V

Figure 27. I_{DVDD} in Manual Mode with SCL



No Activity on SCL and SDA

Figure 28. Static I_{AVDD} in Manual Mode with Temperature

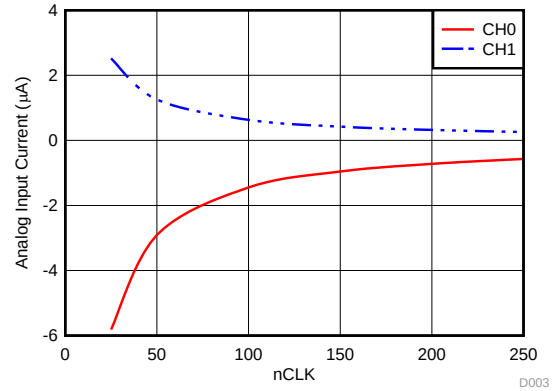


No Activity on SCL and SDA

Figure 29. Static I_{DVDD} in Manual Mode with Temperature

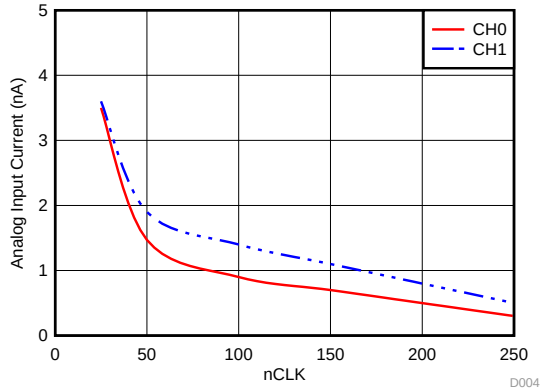
6.13 Typical Characteristics for Autonomous Modes

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.



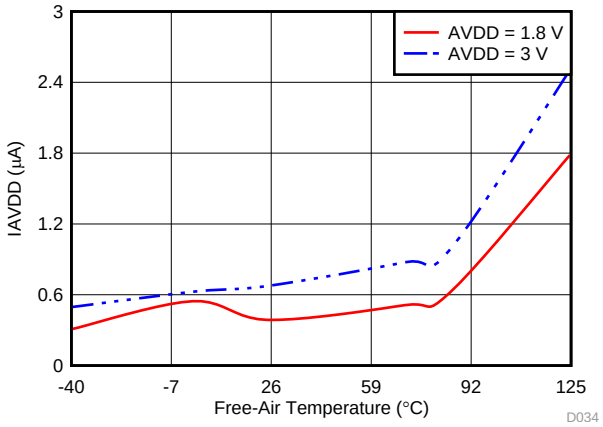
Input Voltage = 1.5 V
Stop Burst Mode
With High Speed Oscillator

Figure 30. Analog Input Current in Autonomous modes with nCLK



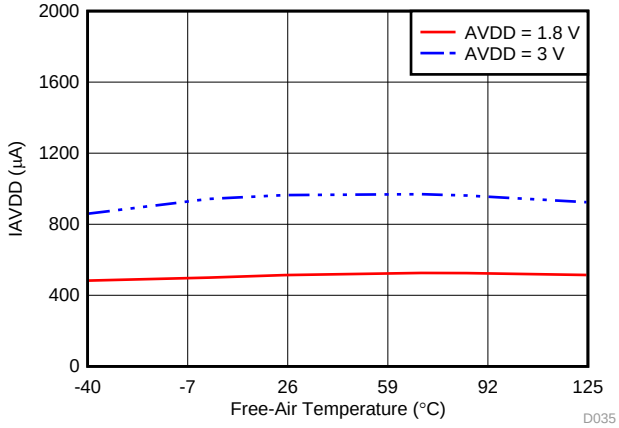
Input Voltage = 1.5 V
Stop Burst Mode
With Low Power Oscillator

Figure 31. Analog Input Current in Autonomous modes with nCLK



Stop Burst Mode
nCLK = 25
With Low Power Oscillator

Figure 32. I_{AVDD} in Autonomous Modes with Temperature



Stop Burst Mode
nCLK = 25
With High Speed Oscillator

Figure 33. I_{AVDD} in Autonomous Modes with Temperature

6.14 Typical Characteristics for High Precision Mode

At T_A = 25°C, AVDD = 3 V, DVDD = 3.3 V, and Two-Channel, Single-Ended Configuration, unless otherwise noted.

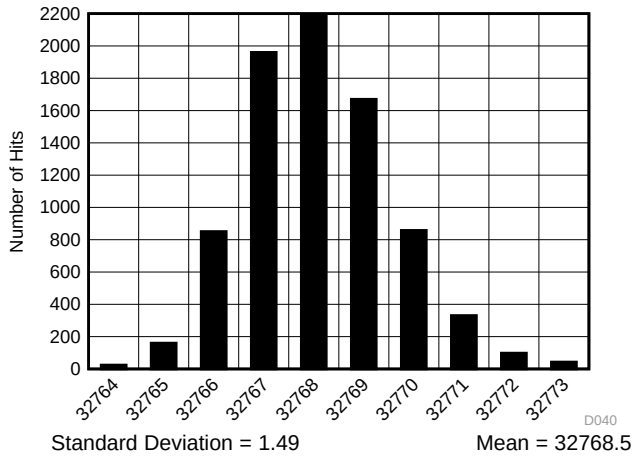


Figure 34. Typical DC Code Spread in High Precision Mode

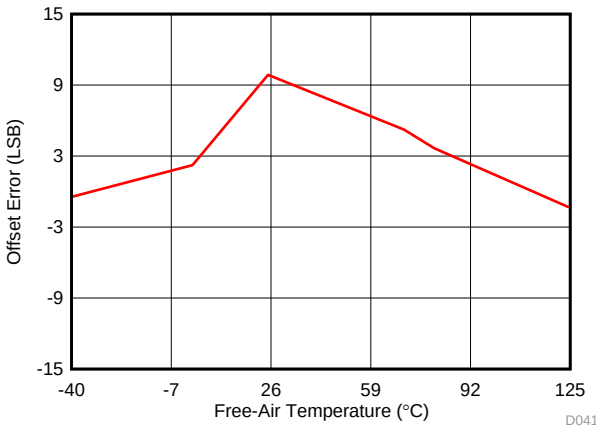


Figure 35. Offset Error in High Precision Mode with Temperature

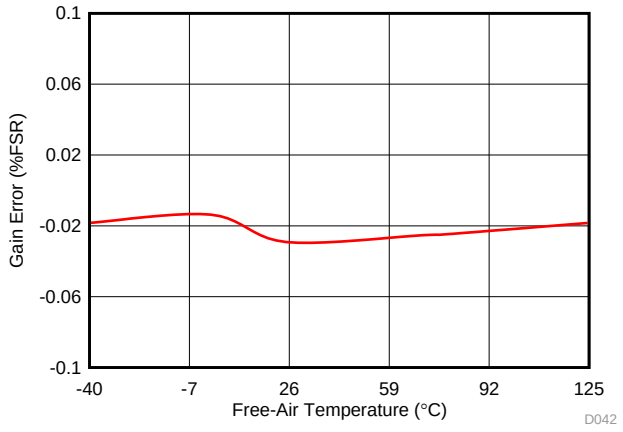


Figure 36. Gain Error in High Precision Mode with Temperature

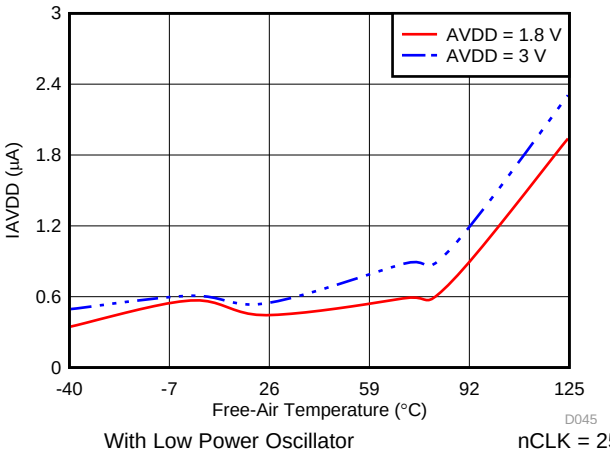


Figure 37. I_{AVDD} in High Precision Mode with Temperature

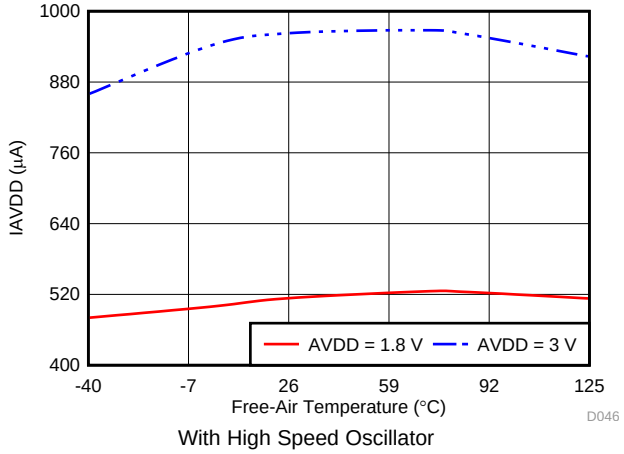


Figure 38. I_{AVDD} in High Precision Mode with Temperature

7 Detailed Description

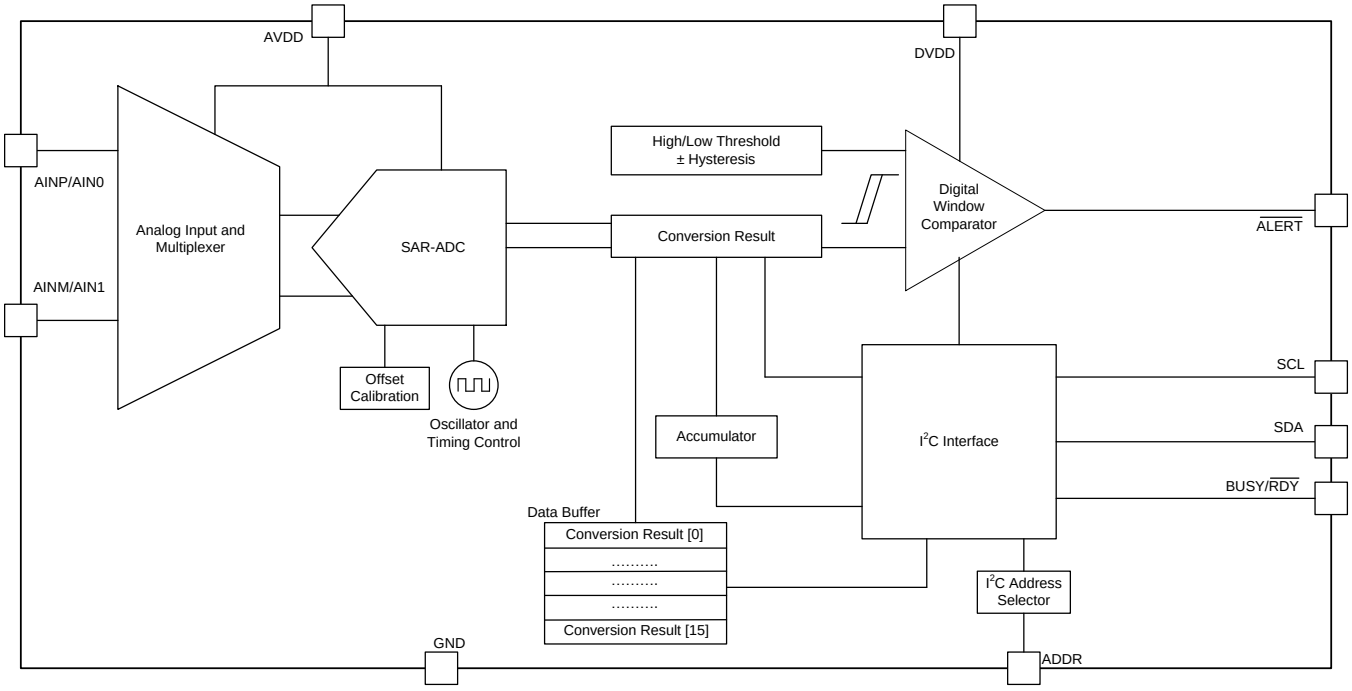
7.1 Overview

The ADS7142 is a nanopower, dual-channel, programmable sensor monitor with an integrated analog-to-digital converter (ADC), input multiplexer, digital comparator, data buffer, accumulator and internal oscillator. The *input multiplexer* can be either configured as two single-ended channels, one single-ended channel with remote ground sensing or one pseudo-differential channel where input can swing around AVDD/2. The device includes a *Digital Window Comparator* with a dedicated output pin, which can be used to alert the host when a programmed high or low threshold is crossed. The device address is configured by *I²C Address Selector* block. The device uses *internal oscillators* (High Speed or Low Power) for conversion. The start of conversion is controlled by the host in *Manual Mode* and by the device in *Autonomous Modes*.

The device also features a *Data Buffer* and an *Accumulator*. The data buffer can store up to 16 conversion results of the ADC in *Autonomous Modes* and the accumulator can accumulate up to 16 conversion results of ADC in *High Precision Mode*.

The device includes *OFFSET Calibration* for calibration of its own offset.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input and Multiplexer

Figure 39 shows a small-signal equivalent circuit for the analog input pins. The device includes a two-channel analog multiplexer with each input pin having ESD protection diodes to AVDD and GND. The sampling switches are represented by ideal switches SW_1 and SW_2 in series with resistors R_{s1} and R_{s2} (typically 150 Ω). The sampling capacitors, C_{s1} and C_{s2}, are typically 15 pF. The multiplexer configuration is set by the *CHANNEL_INPUT_CFG* register.

During acquisition, switches SW_1 and SW_2 are closed to allow the input signal to charge the internal sampling capacitors.

During conversion, switches SW_1 and SW_2 are opened to disconnect the input signal from the sampling capacitors.

The analog input of the device are optimized to be driven by high impedance source (up-to 100 kΩ) in *Autonomous Modes* or in *High Precision Mode* mode with low power oscillator. It is recommended to drive the analog input of the device with an external amplifier when in *Autonomous Modes* or in *High Precision Mode* mode with High Speed oscillator. Figure 30 and Figure 31 provide the analog input current for CH0 and CH1 of the device.

Figure 40, Figure 41 and Figure 42 provide a simplified circuit for analog input for input configurations described in *Two-Channel, Single-Ended Configuration*, *Single-Channel, Single-Ended Configuration* and *Single-Channel, Pseudo-Differential Configuration* respectively. The analog multiplexer supports following input configurations (set by writing into *CHANNEL_INPUT_CFG* register).

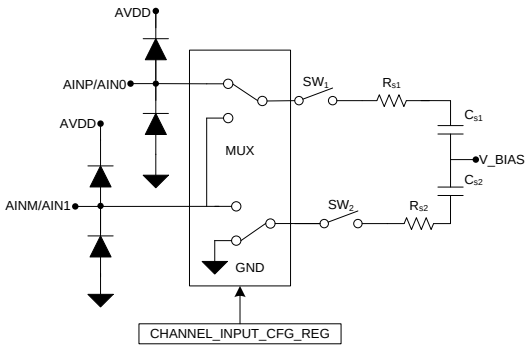


Figure 39. Equivalent Circuit for Analog Input

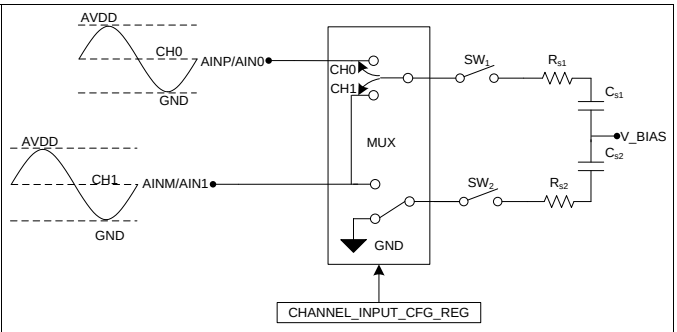


Figure 40. Two-Channel, Single-Ended Configuration

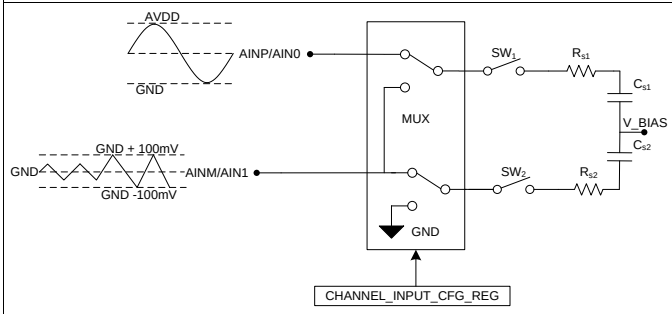


Figure 41. Single-Channel, Single-Ended Configuration with Remote Ground Sensing

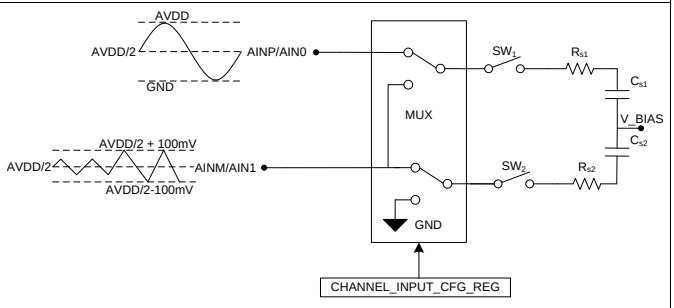


Figure 42. Single-Channel, Pseudo-Differential Configuration

7.3.1.1 Two-Channel, Single-Ended Configuration

Refer to Figure 40 for a simplified block diagram showing a two-channel, single ended configuration. Set CH0_CH1_IP_CFG bits = 00b or 11b to select this configuration. This is also the default configuration of the device after power up. In this configuration, C_{S2} always samples the GND pin and C_{S1} samples the input signal provided on Channel 0 (AINP/AIN0) or Channel 1 (AINM/AIN1) based on the channel selection. Each analog input channel can accept input signals in the range 0 V to AVDD V.

Feature Description (continued)

On power-up, the device wakes up in manual mode with Two-Channel, Single-Ended Configuration and samples CH0 only. This configuration can also be set by setting *OPMODE_SEL* to 000b or 001b,

The device can be configured to sample either CH0 or CH1 or both channels by setting bits in *AUTO_SEQ_CHEN* register to select the channels.

- To select a channel in AUTO sequence, set AUTO_SEQ_CHx bit in *AUTO_SEQ_CHEN* register to 1.
- Set bits in *OPMODE_SEL* register to 100b or 101b for Manual Mode with AUTO sequence.
- Set bits in *OPMODE_SEL* register to 110b for *Autonomous Modes* with AUTO sequence.
- Set bits in *OPMODE_SEL* register to 111b for *High Precision Mode* with AUTO sequence.

7.3.1.2 Single-Channel, Single-Ended Configuration

Refer to Figure 41 for a simplified block diagram showing a single-channel, single ended configuration. Set CH0_CH1_IP_CFG bits = 01b to select this configuration. In this configuration, C_{S1} samples the input signal provided on the AINP/AIN0 pin whereas C_{S2} samples input signal provided on the AINM/AIN1 pin. AINP/AIN0 pin can accept input signals in the range 0 V to AVDD V and AINM/AIN1 pin can accept input signals in the range –100 mV to +100 mV. This input configuration is useful in systems where the sensor and/or the signal conditioning block is placed far from the device and there could be a small difference between the ground potentials. In this channel configuration, remove channel 1 from AUTO sequence by setting the AUTO_SEQ_CH1 bit to 0. Selecting channel 1 in AUTO sequence leads to an error condition and the device sets an error flag in *SEQUENCE_STATUS* register.

7.3.1.3 Single-Channel, Pseudo-Differential Configuration

Refer to Figure 42 for a simplified block diagram showing a single-channel, pseudo-differential configuration. Set CH0_CH1_IP_CFG bits = 10b to select this configuration. In this configuration, C_{S1} samples the input signal provided on the AINP/AIN0 pin whereas C_{S2} samples input signal provided on the AINM/AIN1 pin. AINP/AIN0 pin can accept input signals in the range 0 V to AVDD V and AINM/AIN1 pin can accept input signals in the range (AVDD/2) - 100 mV to (AVDD/2) + 100 mV. This input configuration is useful to interface with sensors that provide pseudo-differential signal with negative output as AVDD/2 like an electrochemical gas sensor. In this channel configuration, remove channel 1 from AUTO sequence by setting the AUTO_SEQ_CH1 bit to 0. Selecting channel 1 in AUTO sequence leads to an error condition and the device sets an error flag in *SEQUENCE_STATUS* register.

7.3.2 OFFSET Calibration

The offset can be calibrated by setting the TRIG_OFFCAL bit in *OFFSET_CAL* register. During offset calibration, the sampling switches are open (Figure 39) and the device keeps BUSY/$\overline{\text{RDY}}$ pin high. The device calculates its offset error and corrects for this error for subsequent conversions. The device calibrates the offset on power up. To nullify the change in offset due to change in temperature or in AVDD voltage, it is recommended to perform this calibration periodically.

7.3.3 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. It is recommended to place a 220-nF, low-ESR ceramic decoupling capacitor between the AVDD pin and the GND pin, close to the AVDD Pin. Refer to *Power-Supply Recommendations* section.

7.3.4 ADC Transfer Function

The ADC provides data in straight binary format. The ADC resolution can be computed by Equation 1:

$$1\ \text{LSB} = V_{REF} / 2^{N} \quad (1)$$

where:

- V_{REF} = AVDD
- N = 12 for Autonomous Monitoring Modes and Manual Mode

Figure 43 and Figure 44 show the ideal transfer characteristics for Single-Ended Input and Pseudo-Differential Input, respectively. Table 1 show the digital output codes for the transfer functions.

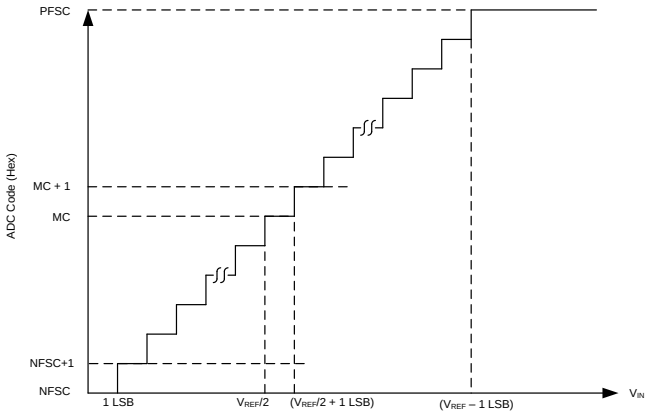


Figure 43. Ideal Transfer Characteristics for Single-Ended Configurations

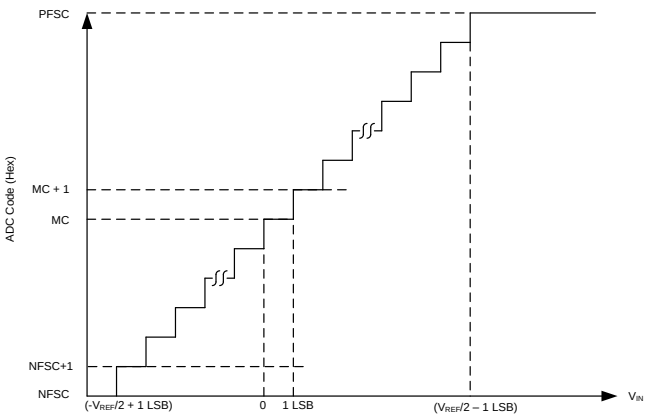


Figure 44. Ideal Transfer Characteristics for Pseudo-Differential Configuration

Table 1. Transfer Characteristics

INPUT VOLTAGE for SINGLE ENDED INPUT	INPUT VOLTAGE for PSEUDO DIFFERENTIAL INPUT	CODE	DESCRIPTION	IDEAL OUTPUT CODE
				Autonomous Monitoring Mode Or Manual Mode
≤1 LSB	≤(-V_{REF}/2 + 1) LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	(-V_{REF}/2 + 1) to (-V_{REF}/2 + 2) LSB	NFSC + 1	—	001
(V_{REF} / 2) to (V_{REF} / 2) + 1 LSB	0 to 1 LSB	MC	Mid code	800
(V_{REF} / 2) + 1 LSB to (V_{REF} / 2) + 2 LSBs	1 to 2 LSB	MC + 1	—	801
≥ V_{REF} – 1 LSB	≥ V_{REF}/2 – 1 LSB	PFSC	Positive full-scale code	FFF

7.3.5 Oscillator and Timing Control

The device uses one of the two internal oscillators (Low Power Oscillator or High Speed Oscillator) for converting the analog input voltage into a digital output code.

The steps for selecting the oscillator and setting the sampling speed are listed below:

1. Select the Low Power Oscillator (*OSC_SEL* = 1b) to monitor slow moving signals(< 300 Hz) at extremely low power consumption and sampling speeds (< 600 SPS). Select the High Speed Oscillator (*OSC_SEL* = 0b) to scan the sensor signals with faster sampling speed (> 50 kHz).
2. Set sampling speed by programming the *nCLK* register:

$$f_S = \frac{Oscillator\ frequency}{nCLK} \quad (2)$$

- f_s = Sampling Speed
- Oscillator Frequency = 1/t_{HSO} or 1/t_{LPO} depending on the OSC_SEL bit, refer the *Specifications* for 1/t_{HSO} or 1/t_{LPO}.
- nCLK is number of clocks in one conversion cycle (*nCLK* register)

7.3.6 I²C Address Selector

The I²C address for the device is determined by connecting external resistors on ADDR pin. The device address are selected on power-up based on the resistor values. The device retains this address until the next power up, or until next device reset, or until the device receives a command to program its own address (*General Call with Write Software programmable part of slave address*). Figure 45 provides the connection diagram for the ADDR pin and Table 2 provides the resistor values for selecting different addresses of the device.

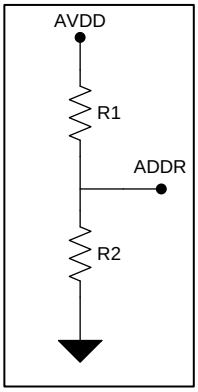


Figure 45. External Resistor Connection Diagram for ADDR Pin

Table 2. I²C Address Selection

Resistors		Address
R1 (1)	R2 (1)	
0 Ω	DNP (2)	0011111b (1Fh)
11 kΩ	DNP (2)	0011110b (1Eh)
33 kΩ	DNP (2)	0011101b (1Dh)
100 kΩ	DNP (2)	0011100b (1Ch)
DNP (2)	0Ω or DNP (2)	0011000b (18h)
DNP (2)	11 kΩ	0011001b (19h)
DNP (2)	33 kΩ	0011010b (1Ah)
DNP (2)	100 kΩ	0011011b (1Bh)

(1) Tolerance for R1,R2 < ±5%
(2) DNP = Do not populate

7.3.7 Data Buffer

When operating in Autonomous Monitoring Mode, the device can use the internal data buffer for data storage. The internal data buffer is 16-bit wide and 16-word deep and follows the FIFO (first-in, first-out) approach.

7.3.7.1 Filling of the Data Buffer

The write operation to the data buffer starts and stops as per the settings in the *DATA_BUFFER_OPMODE* register. The *DATA_BUFFER_STATUS* register provides the number of entries filled in the data buffer and this register can be read during an active sequence to get the current status of the data buffer. The time between two consecutive conversions is set by the *nCLK* register and Equation 3 provides the relationship for time between two consecutive conversions of the same channel and nCLK parameter.

$$t_{cc} = k \times nCLK \times OscillatorTimePeriod \quad (3)$$

where

- t_{cc} is time between two consecutive conversions of same channel, $t_{cc} = k \times t_{cycle}$.
- k is number of channels enabled in the device sequence.
- nCLK is number of clocks used by device for one conversion cycle.
- Oscillator Timer Period is t_{LPO} or t_{HSO} depending on OSC_SEL value . Refer to the *Specifications* for t_{LPO} or t_{HSO} .

The format of the 16-bit contents of each entry in the data buffer are set by programming the *DATA_OUT_CFG* register. The DATA_OUT_CFG register enables the Channel ID and DATA_VALID flag in data buffer. Channel ID represents the channel number for the data entry in the data buffer. DATA_VALID is set to zero in either of the following conditions:

- If the entry in the data buffer is not filled after the last start of sequence.
- If the I^2C master tries to read more than 16 entries from the data buffer, device provides zeros with DATA_VALID set to zero.

At the end of the write operation, the data buffer always has results of 16 (or lesser) consecutive conversions. The data buffer is filled in the order that the data is converted by the ADC. The channels converted by the ADC are controlled by the *AUTO_SEQ_CHEN* register. The entries that are not filled during an active sequence are filled with zeros.

7.3.7.2 Reading data from the Data Buffer

The device brings the BUSY/$\overline{\text{RDY}}$ pin low after completion of the sequence or after the *SEQ_ABORT* bit is set. As illustrated in Figure 46, the device provides the contents of the data buffer (in FIFO fashion) on receiving I^2C read frame, which consists of the device address and the read bit set to 1.

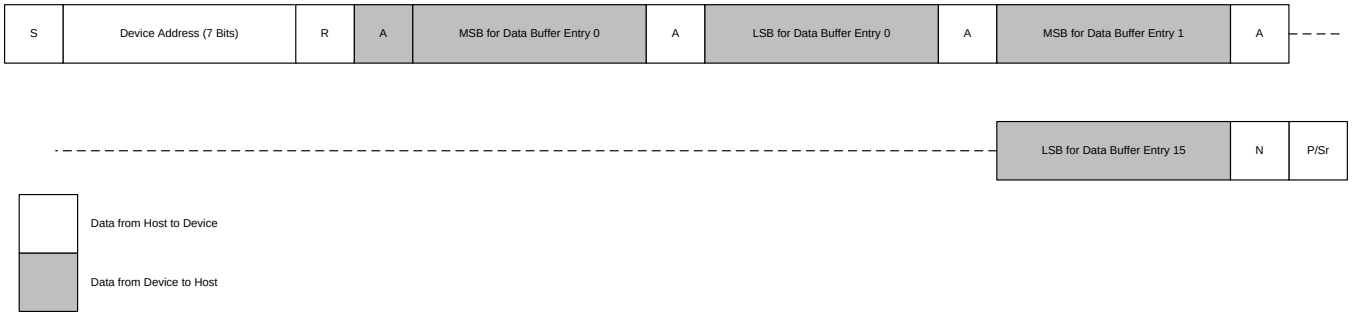


Figure 46. Reading Data Buffer (16 Bit Words × 16 Words)

The device returns zeroes with DATA VALID flag set to zero for all I^2C read frames received after all the valid data words from the data buffer are read or when a I^2C read frame is issued during an active sequence (indicated by high on the BUSY/$\overline{\text{RDY}}$ pin). The I^2C master needs to provide a NACK followed by a STOP or RESTART condition in an I^2C frame to finish the reading process. The data buffer is reset by setting the *SEQ_START* bit or after resetting the device.

7.3.8 Accumulator

When operating in *High Precision Mode*, the device offers a 16-bit internal accumulator per channel. The Accumulator for a channel is enabled only if that channel is selected in the channel scanning sequence. The accumulator adds sixteen 12-bit conversion results. The result of adding 16 twelve bit words is one 16 bit word that has an effective resolution of an 16-bit ADC. The time between two consecutive conversions for accumulation is controlled by the *nCLK* register and Equation 3 provides the relationship for time between two consecutive conversions of same channel and nCLK parameter.

The accumulated data can be read from the *ACCUMULATOR_DATA* registers in the device. *ACCUMULATOR_STATUS* register provides the number of accumulations done in the accumulator since last conversion. This register can be read during an active sequence to get the current status of the accumulator. The accumulator is reset on setting the *SEQ_START* bit and on resetting the device. Equation 4 provides the relationship between high precision data and ADC conversion results.

$$\text{High Precision Data for CHx} = \sum_{k=1}^{16} \text{Conversion Result[k] for CHx} \tag{4}$$

Equation 5 provides the value of LSB in high precision mode for the accumulated result.

$$1\ LSB = \frac{AVDD}{2^{16}} \tag{5}$$

7.3.9 Digital Window Comparator

The internal Digital Window Comparator is available in all modes. In *Autonomous Modes* with Thresholds monitoring and Diagnostics, the digital window comparator controls the filling of the data and the output of the alert pin and in other modes, it only controls the output of the alert pin. Figure 47 provides the block diagram for digital window comparator.

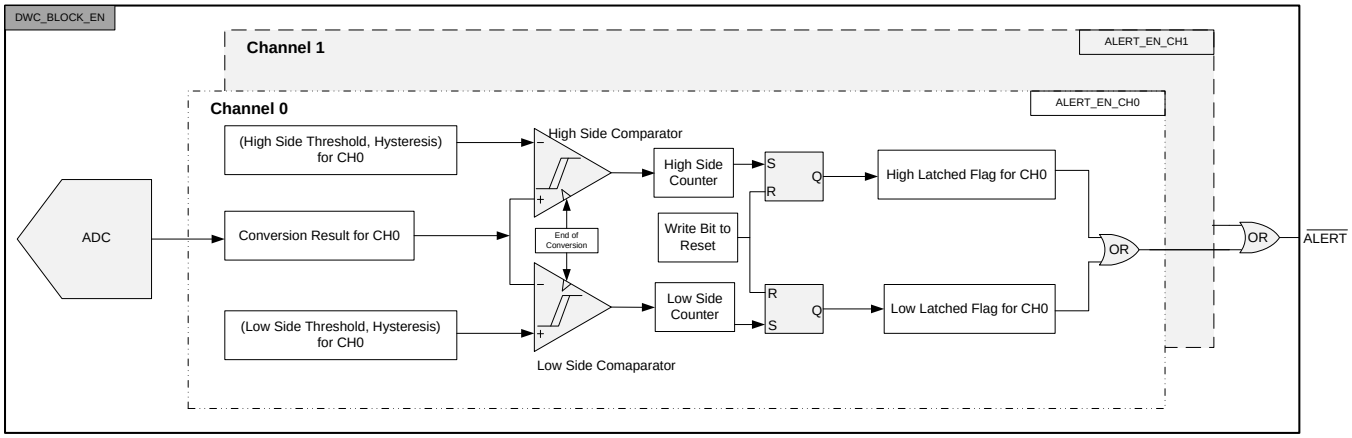


Figure 47. Digital Comparator Block Diagram

The Low Side Threshold, High Side Threshold, and Hysteresis parameters are independently programmable for each input channel. Figure 48 shows the comparison thresholds and hysteresis for the two comparators. A Pre-Alert event counter after each comparator counts the output of the comparator and sets the latched flags. The Pre-Alert Event Counter settings are common to the two channels.

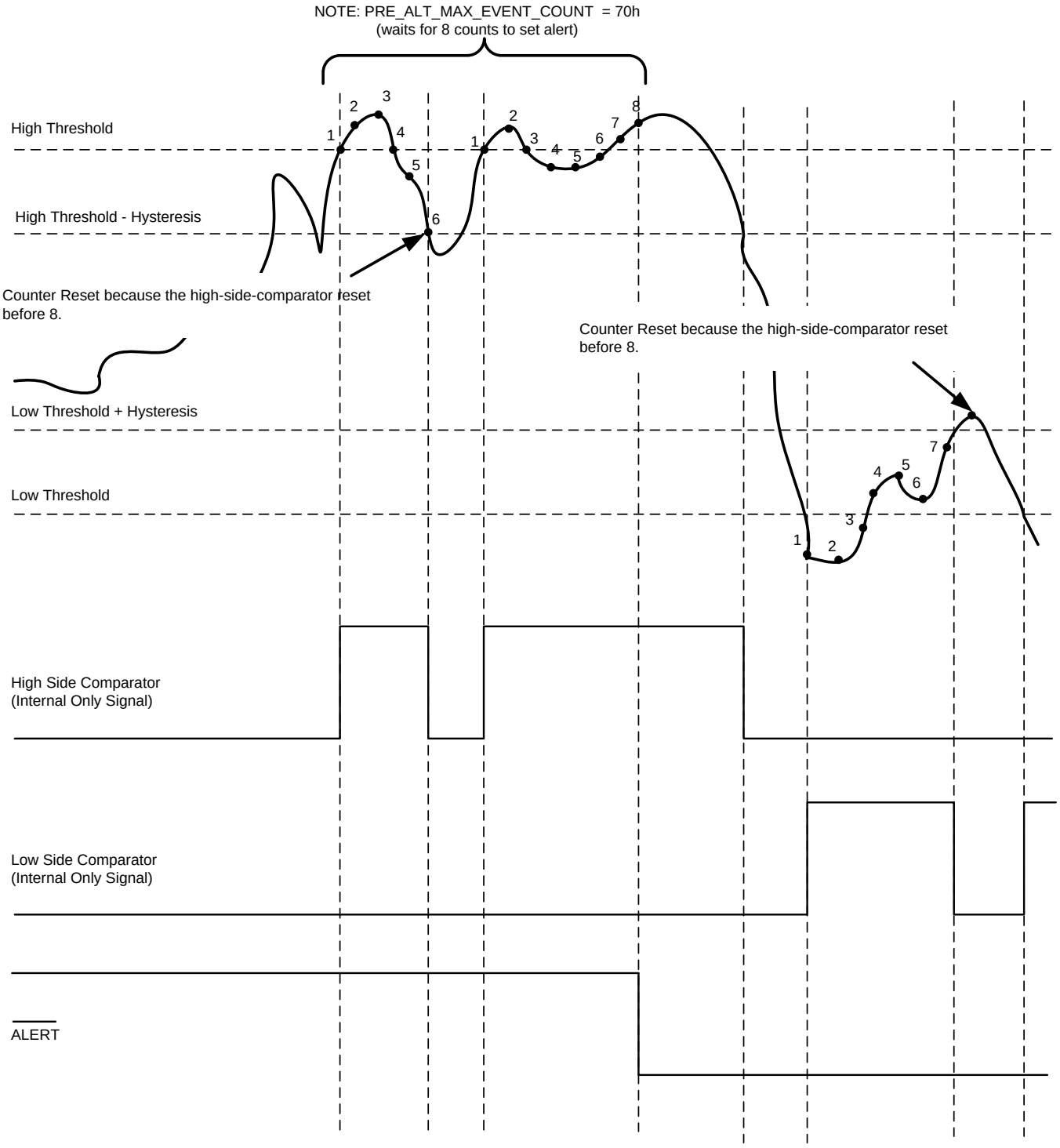


Figure 48. Thresholds, Hysteresis and Event Counter for Digital Window Comparator

DWC_BLOCK_EN bit in *ALERT_DWC_EN* register enables/disables the complete Digital Window Comparator block (disabled at power-up) and ALERT_EN_CHx bits in *ALERT_CHEN* register enables Digital Window Comparator for individual channels. Once enabled, whenever a new conversion result is available:

1. The output of the high side comparator transitions to logic high when the conversion result is greater than the High Threshold. This comparator resets when the conversion result is less than the High Threshold – Hysteresis.

2. The output of the low side comparator transitions to logic high when the conversion result is less than the Low Threshold. This comparator resets when the conversion result is greater than the Low Threshold + Hysteresis.
3. A different threshold and hysteresis can be used for each channel.
4. Once the output of either the high side or low side comparator transitions high the Pre-Alert Event Counter begins to increment for each subsequent conversion. This counter continues to increment until it reaches the value stored in the *PRE_ALT_MAX_EVENT_COUNT* register. Once it reaches PRE_ALT_MAX_EVENT_COUNT, the Alert becomes active and sets the latched flags. If the comparator output becomes zero before counter reaches PRE_ALT_MAX_EVENT_COUNT, then the event counter is reset to zero, Alert does not be set and lateched flag is not set.

Therefore, the latched flags (high and low) for the channel are updated only if the respective comparator output remains 1 for the specified number of consecutive conversions (set by the PRE_ALT_MAX_EVENT_COUNT).

The latched flags can be read from the *ALERT_LOW_FLAGS* and *ALERT_HIGH_FLAGS* registers. To clear a latched flag, write 1 to the applicable bit location. The $\overline{\text{ALERT}}$ pin status is re-evaluated whenever an applicable latched flag gets set or is cleared.

The response time for $\overline{\text{ALERT}}$ pin can be estimated by Equation 6

$$t_{response} = [1 + k \times (PRE\_ALT\_MAX\_EVENT\_COUNT + 1)] \times nCLK \times Oscillator\ TimePeriod \quad (6)$$

where

- k is number of channels enabled in device sequence
- nCLK is number of clocks used by device for one conversion cycle.
- Oscillator Timer Period is t_{LPO} or t_{HSO} depending on OSC_SEL value . Refer to the *Specifications* for t_{LPO} or t_{HSO} .

7.3.10 I²C Protocol Features

7.3.10.1 General Call

On receiving a general call (00h), the device provides an ACK.

7.3.10.2 General Call with Software Reset

On receiving a general call (00h) followed with Software Reset (06h), the device resets itself.

7.3.10.3 General Call with Write Software programmable part of slave address

On receiving a general call (00h) followed by 04h, the device configures its own I²C address configured by the ADDR pin. During this operation, the device keeps BUSY/RDY Pin high and does not respond to other I²C commands except general call.

7.3.10.4 Configuring Device into High Speed I²C mode

The device can be configured in High Speed I²C mode by providing an I²C frame with one of the HS-mode master codes (08h to 0Fh).

After receiving one of the HS-mode master codes, the device sets the HS_MODE bit in *OPMODE_I2CMODE_STATUS* register and remains in High Speed I²C mode until a STOP condition is received in an I²C frame.

7.3.10.5 Bus Clear

If the SDA line is stuck LOW due to an incomplete I²C frame, providing nine clocks on SCL is recommended. The device releases the SDA line within these nine clocks, and then the next I²C frame can be started.

7.3.11 Device Programming

Table 3 provides the acronyms for different conditions in an I²C Frame.

Table 3. I²C Frame Acronyms

Symbol	Description
S	Start condition for I²C Frame
Sr	Re-start condition for I²C Frame
P	Stop condition for I²C Frame
A	ACK (Low)
N	NACK (High)
R	Read Bit (High)
W	Write Bit (Low)

Table 4. Opcodes for Commands

Opcode	Command Description
00010000b	Single Register Read
00001000b	Single Register Write
00011000b	Set Bit
00100000b	Clear Bit
00110000b	Reading a continuous block of registers
00101000b	Writing a continuous block of registers

7.3.11.1 Reading Registers

The I²C master can either read a single register or a continuous block registers from the device as described in *Single Register Read* and in *Reading a Continuous Block of Registers*.

7.3.11.1.1 Single Register Read

To read a single register from the device, the I²C master has to first provide an I²C command with three frames (of 8-bits each) to set the address as illustrated in Figure 49. The register address is the address of the register which must be read. The opcode for register read command is listed in Table 4.

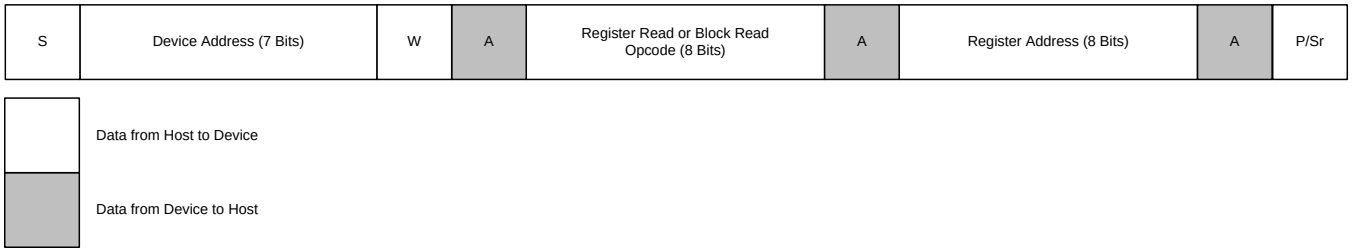


Figure 49. Setting Register Address for Reading Registers

After this, the I²C master has to provide another I²C frame containing the device address and read bit as illustrated in Figure 50. After this frame, the device provides register data. If the host provides more clocks, the device provides same register data. To end the register read command, the master has to provide a STOP or a RESTART condition in the I²C frame.

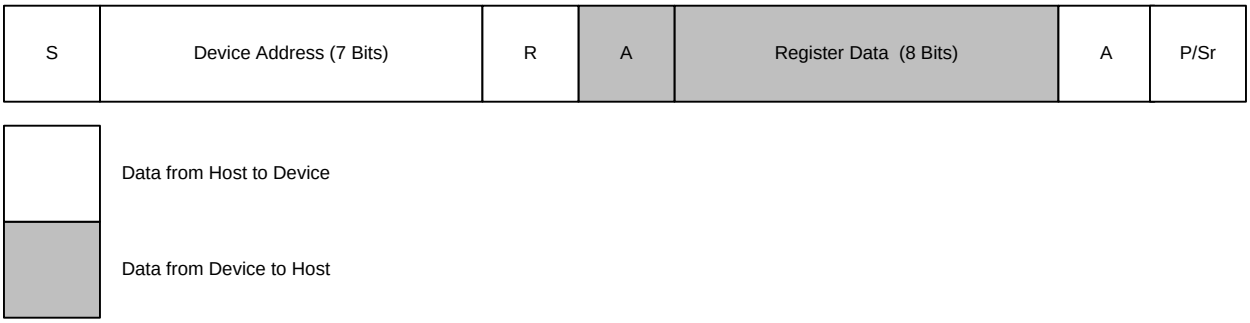


Figure 50. Reading Register Data

7.3.11.1.2 Reading a Continuous Block of Registers

To read a continuous block of registers, the I²C master has to first provide an I²C command to set the address as illustrated in Figure 49. The register address is the address of the first register in the block which must be read. The opcode for reading a continuous block of register is listed in Table 4.

Next, the I²C master has to provide another I²C frame containing the device address and read bit as illustrated in Figure 51. After this frame, the device provides register data. On providing more clocks, the device provides data for next register. On reading data from addresses which does not exist in the *Register Map* of the device, the device returns zeros. If the device does not have any further registers to provide the data, it provides zeros. To end the register read command, the master has to provide a STOP or a RESTART condition in the I²C frame.

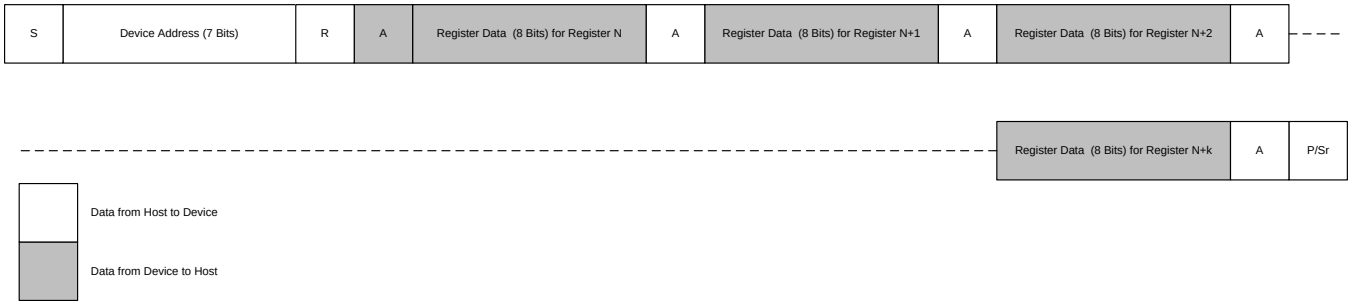


Figure 51. Reading a Continuous Block of Registers

7.3.11.2 Writing Registers

The I²C master can either write a single register or a continuous block registers to the device. It can also set a few bits in a register or clear a few bits in a register.

7.3.11.2.1 Single Register Write

To write to a single register in the device, the I²C master has to provide an I²C command with four frames as illustrated in Figure 52. The register address is the address of the register which must be written and register data is the value that must be written. The opcode for single register write is listed in Table 4. To end the register write command, the master has to provide a STOP or a RESTART condition in the I²C frame.

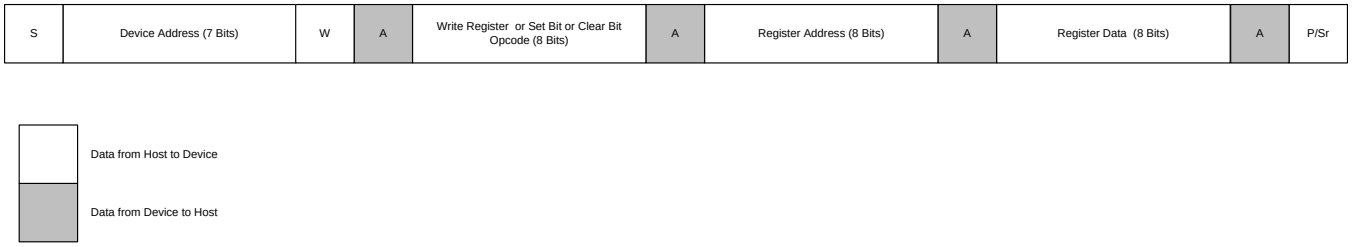


Figure 52. Writing a Single Register

7.3.11.2.2 Set Bit

To set bits in a register without changing the other bits, the I^2C master has to provide an I^2C command with four frames as illustrated in Figure 52. The register address is the address of the register in which the bits needs to be set and register data is the value representing the bits which need to be set. Bits with value as 1 in register data are set and bits with value as 0 in register data are not changed. The opcode for set bit is listed in Table 4. To end this command, the master has to provide a STOP or RESTART condition in the I^2C frame.

7.3.11.2.3 Clear Bit

To clear bits in a register without changing the other bits, the I^2C master has to provide an I^2C command with four frames as illustrated in Figure 52. The register address is the address of the register in which the bits needs to be cleared and register data is the value representing the bits which need to be cleared. Bits with value as 1 in register data are cleared and bits with value as 0 in register data are not changed. The opcode for clear bit is listed in Table 4. To end this command, the master has to provide a STOP or a RESTART condition in the I^2C frame.

7.3.11.2.4 Writing a continuous block of registers

To write to a continuous block of registers, the I^2C master has to provide an I^2C command as illustrated in Figure 53. The register address is the address of the first register in the block which needs to be written. The I^2C master has to provide data for registers in subsequent I^2C frames in an ascending order of register addresses. Writing data to addresses which do not exist in the *Register Map* of the device has no effect. The opcode for writing a continuous block of registers is listed in Table 4. If the data provided by the I^2C master exceeds the address space of the device, the device neglects the data beyond the address space. To end the register write command, the master has to provide a STOP or a RESTART condition in the I^2C frame.

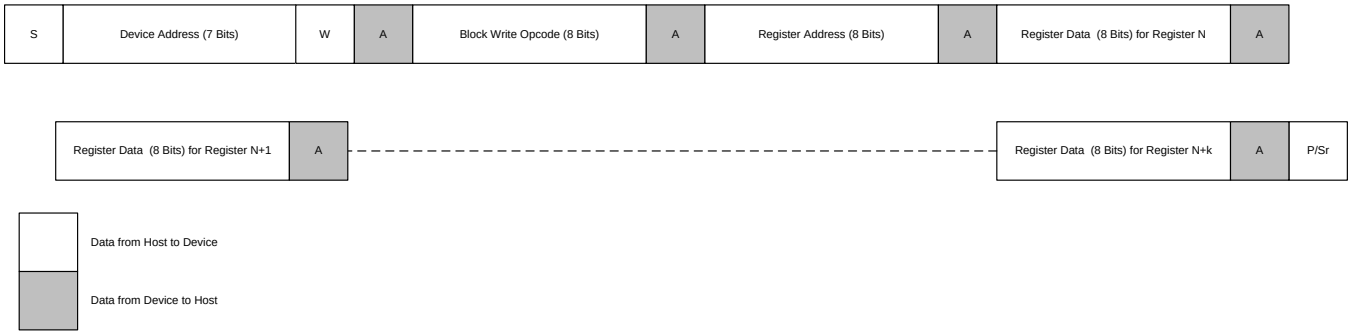


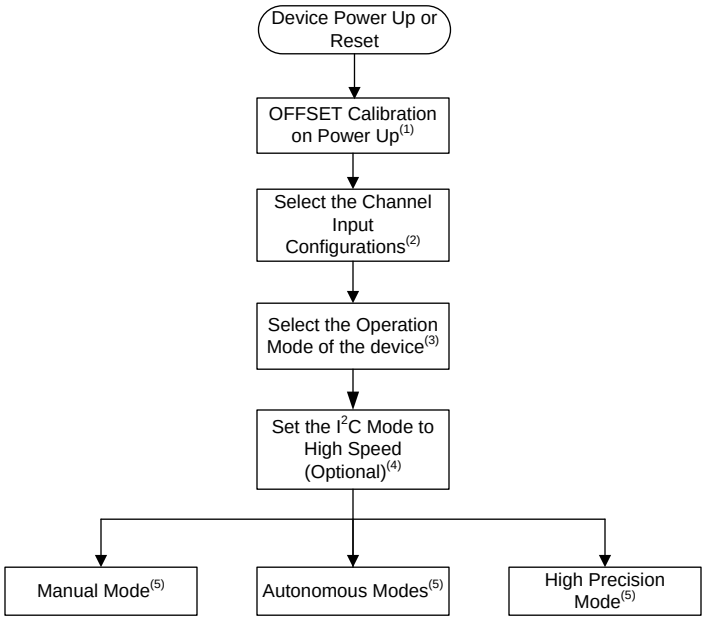
Figure 53. Writing a continuous block of registers

7.4 Device Functional Modes

The device has below functional modes:

- Manual Mode
- Autonomous Modes
  - Autonomous Mode with Threshold Monitoring and Diagnostics.
  - Autonomous Mode with Burst Data
- High Precision Mode

Device powers up in Manual Mode and can be configured into one of the other modes of these modes by writing the configuration registers for the desired mode. Steps for configuring device into different modes are illustrated in Figure 54



(1) Offset can also be calibrated anytime during normal operation by setting the bit in the OFFSET_CAL register.
(2) Configure the CHANNEL_INPUT_CFG register.
(3) Configure the OPMODE_SEL register for the desired operation mode.
(4) Refer to Configuring Device into High Speed I^2C mode section.
(5) Operating mode is selected by configuring the OPMODE_SEL register in step 3.
(6) For reading and writing registers, Refer to Device Programming section.

Figure 54. Configuring Device into different modes

7.4.1 Device Power Up and Reset

On power up, the device calibrates its own offset and calculates the address from the resistors connected on ADDR pin. During this time, the device keeps BUSY/$\overline{\text{RDY}}$ high.

The device can be reset by recycling power on AVDD pin, by General Call(00h) followed by software reset (06h), or by writing the *WKEY* register followed by setting the bit in *DEVICE_RESET* register.

Recycling power on the AVDD pin and on General call(00h) followed by software reset (06h), all the device configurations are reset, and the device initiates offset calibration and re-evaluates its I^2C address.

When setting the bit in *DEVICE_RESET* register, all the device configurations except latched flags for the Digital Window Comparator and *WKEY* register are reset, The device does not initiate offset calibration and does not re-evaluate its I^2C address.

Device Functional Modes (continued)

7.4.2 Manual Mode

On power-up, the device is in Manual Mode using the single ended and dual channel configuration and starts by sampling the analog input applied on Channel 0. In this mode, the device uses the high frequency oscillator for conversions. Manual mode allows the external host processor to directly request and control when the data is sampled. The data capture is initiated by an I^2C command from the host processor and the data is then returned over the I^2C bus at a throughput rate of up to 140-kSPS. Applications that could take advantage of this type of functionality include traditional ADC applications that require 1 or 2 channels of continuous data output.

After setting the operation mode to Manual Mode as illustrated in Figure 54, steps for operating the device to be in Manual Mode and reading data are illustrated in Figure 55. The host can either configure the device to scan through one channel or both channels by configuring the *CHANNEL_INPUT_CFG* register and *AUTO_SEQ_CFG* register.

7.4.2.1 Manual Mode with CH0 Only

Set the *OPMODE_SEL* register to 000b or 001b for Manual Mode with CH0 only. The host has to provide device address and read bit to start the conversions. To continue with conversions and reading data to the host must provide continuous SCL (Figure 56). In this mode, a NACK followed by a STOP condition in I^2C frame is required to abort the operation. Then the device operation mode can be changed to another operation mode.

7.4.2.2 Manual Mode with AUTO Sequence

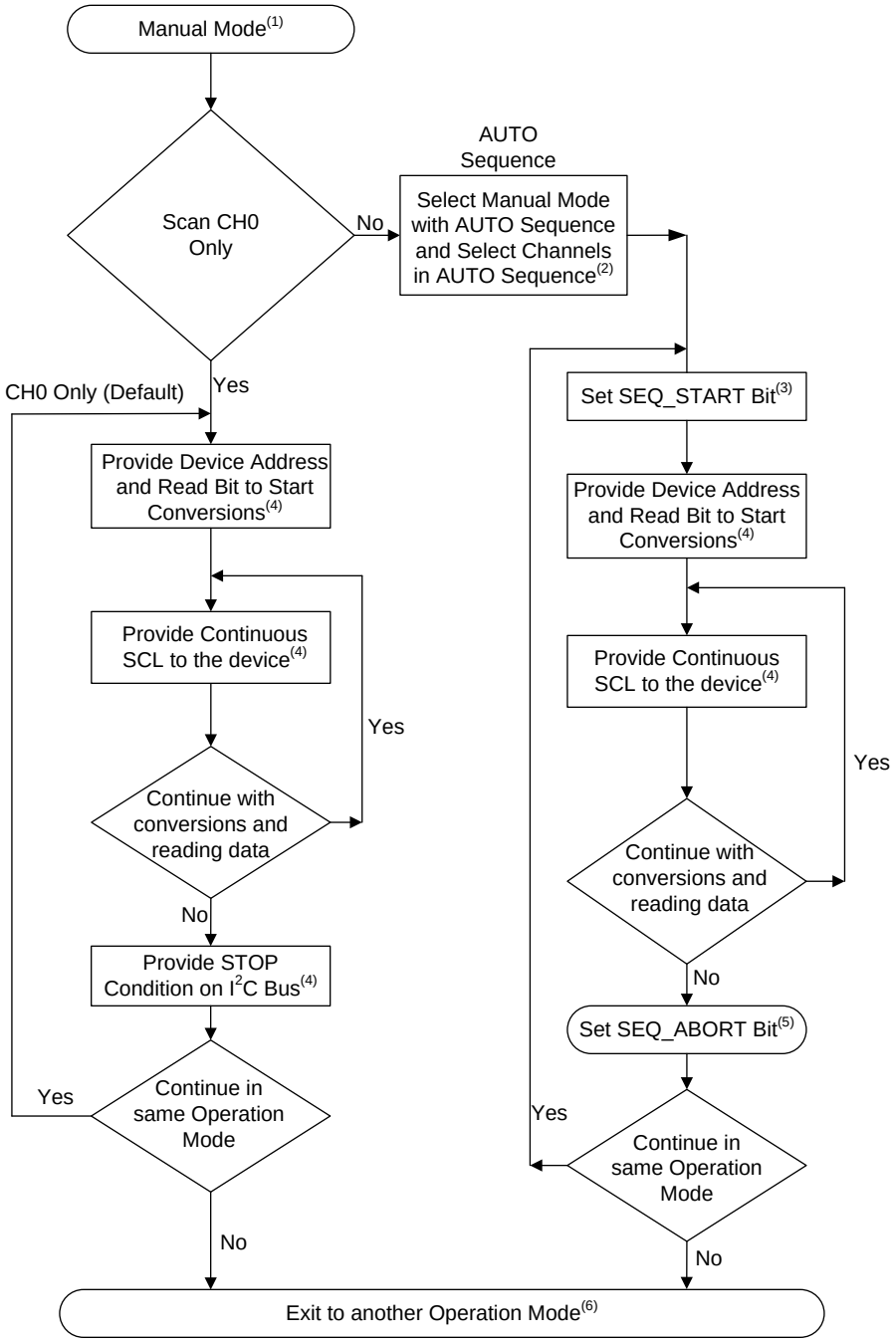
Set the *OPMODE_SEL* register to 100b or 101b for Manual Mode with AUTO Sequence. The host has to set the SEQ_START bit in *START_SEQUENCE* register and provide the device address and read bit to start the conversions. To continue with conversions and reading data, the host must provide continuous SCL (Figure 56). In this mode, the SEQ_ABORT bit in *ABORT_SEQUENCE* register must be set to abort the operation. Then the device operation mode can be changed to another operation mode. In this mode, a register read aborts the AUTO sequence.

In Manual Mode, the device always uses the High Speed Oscillator and the nCLK parameter has no effect. The maximum scan rate is given by Equation 7:

$$f_S = \frac{1000}{\left[18 \times T_{SCL} + k\right]} \quad (7)$$

- f_s = Maximum sampling Speed in kSPS
- T_{SCL}= Time period of SCL clock (in µsec)
- if $T_{SCL\text{-}LOW}$ (Low period of SCL) < 1.8.µsec, k = (1.8 - $T_{SCL\text{-}LOW}$) and Device stretches clock in Manual Mode. Not Applicable for Standard I^2C Mode (100 kHz).
- if $T_{SCL\text{-}LOW}$ (Low period of SCL) ≥ 1.8.µsec, k = 0 and Device does not stretch clock in Manual Mode.

Device Functional Modes (continued)



(1) For setting the operation mode to Manual mode, Refer to Figure 54

(2) Select Manual mode with AUTO sequence in OPMODE_SEL register. Select channels in AUTO_SEQ_CFG register.

(3) Set the bit SEQ_START bit in the START_SEQUENCE register.

(4) Refer to Figure 56 .

(5) Set the bit SEQ_ABORT bit in the ABORT_SEQUENCE register .

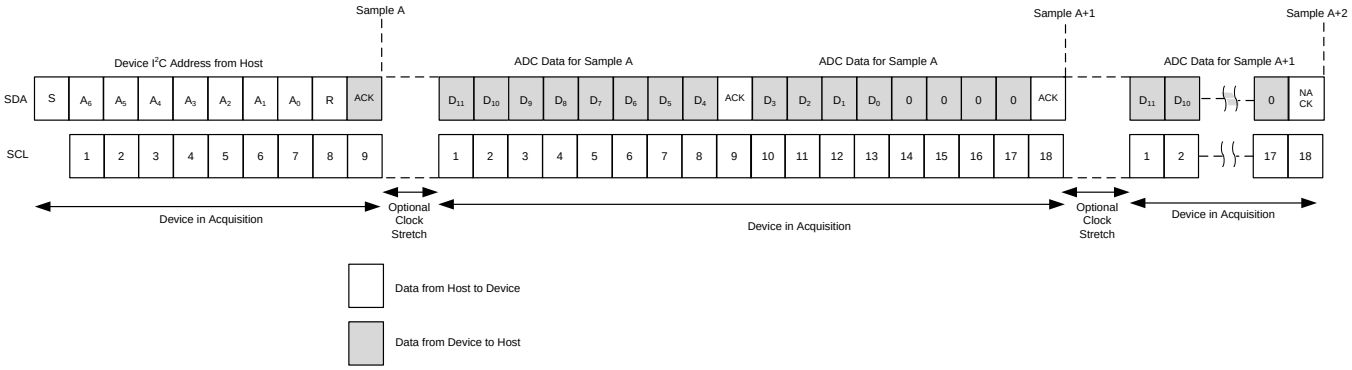
(6) Select another operation mode in the OPMODE_SEL register.

(7) For reading and writing registers, Refer to Device Programming section.

Figure 55. Device Operation in Manual Mode

Device Functional Modes (continued)

Data can be read from the device by providing a device address and read bit followed by continuous SCL as shown in Figure 56.



(1) Refer to Equation 7 for sampling speed in Manual Mode.

(2) If device scans both channels in AUTO sequence, first data (For Sample A) is from CH0 and second data(For Sample A +1) is from CH1.

Figure 56. Starting Conversion and Reading Data in Manual Mode

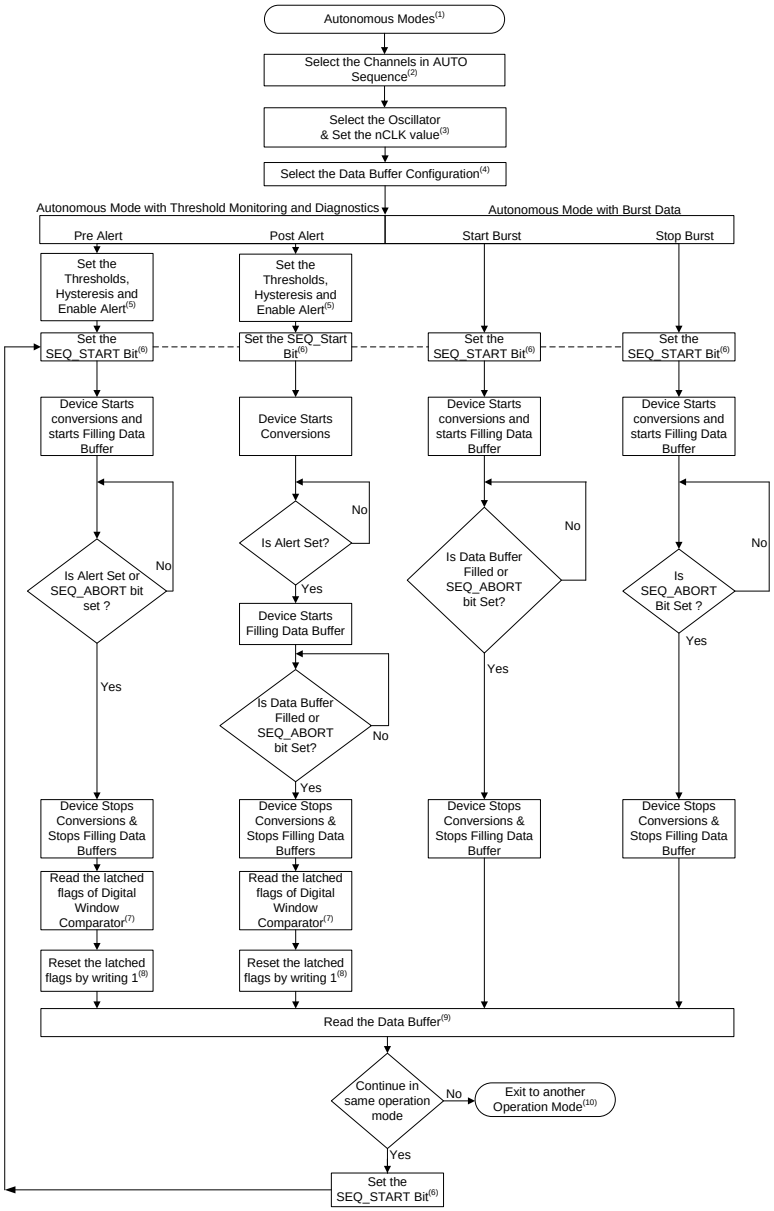
7.4.3 Autonomous Modes

In Autonomous Mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate a signal on the $\overline{\text{ALERT}}$ pin when the programmable high or low threshold values are crossed and store the conversion results in the data buffer before or after the crossing a threshold or before setting the *SEQ_ABORT* bit (Start Burst) or after setting the *START_SEQUENCE* bit.

In Autonomous mode, the device generates the start of conversion using the internal oscillator. The first start of conversion must be provided by the host and the device generates the subsequent start of conversions.

After configuring the operation mode to autonomous mode (Set *OPMODE_SEL* register to 110b) as illustrated in Figure 54, steps for operating the device to be in different autonomous modes are illustrated in Figure 57

Device Functional Modes (continued)



(1) For setting the operation mode to Autonomous modes, Refer to Figure 54

(2) Select channels in the AUTO_SEQ_CFG register.

(3) Select the oscillator by configuring the OSC_SEL register and configure the nCLK register.

(4) Select the data buffer mode in the DATA_BUFFER_OPMODE register.

(5) Configure the thresholds in the DWC_xTH_CHx_xxx registers and hysteresis in the DWC_HYS_CHx registers. Enable the alert for channels in the ALERT_CHEN register and set the DWC_BLOCK_EN bit in the ALERT_DWC_EN register.

(6) Set the bit SEQ_START bit in the START_SEQUENCE register.

(7) Read the ALERT_LOW_FLAGS and/or ALERT_HIGH_FLAGS registers.

(8) Reset the ALERT_LOW_FLAGS and/or ALERT_HIGH_FLAGS registers by writing 03h.

(9) Refer to Reading data from the Data Buffer section.

(10) Select another operation mode in the OPMODE_SEL register.

(11) For reading and writing registers, Refer to Device Programming section.

Figure 57. Configuring Device in Autonomous Modes

Device Functional Modes (continued)

TI recommends aborting the present sequence by setting the *SEQ_ABORT* bit before changing the device operation mode or device configuration.

7.4.3.1 Autonomous Mode with Threshold Monitoring and Diagnostics

The Threshold Monitoring Mode automatically scans the input voltage on the input channel(s) and generates a signal when the programmable high or low threshold values are crossed. This mode is useful for applications where the output of the sensor needs to be continuously monitored and action only taken when the sensor output deviates outside of an acceptable range. Applications that could take advantage of this type of functionality include wireless sensor nodes, environmental sensors, smoke and heat detectors, motion detectors, and so on.

In this mode, the data buffer can be configured to store the conversion results of the ADC in two different ways.

7.4.3.1.1 Autonomous Mode with Pre Alert Data

In this mode, the device stores the sixteen conversion prior to the activation of the Alert. Upon activation of Alert, conversion stops. For this mode, Set *DATA_BUFFER_OPMODE* to 100b. In this mode, the device starts converting and stores the data on setting the bit in the *SEQ_START* register and continues to store the data into the data buffer until one of the digital comparator flags is set for crossing a high threshold or a low threshold for the channels selected in the sequence. If the *SEQ_ABORT* bit is set before the data buffer is filled, the device aborts the sequence and stops storing the conversion results. If more than 16 conversions occur between start of sequence and alert output, the first entries written into the data buffer are over-written.

Figure 58 and Figure 59 illustrates the filling of data buffer in autonomous mode with Pre alert Data.

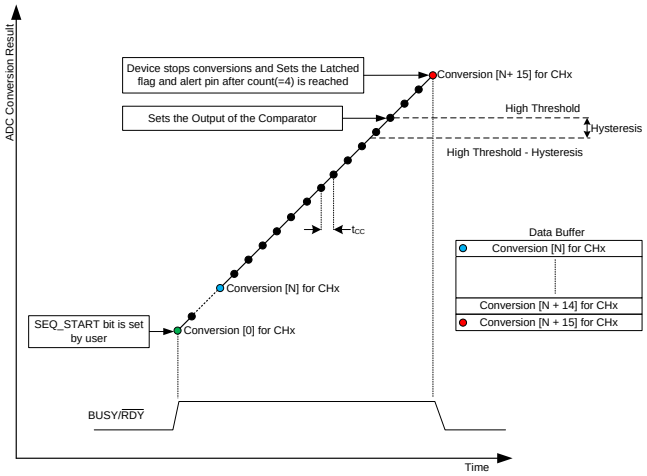


Figure 58. Pre Alert Data for Single Channel Configurations

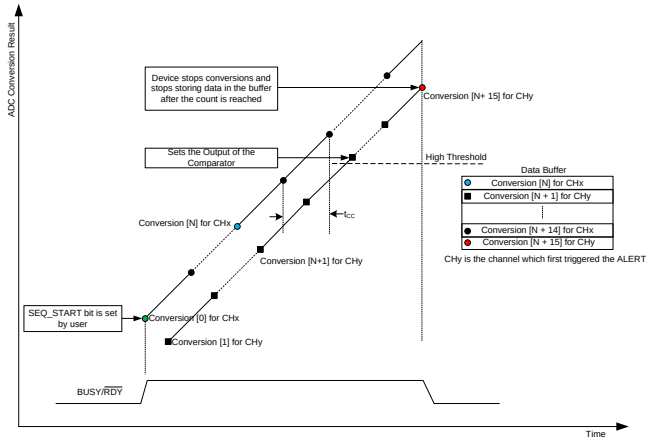


Figure 59. Pre Alert Data for Dual Channel Configuration

7.4.3.1.2 Autonomous Mode with Post Alert Data

In this mode, the device captures the next sixteen conversion results after the Alert is active. Once these sixteen conversions are stored in the data buffer, all conversion stops. For this mode, Set *DATA_BUFFER_OPMODE* to 110b. In this mode, the device starts converting the data on setting the *SEQ_START* bit and stores the data in the data buffer when one of the digital comparator flags is set after the crossing a high threshold or a low threshold for the channels selected in the sequence. if the *SEQ_ABORT* bit is set before the data buffer is filled, the device aborts the sequence and stops storing the conversion results.

Figure 60 and Figure 61 illustrates the filling of the data buffer in autonomous mode with Post Alert Data.

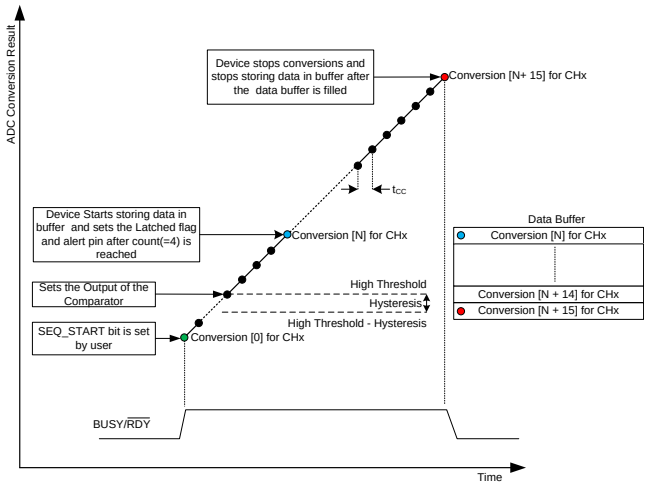


Figure 60. Post Alert Data for Single Channel Configurations

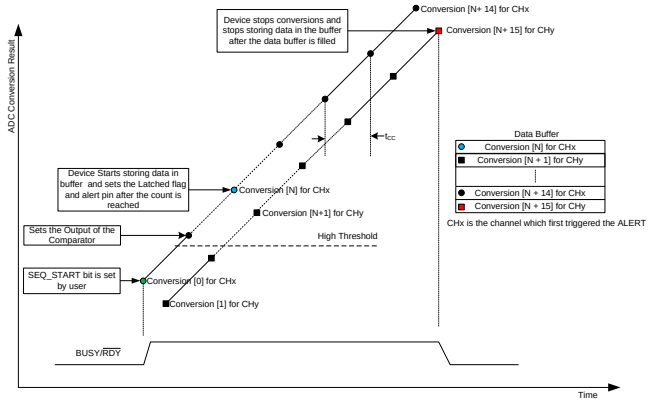


Figure 61. Post Alert Data for Dual Channel Configuration

7.4.3.2 Autonomous Mode with Burst Data

In this mode, the device can be configured to store up-to 16 conversion results in the data buffer based on user command. Applications that could take advantage of this mode are remote data loggers, environmental sensing and patient monitors. In this mode, the user can either start the burst or stop the burst of data as described in the following sections:

7.4.3.2.1 Autonomous Mode with Start Burst

For this mode, set *DATA_BUFFER_OPMODE* to 001b. With Start Burst, the user can configure the device to start the filling of data buffer with conversion results by setting the *SEQ_START* bit and the device stops converting data and filling the data buffer after the data buffer is filled.

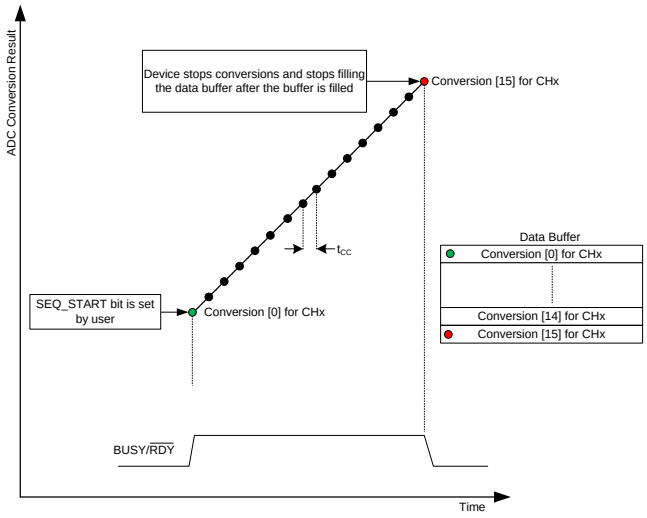


Figure 62. Start Burst with Single Channel Configurations

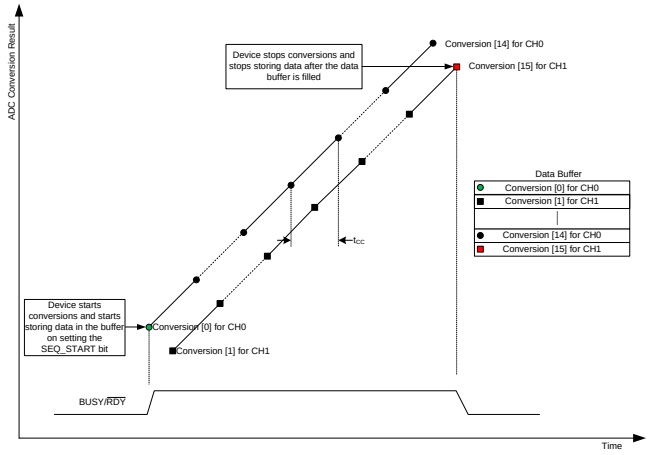


Figure 63. Start Burst with Dual Channel Configuration

7.4.3.2.2 Autonomous Mode with Stop Burst

For this mode, Set *DATA_BUFFER_OPMODE* to 000b. With Stop Burst, the user can configure the device to stop filling the data buffer with conversion results by setting the *SEQ_ABORT* bit. If more than 16 conversions occur between start of sequence and abort of sequence, the entries first written into the data buffer are over-written. Figure 64 and Figure 65 illustrate the filling of the data buffer in autonomous mode with Stop Burst.

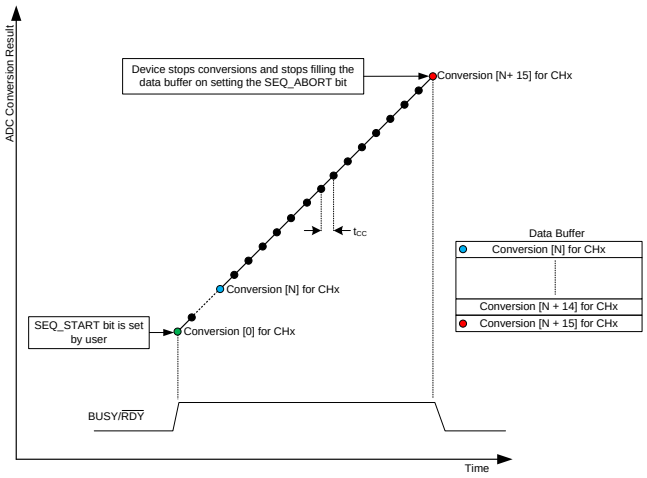


Figure 64. Stop Burst with Single Channel Configurations

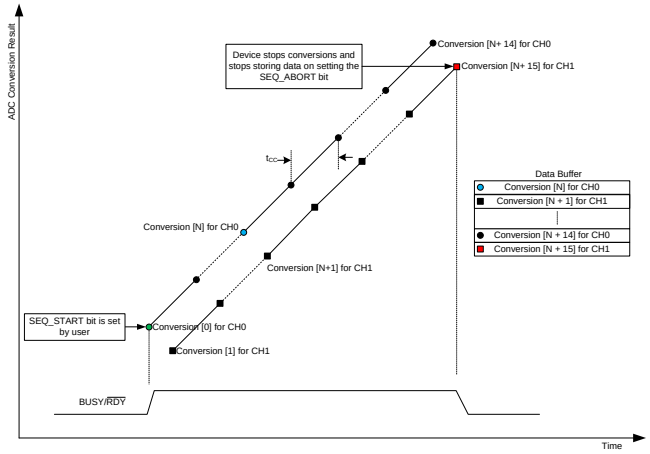
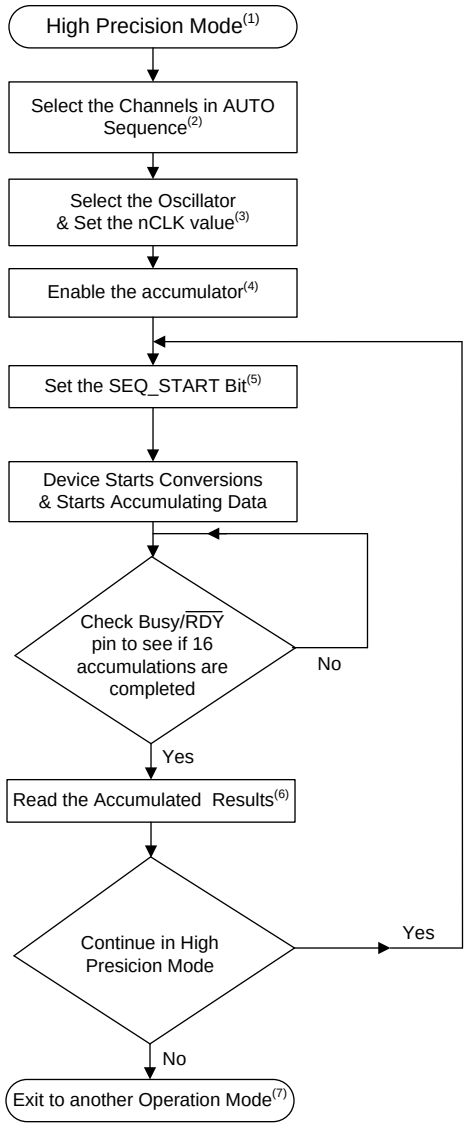


Figure 65. Stop Burst with Dual Channel Configuration

7.4.4 High Precision Mode

The High Precision Mode increases the accuracy of the data measurement to 16-bit accuracy. This is useful for applications where the level of precision required to accurately measure the sensor output needs to be higher than 12 bits. Applications that could take advantage of this type of functionality include gas detectors, air quality testers, water quality testers, and so on.

For this mode, Set *OPMODE_SEL* register to 111b. In this mode, the device starts converting and starts accumulating the conversion results in an accumulator on setting the *SEQ_START* bit. The device stops accumulating the conversion results in accumulator after 16 conversions or when the *SEQ_ABORT* bit is set. Upon accumulating 16 twelve bit conversions, the accumulator contains one 16 bit conversion result. The device has an accumulator for each channel and the device accumulates conversion results from each channel into the respective accumulator. If the operation of the device is aborted in high precision mode before the BUSY/$\overline{\text{RDY}}$ pin goes low, the device provides invalid data. In this mode, on providing a device address and read bit for reading data buffer (Figure 46), the device provides zeroes as output. In this mode, the BUSY/$\overline{\text{RDY}}$ can be used to wake up the MCU or host from sleep or hibernation on completion of accumulation. The steps for configuring the device into High Precision Mode are illustrated in Figure 66 .



(1) For setting the operation mode to High Precision mode, Refer to Figure 54
(2) Select the channels in the AUTO_SEQ_CFG register.
(3) Select the oscillator by configuring the OSC_SEL register and configure the nCLK register.
(4) Enable the accumulator by setting bits in the ACC_EN register.
(5) Set the bit SEQ_START bit in the START_SEQUENCE register.
(6) Read the ACC_CHx_xxx registers.
(7) Select another operation mode in the OPMODE_SEL register.
(8) For reading and writing registers, Refer to Device Programming section.

Figure 66. Configuring Device in High Precision Mode

It is recommended to abort the present sequence by setting the *SEQ_ABORT* bit before changing the device operation mode or device configuration.

Figure 67 illustrates the accumulation of conversion results in high precision mode.

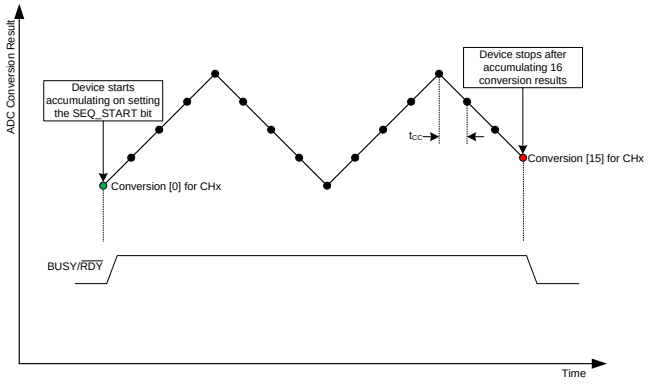


Figure 67. High Precision Mode with Single Channel Configurations

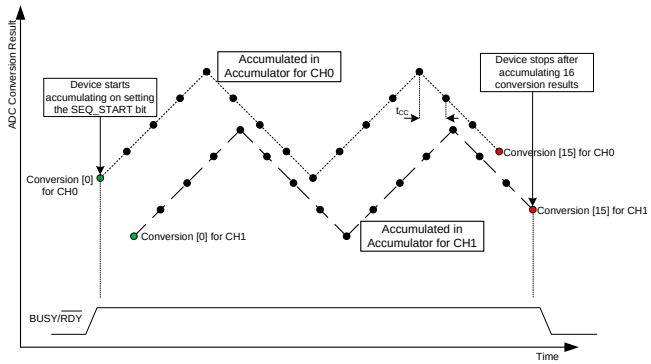


Figure 68. High Precision Mode with Dual Channel Configurations

7.5 Optimizing Power Consumed by the Device

- Keep the analog supply voltage (AVDD) as close as possible to the analog input signal to the device. Set AVDD to be greater than or equal to the analog input signal to the device.
- Keep the digital supply voltage (DVDD) at the lowest permissible value.
- In Manual Mode, run the device at the optimum sampling speed. Power consumption scales with Sampling Speed. In Manual Mode, the sampling speed is dependent on time period (or frequency) of SCL (Equation 7). Figure 69 and Figure 70 illustrate scaling of I_{AVDD} and I_{DVDD} with SCL in Manual Mode.

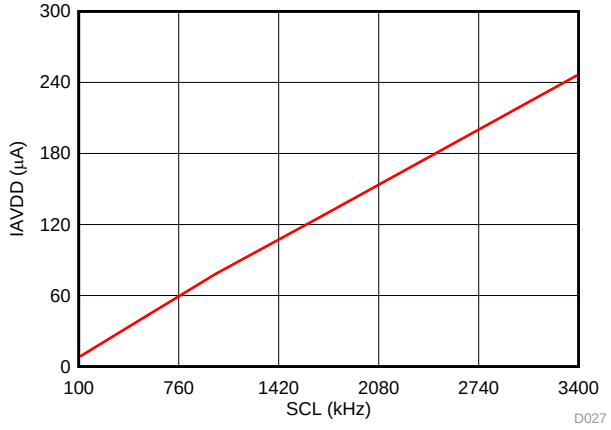


Figure 69. I_{AVDD} in Manual Mode with SCL

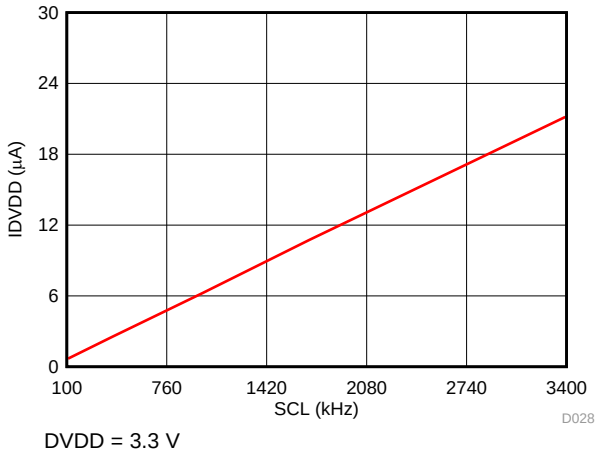


Figure 70. I_{DVDD} in Manual Mode with SCL

- In *Autonomous Modes* and *High Precision Mode*, the balance between sampling speed and power consumption can be obtained by selecting the oscillator for conversion and setting the nCLK value. The device sampling speed and power consumption reduce by increasing the nCLK value. Refer to Figure 71, Figure 72, Figure 73 and Figure 74 for current consumption in Autonomous modes and High Precision mode with different nCLK values.

Optimizing Power Consumed by the Device (continued)

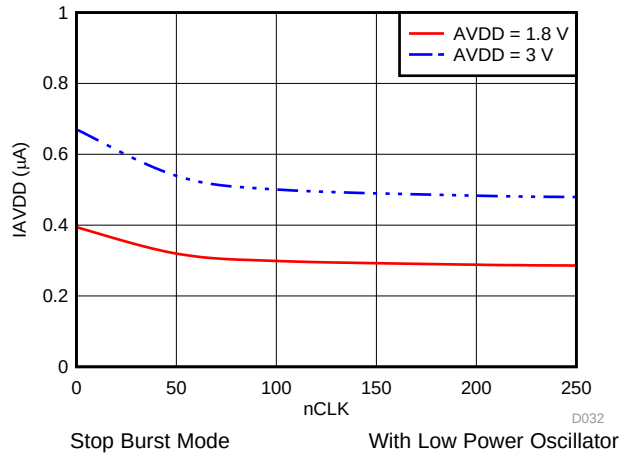


Figure 71. I_{AVDD} in Autonomous Modes with nCLK

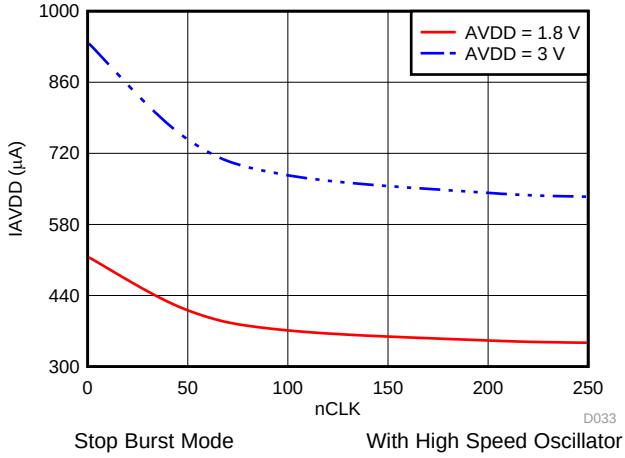


Figure 72. I_{AVDD} in Autonomous Modes with nCLK

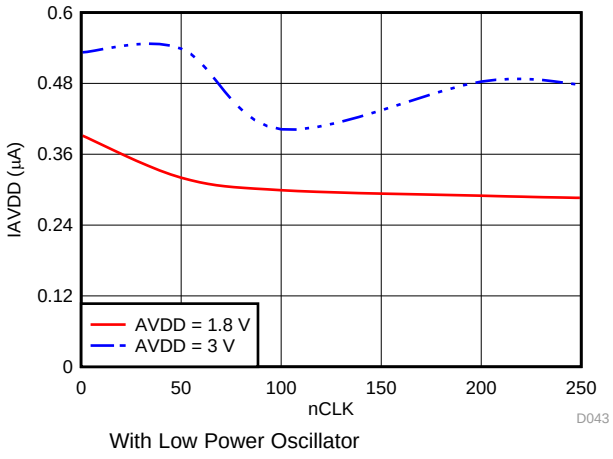


Figure 73. I_{AVDD} in High Precision Mode with nCLK

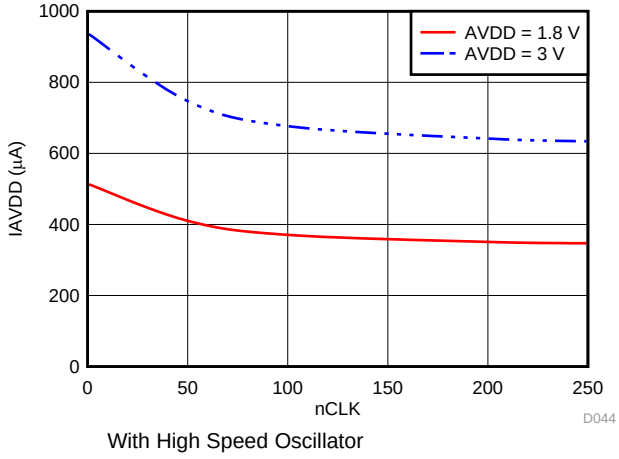


Figure 74. I_{AVDD} in High Precision Mode with nCLK

7.6 Register Map

Table 5 provides the list of registers in the device. All the registers reset to their default values on power up and on receiving a *General Call with Software Reset*. (See *Reset* section).

Table 5. Register Map

S.NO.	ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
RESET REGISTERS			
1	17h	WKEY	Write Key for writing into DEVICE_RESET register
2	14h	DEVICE_RESET	Resets the device
FUNCTIONAL MODE SELECT REGISTERS			
3	15h	OFFSET_CAL	Initiates Internal Offset Calibration Cycle
4	1Ch	OPMODE_SEL	Sets the operation mode and enables auto-sequencing
5	00h	OPMODE_I2CMODE_STATUS	Provides the present Operating Mode and I^2C mode information
INPUT CONFIG REGISTER			
6	24h	CHANNEL_INPUT_CFG	Configures the analog input channels
ANALOG MUX and SEQUENCER REGISTERS			
7	20h	AUTO_SEQ_CHEN	Enables Auto sequencing for selected channels
8	1Eh	START_SEQUENCE	Starts the channel scanning sequence
9	1Fh	ABORT_SEQUENCE	Aborts the channel scanning sequence
10	04h	SEQUENCE_STATUS	Provides the status of sequence in device
OSCILLATOR and TIMING CONTROL REGISTERS			
11	18h	OSC_SEL	Selects the oscillator for the conversion process
12	19h	nCLK_SEL	Sets the nCLK for the device
DATA BUFFER CONTROL REGISTER			
13	2Ch	DATA_BUFFER_OPMODE	Selects Data Buffer operation mode
14	28h	DOUT_FORMAT_CFG	Configures the data output format for data buffer
15	01h	DATA_BUFFER_STATUS	Provides the present status of Data Buffer
ACCUMULATOR CONTROL REGISTERS			
16	30h	ACC_EN	Enables the Accumulator
17	08h	ACC_CH0_LSB	Provides the LSB of accumulated data for CH0 (Read Only)
18	09h	ACC_CH0_MSB	Provides the MSB of accumulated data for CH0 (Read Only)
19	0Ah	ACC_CH1_LSB	Provides the LSB of accumulated data for CH1 (Read Only)
20	0Bh	ACC_CH1_MSB	Provides the MSB of accumulated data for CH1 (Read Only)
21	02h	ACCUMULATOR_STATUS	Provides the present status of Accumulator
DIGITAL WINDOW COMPARATOR REGISTERS			
22	37h	ALERT_DWC_EN	Enables the Alert and Digital Window Comparator block
23	34h	ALERT_CHEN	Enables Alert functionality for individual channels
24	39h	DWC_HTH_CH0_MSB	Sets the MSB for High threshold for CH0
25	38h	DWC_HTH_CH0_LSB	Sets the LSB for High Threshold for CH0
26	3Bh	DWC_LTH_CH0_MSB	Sets the MSB for Low threshold for CH0
27	3Ah	DWC_LTH_CH0_LSB	Sets the LSB for Low threshold for CH0
28	40h	DWC_HYS_CH0	Sets Hysteresis for CH0
29	3Dh	DWC_HTH_CH1_MSB	Sets the MSB for High threshold for CH1
30	3Ch	DWC_HTH_CH1_LSB	Sets the LSB for High threshold for CH1
31	3Fh	DWC_LTH_CH1_MSB	Sets the MSB for Low threshold for CH1
32	3Eh	DWC_LTH_CH1_LSB	Sets the LSB for Low threshold for CH1
33	41h	DWC_HYS_CH1	Sets Hysteresis for CH1
34	36h	PRE_ALT_MAX_EVENT_COUNT	Sets the Pre-Alert Event Counter for both channels
35	03h	ALERT_TRIG_CHID	Provides the channel ID of channel which was first to set the alert output
36	0Ch	ALERT_LOW_FLAGS	Latched flags for Low alert
37	0Eh	ALERT_HIGH_FLAGS	Latched flags for High alert

7.6.1 RESET REGISTERS

These registers control the device reset operation (see Reset section).

7.6.1.1 WKEY Register (address = 17h), [reset = 00h]

A write to this register enables write access to the DEVICE_RESET register.

NOTE

WKEY register is not reset to default value on device reset (see Reset section). After coming out of device reset, write 00h to the WKEY register to prevent erroneous reset.

Figure 75. WKEY Register

7	6	5	4	3	2	1	0
0	0	0	0	KEYWORD[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. WKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved Bits. Do not write. Read returns 0000b
3-0	KEYWORD[3:0]	R/W	0000b	Write 1010b into these bits to get write access for the DEVICE_RESET register.

7.6.1.2 DEVICE_RESET Register (address = 14h), [reset = 00h]

A write to this register resets the device (see Reset section).

NOTE

KEYWORD[3:0] bits in the WKEY register must be programmed to 1010b to enable write into the DEVICE_RESET register.

Figure 76. DEVICE_RESET Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DEV_RST
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	W-0b

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 7. DEVICE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved Bits. Read returns 0000000b
0	DEV_RST	W	0b	Writing 1 into this bit resets the device.

7.6.2 FUNCTIONAL MODE SELECT REGISTERS

These set of registers select the functional mode of the device.

7.6.2.1 OFFSET_CAL Register (address = 15h), [reset = 00h]

Write to this register initiates internal offset calibration cycle (see Offset Calibration).

Figure 77. OFFSET_CAL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	TRIG_OFFCAL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	W-0b

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 8. OFFSET_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved Bits. Read returns 0000000b
0	TRIG_OFFCAL	W	0b	Writing 1 into this bit triggers internal offset calibration.

7.6.2.2 OPMODE_SEL Register (address = 1Ch), [reset = 00h]

Write to this register sets the Operation Mode of the device.

Figure 78. OPMODE_SEL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	SEL_OPMODE[2:0]		
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-000b		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. OPMODE_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved Bits. Read returns 00000b
2-0	SEL_OPMODE[2:0]	R/W	000b	These bits set the functional mode for the device 000b = Manual Mode with CH0 only. (Default Mode). 001b = Same as 000b. 010b = Reserved, Do not use. 011b = Reserved, Do not use. 100b = Manual Mode with AUTO Sequencing enabled. 101b = Manual Mode with AUTO Sequencing enabled. 110b = Autonomous Monitoring Mode with AUTO Sequencing enabled. 111b = High Precision Mode with AUTO Sequencing enabled.

7.6.2.3 OPMODE_I2CMODE_STATUS Register (address = 00h), [reset = 00h]

This register provides the present operation mode and I^2C mode information (Read Only).

Figure 79. OPMODE_I2CMODE_STATUS Register

7	6	5	4	3	2	1	0
0	0	0	0	0	HS_MODE	DEV_OPMODE[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. OPMODE_I2CMODE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved bits. Reads return 00000b.
2	HS_MODE	R	0b	Indicates when device in High speed mode for I^2C Interface. 0b = Device is not in High speed mode for I^2C Interface. 1b = Device is in High speed mode for I^2C Interface.
1-0	DEV_OPMODE[1:0]	R	00b	Indicates the functional mode of the device. 00b = Device is operating in Manual Mode 01b = Not Used 10b = Device is operating in Autonomous Monitoring Mode 11b = Device is operating in High Precision Mode

7.6.3 INPUT CONFIG REGISTER

This register configures the analog input pins of the device (see Analog Input and Multiplexer).

7.6.3.1 CHANNEL_INPUT_CFG Register (address = 24h), [reset = 00h]

Write to this register configures the analog input channels. .

Figure 80. CHANNEL_INPUT_CFG Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CH0_CH1_IP_CFG[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. CHANNEL_INPUT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved Bits. Read returns 000000b
1-0	CH0_CH1_IP_CFG[1:0]	R/W	00b	Selects configuration for the input pins 00b = Two-Channel, Single-Ended configuration 01b = Single-Channel, Single-Ended configuration with Remote Ground Sensing 10b = Single-Channel, Pseudo-Differential configuration 11b = Two-Channel, Single-Ended configuration

7.6.4 ANALOG MUX and SEQUENCER REGISTERS

These registers configure the analog multiplexer and channel sequencing.

7.6.4.1 AUTO_SEQ_CHEN Register (address = 20h), [reset = 03h]

This register selects the channels that are scanned when Auto-Sequencing is enabled. By default, both channels are selected at power up.

Figure 81. AUTO_SEQ_CHEN Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	AUTOSEQ_EN_CH1	AUTOSEQ_EN_CH0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-1b	R/W-1b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. AUTO_SEQ_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved Bits. Read returns 000000b
1	AUTO_SEQ_CH1	R/W	1b	0 = Channel 1 is not selected for auto sequencing 1= Channel 1 is selected for auto sequencing
0	AUTO_SEQ_CH0	R/W	1b	0 = Channel 0 is not selected for auto sequencing 1= Channel 0 is selected for auto sequencing

7.6.4.2 START_SEQUENCE Register (address = 1Eh), [reset = 00h]

A write to this register starts the channel scanning sequence.

Figure 82. START_SEQUENCE Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEQ_START
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. START_SEQUENCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved Bits. Read returns 0000000b
0	SEQ_START	W	0b	Setting this bit = 1 brings the BUSY/$\overline{\text{RDY}}$ pin high and starts the first conversion in the sequence

7.6.4.3 ABORT_SEQUENCE Register (address = 1Fh), [reset = 00h]

A write to this register aborts the channel scanning sequence. Once sequence is aborted using this register, it is recommended to read the *DATA_BUFFER_STATUS* register to know the number of entries filled in the data buffer or *ACCUMULATOR_STATUS* register to know number of accumulations finished before the abort.

Figure 83. ABORT_SEQUENCE Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEQ_ABORT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. ABORT_SEQUENCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved Bits. Read returns 0000000b
0	SEQ_ABORT	W	0b	Setting this bit = 1 aborts the ongoing conversion and brings the BUSY/RDY pin low

7.6.4.4 SEQUENCE_STATUS Register (address = 04h), [reset = 00h]

Provides the status of sequence in device (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 84. SEQUENCE_STATUS Register

7	6	5	4	3	2	1	0
0	0	0	0	0	SEQ_ERR_ST[1:0]		0
R-0b	R-0b	R-0b	R-0b	R-0b	R-00b		R-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. SEQUENCE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved bits. Reads return 00000b.
2-1	SEQ_ERR_ST[1:0]	R	00b	Status of device sequence 00b = Auto Sequencing disabled, no error. 01b = Auto Sequencing enabled, no error. 10b = Not used 11b = Auto Sequencing enabled, device in error.
0	0	R	0b	Reserved bit. Reads return 0.

7.6.5 OSCILLATOR and TIMING CONTROL REGISTERS

These registers select the oscillator used for the conversion process and cycle time for a single conversion (see *Oscillator and Timing Control* section).

7.6.5.1 OSC_SEL Register (address = 18h), [reset = 00h]

A write to this register selects the oscillator used for the conversion process.

Figure 85. OSC_SEL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HSZ_LP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. OSC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved Bits. Read returns 0000000b
0	HSZ_LP	R/W	0b	0b = Device uses High Speed Oscillator 1b = Device uses Low Power Oscillator

7.6.5.2 nCLK_SEL Register (address = 19h), [reset = 00h]

This register controls the cycle time for a single conversion by setting the nCLK parameter. nCLK is the number of clocks of the selected oscillator that the device uses for one conversion cycle.

Figure 86. nCLK_SEL Register

7	6	5	4	3	2	1	0
nCLK[7:0]							
R/W-00000000b							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. nCLK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	nCLK[7:0]	R/W	00000000b	Sets number of clocks of the oscillator that the device uses for one conversion cycle. When using the High Speed Oscillator: For Value x written into the nCLK register • if x ≤ 21, nCLK is set to 21 (00010101b) • if x > 21, nCLK is set to x When using the Low Power Oscillator, For Value x written into the nCLK register: • if x ≤ 18, nCLK is set to 18 (00010010b) • if x > 18, nCLK is set to x

7.6.6 DATA BUFFER CONTROL REGISTER

This register controls the operation of the Data Buffer (see *Data Buffer* section).

7.6.6.1 DATA_BUFFER_OPMODE Register (address = 2Ch), [reset = 01h]

A write to this register selects the operation mode of the Data Buffer.

Figure 87. DATA_BUFFER_OPMODE Register

7	6	5	4	3	2	1	0
0	0	0	0	0	STARTSTOP_CNTRL[2:0]		
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-001b		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. DATA_BUFFER_OPMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved Bits. Read returns 00000b
2-0	STARTSTOP_CNTRL [2:0]	R/W	001b	000b = Stop Burst Mode 001b = Start Burst Mode, default 010b = Reserved, do not use 011b = Reserved, do not use 100b = Pre Alert Data Mode 101b = Reserved, do not use 110b = Post Alert Data Mode 111b = Reserved, do not use

7.6.6.2 DOUT_FORMAT_CFG Register (address = 28h), [reset = 00h]

This register controls the 16-bit contents of the data word in the data buffer.

Figure 88. DOUT_FORMAT_CFG Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DOUT_FORMAT[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. DOUT_FORMAT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved Bits. Read returns 000000b
1-0	DOUT_FORMAT[1:0]	R/W	00b	00b = 12-bit conversion result followed by 0000b 01b = 12-bit conversion result followed by 3-bit Channel ID (000b for CH0, 001b for CH1) 10b = 12-bit conversion result followed by 3-bit Channel ID (000b for CH0, 001b for CH1) followed by DATA_VALID bit 11b = 12-bit conversion result followed by 0000b

7.6.6.3 DATA_BUFFER_STATUS Register (address = 01h), [reset = 00h]

Provides the number of entries filled in the data buffer till last conversion. (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 89. DATA_BUFFER_STATUS Register

7	6	5	4	3	2	1	0
0	0	0	DATA_WORDCOUNT[4:0]				
R-0b	R-0b	R-0b	R-00000b				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. DATA_BUFFER_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000b	Reserved Bits. Read returns 000b
4-0	DATA_WORDCOUNT [4:0]	R	00000b	DATA_WORDCOUNT [00000] to [10000] = Number of entries filled in data buffer (0 to 16)

7.6.7 ACCUMULATOR CONTROL REGISTERS

These registers control the operation of the Accumulator (see *Accumulator* section).

7.6.7.1 ACC_EN Register (address = 30h), [reset = 00h]

This register enables the accumulator.

Figure 90. ACC_EN Register

7	6	5	4	3	2	1	0
0	0	0	0	EN_ACC[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. ACC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved Bits. Read returns 0000b
3-0	EN_ACC[3:0]	R/W	0000b	0000b = Accumulator is disabled 0001b to 1110b = Reserved, do not use 1111b = Accumulator is enabled

7.6.7.2 ACC_CH0_LSB Register (address = 08h), [reset = 00h]

Provides the LSB of accumulated data for CH0 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 91. ACC_CH0_LSB Register

7	6	5	4	3	2	1	0
CH0_LSB[7:0]							
R-00000000b							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 22. ACC_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH0_LSB[7:0]	R	00000000b	LSB of accumulated data for CH0

7.6.7.3 ACC_CH0_MSB Register (address = 09h), [reset = 00h]

Provides the MSB of accumulated data for CH0 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 92. ACC_CH0_MSB Register

7	6	5	4	3	2	1	0
CH0_MSB[7:0]							
R-00000000b							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 23. ACC_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH0_MSB[7:0]	R	00000000b	MSB of accumulated data for CH0

7.6.7.4 ACC_CH1_LSB Register (address = 0Ah), [reset = 00h]

Provides the LSB of accumulated data for CH1 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 93. ACC_CH1 LSB Register

7	6	5	4	3	2	1	0
CH1_LSB[7:0]							
R-00000000b							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 24. ACC_CH1 LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_LSB[7:0]	R	00000000b	LSB of accumulated data for CH1

7.6.7.5 ACC_CH1_MSB Register (address = 0Bh), [reset = 00h]

Provides the MSB of accumulated data for CH1 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 94. ACC_CH1 MSB Register

7	6	5	4	3	2	1	0
CH1_MSB[7:0]							
R-00000000b							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 25. ACC_CH1 MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_MSB[7:0]	R	00000000b	MSB of accumulated data for CH1

7.6.7.6 ACCUMULATOR_STATUS Register (address = 02h), [reset = 00h]

Provides the present status of Accumulator (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 95. ACCUMULATOR_STATUS Register

7	6	5	4	3	2	1	0
0	0	0	0	ACC_COUNT[3:0]			
R-0b	R-0b	R-0b	R-0b	R-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. ACCUMULATOR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved Bits. Read returns 0000b
3-0	ACC_COUNT[3:0]	R	0000b	ACC_COUNT = Number of accumulation completed till last finished conversion.

7.6.8 DIGITAL WINDOW COMPARATOR REGISTERS

These registers control the operation of the Digital Window Comparator (see *Digital Window Comparator* section).

7.6.8.1 ALERT_DWC_EN Register (address = 37h), [reset = 00h]

Write to this register enables the Alert and Digital Window Comparator block.

Figure 96. ALERT_DWC_EN Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DWC_BLOCK_EN
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. ALERT_DWC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved Bits. Read returns 0000000b
0	DWC_BLOCK_EN	R/W	0b	0 = Disables Digital Window Comparator 1 = Enables Digital Window Comparator

7.6.8.2 ALERT_CHEN (address = 34h), [reset = 00h]

This register enables Alert functionality for individual channels.

Figure 97. ALERT_CHEN Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALERT_EN_CH1	ALERT_EN_CH0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-1b	R/W-1b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. ALERT_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved Bits. Read returns 000000b
1	ALERT_EN_CH1	R/W	0b	Enables alert functionality for CH1 0b = Alert is disabled for CH1, default 1b = Alert is enabled for CH1
0	ALERT_EN_CH0	R/W	0b	Enables alert functionality for CH0 0b = Alert is disabled for CH0, default 1b = Alert is enabled for CH0

7.6.8.3 DWC_HTH_CH0_MSB Register (address = 39h), [reset = 00h]

This register sets the four most significant bits of high threshold for CH0.

Figure 98. DWC_HTH_CH0_MSB Register

7	6	5	4	3	2	1	0
0	0	0	0	HTH_CH0_MSB[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. DWC_HTH_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved Bits. Read returns 0000b
3-0	HTH_CH0_MSB[3:0]	R/W	0000b	4 most significant bits of high threshold for CH0

7.6.8.4 DWC_HTH_CH0_LSB Register (address = 38h), [reset = 00h]

This register sets the eight least significant bits of high threshold for CH0.

Figure 99. DWC_HTH_CH0_LSB Register

7	6	5	4	3	2	1	0
HTH_CH0_LSB[7:0]							
R/W-00000000b							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 30. DWC_HTH_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HTH_CH0_LSB[7:0]	R/W	00000000b	8 least significant bits of high threshold for CH0

7.6.8.5 DWC_LTH_CH0_MSB Register (address = 3Bh), [reset = 00h]

This register sets the four most significant bits of low threshold for CH0.

Figure 100. DWC_LTH_CH0_MSB Register

7	6	5	4	3	2	1	0
0	0	0	0	LTH_CH0_MSB[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. DWC_LTH_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved Bits. Read returns 0000b
3-0	LTH_CH0_MSB[3:0]	R/W	0000b	4 most significant bits of low threshold for CH0

7.6.8.6 DWC_LTH_CH0_LSB Register (address = 3Ah), [reset = 00h]

This register sets the eight least significant bits of low threshold for CH0.

Figure 101. DWC_LTH_CH0_LSB Register

7	6	5	4	3	2	1	0
LTH_CH0_LSB[7:0]							
R/W-00000000b							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 32. DWC_LTH_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LTH_CH0_LSB[7:0]	R/W	00000000b	8 least significant bits of low threshold for CH0

7.6.8.7 DWC_HYS_CH0 (address = 40h), [reset = 00h]

This register sets the hysteresis for both comparators for CH0.

Figure 102. DWC_HYS_CH0 Register

7	6	5	4	3	2	1	0
0	0	HYS_CH0[5:0]					
R-0b	R-0b	R/W-000000b					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. DWC_HYS_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved Bits. Read returns 0000000b
5-0	HYS_CH0[5:0]	R/W	000000b	Hysteresis for both comparators for CH0

7.6.8.8 DWC_HTH_CH1_MSB Register (address = 3Dh), [reset = 00h]

This register sets the four most significant bits of high threshold for CH1.

Figure 103. DWC_HTH_CH1_MSB Register

7	6	5	4	3	2	1	0
0	0	0	0	HTH_CH1_MSB[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. DWC_HTH_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved Bits. Read returns 0000b
3-0	HTH_CH1_MSB[3:0]	R/W	0000b	4 most significant bits of high threshold for CH1

7.6.8.9 DWC_HTH_CH1_LSB Register (address = 3Ch), [reset = 00h]

This register sets the eight least significant bits of high threshold for CH1.

Figure 104. DWC_HTH_CH1_LSB Register

7	6	5	4	3	2	1	0
HTH_CH1_LSB[7:0]							
R/W-00000000b							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 35. DWC_HTH_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HTH_CH1_LSB[7:0]	R/W	00000000b	8 least significant bits of high threshold for CH1

7.6.8.10 DWC_LTH_CH1_MSB Register (address = 3Fh), [reset = 00h]

This register sets the four most significant bits of low threshold for CH1.

Figure 105. DWC_LTH_CH1_MSB Register

7	6	5	4	3	2	1	0
0	0	0	0	LTH_CH1_MSB[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. DWC_LTH_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved Bits. Read returns 0000b
3-0	LTH_CH1_MSB[3:0]	R/W	0000b	4 most significant bits of low threshold for CH1

7.6.8.11 DWC_LTH_CH1_LSB Register (address = 3Eh), [reset = 00h]

This register sets the eight least significant bits of low threshold for CH1.

Figure 106. DWC_LTH_CH1_LSB Register

7	6	5	4	3	2	1	0
LTH_CH1_LSB[7:0]							
R/W-00000000b							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 37. DWC_LTH_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LTH_CH1_LSB[7:0]	R/W	00000000b	8 least significant bits of low threshold for CH1

7.6.8.12 DWC_HYS_CH1 (address = 41h), [reset = 00h]

This register sets the hysteresis for both comparators for CH1.

Figure 107. DWC_HYS_CH1 Register

7	6	5	4	3	2	1	0
0	0	HYS_CH1[5:0]					
R-0b	R-0b	R/W-000000b					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. DWC_HYS_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved Bits. Read returns 0000000b
5-0	HYS_CH1[5:0]	R/W	000000b	Hysteresis for both comparators for CH1

7.6.8.13 PRE_ALT_MAX_EVENT_COUNT Register (address = 36h), [reset = 00h]

This register sets the Pre-Alert Event Count for both, high and low comparators, for both the channels.

Figure 108. PRE_ALT_MAX_EVENT_COUNT Register

7	6	5	4	3	2	1	0
PREALERT_COUNT[3:0]				0	0	0	0
R/W-0000b				R-0b	R-0b	R-0b	R-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. PRE_ALT_MAX_EVENT_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PREALERT_COUNT[3:0]	R/W	0000b	Sets the Pre-Alert Event Count = PREALERT_COUNT[3:0] + 1
3-0	RESERVED	R	0000b	Reserved Bits. Read returns 0000b

7.6.8.14 ALERT_TRIG_CHID Register (address = 03h), [reset = 00h]

Provides the channel ID of channel which was first to set the alert output (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

Figure 109. ALERT_TRIG_CHID Register

7	6	5	4	3	2	1	0
ALERT_TRIG_CHID[3:0]				0	0	0	0
R-0000b				R-0b	R-0b	R-0b	R-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. ALERT_TRIG_CHID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ALERT_TRIG_CHID[3:0]	R	0000b	Provides the channel ID of channel which was first to set the alert output 0000b = Channel 0 0001b = Channel 1 0010b to 1111b = Not used
3-0	RESERVED	R	0000b	Reserved bits. Reads return 0000b.

7.6.8.15 ALERT_LOW_FLAGS Register (address = 0C), [reset = 00h]

This register provides the status of latched flags for low alert. All flags are cleared at power up, on general call reset (*General Call with Software Reset*), or by writing FFh to this register. To clear individual alert flag, write 1 to the corresponding bit location. It is recommended to reset the flags when device is not busy (BUSY/$\overline{\text{RDY}}$ pin is low).

Figure 110. ALERT_LOW_FLAGS Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALERT_LOW_CH1	ALERT_LOW_CH0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. ALERT_LOW_FLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved Bits. Read returns 000000b
1	ALERT_LOW_CH1	R/W	0b	Indicates alert on low side comparator for CH1 0b = Alert is not set for low side comparator for CH1 1b = Alert is set for low side comparator for CH1.
0	ALERT_LOW_CH0	R/W	0b	Indicates alert on low side comparator for CH0 0b = Alert is not set for low side comparator for CH0 1b = Alert is set for low side comparator for CH0.

7.6.8.16 ALERT_HIGH_FLAGS Register (address = 0Eh), [reset = 00h]

This register provides the status of latched flags for high alert. All flags are cleared at power up, on general call reset (*General Call with Software Reset*), or by writing FFh to this register. To clear individual alert flag, write 1 to the corresponding bit location. It is recommended to reset the flags when device is not busy (BUSY/$\overline{\text{RDY}}$ pin is low).

Figure 111. ALERT_HIGH_FLAGS Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALERT_HIGH_CH1	ALERT_HIGH_CH0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. ALERT_HIGH_FLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved Bits. Read returns 000000b
1	ALERT_HIGH_CH1	R/W	0b	Indicates alert on high side comparator for CH1 0b = Alert is not set for high side comparator for CH1 1b = Alert is set for high side comparator for CH1.
0	ALERT_HIGH_CH0	R/W	0b	Indicates alert on high side comparator for CH0 0b = Alert is not set for high side comparator for CH0 1b = Alert is set for high side comparator for CH0.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In an increasing number of industrial applications, data acquisition sub-systems are collecting more data about the environment in which the system is operating and applying deep learning algorithms in order to improve system reliability, implement preventative maintenance, and/or enhance the quality of data collected by the system. The ADS7142 can be used to connect to a variety of sensors and can provide deeper data analytics at lower power levels than existing solutions. The depth of analysis that can be performed on the data collected by the ADS7142 is enhanced by the internal data buffer, programmable alarm thresholds and hysteresis, event counter, and internal calibration circuitry. The applications circuits described in this section highlight specific use-cases of the ADS7142 for data collection that can further increase the depth and quality of the data being measured by the system.

8.2 Typical Applications

8.2.1 ADS7142 as a Programmable Comparator with False Trigger Prevention and Diagnostics

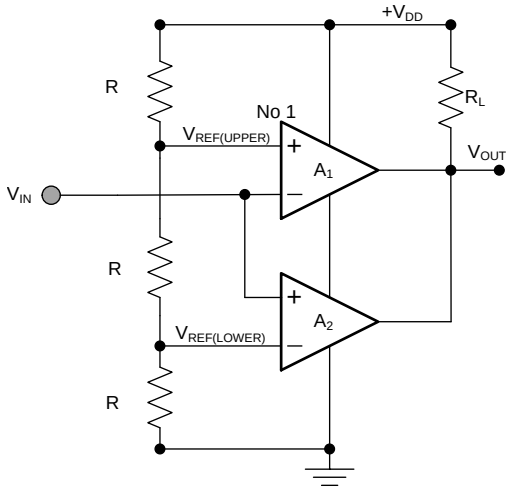


Figure 112. Analog Window Comparator

8.2.1.1 Design Requirements

In many applications such as industrial alarms, sensor monitors, and level sensors, there is a need to make a decision at the system-level when the input signal crosses a predefined threshold. Analog window comparators are being used extensively in such applications.

An analog window comparator has a set of comparators. The external input signal is connected to the inverting terminal of one comparator and the noninverting terminal of the other comparator. The remaining input of each comparator is connected to the internal reference. The outputs are tied together and are often connected to a reset or general-purpose input of a processor (such as a digital signal processor, field-programmable gate array, or application-specific integrated circuit) or the enable input of a voltage regulator (such as a DC-DC or low-dropout regulator). Figure 112 shows the circuit diagram for an analog window comparator.

Typical Applications (continued)

Though analog comparators are easy to design, there are certain disadvantages associated with analog comparators.

8.2.1.1.1 Higher Power Consumption

If the voltage that is monitored is greater than the window comparator supply voltage, then there is a need for a resistive divider ladder to scale down that voltage. This resistive ladder draws a constant current and adds to the power consumption of the system. In battery powered applications, this becomes a challenge and can adversely affect the battery life.

8.2.1.1.2 Fixed Threshold Voltages

The window comparator thresholds cannot be changed on-the-fly since these are set by hardware (typically with a resistive ladder). This may add a limitation if the user wants to change the comparator thresholds during operation without switching in a new resistor ladder.

Many applications in the field of preventive maintenance, building automation, and Internet of Things (IoT) require a sensor monitor which operates autonomously and gives an alert/interrupt to the host MCU only when the sensor output crosses a predefined, programmable threshold. Typically battery-operated, wireless sensor nodes like smoke detectors, temperature monitors, ambient light sensors, proximity sensors and gas sensors fall under this category. The ADS7142 is an excellent fit for such sensor monitoring systems due to its ability to autonomously monitor sensor output and wake up the host controller whenever the sensor output crosses pre-defined thresholds. Additionally, the ADS7142 has an internal data buffer which can store 16 sample data which the user can read if further analysis is required. Figure 113 shows typical block diagram of ADS7142 as sensor monitor. As is shown in Figure 113, the sensor can be connected directly to the input of the ADC (depending on the sensor output signal characteristics).

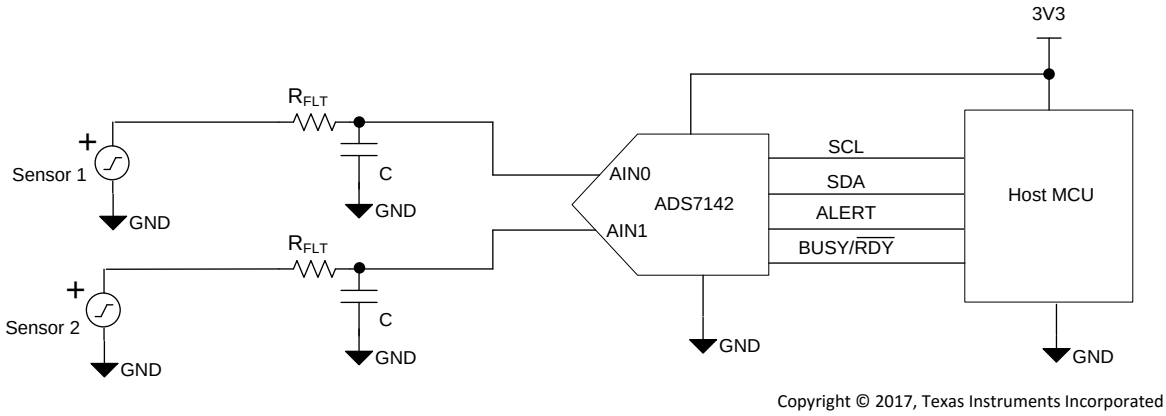


Figure 113. Sensor Monitor Circuit with ADS7142

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Programmable Thresholds and Hysteresis

The ADS7142 can be programmed to monitor sensor output voltages and generate an ALERT signal for the host controller if the sensor output voltage crosses a threshold.

The device can be configured to monitor for signals rising above a programmed threshold. Figure 114 illustrates the operation of the device when monitoring for signal crossings on the low threshold by setting the high threshold to 0xFFF. In this example, the output of the low-side comparator is set whenever the ADC conversion result is less than or equal to the low threshold, and the output of the high-side comparator is only set when the ADC conversion result is equal to 0xFFF.

The device can also be configured to monitor for signals falling below a programmed threshold. Figure 115 illustrates the operation of the device when monitoring for signal crossings on the high threshold by setting the low threshold to 0x000. In this example, the output of high-side comparator is set whenever the ADC conversion result is greater than or equal to the high threshold and the output of the low-side comparator is only set when the ADC conversion result is equal to 0x000.

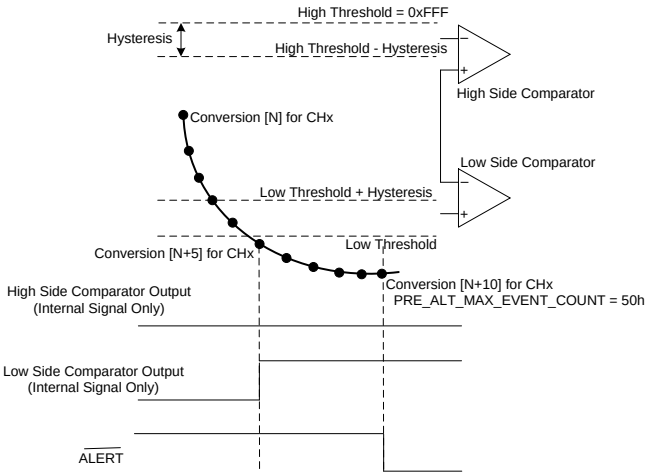


Figure 114. Low Alert with ADS7142

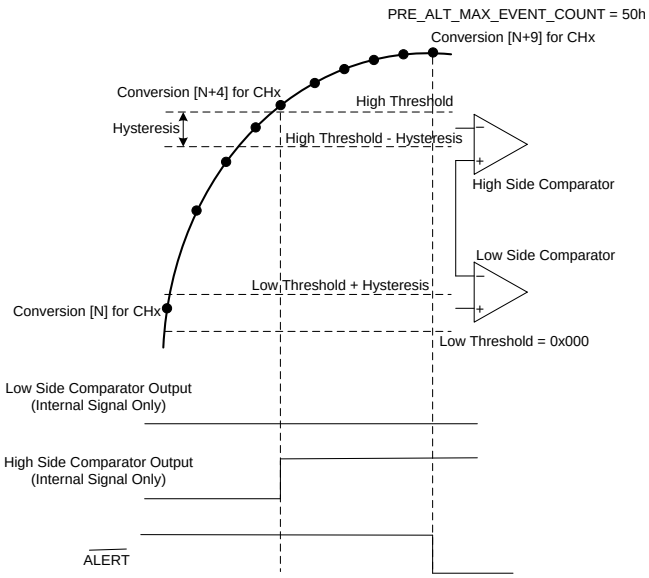


Figure 115. High Alert with ADS7142

The device can also be configured to monitor for signals falling outside of a programmed window. Figure 116 illustrates the operation of the device for an out-of-range alert where the signal leaves the pre-defined window and crosses either the high or low threshold. In this example, the output of low side comparator is set whenever the ADC conversion result is less than or equal to the low threshold, and the output of high side comparator is set when the ADC conversion result is greater than or equal to the high threshold.

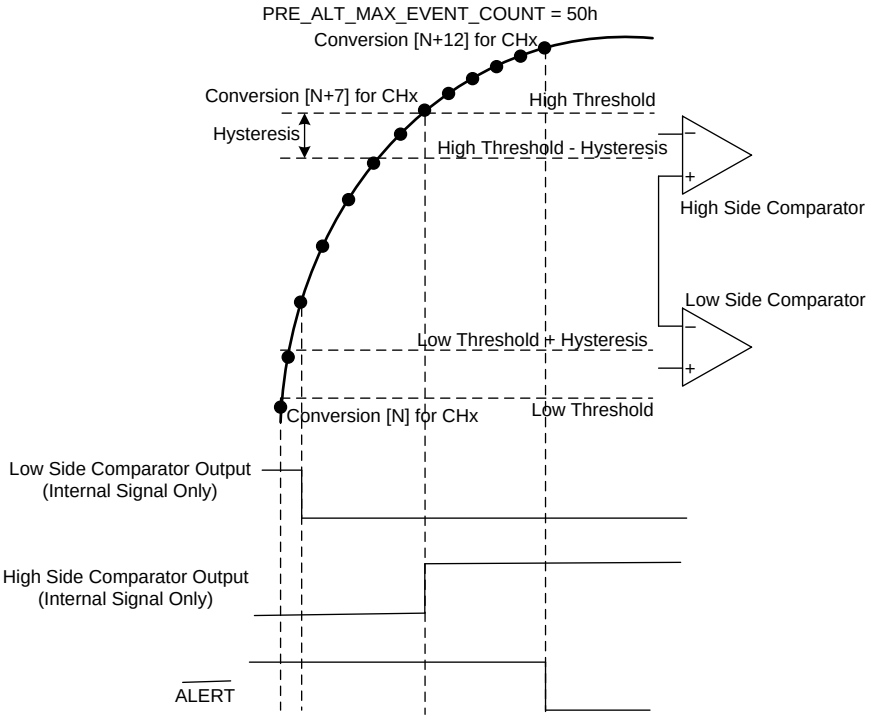


Figure 116. Out of Range Alert with ADS7142

8.2.1.2.2 False Trigger Prevention with Event Counter

The Pre-Alert event counter in the *Digital Window Comparator* helps to prevent false triggers. The alert output is not set until the output of the comparator remains set for a pre-defined number (count) of consecutive conversions.

8.2.1.2.3 Fault Diagnostics with Data Buffer

The modes which are specifically designed for autonomous sensor monitor applications are Pre-Alert mode and Post-Alert mode. In Pre-Alert mode, the ADS7142 can be configured to monitor sensor outputs and continuously fill the internal data buffer until a threshold crossing occurs. The ADS7142 generates an ALERT signal when the sensor output falls outside of the predefined window of operation. In this particular mode, the ADS7142 stops filling the data buffer when the threshold is crossed and provides the last 16 samples (15 sample data preceding the sample at which the ALERT is generated and 1 sample data for which the ALERT is generated). Figure 117 shows the ADS7142 operation in Pre-Alert mode showing 16 data samples before the sensor output crosses the low threshold. This is useful for applications where the state of the signal before the threshold is crossed is important to capture. Using the data captured before the alert, deep data analysis can be performed to determine the state of the system before the alert. This type of data is not available with analog comparators.

In Post-Alert mode, ADS7142 can be configured to monitor sensor outputs and start filling the internal data buffer after a threshold crossing occurs. The ADS7142 generates an ALERT signal when the sensor output falls outside of the predefined window of operation. In this particular mode, the ADS7142 continues to fill the data buffer after the threshold is crossed for a total of 16 samples (1 sample data for which ALERT is generated and 15 sample data after the sample at which ALERT is generated). Figure 118 shows the ADS7142 operation in Post-Alert mode showing 16 data samples after the sensor output crosses the high threshold. This is useful for applications where the state of the signal after the threshold is crossed is important to capture. Using the data captured after the alert, deep data analysis can be performed for to determine the state of the system after the alert to detect system-level events such as saturation. This data is not available with analog comparators.

8.2.1.3 Application Curve

Figure 117. Pre-Alert Data Capture

Figure 118. Post Alert Data Capture

8.2.2 Event-triggered PIR sensing with ADS7142

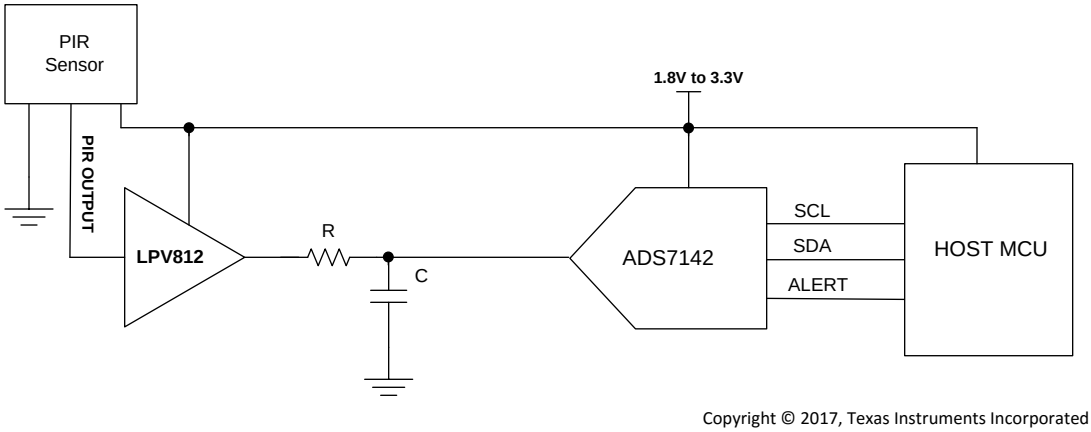


Figure 119. PIR Sensor with ADS7142

8.2.2.1 Design Requirements

A passive infrared (PIR) sensor is a commonly used sensor to detect motion by measuring infrared light emitted from any object that generates heat. PIR sensors are small, inexpensive, low-power, rugged, have a wide lens range, and are easy to use. PIR sensors are commonly used in security lighting and alarm systems used in indoor environments. When there is no motion or heat-emitting object in the vicinity of the sensor, the PIR sensor output is a DC voltage which is typically specified in the PIR datasheet. When a source of heat, such as a person or animal, comes into the sensor field of view, then the PIR sensor output changes. The amplitude of this signal is proportional to the speed and distance of the object relative to the sensor and is in the range of millivolts peak-to-peak. PIR sensors are often followed by a signal conditioning stage which amplifies the IR sensor output. A PIR sensor can be interfaced with the ADS7142 to make an ultra-low-power, autonomous PIR motion detector. The *Autonomous Modes* of the ADS7142 with threshold monitoring enables the system to put the host MCU into a low-power sleep mode and wake up the MCU only when motion is detected by the PIR sensor. Figure 119 shows a typical block diagram for an autonomous PIR motion detector using the ADS7142.

8.2.2.2 Detailed Design Procedure

The analog signal conditioning circuit is shown in the schematic in Figure 120. The first stage of the amplifier filter acts as a bandpass filter while the second stage applies an inverting gain. Components R10 and C5 serve as a low-pass filter to stabilize the supply voltage at the input to the sensor. Resistor R5 sets the bias current in the JFET output transistor of the PIR motion sensor. To save power, R5 is larger than recommended and essentially current starves the sensor. This comes at the expense of decreased sensitivity and higher output noise at the sensor output, which is a fair tradeoff for increased battery lifetime. Some of the loss in sensitivity at the sensor output can be compensated by a gain increase in the filter stages. Stage 1 of Figure 120 is arranged as a non-inverting gain filter stage. This provides a high-impedance load to the sensor so its bias point remains fixed. Because this stage has an effective DC gain of one due to C2, the sensor output bias voltage provides the DC bias for the first filter stage. Feedback diodes D1 and D2 provide clamping so that the op amps in both filter stages stay out of saturation for motion events which are close to the sensor. Stage 1 has a low and high cutoff frequency of 0.7 Hz and 10.6 Hz respectively and a gain of 220. Stage 2 is arranged as an inverting summer gain stage and is AC-coupled to Stage 1. A DC bias of VCC/2 is connected to the non-inverting input of the amplifier in this stage. Due to the higher gain in the filter stages and higher output noise from the sensor, care must be taken to optimize the placement of the high-frequency filter pole and the window comparator thresholds to avoid false detection.

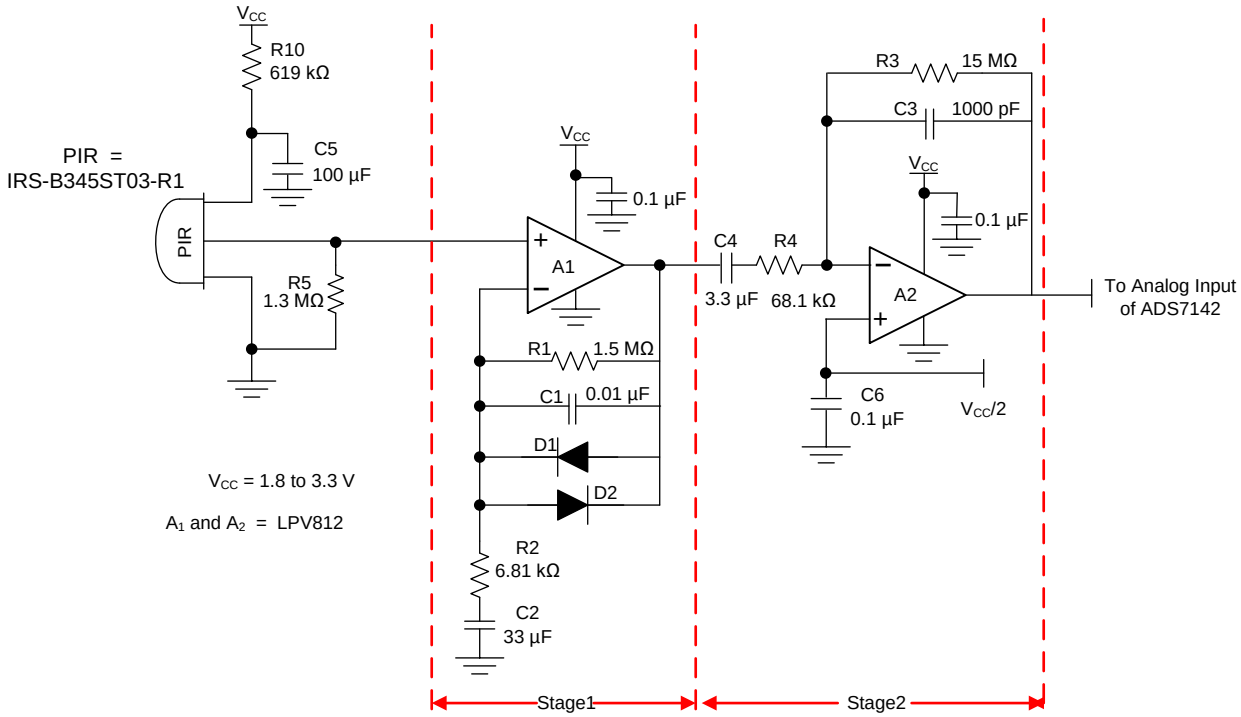


Figure 120. Signal Conditioning Circuit for PIR Sensor

8.2.2.3 Application Curves

When the PIR sensor detects motion, its output crosses the threshold and is detected by the ADS7142 as shown on Channel 1 in Figure 121.

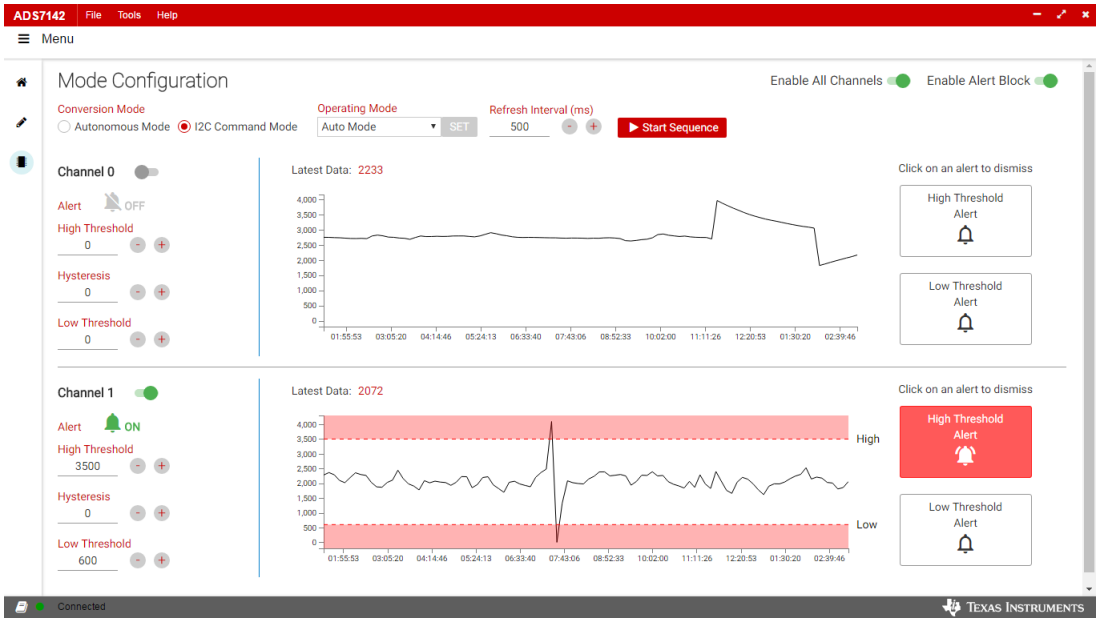


Figure 121. Alert Output from ADS7142 with PIR Sensor

9 Power-Supply Recommendations

9.1 AVDD and DVDD Supply Recommendations

The ADS7142 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. The AVDD supply also defines the full-scale input range of the device. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes. Decouple the AVDD and DVDD pins respectively with 220-nF and 100-nF ceramic decoupling capacitors, as shown in Figure 122 .

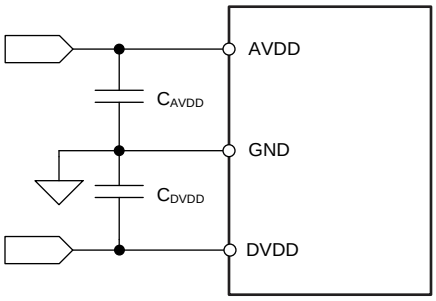


Figure 122. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

Figure 124 shows a board layout example for the circuit illustrated in Figure 123. The key considerations for layout are:

- Use a solid ground plane underneath the device and partition the PCB into analog and digital sections.
- Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.
- The power sources to the device must be clean and well-bypassed. Use C_{AVDD} decoupling capacitors in close proximity to the analog (AVDD) power supply pin.
- Use a C_{DVDD} decoupling capacitor close to the digital (DVDD) power-supply pin.
- Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors.
- Connect the ground pin to the ground plane using a short, low-impedance path.
- Place the charge kickback filter components close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors are recommended because these components provide the most stable electrical properties over voltage, frequency, and temperature changes.

10.2 Layout Example

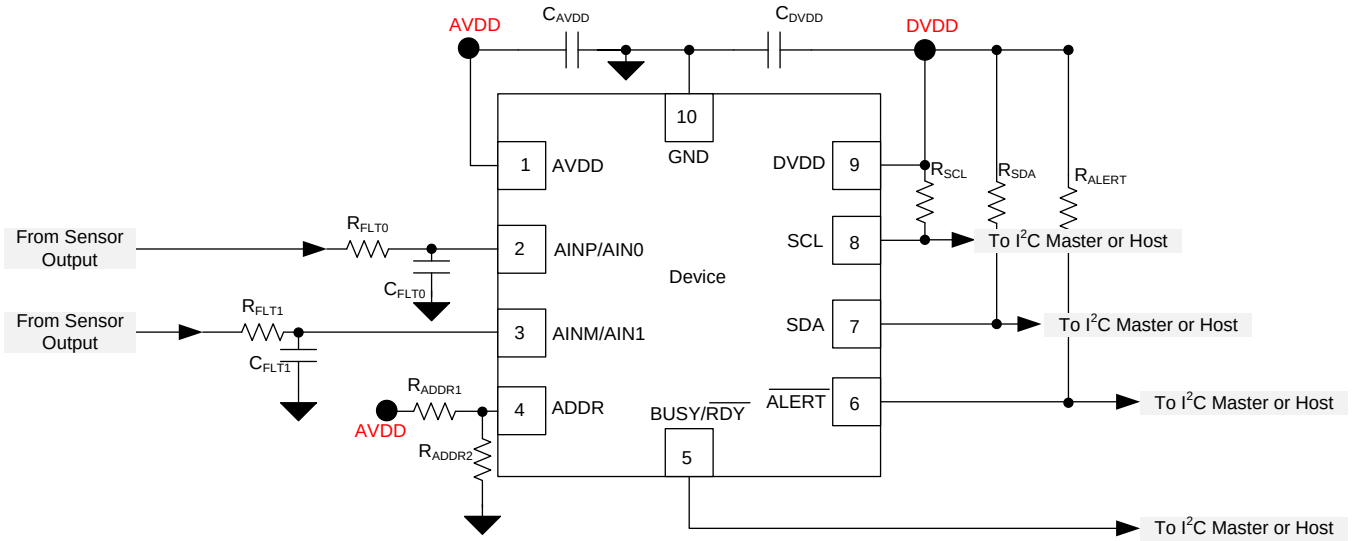


Figure 123. Example Circuit

Layout Example (continued)

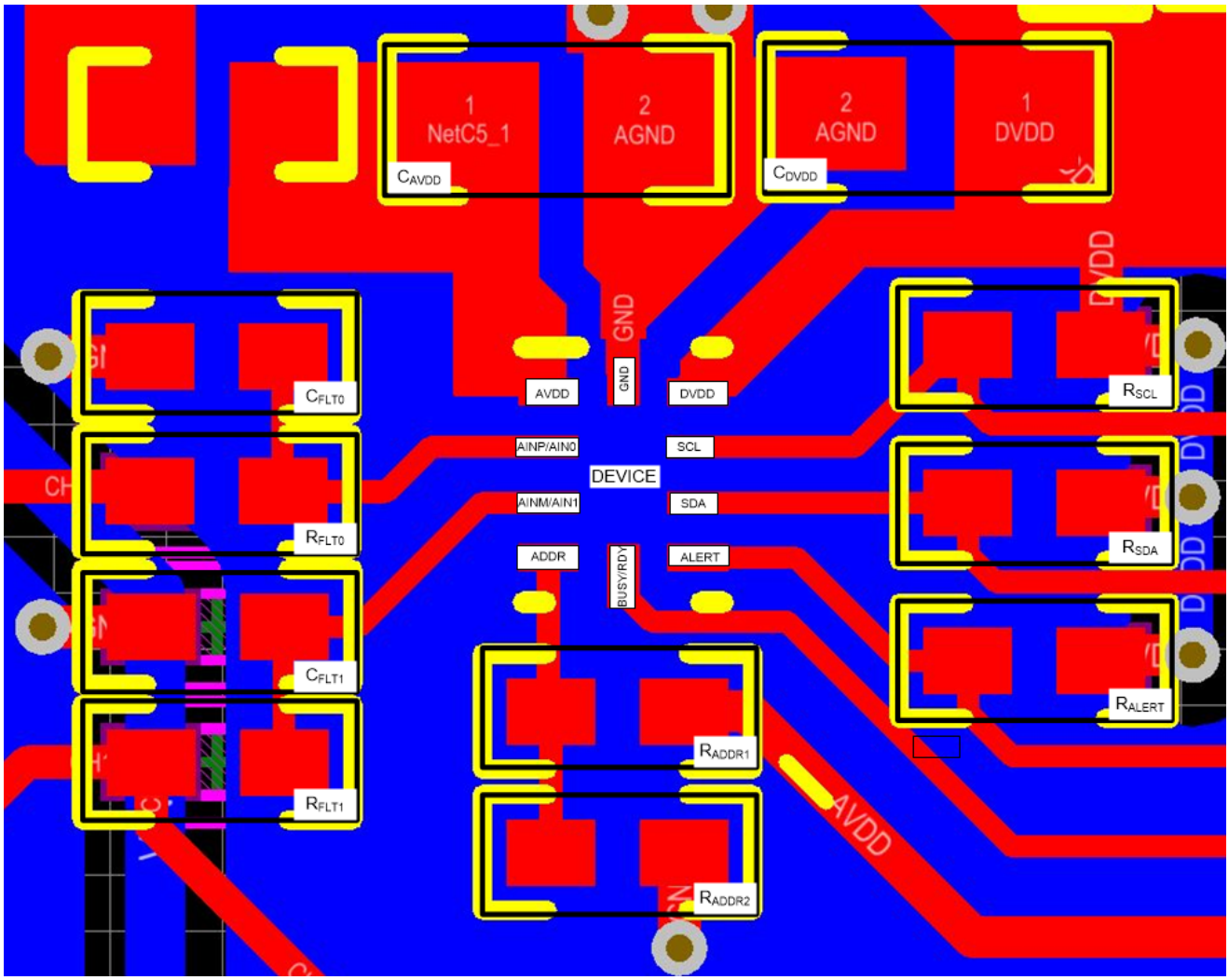


Figure 124. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7142IRUGR	ACTIVE	X2QFN	RUG	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18M	Samples
ADS7142IRUGT	ACTIVE	X2QFN	RUG	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS7142 :

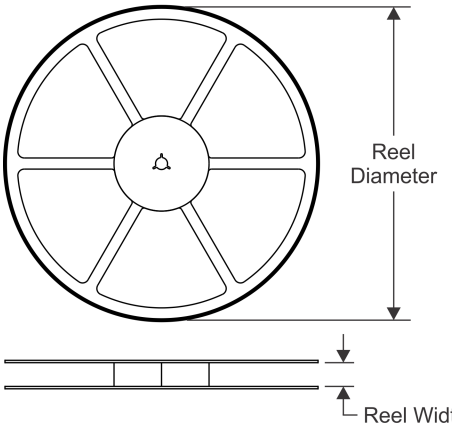
- Automotive: ADS7142-Q1

NOTE: Qualified Version Definitions:

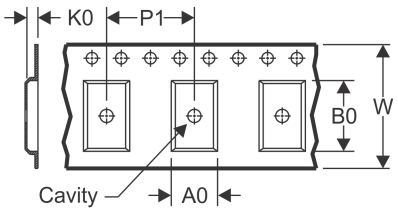
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

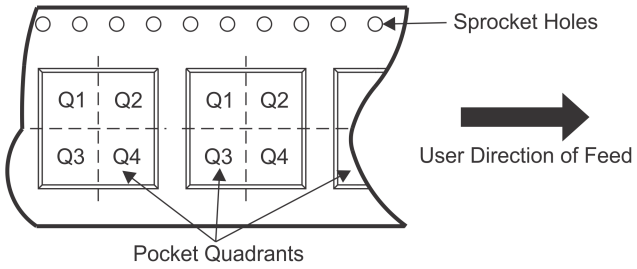


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

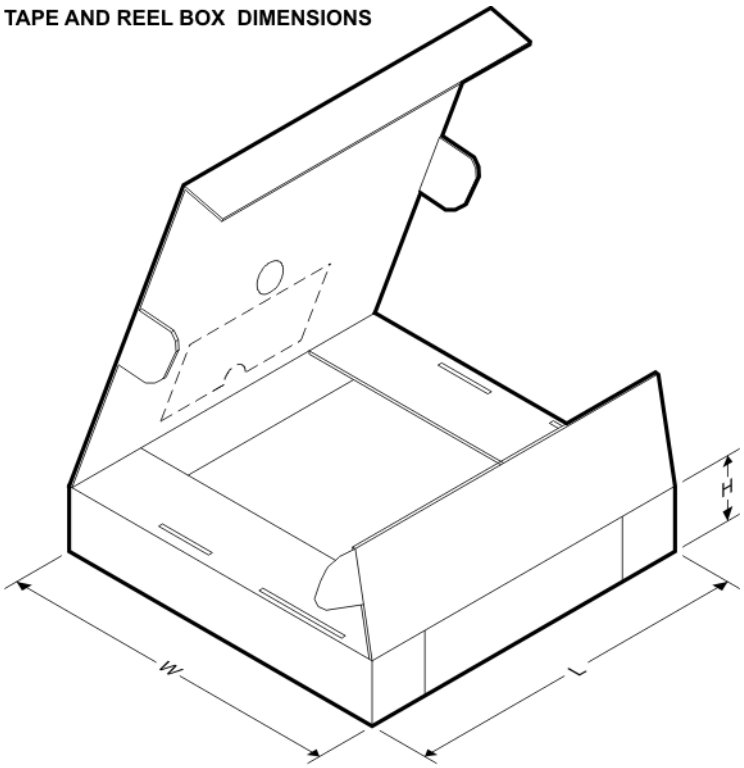
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7142IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
ADS7142IRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1

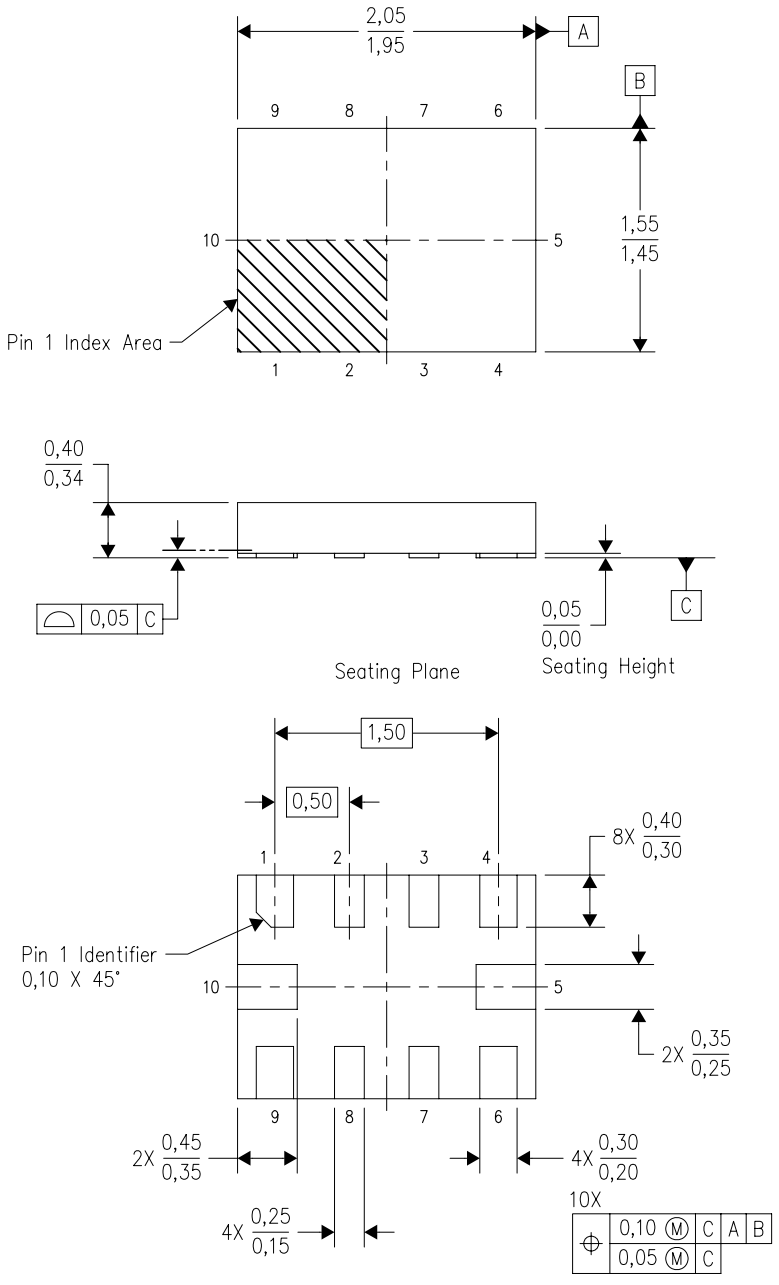
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7142IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
ADS7142IRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0

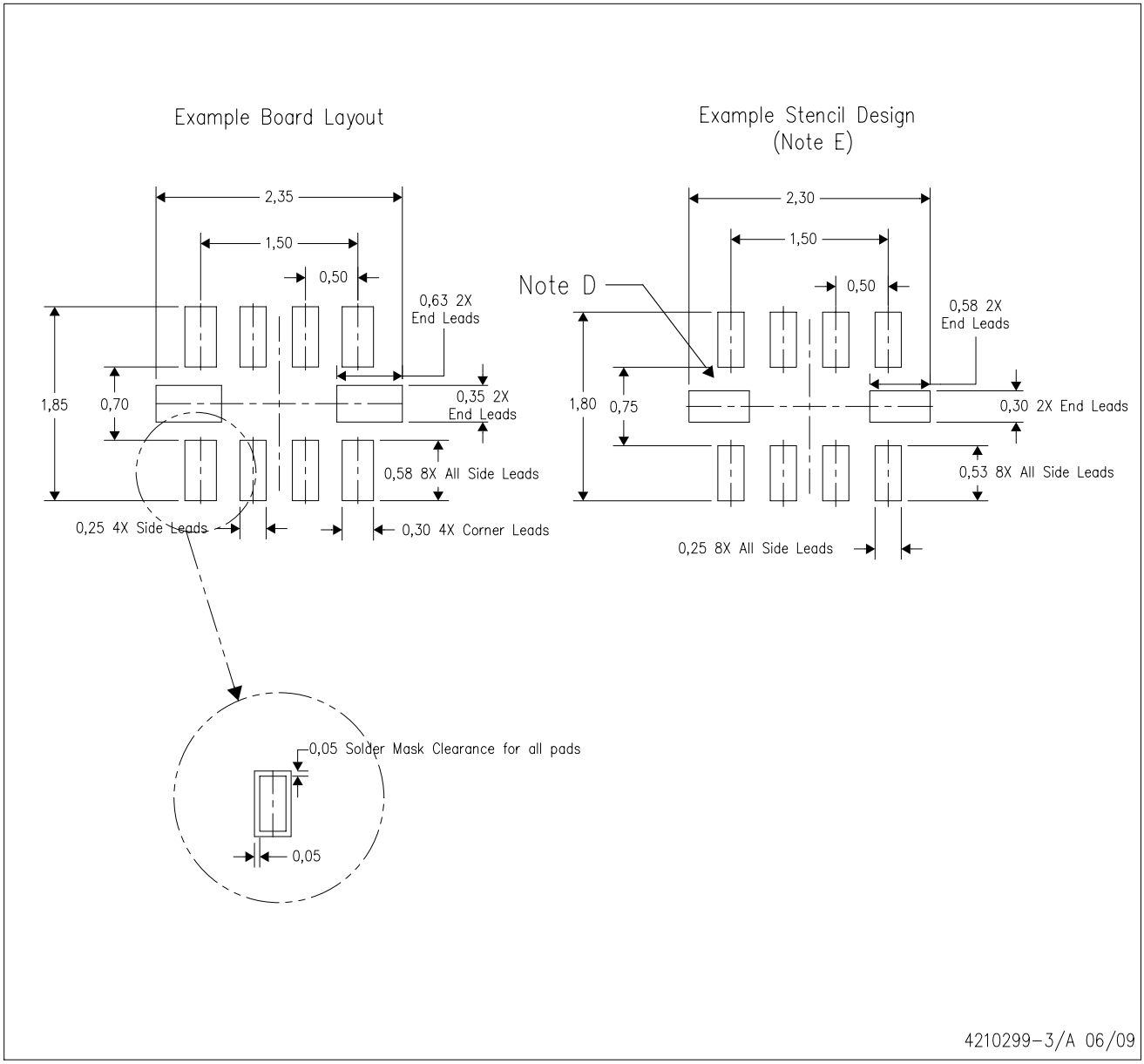
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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