

# bq24308 Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC

## 1 Features

- Provides Protection for Three Variables:
  - Input Overvoltage
  - Input Overcurrent with Current Limiting
  - Battery Overvoltage
- Maximum Input Voltage of 30 V
- Supports Up to 1.5-A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- LDO Mode Voltage Regulation of 5 V
- Available in Space-Saving Small 2 mm x 2 mm 8-Pin WSON Package

## 2 Applications

- Mobile and Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

## 3 Description

The bq24308 device is a highly integrated circuit (IC) designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current to a safe value for a blanking duration before turning the switch off. Battery voltage may also be monitored and if the battery voltage exceeds the specified value the internal switch is turned off. Additionally, the device also monitors its own die temperature and switches off if it becomes too hot.

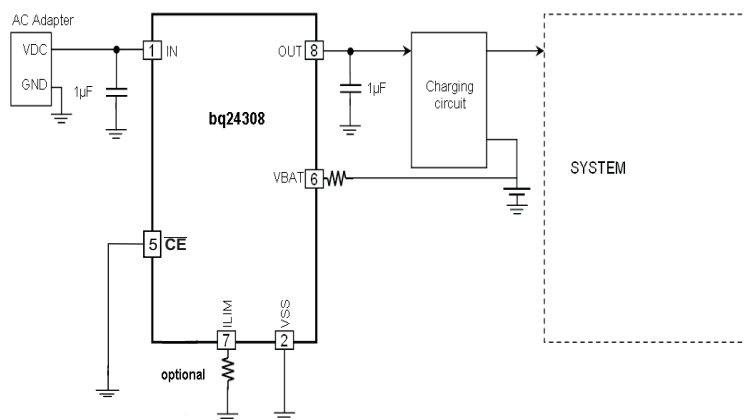
The input overcurrent threshold can be increased using an external resistor. The device also offers optional protection against reverse voltage at the input using an external P-channel FET.

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE  | BODY SIZE (NOM)   |
|-------------|----------|-------------------|
| bq24308     | WSON (8) | 2.00 mm x 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Application Circuit



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision A (November 2009) to Revision B</b>   | <b>Page</b> |
|--|-------------|
| • Changed SON to WSON throughout the document .....  | <b>1</b>    |
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. .... | <b>1</b>    |
| • Changed the location of the ESD information from the ABS MAX table to the new ESD Ratings table .....  | <b>4</b>    |
| • Moved Figures 1 through 10 from <i>Typical Characteristics</i> to <i>Application Curves</i> section .....  | <b>14</b>   |

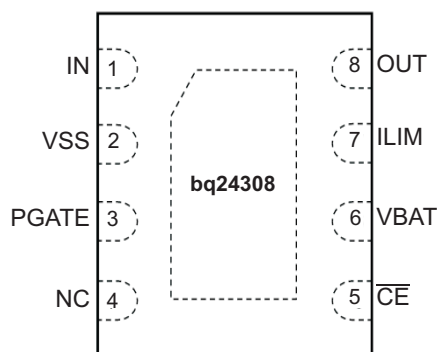
| <b>Changes from Original (September 2009) to Revision A</b>  | <b>Page</b> |
|--|-------------|
| • Changed Units from V to A for Input and Output Current spec in Absolute Maximum Ratings table .....  | <b>4</b>    |
| • Changed $V_{O(REG)}$ test condition, $I_{OUT}$ value from 50 mA to 250 mA .....                      | <b>5</b>    |
| • Added $T_J = 0^{\circ}\text{C}$ to $125^{\circ}\text{C}$ to test conditions for $I_{OCP}$ spec. .... | <b>5</b>    |
| • Changed $Q_{EXT}$ device symbol in the Input Reverse-Polarity Protection schematic. ....             | <b>14</b>   |

## 5 Device Comparison Table

| PART NUMBER | MARKING | MEDIUM        | QUANTITY | PACKAGE                |
|-------------|---------|---------------|----------|------------------------|
| bq24308DSGR | DAS     | Tape and Reel | 3000     | 2.00 mm × 2.00 mm WSON |
| bq24308DSGT | DAS     | Tape and Reel | 250      | 2.00 mm × 2.00 mm WSON |

## 6 Pin Configuration and Functions

**DSG Package**  
8-Pin WSON With Exposed Thermal Pad  
Top View



**Pin Functions**

| PIN             |     | I/O | DESCRIPTION   |
|-----------------|-----|-----|---|
| NAME            | NO. |     |   |
| $\overline{CE}$ | 5   | I   | Chip enable input. Active low. When $\overline{CE}$ = High, the input FET is off. Internally pulled down.   |
| ILIM            | 7   | I   | Input overcurrent threshold programming. An optional external resistor can be used to increase input overcurrent threshold. Connect a resistor to VSS to increase the OCP threshold.  |
| IN              | 1   | I   | Input power, connect to external DC supply. Connect external 0.1 $\mu$ F (minimum) ceramic capacitor to VSS.  |
| NC              | 4   | —   | Do not connect to any external circuit. This pin may have internal connections used for test purposes.  |
| OUT             | 8   | O   | Output terminal to the charging system. Connect external 1- $\mu$ F capacitor (minimum) ceramic capacitor to VSS.   |
| PGATE           | 3   | O   | Gate drive for optional external P-FET  |
| VBAT            | 6   | I   | Battery voltage sense input. Connect to pack positive terminal through a resistor.  |
| VSS             | 2   | —   | Ground terminal   |
| Thermal Pad     |     |     | There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times. |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                |  | MIN  | MAX | UNIT |
|--------------------------------|--|------|-----|------|
| Input voltage                  | IN, PGATE (with respect to VSS)                    | -0.3 | 30  | V    |
|                                | OUT (with respect to VSS)                          | -0.3 | 12  |      |
|                                | ILIM, $\overline{CE}$ , VBAT (with respect to VSS) | -0.3 | 7   |      |
| Input current                  | IN   |      | 2   | A    |
| Output current                 | OUT  |      | 2   | A    |
|                                | PGATE  |      | 5   | mA   |
| Junction temperature, $T_J$    |  | -40  | 150 | °C   |
| Storage temperature, $T_{stg}$ |  | -65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|                                     |  | VALUE         | UNIT |        |
|-------------------------------------|--|---------------|------|--------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000         | V    |        |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500          |      |        |
|                                     | IN (IEC 61000-4-2) <sup>(3)</sup>  | Air Discharge |      | ±15000 |
|                                     |  | Contact       |      | ±8000  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.  
 (3) With IN bypassed to the VSS with a 1- $\mu$ F low-ESR ceramic capacitor

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|            |                          | MIN | NOM | MAX | UNIT       |
|------------|--------------------------|-----|-----|-----|------------|
| $V_{IN}$   | Input voltage range      | 3.3 |     | 26  | V          |
| $I_{IN}$   | Input current, IN pin    |     |     | 1.5 | A          |
| $I_{OUT}$  | Output current, OUT pin  |     |     | 1.5 | A          |
| $R_{ILIM}$ | OCP programming resistor | 31  |     |     | k $\Omega$ |
| $T_J$      | Junction temperature     | -40 |     | 125 | °C         |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | bq24308    | UNIT |
|-------------------------------|--|------------|------|
|                               |  | DSG (WSON) |      |
|                               |  | 8 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 58.6       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 67.9       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 29.7       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 1.2        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 30.3       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 7.6        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  and recommended supply voltage (unless otherwise noted)

| PARAMETER                              |   | TEST CONDITIONS   | MIN        | TYP  | MAX  | UNIT               |
|--|---|---|------------|------|------|--------------------|
| <b>IN</b>                              |   |   |            |      |      |                    |
| $V_{UVLO}$                             | Undervoltage lock-out, input power detected threshold                                   | $\overline{CE} = \text{Low}, V_{IN}: 0\text{ V} \rightarrow 3\text{ V}$   | 2.5        | 2.7  | 2.8  | V                  |
| $V_{HYS-UVLO}$                         | Hysteresis on UVLO  | $\overline{CE} = \text{Low}, V_{IN}: 3\text{ V} \rightarrow 0\text{ V}$   | 200        | 260  | 300  | mV                 |
| $t_{DGL(PGOOD)}$                       | Deglintch time, input power detected status   | $\overline{CE} = \text{Low}$ . Time measured from $V_{IN}$ $0\text{ V} \rightarrow 4\text{ V}$ $1\text{ }\mu\text{s}$ rise-time, to output turning ON                                   |            | 8    |      | ms                 |
| $I_{DD}$                               | Operating current   | $\overline{CE} = \text{Low}, V_{IN} = 5\text{ V}$ , no load on OUT pin  |            | 410  | 500  | $\mu\text{A}$      |
| $I_{STDBY}$                            | Standby current   | $\overline{CE} = \text{High}, V_{IN} = 5\text{ V}$  |            | 65   | 95   | $\mu\text{A}$      |
| <b>INPUT TO OUTPUT CHARACTERISTICS</b> |   |   |            |      |      |                    |
| $V_{DO}$                               | Drop-out voltage IN to OUT  | $\overline{CE} = \text{Low}, V_{IN} = 4\text{ V}, I_{OUT} = 250\text{ mA}$  |            | 45   | 75   | mV                 |
| <b>INPUT OVERVOLTAGE PROTECTION</b>    |   |   |            |      |      |                    |
| $V_{OVP}$                              | Input overvoltage protection threshold  | $\overline{CE} = \text{Low}, V_{IN}: 4\text{ V to } 10\text{ V}$  | 6.1        | 6.3  | 6.5  | V                  |
| $V_{HYS-OVP}$                          | Hysteresis on OVP   | $\overline{CE} = \text{Low}, V_{IN}: 10\text{ V to } 4\text{ V}$  | 20         | 60   | 110  | mV                 |
| $t_{PD(OVP)}$                          | Input OVP propagation delay <sup>(1)</sup>  | $\overline{CE} = \text{Low}$ , Time measured from $V_{IN}$ $4\text{ V} \rightarrow 10\text{ V}$ , $1\text{ }\mu\text{s}$ rising time, to output turning OFF                             |            | 0.2  | 1    | $\mu\text{s}$      |
| $t_{ON(OVP)}$                          | Recovery time from input overvoltage condition  | $\overline{CE} = \text{Low}$ , Time measured from $V_{IN}$ $10\text{ V} \rightarrow 4\text{ V}$ , $1\text{ }\mu\text{s}$ fall-time, to output turning ON                                |            | 8    |      | ms                 |
| <b>OUTPUT VOLTAGE REGULATION</b>       |   |   |            |      |      |                    |
| $V_{O(REG)}$                           | Output voltage  | $\overline{CE} = \text{Low}, V_{IN} = 6\text{ V}, I_{OUT} = 250\text{ mA}$  | 4.85       | 5    | 5.15 | V                  |
| <b>INPUT OVERCURRENT PROTECTION</b>    |   |   |            |      |      |                    |
| $I_{OCP}$                              | Internal input overcurrent protection threshold   | $\overline{CE} = \text{Low}, V_{IN} = 5\text{ V}$ , ILIM floating; $T_J = 0^{\circ}\text{C to } 125^{\circ}\text{C}$  | 630        | 700  | 770  | mA                 |
|  | Input overcurrent protection range  | $\overline{CE} = \text{Low}, V_{IN} = 5\text{ V}; T_J = 0^{\circ}\text{C to } 125^{\circ}\text{C}$  | 630        |      | 1500 | mA                 |
| $\Delta I_{OCP}$                       | OCP threshold accuracy  | $T_J = 0^{\circ}\text{C to } 125^{\circ}\text{C}$   | $\pm 10\%$ |      |      |                    |
|  |   | $T_J = -40^{\circ}\text{C to } 125^{\circ}\text{C}$   | $\pm 13\%$ |      |      |                    |
| $K_{ILIM}$                             | Current limit programming: $I_{OCP}(\text{program}) = I_{OCP} + K_{ILIM} \div R_{ILIM}$ |   | 25000      |      |      | $\text{A}\Omega$   |
| $t_{BLANK(OCP)}$                       | Blanking time, input overcurrent detected   | $\overline{CE} = \text{Low}$  |            | 5    |      | ms                 |
| $t_{REC(OCP)}$                         | Recovery time from input overcurrent condition  | $\overline{CE} = \text{Low}$  |            | 64   |      | ms                 |
| <b>BATTERY OVERVOLTAGE PROTECTION</b>  |   |   |            |      |      |                    |
| $BV_{OVP}$                             | Battery overvoltage protection threshold  | $\overline{CE} = \text{Low}, V_{IN} > 4.4\text{ V}, V_{VBAT}: 4.2\text{ V} \rightarrow 4.5\text{ V}$  | 4.3        | 4.35 | 4.40 | V                  |
| $V_{HYS-BOVP}$                         | Hysteresis on $BV_{OVP}$  | $\overline{CE} = \text{Low}, V_{IN} > 4.4\text{ V}, V_{VBAT}: 4.5\text{ V} \rightarrow 3.9\text{ V}$  | 200        | 275  | 320  | mV                 |
| $I_{VBAT}$                             | Input bias current on VBAT pin  | $V_{VBAT} = 4.4\text{ V}, T_J = 25^{\circ}\text{C}$   |            |      | 10   | nA                 |
| $t_{DGL(BOVP)}$                        | Deglintch time, battery overvoltage detected  | $\overline{CE} = \text{Low}, V_{IN} > 4.4\text{ V}$ , time measured from $V_{VBAT}$ $4.2\text{ V} \rightarrow 4.5\text{ V}$ , $1\text{ }\mu\text{s}$ rising time, to output turning OFF |            | 176  |      | $\mu\text{s}$      |
| <b>THERMAL PROTECTION</b>              |   |   |            |      |      |                    |
| $T_{J(OFF)}$                           | Thermal shutdown temperature  |   |            | 140  | 150  | $^{\circ}\text{C}$ |
| $T_{J(OFF-HYS)}$                       | Thermal shutdown hysteresis   |   |            | 20   |      | $^{\circ}\text{C}$ |
| <b>P-FET GATE DRIVER</b>               |   |   |            |      |      |                    |
| $V_{GCLMP}$                            | Gate driver clamp voltage   | $V_{IN} > 17\text{ V}$  | 13         | 15   | 17   | V                  |

(1) Not tested in production. Specified by design.

## Electrical Characteristics (continued)

over junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  and recommended supply voltage (unless otherwise noted)

| PARAMETER  |                          | TEST CONDITIONS         | MIN | TYP | MAX | UNIT          |
|--|--------------------------|-------------------------|-----|-----|-----|---------------|
| <b>LOGIC LEVELS ON <math>\overline{\text{CE}}</math></b> |                          |                         |     |     |     |               |
| $V_{IL}$   | Low-level input voltage  |                         | 0   |     | 0.4 | V             |
| $V_{IH}$   | High-level input voltage |                         | 1.4 |     |     | V             |
| $I_{IL}$   | Low-level input current  |                         |     |     | 1   | $\mu\text{A}$ |
| $I_{IH}$   | High-level input current | $V_{CE} = 1.8\text{ V}$ |     |     | 15  | $\mu\text{A}$ |

## 7.6 Typical Characteristics

Test conditions (unless otherwise noted) for typical operating performance are:  $V_{IN} = 5\text{ V}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 1\ \mu\text{F}$ ,  $R_{BAT} = 100\ \text{k}\Omega$ ,  $R_{OUT} = 16\ \Omega$ ,  $T_A = 25^{\circ}\text{C}$  (see [Figure 12](#))

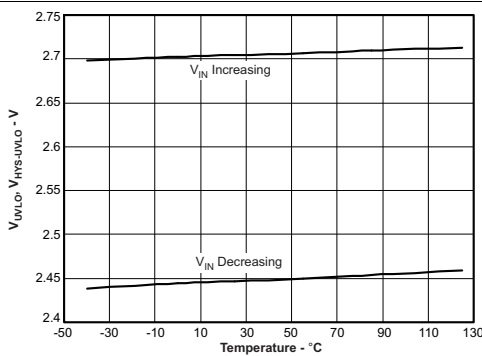


Figure 1. Undervoltage Lockout vs Free-Air Temperature

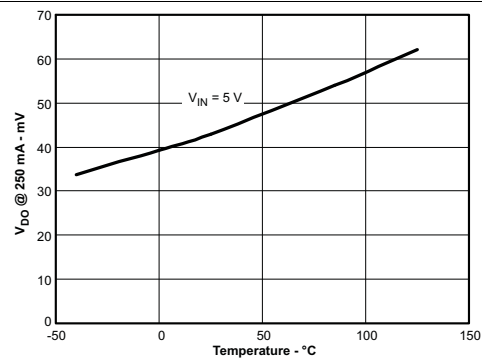


Figure 2. Dropout Voltage (IN to OUT) vs Free-Air Temperature

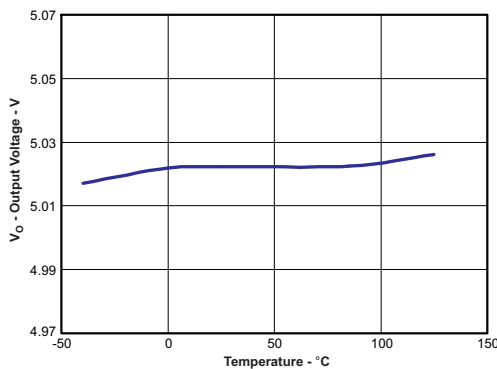


Figure 3. Regulation Voltage (OUT Pin) vs Free-Air Temperature

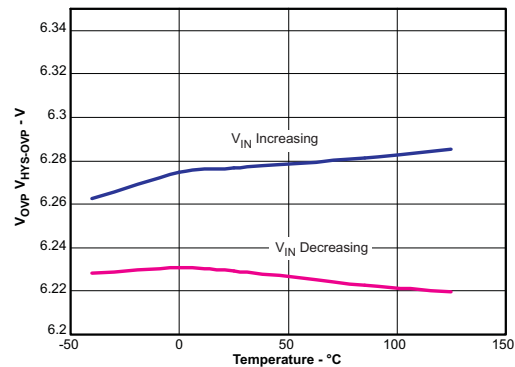


Figure 4. OVP Threshold vs Free-Air Temperature

Typical Characteristics (continued)

Test conditions (unless otherwise noted) for typical operating performance are:  $V_{IN} = 5\text{ V}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 1\ \mu\text{F}$ ,  $R_{BAT} = 100\ \text{k}\Omega$ ,  $R_{OUT} = 16\ \Omega$ ,  $T_A = 25^\circ\text{C}$  (see Figure 12)

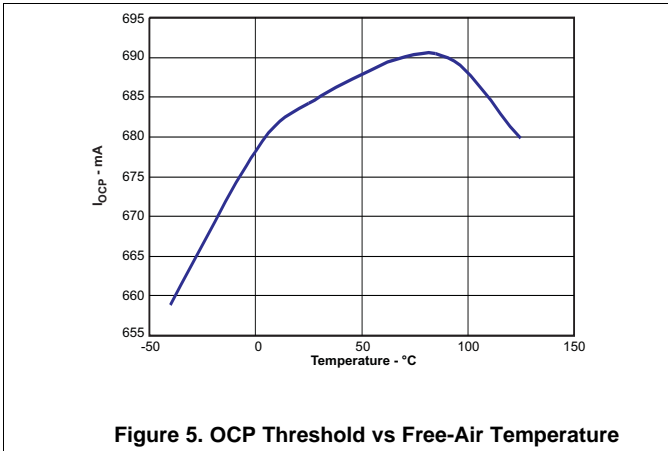


Figure 5. OCP Threshold vs Free-Air Temperature

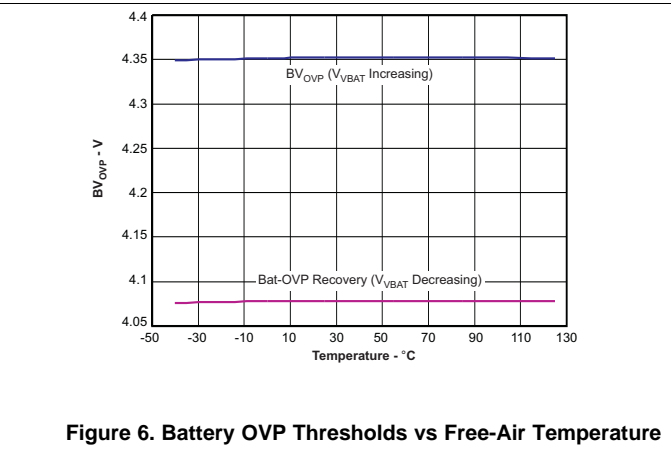


Figure 6. Battery OVP Thresholds vs Free-Air Temperature

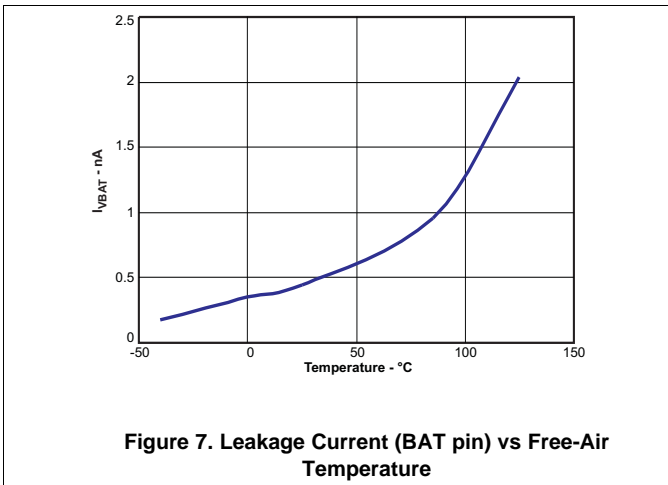


Figure 7. Leakage Current (BAT pin) vs Free-Air Temperature

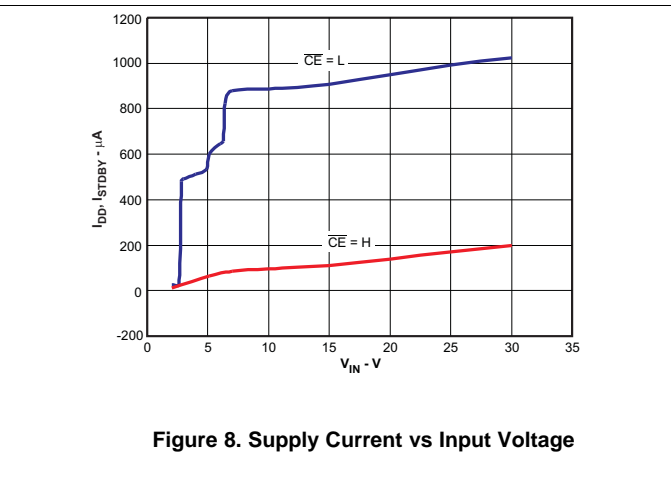


Figure 8. Supply Current vs Input Voltage

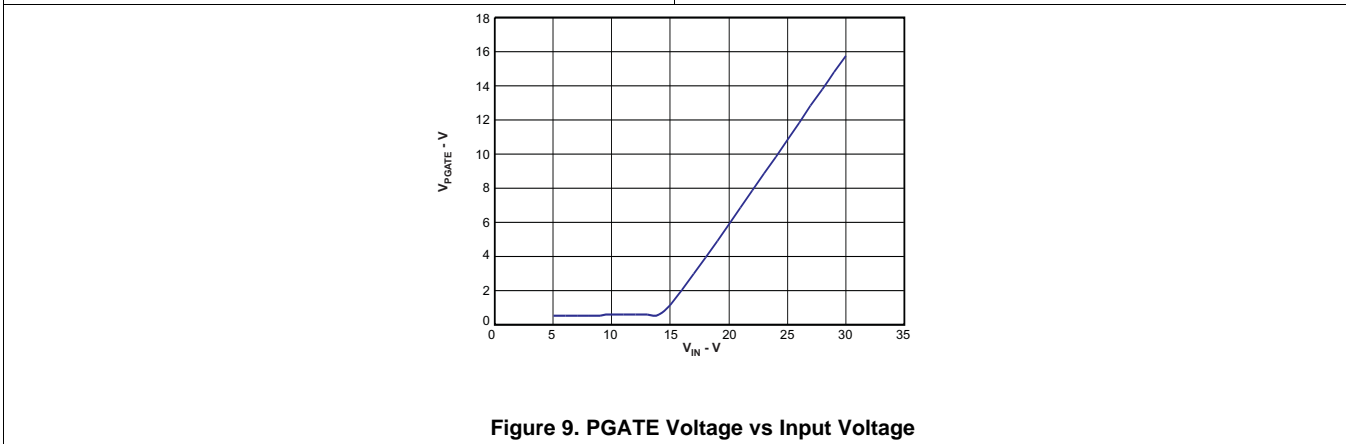


Figure 9. PGATE Voltage vs Input Voltage

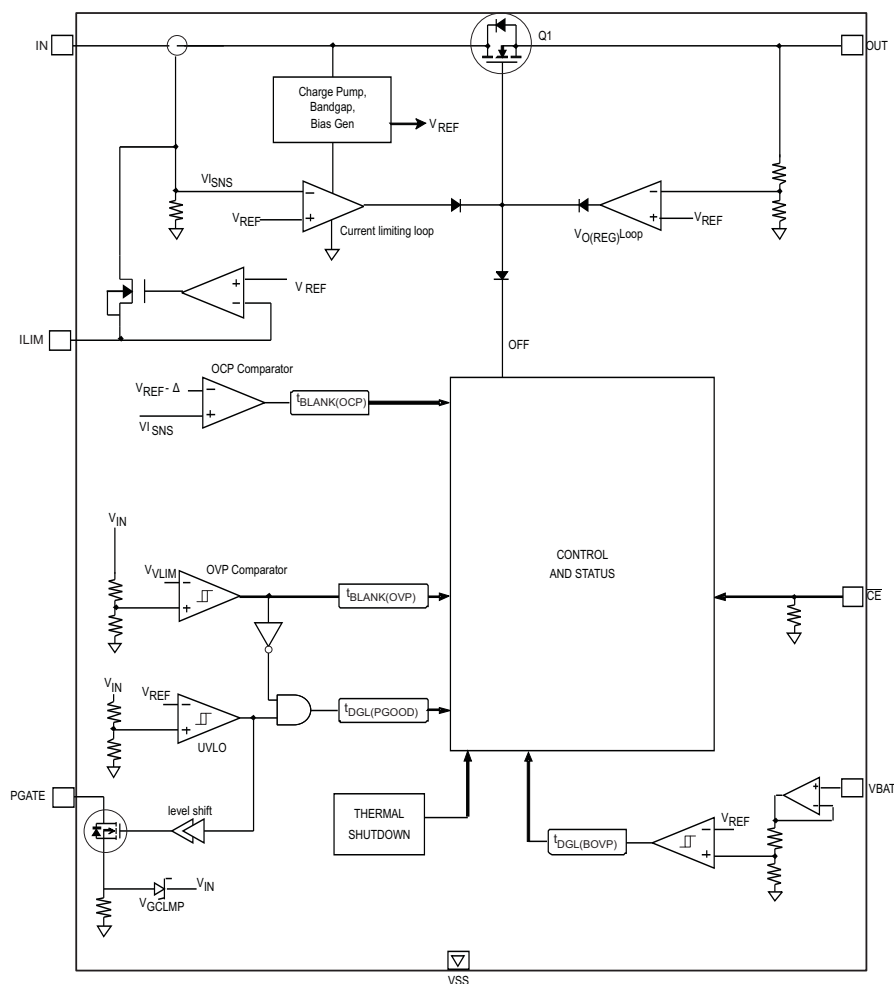
## 8 Detailed Description

### 8.1 Overview

The bq24308 device is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the current to a safe value for a blanking duration before turning the switch off. Additionally, the device also monitors its own die temperature and switches off if it becomes too hot.

The input and overcurrent threshold is user-programmable. The device can be controlled by a processor using the CE pin.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Input Overvoltage Protection

The bq24308 device integrates an input overvoltage protection feature to protect downstream devices from faulty input sources. If the input voltage rises above  $V_{OVP}$ , the internal FET Q1 is turned off, removing power from the circuit. As shown in [Figure 16](#) to [Figure 17](#), the response is very rapid, with the FET turning off in less than a microsecond. When the input voltage returns below  $V_{OVP} - V_{hys(OVP)}$  (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of  $t_{ON(OVP)}$  to ensure that the input supply has stabilized. [Figure 18](#) shows the recovery from input OVP.

### 8.3.2 Input Overcurrent Protection

The device can supply load current up to  $I_{OCP}$  continuously. If the load current tries to exceed this threshold, the current limits  $I_{OCP}$  for a maximum duration of  $t_{BLANK(OCP)}$ . If the load current returns to less than  $I_{OCP}$  before  $t_{BLANK(OCP)}$  times out, the device continues to operate (see [Figure 19](#)). However, if the overcurrent situation persists for  $t_{BLANK(OCP)}$ , the FET Q1 is turned off for a duration of  $t_{REC(OCP)}$ . The FET is then turned on again and the current is monitored all over again (see [Figure 20](#) and [Figure 21](#)).

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly in an overcurrent fault condition, resulting in a "soft-stop", as shown in [Figure 22](#). The overcurrent threshold is programmed to a level greater than  $I_{OCP}$  by connecting a resistor  $R_{ILIM}$  from the ILIM pin to VSS. The programmed overcurrent threshold is given by the following equation:

$$I_{OCP(program)} = I_{OCP} + K_{ILIM} \div R_{ILIM} \quad (1)$$

### 8.3.3 Battery Overvoltage Protection

The battery overvoltage threshold  $BV_{OVP}$  is internally set to 4.35 V. If the battery voltage exceeds the  $BV_{OVP}$  threshold for longer than  $t_{DGL(BOVP)}$ , the FET Q1 is turned off (see [Figure 23](#)). This switch-off is also a soft-stop. The FET Q1 is turned ON (soft-start) once the battery voltage drops to  $BV_{OVP} - V_{HYS-BOVP}$ .

### 8.3.4 Thermal Protection

If the junction temperature of the device exceeds  $T_{J(OFF)}$ , FET Q1 is turned off. The FET is turned back on when the junction temperature falls below  $T_{J(OFF)} - T_{J(OFF-HYS)}$ .

### 8.3.5 Enable Function

The device has an enable pin, which can be used to enable or disable the device. When the  $\overline{CE}$  pin is driven high, the internal FET is turned off. When the  $\overline{CE}$  pin is low, the FET is turned on if other conditions are safe. The  $\overline{CE}$  pin has an internal pulldown resistor of 200 k $\Omega$  (typical) and can be left floating.

### 8.3.6 PGATE Output

The bq24308 contains an external PFET driver (PGATE) for reverse polarity protection. When used with an external P-Channel MOSFET, in addition to OVP, OCP, and Battery-OVP, the device offers protection against input reverse polarity up to  $-30$  V. When an input source with correct polarity is connected, the device first turns on due to current flow through the body-diode of the external FET. The PGATE pin then goes low, turning ON the external FET. For input voltages larger than  $V_{GCLMP}$ , the voltage on the PGATE pin is driven to  $V_{IN} - V_{GCLMP}$ . This ensures that the gate to source voltage seen by the external FET does not exceed  $-V_{GCLMP}$ .

## 8.4 Device Functional Modes

### 8.4.1 OPERATION Mode

The bq24308 device continuously monitors the input voltage, the input current, and the battery voltage. As long as the input voltage is less than  $V_{OVP}$ , the output voltage tracks the input voltage (less the drop caused by  $R_{DS(ON)}$  of Q1). During fault conditions, the internal FET is turned off and the output is isolated from the input source.

### 8.4.2 POWER-DOWN Mode

The device remains in POWER-DOWN mode when the input voltage at the IN pin is below the undervoltage lock-out threshold,  $V_{UVLO}$ . The FET Q1 (see [Functional Block Diagram](#)) connected between IN and OUT pins is off. See [Figure 10](#).

### 8.4.3 POWER-ON RESET Mode

The device resets all internal timers when the input voltage at the IN pin exceeds the UVLO threshold. The gate driver for the external P-FET is enabled. The device then waits for duration  $t_{DGL(PGOOD)}$  for the input voltage to stabilize. If, after  $t_{DGL(PGOOD)}$ , the input voltage and battery voltage are safe, FET Q1 is turned ON. The device has a soft-start feature to control the inrush current. This soft-start minimizes voltage ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). [Figure 14](#) shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, as shown in [Figure 15](#).

Device Functional Modes (continued)

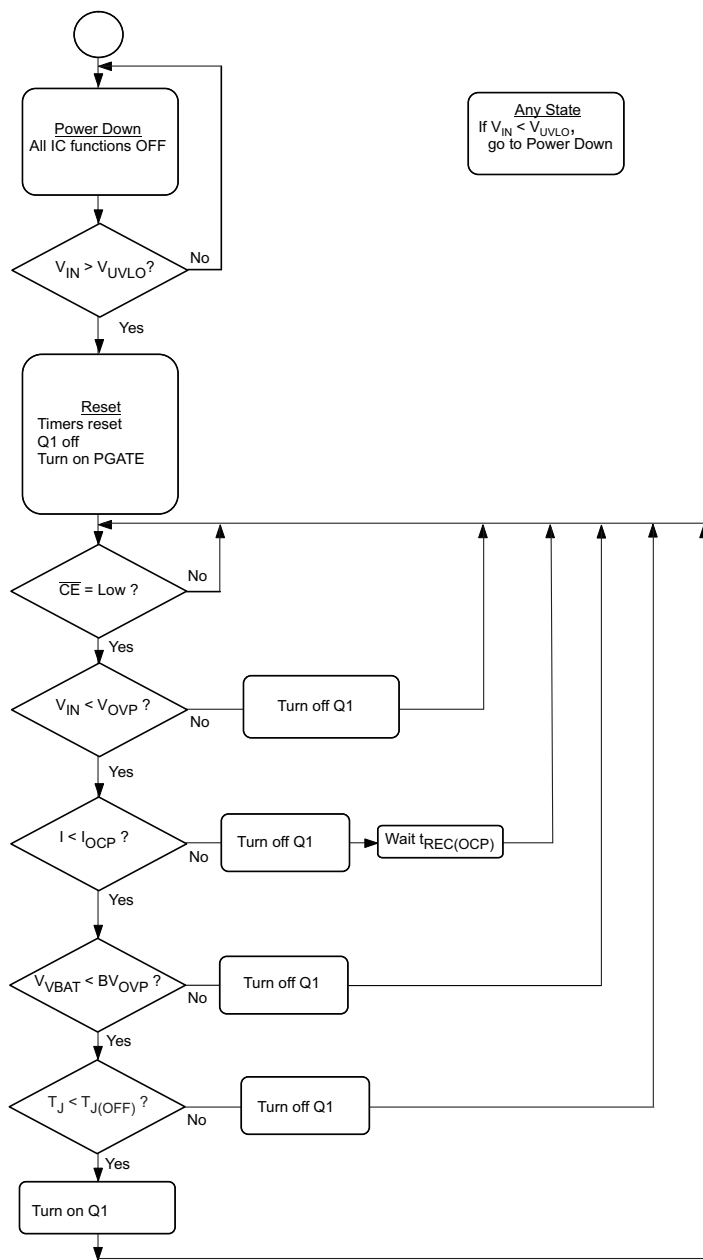


Figure 10. State Diagram

## 9 Application and Implementation

### NOTE

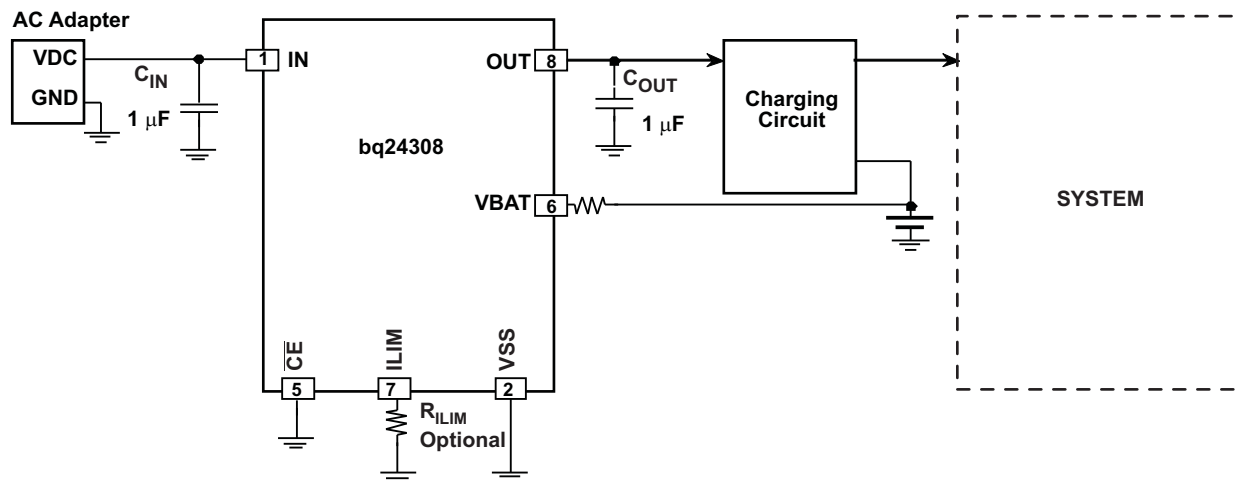
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The bq24308 device protects against overvoltage, overcurrent, and battery overvoltage events that occur due to faulty adapter or other input sources. If any of these faults occur, the bq24308 device isolates the downstream devices from the input source.

### 9.2 Typical Application

The typical values for an application are  $V_{OVP} = 6.3\text{ V}$ ,  $I_{OCP} = 700\text{ mA}$ , and  $BV_{OVP} = 4.35\text{ V}$ .



Terminal numbers shown are for the 2 x 2 DSG package.

**Figure 11. Typical Application Diagram**

#### 9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#).

**Table 1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|------------------|---------------|
| Supply Voltage   | 5 V           |
| INILIM           | 1 A           |

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Selection of $R_{BAT}$

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the device, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery in case of the failure of the device and can be hazardous. Connecting the VBAT pin through  $R_{BAT}$  prevents a large current from flowing into the battery in case of failure of the device. In the interests of safety,  $R_{BAT}$  should have a very high value. The problem with a large  $R_{BAT}$  is that the voltage drop across this resistor because of the VBAT bias current  $I_{VBAT}$  causes an error in the  $BV_{OVP}$  threshold. This error is over and above the tolerance on the nominal 4.35-V  $BV_{OVP}$  threshold.

Choosing  $R_{BAT}$  in the range from 100 k $\Omega$  to 470 k $\Omega$  is a good compromise. In the case of a device failure, with  $R_{BAT}$  equal to 100 k $\Omega$ , the maximum current flowing into the battery would be  $(30\text{ V} - 3\text{ V}) \div 100\text{ k}\Omega = 270\text{ }\mu\text{A}$ , which is low enough to be absorbed by the bias currents of the system components.  $R_{BAT}$  equal to 100 k $\Omega$  would result in a worst-case voltage drop of  $R_{BAT} \times I_{VBAT} = 1\text{ mV}$ . This is negligible compared to the internal tolerance of 50 mV on the  $BV_{OVP}$  threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

### 9.2.2.2 Selection of $R_{CE}$

The  $\overline{CE}$  pin can be used to enable and disable the device. If host control is not required, the  $\overline{CE}$  pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the  $\overline{CE}$  pin can be controlled by a host processor. As in the case of the VBAT pin (see previous discussion), the  $\overline{CE}$  pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum  $V_{OH}$  of the host GPIO pin less the drop across the resistor should be greater than  $V_{IH}$  of the bq24308 device's  $\overline{CE}$  pin. The drop across the resistor is given by  $R_{CE} \times I_{IH}$ .

### 9.2.2.3 Selection of Input and Output Bypass Capacitors

The input capacitor  $C_{IN}$  in Figure 12 and Figure 13 is for decoupling and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up.  $C_{IN}$  prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1  $\mu\text{F}$  be used at the input of the device. It should be located in close proximity to the IN pin.

$C_{OUT}$  in Figure 12 and Figure 13 is also important: If a very fast ( $< 1\text{ }\mu\text{s}$  rise-time) overvoltage transient occurs at the input, the current that charges  $C_{OUT}$  causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection.  $C_{OUT}$  should also be a ceramic capacitor of at least 1  $\mu\text{F}$ , located close to the OUT pin.  $C_{OUT}$  also serves as the input decoupling capacitor for the charging circuit downstream of the protection device.

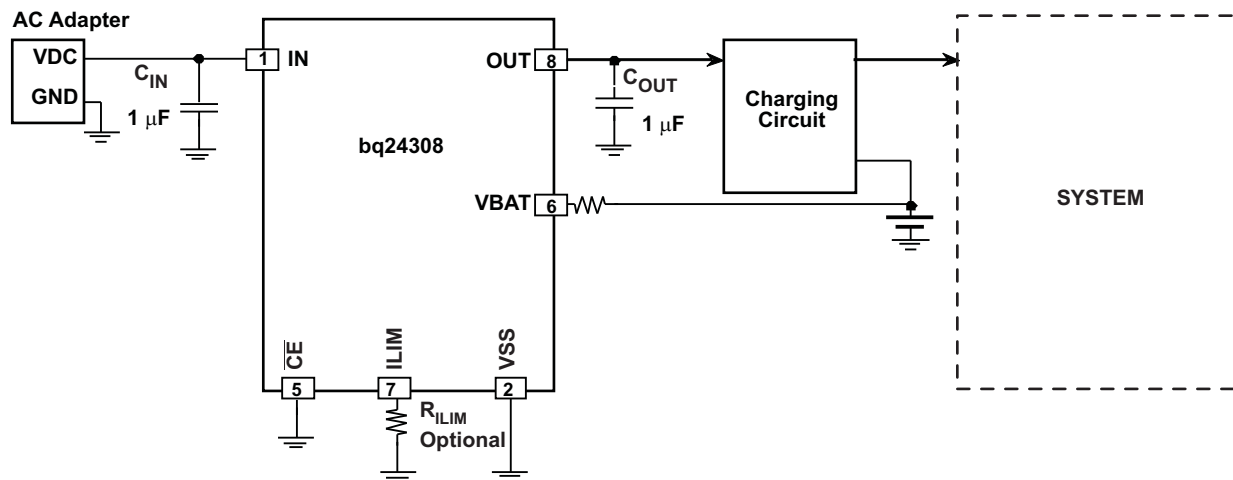
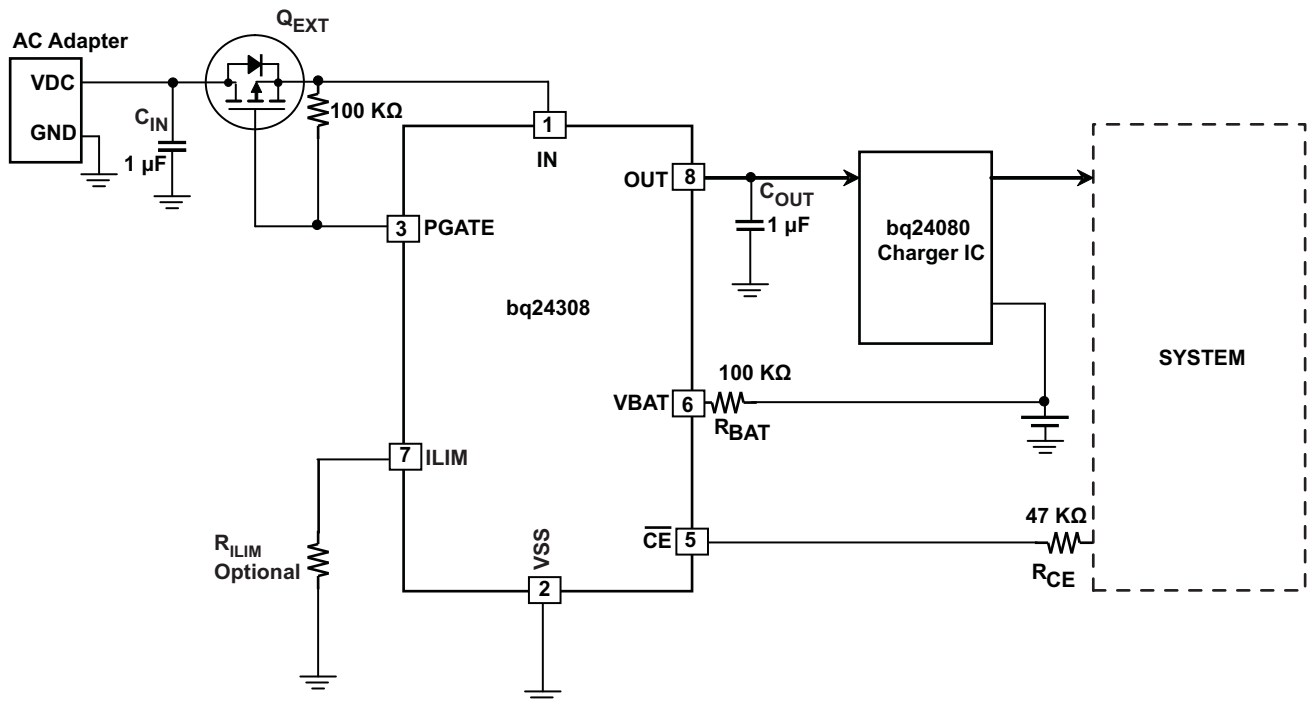


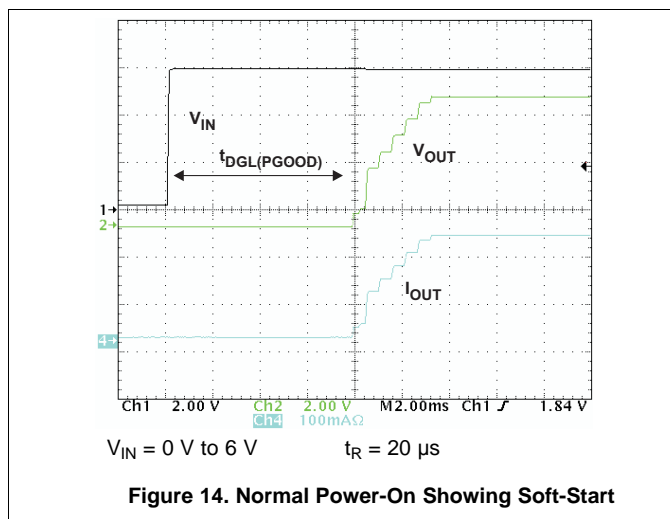
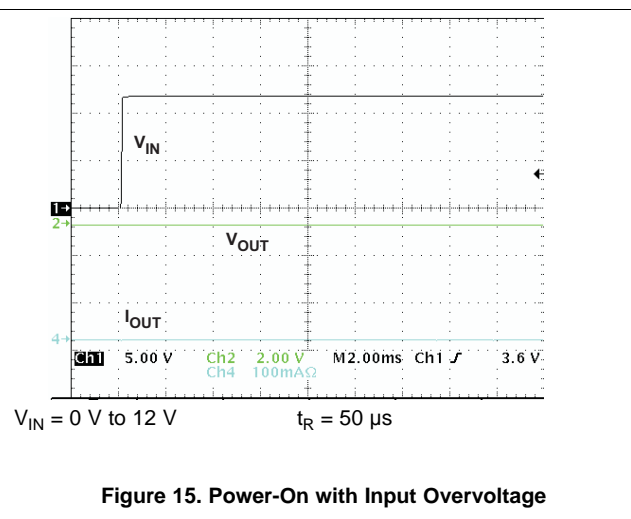
Figure 12. Overvoltage, Overcurrent, and Battery Overvoltage Protection

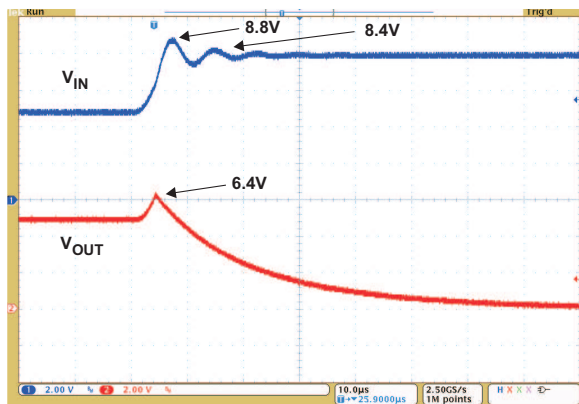

**Figure 13. OVP, OCP, BATOVP With Input Reverse-Polarity Protection**

### 9.2.2.4 Selection of the PGATE External MOSFET

The PGATE output drives the gate of an external MOSFET to protect the device from reverse polarity input voltages. The MOSFET must be sized to handle the expected current in the application. Additionally, the impedance of the MOSFET is in series with the internal FET of the bq24308, so that the overall acceptable system resistance must be taken into account. Ensure the MOSFET VDS maximum rating exceeds the worst-case expected reverse voltage in the application. The bq24308 withstands up to  $-30$  V, so a 30 V rating on the MOSFET is a good target. The maximum VGS of the MOSFET must be greater than  $-17$  V to ensure operation up to 30 V inputs.

### 9.2.3 Application Curves


**Figure 14. Normal Power-On Showing Soft-Start**

**Figure 15. Power-On with Input Overtolerance**



$V_{IN} = 5\text{ V to } 8\text{ V}$   $t_R = 3\ \mu\text{s}$

Figure 16. OVP Response for Input Step

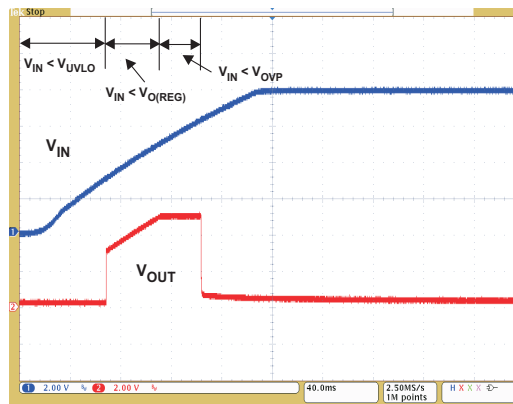
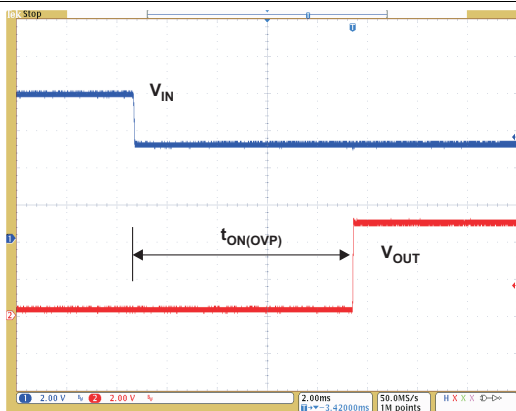


Figure 17. OUT Pin Response to Slow Input Ramp



$V_{IN} = 8\text{ V to } 5\text{ V}$   $t_F = 100\ \mu\text{s}$

Figure 18. Recovery from Input OVP

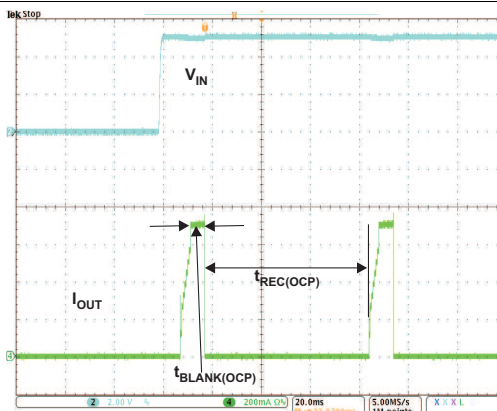
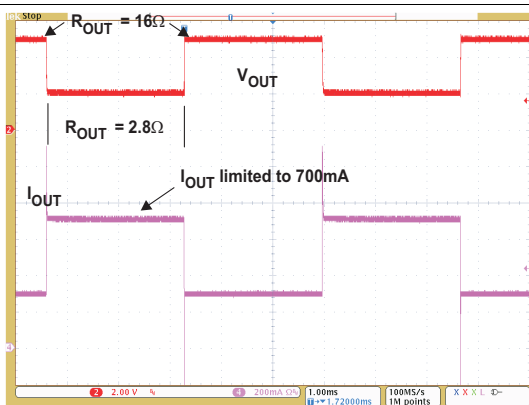
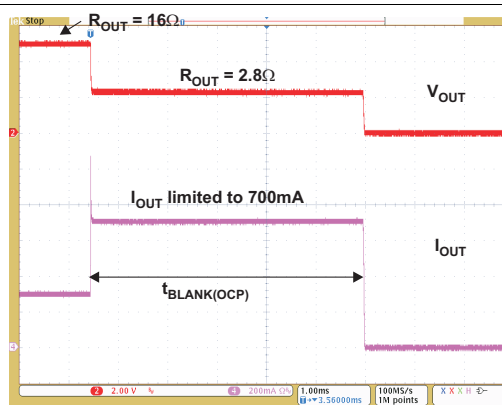


Figure 19. OCP, Powering up with OUT Pin Shorted to VSS



$R_{OUT}$  Switches from  $16\ \Omega$  to  $2.8\ \Omega$

Figure 20. OCP, Showing Current Limiting



$R_{OUT}$  Switches from  $16\ \Omega$  to  $2.8\ \Omega$

Figure 21. OCP, Showing Current Limiting and OCP Blanking

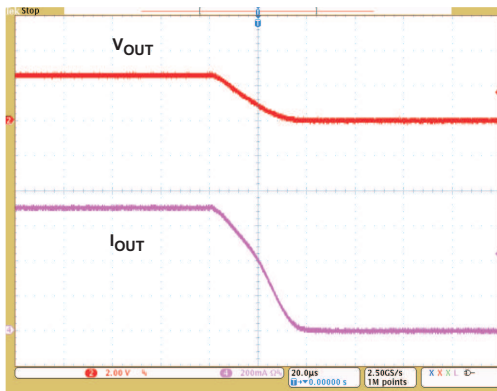
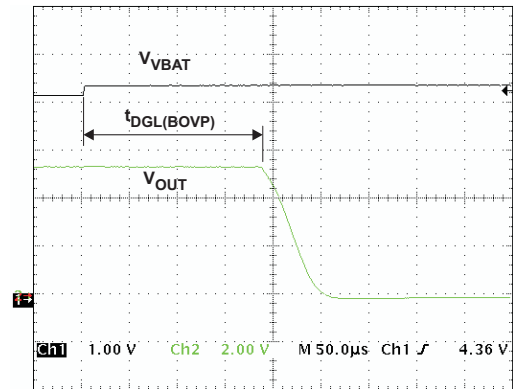


Figure 22. Zoom-in on Turnoff Region of Figure 21, Showing Soft-Stop



$V_{BAT}$  Steps from 4.3 V to 4.5 V.

Figure 23. Battery OVP,  $t_{DGL(BOVP)}$  and Soft-Stop

## 10 Power Supply Recommendations

The intention is for the bq24308 device to operate with 5-V adapters with a maximum current rating of 1.5 A. The device operates from sources from 3 V to 5.7 V. Outside of this range, the output is disconnected due to either UVLO or the OVP function.

## 11 Layout

### 11.1 Layout Guidelines

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this device. It must be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the high voltages. See [Figure 24](#).
- The device uses WSON packages with a thermal pad. For good thermal performance, the thermal pad must be thermally coupled with the PCB ground plane (GND). This requires a copper pad directly under the device. This copper pad must be connected to the ground plane with an array of thermal vias.
- $C_{IN}$  and  $C_{OUT}$  should be located close to the device. Other components like  $R_{ILIM}$  (optional) and  $R_{BAT}$  must also be located close to the device.

### 11.2 Layout Example

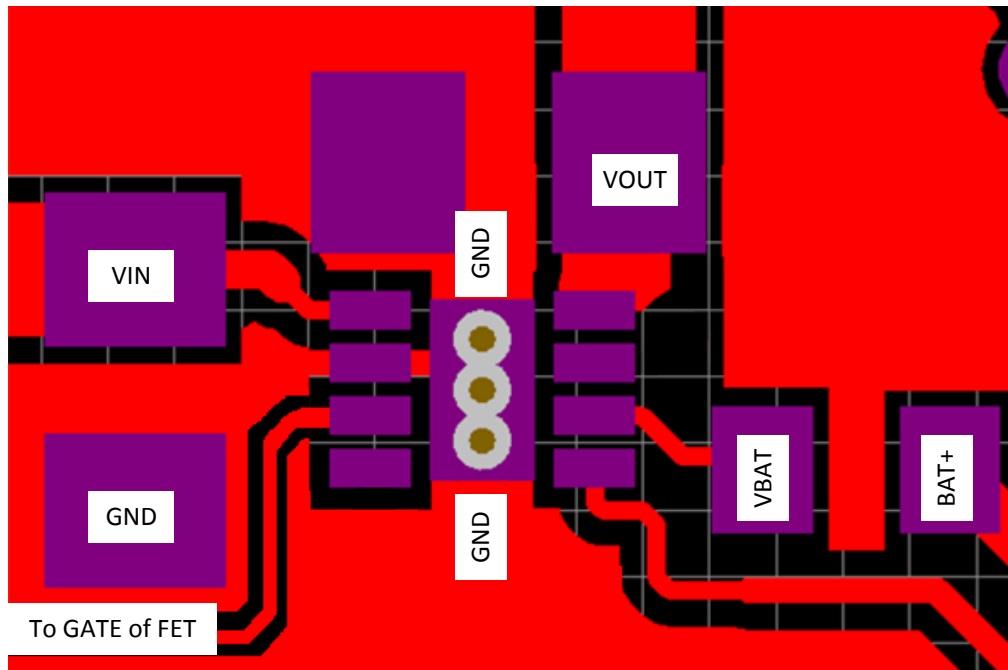


Figure 24. Layout Example Recommendation

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.  
 Bluetooth is a trademark of Bluetooth SIG, Inc..  
 All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| BQ24308DSGR      | ACTIVE        | WSON         | DSG             | 8    | 3000        | Green (RoHS & no Sb/Br) | Call TI   NIPDAU        | Level-2-260C-1 YEAR  | 0 to 125     | DAS                     | <a href="#">Samples</a> |
| BQ24308DSGT      | ACTIVE        | WSON         | DSG             | 8    | 250         | Green (RoHS & no Sb/Br) | Call TI   NIPDAU        | Level-2-260C-1 YEAR  | 0 to 125     | DAS                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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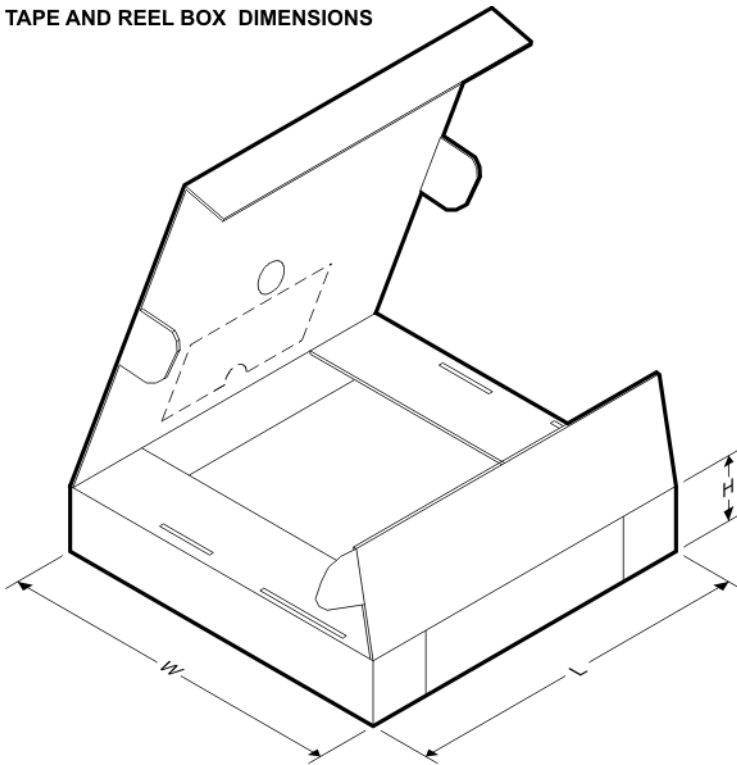
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ24308DSGR | WSON         | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| BQ24308DSGT | WSON         | DSG             | 8    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ24308DSGR | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| BQ24308DSGT | WSON         | DSG             | 8    | 250  | 210.0       | 185.0      | 35.0        |

## GENERIC PACKAGE VIEW

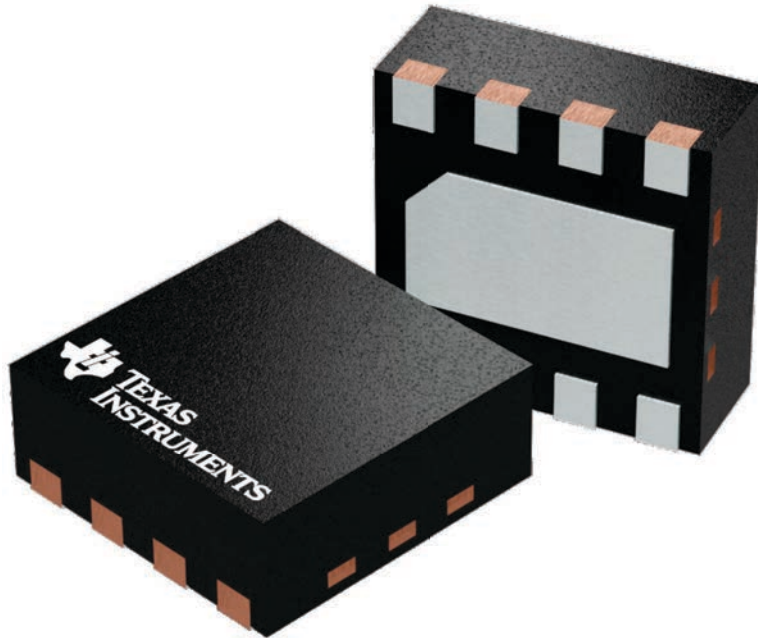
**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

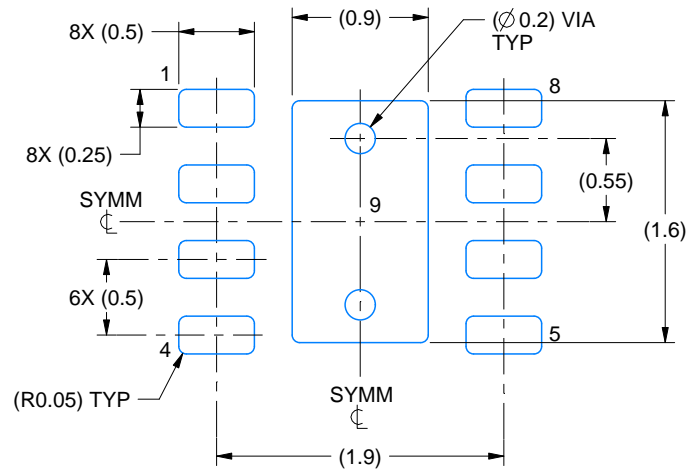


# EXAMPLE BOARD LAYOUT

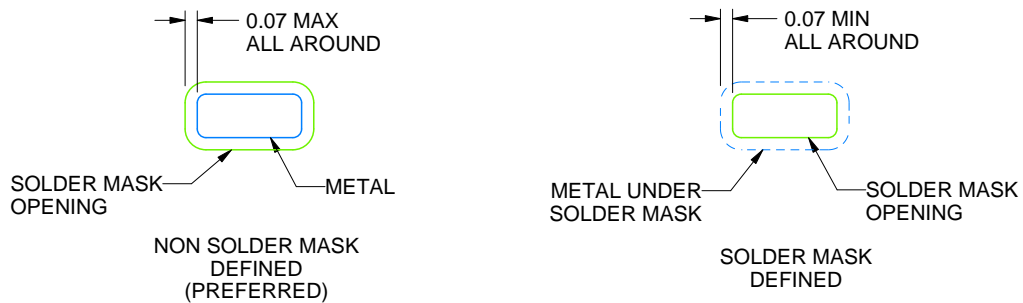
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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