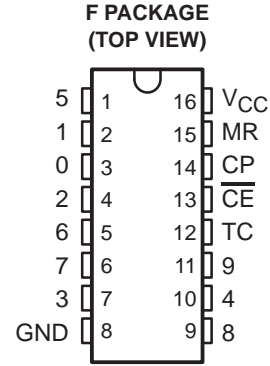


CD54HC4017 DECADE COUNTER/DIVIDER WITH TEN DECODED OUTPUTS

SGDS011 – MAY 1999

- 2-V to 6-V Operation
- Fully Static Operation
- Buffered Inputs
- Common Reset
- Positive-Edge Clocking
- Balanced Propagation Delay and Transition Times
- High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{ V}$
- Packaged in Ceramic (F) DIP Package and Also Available in Chip Form (H)



description

The CD54HC4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each decoded output normally is low and sequentially goes high on the low-to-high transition of the clock (CP) input. Each output stays high for one clock period of the ten-clock-period cycle. The terminal count (TC) output transitions low to high after output ten (9) goes low, and can be used in conjunction with the clock enable (\overline{CE}) input to cascade several stages. \overline{CE} disables counting when in the high state. The master reset (MR) input, when taken high, sets all the decoded outputs, except 0, to low.

The CD54HC4017 is characterized for operation over the full military temperature range of -55°C to 125°C .

FUNCTION TABLE

INPUTS			OUTPUT STATE†
CP	\overline{CE}	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

† If $n < 5$, TC = H; otherwise, TC = L.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

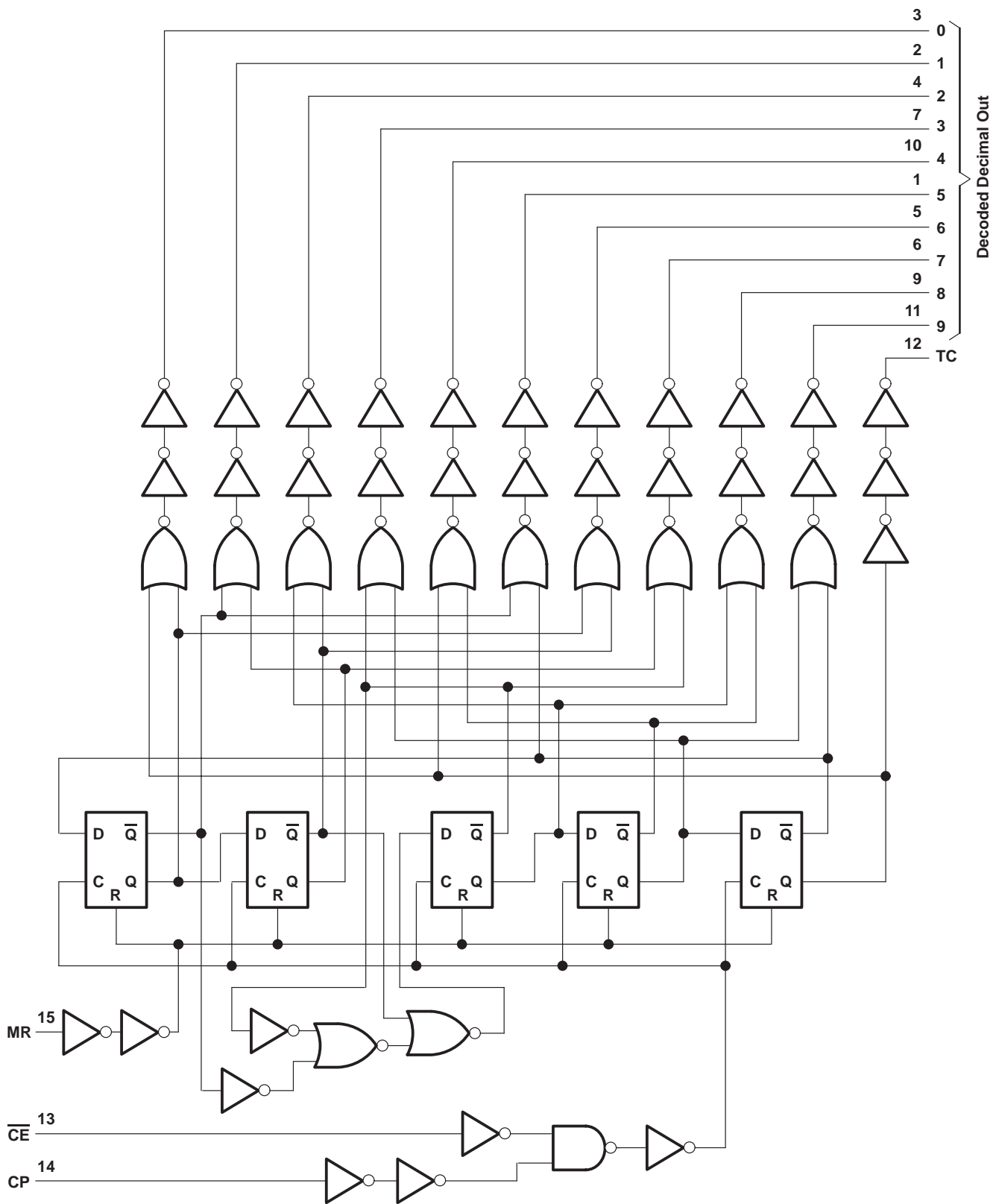
**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

CD54HC4017
DECADE COUNTER/DIVIDER
WITH TEN DECODED OUTPUTS
 SGDS011 – MAY 1999

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$)	±20 mA
Continuous output current, each output pin, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
V_{CC} or ground current, I_{CC}	±50 mA
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating (see Note 1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 4.5$ V	3.15	
		$V_{CC} = 6$ V	4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0 0.5	V
		$V_{CC} = 4.5$ V	0 1.35	
		$V_{CC} = 6$ V	0 1.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V	0 1000	ns
		$V_{CC} = 4.5$ V	0 500	
		$V_{CC} = 6$ V	0 400	
T_A	Operating free-air temperature	–55	125	°C

NOTE 1: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
					MIN	MAX			
V_{OH}	CMOS loads	$V_I = V_{IH}$ or V_{IL} ,	$I_{OH} = -0.02$ mA	2 V	1.9	1.9	V		
				4.5 V	4.4	4.4			
				6 V	5.9	5.9			
	TTL loads	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -4$ mA	4.5 V	3.98	3.7			
$I_{OH} = -5.2$ mA	6 V		5.48	5.2					
V_{OL}	CMOS loads	$V_I = V_{IH}$ or V_{IL} ,	$I_{OL} = 0.02$ mA	2 V	0.1	0.1	V		
				4.5 V	0.1	0.1			
				6 V	0.1	0.1			
	TTL loads	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 4$ mA	4.5 V	0.26	0.4			
$I_{OL} = 5.2$ mA	6 V		0.26	0.4					
I_I		$V_I = V_{CC}$ or 0		6 V	±100	±1000	nA		
I_{CC}		$V_I = V_{CC}$ or 0,	$I_O = 0$	6 V	8	160	µA		
C_i				2 V to 6 V	10	10	pF		

CD54HC4017
DECADE COUNTER/DIVIDER
WITH TEN DECODED OUTPUTS

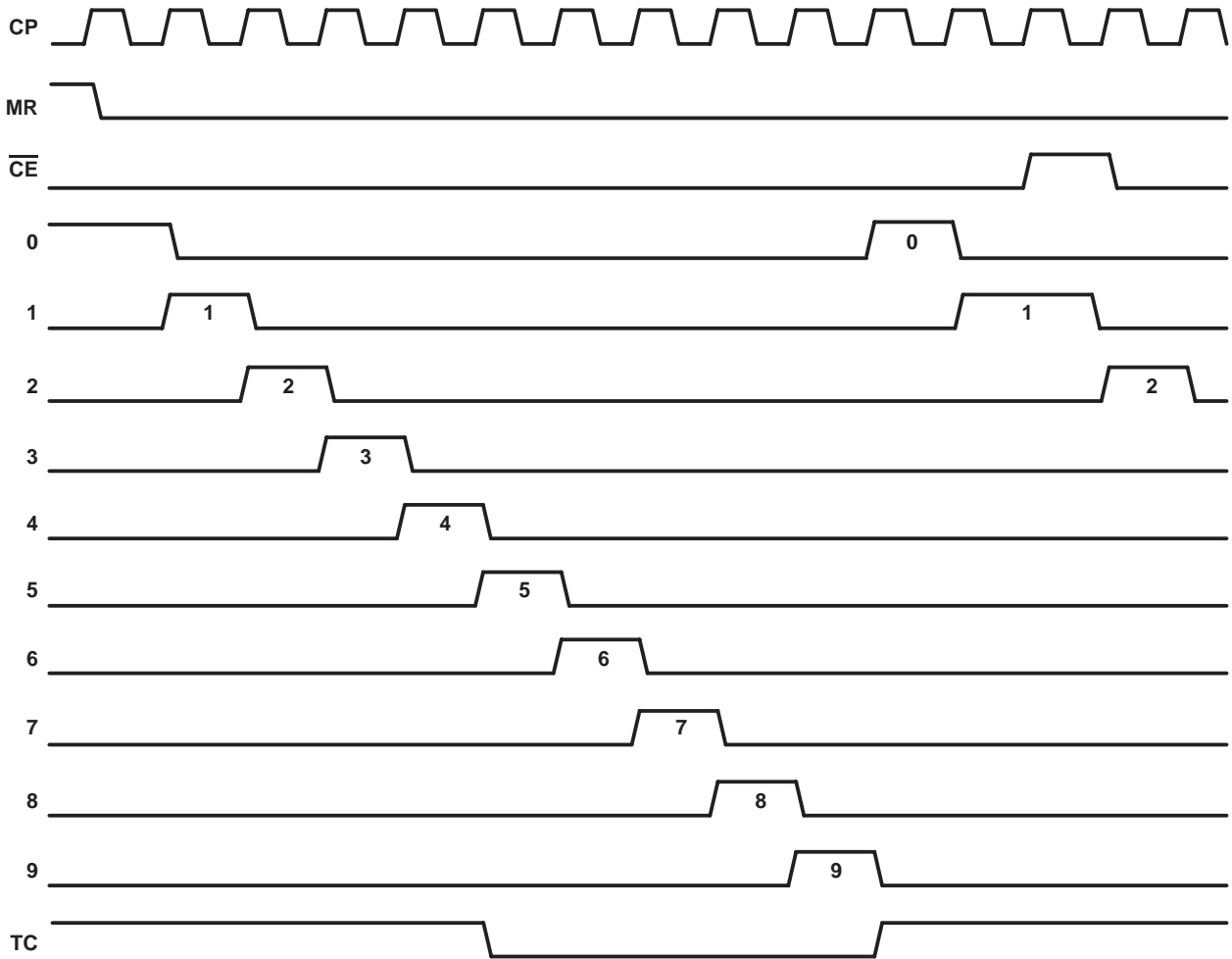
SGDS011 – MAY 1999

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V _{CC}	T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f _{clock}	Maximum clock frequency	2 V	6		4		MHz
		4.5 V	30		20		
		6 V	35		23		
t _w	Pulse duration	CP	2 V	80	120		ns
			4.5 V	16	24		
			6 V	14	20		
		MR	2 V	80	120		
			4.5 V	16	24		
			6 V	14	20		
t _{su}	Setup time, \overline{CE} to CP	2 V	75	110		ns	
		4.5 V	15	22			
		6 V	13	19			
t _h	Hold time, \overline{CE} to CP	2 V	0	0		ns	
		4.5 V	0	0			
		6 V	0	0			
t _{rem}	Removal time, MR	2 V	5	5		ns	
		4.5 V	5	5			
		6 V	5	5			



timing requirements



CD54HC4017
DECADE COUNTER/DIVIDER
WITH TEN DECODED OUTPUTS

SGDS011 – MAY 1999

switching characteristics, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Figures 1 and 2)

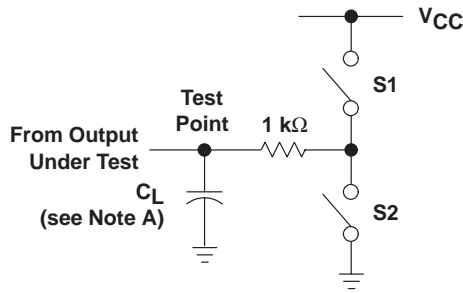
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C		T _A = -55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	
f _{max}			2 V	6		4		MHz
			4.5 V	20		20		
			6 V	35		23		
t _{pd}	CP	Any output	2 V	230		345		ns
			4.5 V	46		69		
			6 V	39		59		
t _{pd}		TC	2 V	230		345		ns
			4.5 V	46		69		
			6 V	39		59		
t _{pd}	$\overline{\text{CE}}$	Any output	2 V	250		375		ns
			4.5 V	50		75		
			6 V	43		64		
t _{pd}		TC	2 V	250		375		ns
			4.5 V	50		75		
			6 V	43		64		
t _{pd}	MR	Any output	2 V	230		345		ns
			4.5 V	46		69		
			6 V	39		59		
t _{pd}		TC	2 V	230		345		ns
			4.5 V	46		69		
			6 V	39		59		

operating characteristics

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load	39	pF

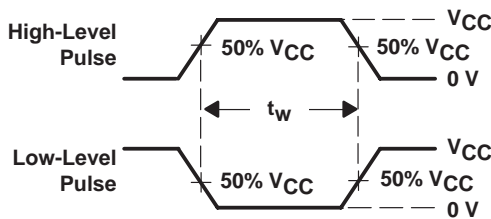


PARAMETER MEASUREMENT INFORMATION

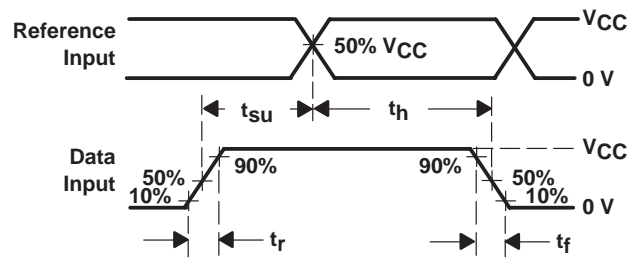


LOAD CIRCUIT

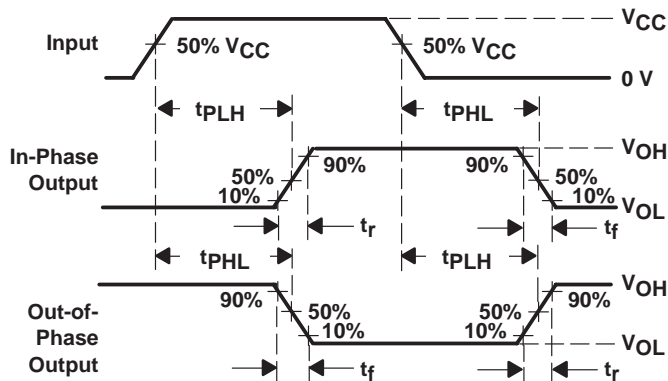
PARAMETER		S1	S2
t_{en}	tpZH	Open	Closed
	tpZL	Closed	Open
t_{dis}	tPHZ	Open	Closed
	tPLZ	Closed	Open
t_{pd} or t_t		Open	Open



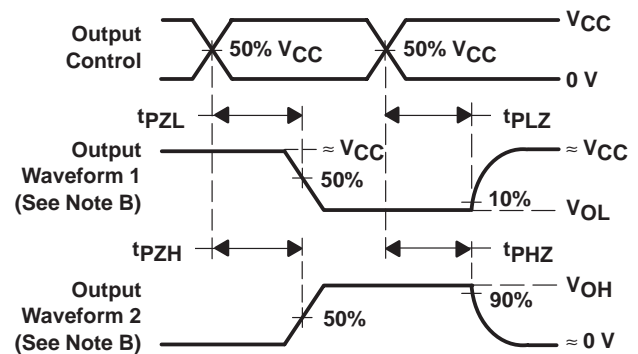
VOLTAGE WAVEFORMS
 PULSE DURATIONS



VOLTAGE WAVEFORMS
 SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

CD54HC4017
DECADE COUNTER/DIVIDER
WITH TEN DECODED OUTPUTS

SGDS011 – MAY 1999

PARAMETER MEASUREMENT INFORMATION

INPUT LEVEL	V_{CC}
V_S	$0.5 V_{CC}$

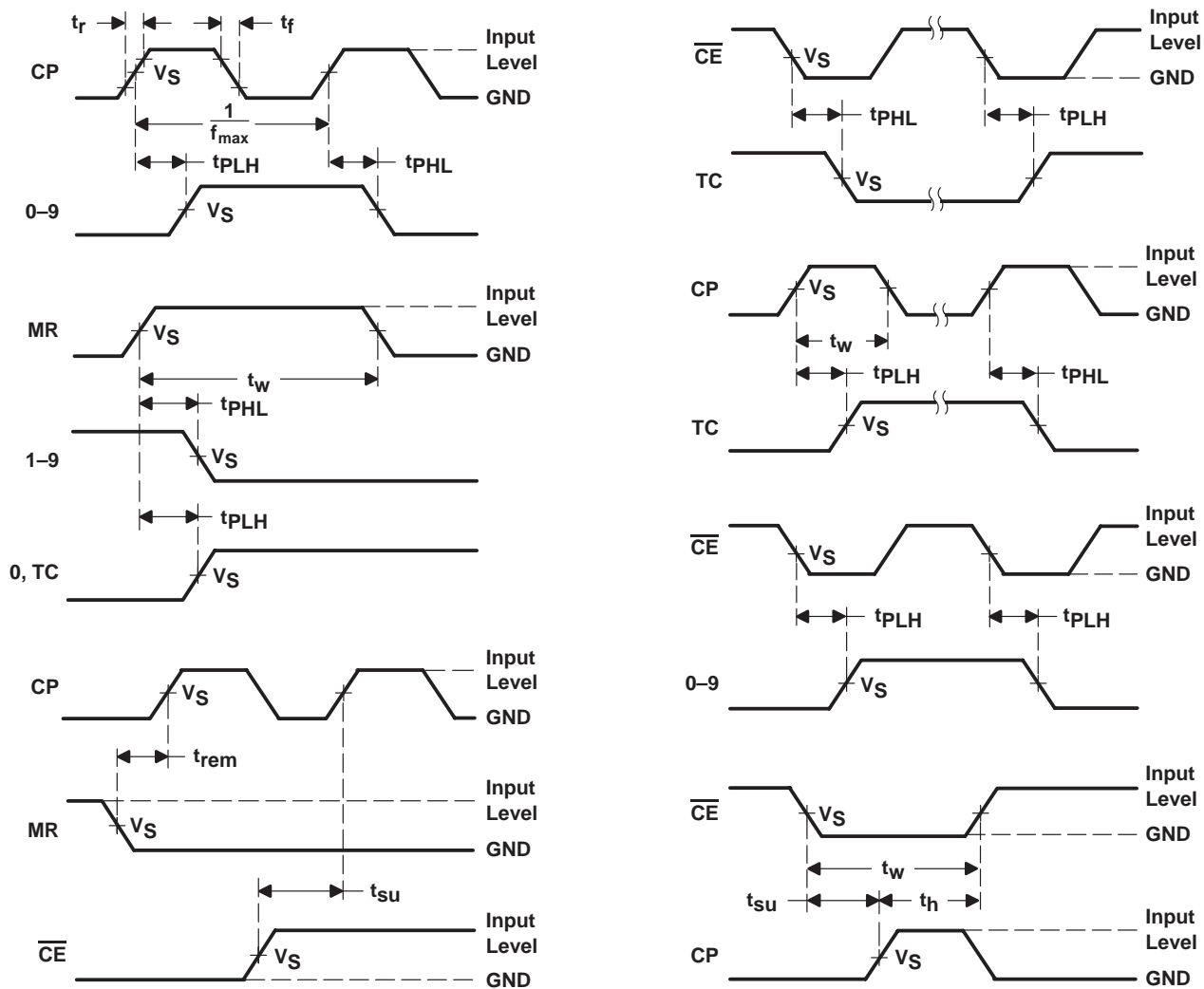


Figure 2. Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8601101EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8601101EA CD54HC4017F3A	Samples
CD54HC4017F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8601101EA CD54HC4017F3A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4017 :

- Catalog: [CD74HC4017](#)
- Automotive: [CD74HC4017-Q1](#)
- Enhanced Product: [CD74HC4017-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated