

## DS10CP152 1.5 Gbps 2X2 LVDS Crosspoint Switch

Check for Samples: [DS10CP152](#)

### FEATURES

- DC - 1.5 Gbps Low Jitter, Low Skew, Low Power Operation
- Pin Configurable, Fully Differential, Non-Blocking Architecture
- Wide Input Common Mode Voltage Range Allows DC-Coupled Interface to LVDS, CML and LVPECL Drivers
- On-chip 100Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count and Minimizes Board Space
- 7 kV ESD on LVDS I/O Pins Protects Adjoining Components
- Small SOIC-16 Space Saving Package

### DESCRIPTION

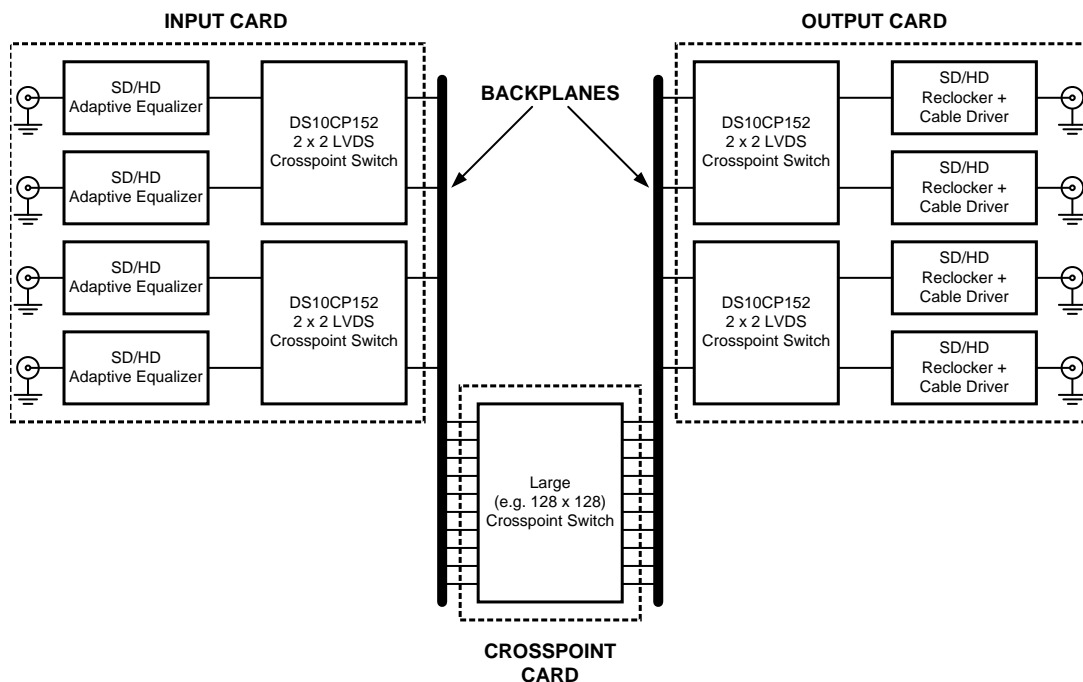
The DS10CP152 is a 1.5 Gbps 2x2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.

### APPLICATIONS

- High-Speed Channel Select Applications
- Clock and Data Buffering and Muxing
- SD/HD SDI Routers

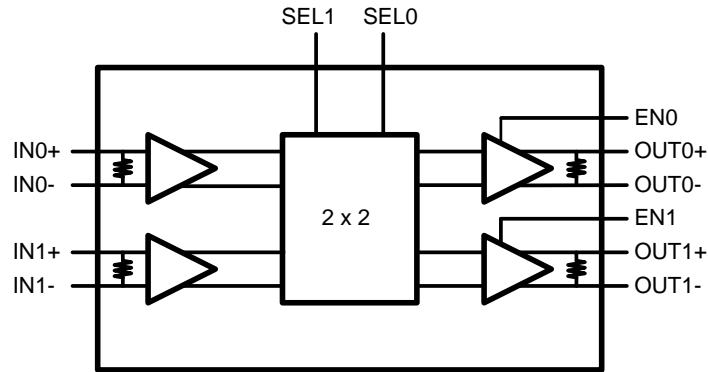
### Typical Application



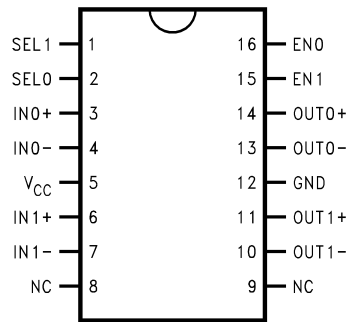
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

**Block Diagram**



**Connection Diagram**



**DS10CP152 Pin Diagram**  
See Package Number D (R-PDSO-G16)

**PIN DESCRIPTIONS**

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0-, IN1+, IN1-	3, 4, 6, 7	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-	14, 13, 11, 10	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
SEL1, SEL0	1, 2	I, LVCMOS	Switch configuration pins.
EN0, EN1	16, 15	I, LVCMOS	Output enable pins.
NC	8, 9	NC	"NO CONNECT" pins.
VDD	5	Power	Power supply pin.
GND	12	Power	Ground pin.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)(2)</sup>

Supply Voltage	-0.3V to +4V
LVCMOS Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Input Voltage	-0.3V to +4V
Differential Input Voltage  VID	1V
LVDS Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Differential Output Voltage	0V to 1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
D Package	1.72W
Derate D Package	13.75 mW/°C above +25°C
Package Thermal Resistance	
$\theta_{JA}$	+72.7°C/W
$\theta_{JC}$	+41.2°C/W
ESD Susceptibility	
HBM <sup>(3)</sup>	≥7 kV
MM <sup>(4)</sup>	≥250V
CDM <sup>(5)</sup>	≥1250V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

### Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Receiver Differential Input Voltage ( $V_{ID}$ )	0		1	V
Operating Free Air Temperature ( $T_A$ )	-40	+25	+85	°C

## DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. <sup>(1)(2)(3)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LVCMOS DC SPECIFICATIONS</b>						
V <sub>IH</sub>	High Level Input Voltage		2.0		V <sub>DD</sub>	V
V <sub>IL</sub>	Low Level Input Voltage		GND		0.8	V
I <sub>IH</sub>	High Level Input Current	V <sub>IN</sub> = 3.6V V <sub>CC</sub> = 3.6V	40	175	250	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>IN</sub> = GND V <sub>CC</sub> = 3.6V		±1	±10	μA
V <sub>CL</sub>	Input Clamp Voltage	I <sub>CL</sub> = -18 mA, V <sub>CC</sub> = 0V		-0.9	-1.5	V
<b>LVDS INPUT DC SPECIFICATIONS</b>						
V <sub>ID</sub>	Input Differential Voltage		0		1	V
V <sub>TH</sub>	Differential Input High Threshold	V <sub>CM</sub> = +0.05V or V <sub>CC</sub> -0.05V		0	+100	mV
V <sub>TL</sub>	Differential Input Low Threshold		-100	0		mV
V <sub>CMR</sub>	Common Mode Voltage Range	V <sub>ID</sub> = 100 mV	0.05		V <sub>CC</sub> - 0.05	V
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = 3.6V or 0V V <sub>CC</sub> = 3.6V or 0V		±1	±10	μA
C <sub>IN</sub>	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R <sub>IN</sub>	Input Termination Resistor	Between IN+ and IN-		100		Ω
<b>LVDS OUTPUT DC SPECIFICATIONS</b>						
V <sub>OD</sub>	Differential Output Voltage		250	350	450	mV
ΔV <sub>OD</sub>	Change in Magnitude of V <sub>OD</sub> for Complimentary Output States	R <sub>L</sub> = 100Ω	-35		35	mV
V <sub>OS</sub>	Offset Voltage		1.05	1.2	1.375	V
ΔV <sub>OS</sub>	Change in Magnitude of V <sub>OS</sub> for Complimentary Output States	R <sub>L</sub> = 100Ω	-35		35	mV
I <sub>OS</sub>	Output Short Circuit Current <sup>(4)</sup>	OUT to GND		-23	-55	mA
		OUT to V <sub>CC</sub>		8	55	mA
C <sub>OUT</sub>	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R <sub>OUT</sub>	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
<b>SUPPLY CURRENT</b>						
I <sub>CC</sub>	Supply Current	EN0 = EN1 = H		58	70	mA
I <sub>CCZ</sub>	Outputs Powered Down Supply Current	EN0 = EN1 = L		25	30	mA

- (1) The [Electrical Characteristics](#) tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V<sub>OD</sub> and ΔV<sub>OD</sub>.
- (3) Typical values represent most likely parametric norms for V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Output short circuit current (I<sub>OS</sub>) is specified as magnitude only, minus sign indicates direction only.

## AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. <sup>(1)(2)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>LVDS OUTPUT AC SPECIFICATIONS</b>							
$t_{PLHD}$	Differential Propagation Delay Low to High <sup>(3)</sup>	$R_L = 100\Omega$		440	650	ps	
$t_{PHLD}$	Differential Propagation Delay High to Low <sup>(3)</sup>			400	650	ps	
$t_{SKD1}$	Pulse Skew $ t_{PLHD} - t_{PHLD} $ <sup>(3) (4)</sup>			40	120	ps	
$t_{SKD2}$	Channel to Channel Skew <sup>(3)(5)</sup>			25	60	ps	
$t_{SKD3}$	Part to Part Skew <sup>(3)(6)</sup>			45	190	ps	
$t_{LHT}$	Rise Time <sup>(3)</sup>	$R_L = 100\Omega$		170	350	ps	
$t_{HLT}$	Fall Time <sup>(3)</sup>			170	350	ps	
$t_{ON}$	Output Enable Time			5	20	$\mu$ s	
$t_{OFF}$	Output Disable Time			3	12	ns	
$t_{SEL}$	Select Time			3	12	ns	
<b>JITTER PERFORMANCE <sup>(3)</sup></b>							
$t_{RJ1}$	Random Jitter (RMS Value) <sup>(7)</sup>	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ Clock (RZ)	135 MHz		0.5	1.2	ps
$t_{RJ2}$			311 MHz		0.5	1.2	ps
$t_{RJ3}$			503 MHz		0.5	1.2	ps
$t_{RJ4}$			750 MHz		0.5	1.2	ps
$t_{DJ1}$	Deterministic Jitter (Peak-to-Peak Value) <sup>(8)</sup>	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ Clock (RZ)	270 Mbps		9	38	ps
$t_{DJ2}$			622 Mbps		7	36	ps
$t_{DJ3}$			1.06 Gbps		7	34	ps
$t_{DJ4}$			1.5 Gbps		9	35	ps
$t_{TJ1}$	Total Jitter (Peak to Peak Value) <sup>(9)</sup>	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ PRBS-23 (NRZ)	270 Mbps		0.01	0.03	UI <sub>P-P</sub>
$t_{TJ2}$			622 Mbps		0.01	0.04	UI <sub>P-P</sub>
$t_{TJ3}$			1.06 Gbps		0.01	0.05	UI <sub>P-P</sub>
$t_{TJ4}$			1.5 Gbps		0.01	0.07	UI <sub>P-P</sub>

- (1) The [Electrical Characteristics](#) tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms for  $V_{CC} = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (3) Specification is ensured by characterization and is not tested in production.
- (4)  $t_{SKD1}$ ,  $|t_{PLHD} - t_{PHLD}|$ , Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (5)  $t_{SKD2}$ , Channel to Channel Skew, is the difference in propagation delay ( $t_{PLHD}$  or  $t_{PHLD}$ ) among all output channels in Broadcast mode (any one input to all outputs).
- (6)  $t_{SKD3}$ , Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.
- (7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
- (8) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
- (9) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

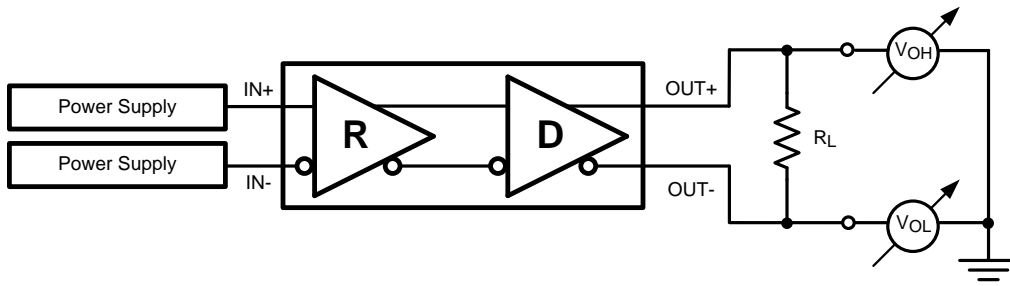


Figure 1.

AC Test Circuits and Timing Diagrams

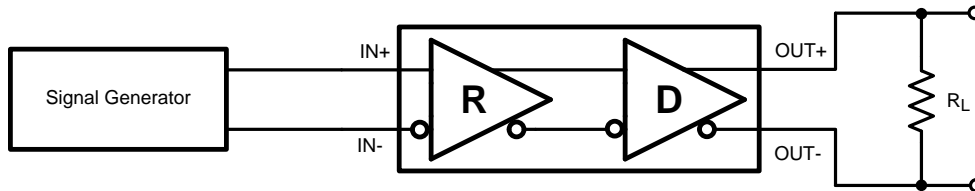


Figure 2.

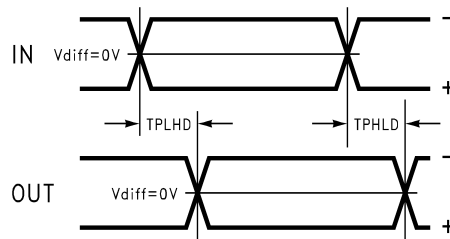


Figure 3.

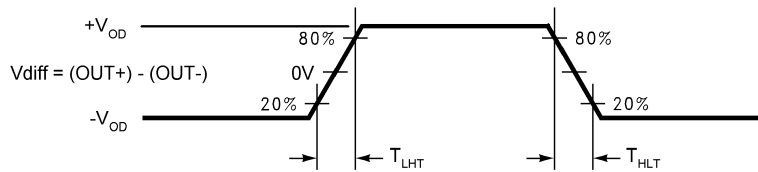


Figure 4.

### FUNCTIONAL DESCRIPTION

The DS10CP152 is a 1.5 Gbps 2x2 LVDS digital crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables.

**Table 1. Switch Configuration Truth Table**

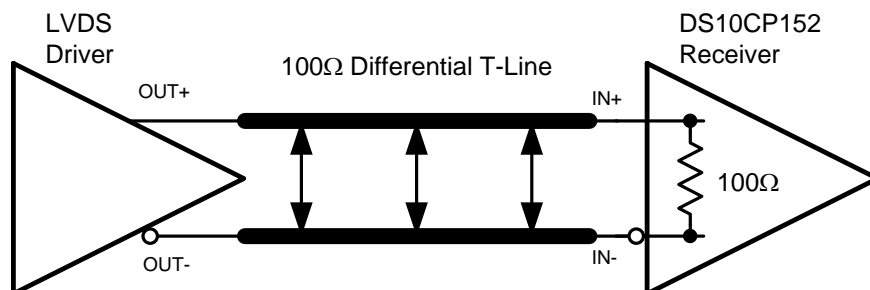
SEL1	SEL0	OUT1	OUT0
0	0	IN0	IN0
0	1	IN0	IN1
1	0	IN1	IN0
1	1	IN1	IN1

**Table 2. Output Enable Truth Table**

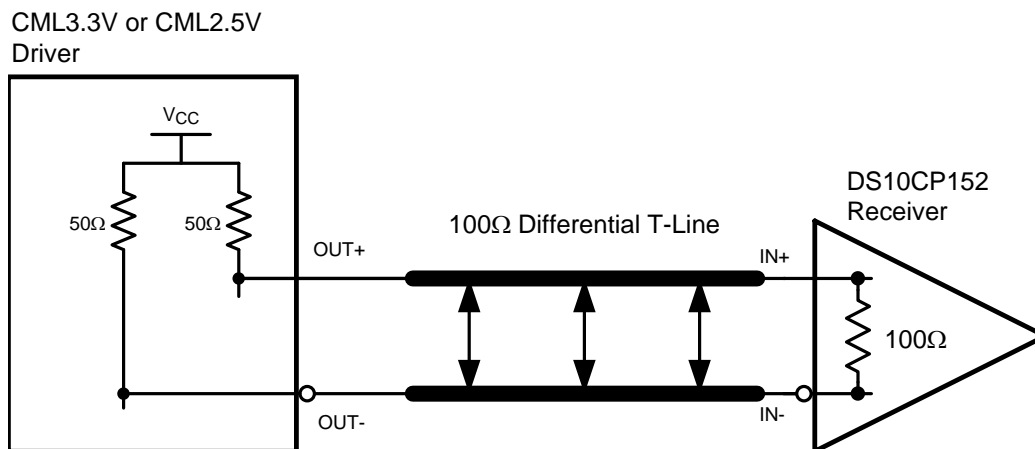
EN1	EN0	OUT1	OUT0
0	0	Disabled	Disabled
0	1	Disabled	Enabled
1	0	Enabled	Disabled
1	1	Enabled	Enabled

### Input Interfacing

The DS10CP152 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS10CP152 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS10CP152 inputs are internally terminated with a 100Ω resistor.



**Figure 5. Typical LVDS Driver DC-Coupled Interface to an DS10CP152 Input**



**Figure 6. Typical CML Driver DC-Coupled Interface to an DS10CP152 Input**

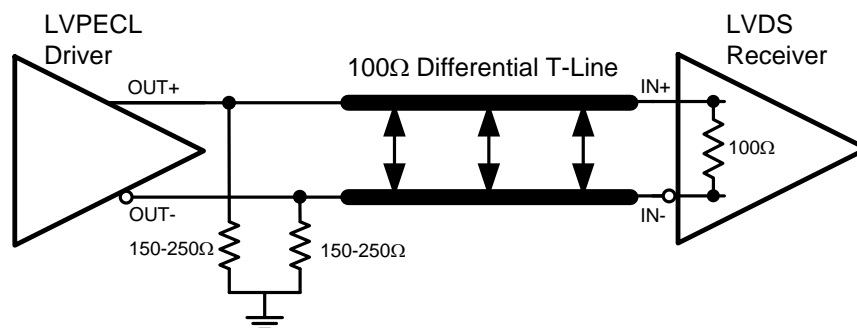


Figure 7. Typical LVPECL Driver DC-Coupled Interface to an DS10CP152 Input

### Output Interfacing

The DS10CP152 outputs signals compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

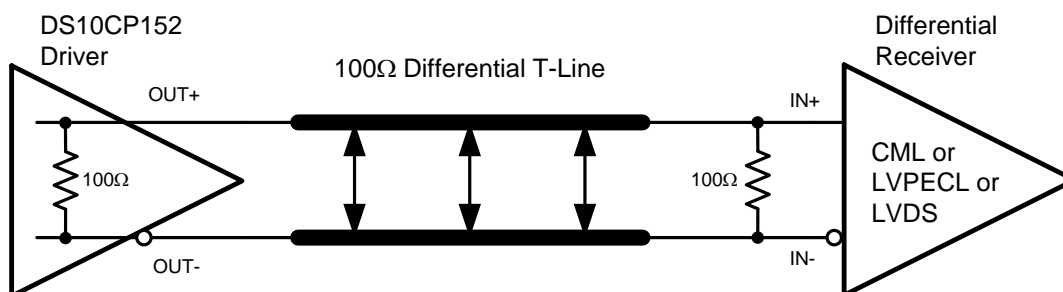


Figure 8. Typical DS10CP152 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance Characteristics

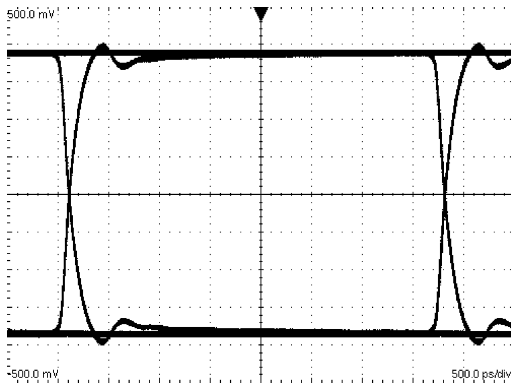


Figure 9. A 270 Mbps NRZ PRBS-7 After 2" Differential FR-4 Stripline  
V:100 mV / DIV, H:500 ps / DIV

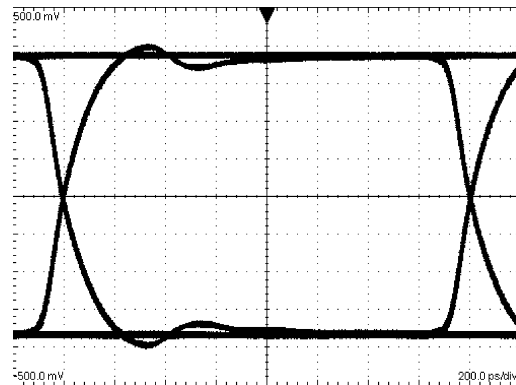


Figure 10. A 622 Mbps NRZ PRBS-7 After 2" Differential FR-4 Stripline  
V:100 mV / DIV, H:200 ps / DIV

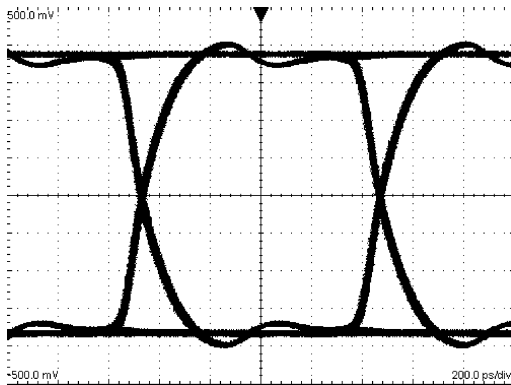


Figure 11. A 1.06 Gbps NRZ PRBS-7 After 2" Differential FR-4 Stripline  
V:100 mV / DIV, H:200 ps / DIV

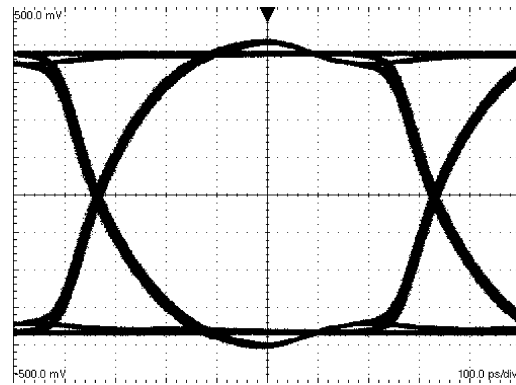


Figure 12. A 1.5 Gbps NRZ PRBS-7 After 2" Differential FR-4 Stripline  
V:100 mV / DIV, H:100 ps / DIV

## REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">9</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS10CP152TMA/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS10CP152 TMA	<a href="#">Samples</a>
DS10CP152TMAX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS10CP152 TMA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS10CP152TMAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS10CP152TMAX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated