HD3SS214 8.1 Gbps DisplayPort 1.4 2:1/1:2 Differential Switch

1 Features

- Compatible with DisplayPort 1.4 Electrical Standard
- 2:1 and 1:2 Switching Supporting Data Rates up to 8.1 Gbps
- Supports HPD, AUX and DDC Switching
- Wide Differential BW of 8 GHz
- Excellent Dynamic Electrical Characteristics
- V_{DD} Operating Range 3.3 V ±10%
- Extended Industrial Temperature Range of -40°C to 105°C
- 5 mm x 5 mm, 50-Ball ɥBGA Package
- Output Enable (OE) Pin Disables Switch to Save Power
- Power Consumption
  - Active < 2 mW Typical
  - Standby < 10 µW Typical (When OE = L)

2 Applications

- Notebook PCs
- Desktops/All-in-Ones
- Docking Station
- Digital Television

3 Description

HD3SS214 is a high-speed passive switch capable of switching two full DisplayPort 4 lane ports from one of two sources to one target location in an application. It will also switch one source to one of two sinks. For DisplayPort Applications, the HD3SS214 supports switching of the Auxiliary (AUX), Display Data Channel (DDC) and Hot Plug Detect (HPD) signals in the ZQE package.

One typical application would be a mother board that includes two GPUs that need to drive one DisplayPort sink. The GPU is selected by the Dx_SEL pin. Another application is when one source needs to switch between one of two sinks, example would be a side connector and a docking station connector. The switching is controlled using the Dx_SEL and AUX_SEL pins. The HD3SS214 operates from a single supply voltage of 3.3 V over extended industrial temperature range -40°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HD3SS214	µBGA (50)	5.00 mm x 5.00 mm
HD3SS214I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

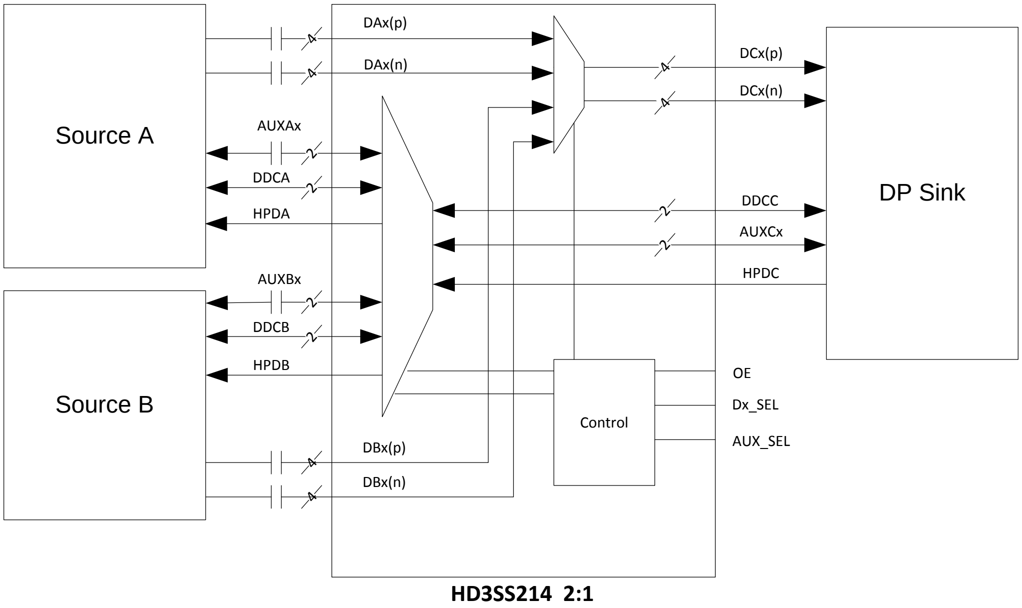


Table of Contents

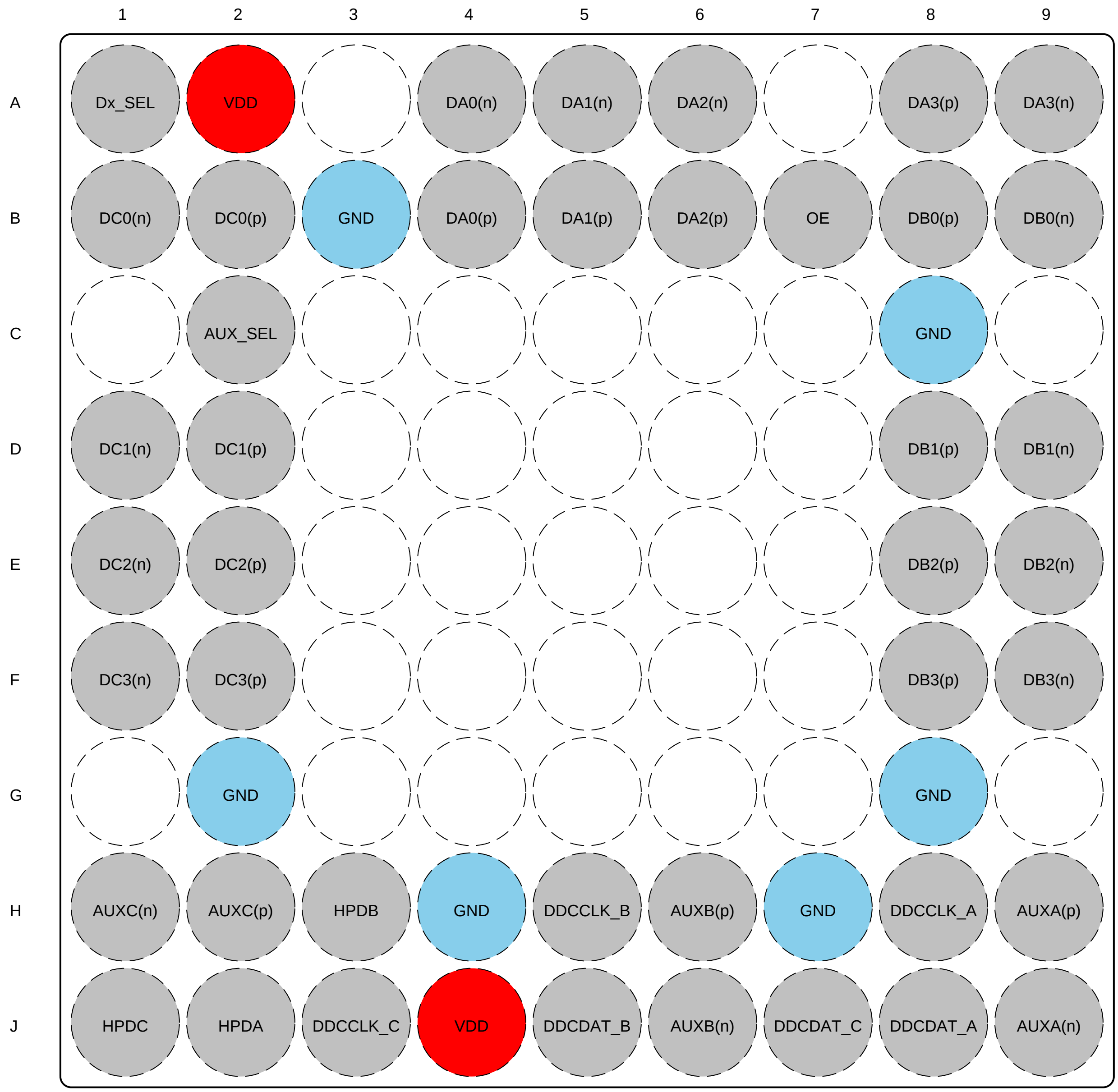
4 Revision History

Changes from Revision A (July 2016) to Revision B	**Page**
• Changed *Title* and *Feature* From: DisplayPort 1.3 To: DisplayPort 1.4	1

Changes from Original (December 2015) to Revision A	**Page**
• Changed DC2(p) to DC2(n) in Pin Functions	4
• Changed DC2(n) to DC2(p) in Pin Functions	4

5 Pin Configuration and Functions

ZQE Package
50-ball (µBGA)
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION[1]
NO.	NAME		
A1	Dx_SEL	Control I	High Speed Port Selection Control Pins
A2,J4	VDD	Supply	3.3 V Positive power supply voltage
A4	DA0(n)	I/O	Port A, Channel 0, High Speed Negative Signal
A5	DA1(n)	I/O	Port A, Channel 1, High Speed Negative Signal

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(1) The high speed data ports incorporate 20-kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

Pin Functions (continued)

PIN		I/O	DESCRIPTION[(1)]
NO.	NAME		
A6	DA2(n)	I/O	Port A, Channel 2, High Speed Negative Signal
A8	DA3(p)	I/O	Port A, Channel 3, High Speed Positive Signal
A9	DA3(n)	I/O	Port A, Channel 3, High Speed Negative Signal
B1	DC0(n)	I/O	Port C, Channel 0, High Speed Negative Signal
B2	DC0(p)	I/O	Port C, Channel 0, High Speed Positive Signal
B3,C8,G2,G8,H4,H7	GND	Supply	Ground
B4	DA0(p)	I/O	Port A, Channel 0, High Speed Positive Signal
B5	DA1(p)	I/O	Port A, Channel 1, High Speed Positive Signal
B6	DA2(p)	I/O	Port A, Channel 2, High Speed Positive Signal
B7	OE	I	Output Enable: OE = V_{IH}: Normal Operation OE = V_{IL}: Standby Mode
B8	DB0(p)	I/O	Port B, Channel 0, High Speed Positive Signal
B9	DB0(n)	I/O	Port B, Channel 0, High Speed Negative Signal
C2	AUX_SEL	Control I	AUX/DDC Selection Control Pin in Conjunction with Dx_SEL Pin
D1	DC1(n)	I/O	Port C, Channel 1, High Speed Negative Signal
D2	DC1(p)	I/O	Port C, Channel 1, High Speed Positive Signal
D8	DB1(p)	I/O	Port B, Channel 1, High Speed Positive Signal
D9	DB1(n)	I/O	Port B, Channel 1, High Speed Negative Signal
E1	DC2(n)	I/O	Port C, Channel 2, High Speed Negative Signal
E2	DC2(p)	I/O	Port C, Channel 2, High Speed Positive Signal
E8	DB2(p)	I/O	Port B, Channel 2, High Speed Positive Signal
E9	DB2(n)	I/O	Port B, Channel 2, High Speed Negative Signal
F1	DC3(n)	I/O	Port C, Channel 3, High Speed Negative Signal
F2	DC3(p)	I/O	Port C, Channel 3, High Speed Positive Signal
F8	DB3(p)	I/O	Port B, Channel 3, High Speed Positive Signal
F9	DB3(n)	I/O	Port B, Channel 3, High Speed Negative Signal
H1	AUXC(n)	I/O	Port C AUX Negative Signal
H2	AUXC(p)	I/O	Port C AUX Positive Signal
H3	HPDB	I/O	Port B Hot Plug Detect
H6	AUXB(p)	I/O	Port B AUX Positive Signal
H5	DDCCLK_B	I/O	Port B DDC Clock Signal
H8	DDCCLK_A	I/O	Port A DDC Clock Signal
H9	AUXA(p)	I/O	Port A AUX Positive Signal
J1	HPDC	I/O	Port C Hot Plug Detect
J2	HPDA	I/O	Port A Hot Plug Detect
J3	DDCCLK_C	I/O	Port C DDC Clock Signal
J5	DDCDAT_B	I/O	Port B DDC Data Signal
J6	AUXB(n)	I/O	Port B AUX Negative Signal
J7	DDCDAT_C	I/O	Port C DDC Data Signal
J8	DDCDAT_A	I/O	Port A DDC Data Signal
J9	AUXA(n)	I/O	Port A AUX Negative Signal

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range[3]	V_{DD}	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control pin	–0.5	V_{DD} + 0.5	
Continuous power dissipation		See Thermal Information		

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[2] All voltage values, except differential voltages, are with respect to network ground terminal.
[3] Tested in accordance with JEDEC Standard 22, Test Method A114-B

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C. All temperature limits are specified by design.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins, Signal Pins (Dx_SEL, AUX_SEL, MODE, OE)	2		V_{DD}	V
V_{IM}	Input mid level voltage	AUX_SEL Pin	V_{DD}/2 -300 mV	V_{DD}/2	V_{DD}/2 -300 mV	V
V_{IL}	Input low voltage	Control Pins, Signal Pins (Dx_SEL, AUX_SEL, MODE, OE)	-0.1		0.8	V
V_{I/O_Diff}	Differential voltage (Dx, AUXx)	Switch I/O diff voltage	0		1.8	Vpp
V_{I/O_CM}	Dx switching I/O Common mode voltage	Switch I/O common mode voltage	0		2	V
	AUXx (1) switching I/O Common mode voltage		0		3.6	
	Operating free-air temperature	HD3SS214	0		70	°C
		HD3SS214I	–40		105	°C

6.4 Thermal Information

THERMAL METRIC[1]		HD3SS214	UNIT
		ZQE (µBGA)	
		50 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

[1] For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input High Current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = V_{DD}			1	µA
I_{IM}	Input Mid Current (AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = V_{DD}/2			1	µA
I_{IL}	Input Low Current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} =GND			1	µA
I_{LKG}	Leakage Current (Dx_SEL, AUX_SEL)	V_{DD} = 3.3 V, V_{IN} = 2 V, OE = 3.3 V			1	µA
	Leakage Current (HPDx)	V_{DD} = 3.3 V, V_{IN} = 2 V, OE = 3.3 V; Dx_SEL = 3.3 V			1	µA
	Leakage Current (HPDx)	V_{DD} = 3.3 V, V_{IN} = 2 V, OE = 3.3 V; Dx_SEL = GND			1	µA
I_{OFF}	Device Shut Down Current	V_{DD} = 3.6 V, OE = GND			2.5	µA
I_{DD}	Supply Current	V_{DD} = 3.6 V, Dx_SEL/AUX_SEL = VDD/GND		0.6	1	mA
DA, DB, DC HIGH SPEED SIGNAL PATH						
C_{ON}	Outputs ON Capacitance	V_{IN} = 0 V, Outputs Open, Switch ON		0.6		pF
C_{OFF}	Outputs OFF Capacitance	V_{IN} = 0 V, Outputs Open, Switch OFF		0.8		pF
R_{ON}	ON resistance	V_{DD} = 3.3 V, VC_M = 0.5 V – 1.5 V, I_O = -40 mA		8	12	Ω
ΔR_{ON}	On resistance match between pairs of the same channel	V_{DD} = 3.3 V, V_{CM} = 0.5 V ≤ V_{IN} ≤ 1.2 V, I_O = -40 mA			1.5	Ω
$R_{(FLAT\_ON)}$	On resistance flatness ($R_{ON(MAX)}$ – $R_{ON(MAIN)}$)	V_{DD} = 3.3 V, V_{CM} = 0.5 V ≤ V_{IN} ≤ 1.2 V		1.3		Ω
AUXX, DDC, SIGNAL PATH						
R_{ON}(AUX)	ON resistance on AUX channel	V_{DD} = 3.3 V, V_{CM} = 0 V – V_{DD}, I_O = -8 mA		6	10	Ω
R_{ON}(DDC)	ON resistance on DDC channel	V_{DD} = 3.3 V, V_{CM} = 0.4 V, I_O = -3 mA		20	30	Ω

6.6 Electrical Characteristics, Device Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Dx Differential Insertion Loss	1.35 GHz		–0.9		dB
		2.7 GHz		–1.4		dB
		4.05 GHz		–1.6		dB
R_L	Dx Differential Return Loss	1.35 GHz		–17		dB
		2.7 GHz		–13		dB
		4.05 GHz		–11		dB
X_{TALK}	Dx Differential Crosstalk	1.35 GHz				dB
		2.7 GHz		–53		dB
		4.05 GHz		–47		dB
O_{IRR}	Dx Differential Off-Isolation	1.35 GHz				dB
		2.7 GHz		–26		dB
		4.05 GHz		–24		dB
	AUX Bandwidth			500		MHz

(1) For Return Loss, Crosstalk, Off-Isolation, and Insertion Loss values the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

6.7 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	R_{SC} and R_L = 50 Ω			100	ps
t_{on}	Dx_SEL/AUX_SEL–to-Switch t_{on} (Data and AUX and DDC)	R_{SC} and R_L = 50 Ω		0.7	1	µs
t_{off}	Dx_SEL/AUX_SEL–to-Switch t_{off} (Data and AUX and DDC)			0.7	1	
t_{on}	Dx_SEL/AUX_SEL –to-Switch t_{on} (HPD)	R_L = 1 kΩ		0.7	1	µs
t_{off}	Dx_SEL/AUX_SEL –to-Switch t_{off} (HPD)			0.7	1	
$t_{SK(O)}$	Inter-Pair Output Skew (CH-CH)	R_{SC} and R_L = 50 kΩ			30	ps
$t_{SK(b-b)}$	Intra-Pair Skew added (Bit-Bit)			1	5	ps

6.8 Typical Characteristics

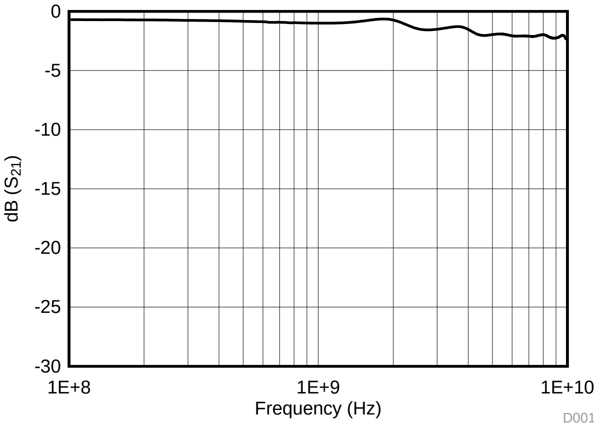


Figure 1. Insertion Loss and –3 dB Bandwidth

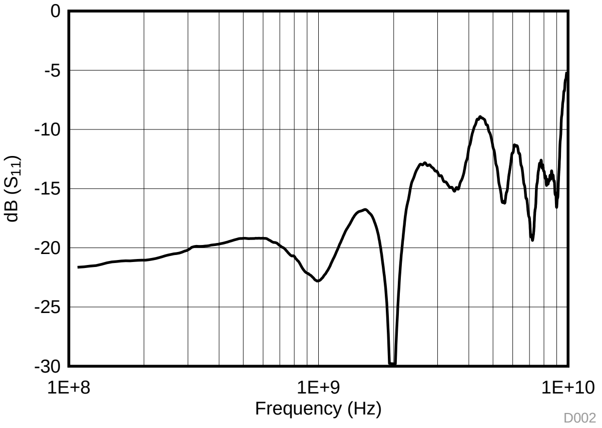


Figure 2. Return Loss

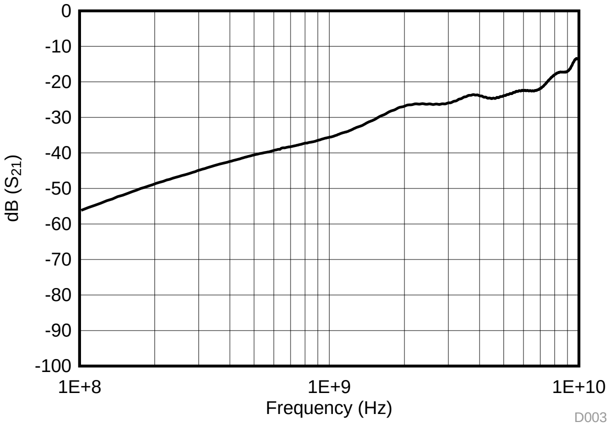


Figure 3. Off Isolation

7 Detailed Description

7.1 Overview

The HD3SS214 is an analog, differential passive switch that can work for any high speed interface applications, as long as it is biased at a common mode voltage range of 0 V to 2 V and has differential signaling with differential amplitude up to 1800 mVpp.

NOTE

HD3SS214 MUX does not provide common mode biasing for the channel. Therefore, it is required that the device is biased from either side for all active channels.

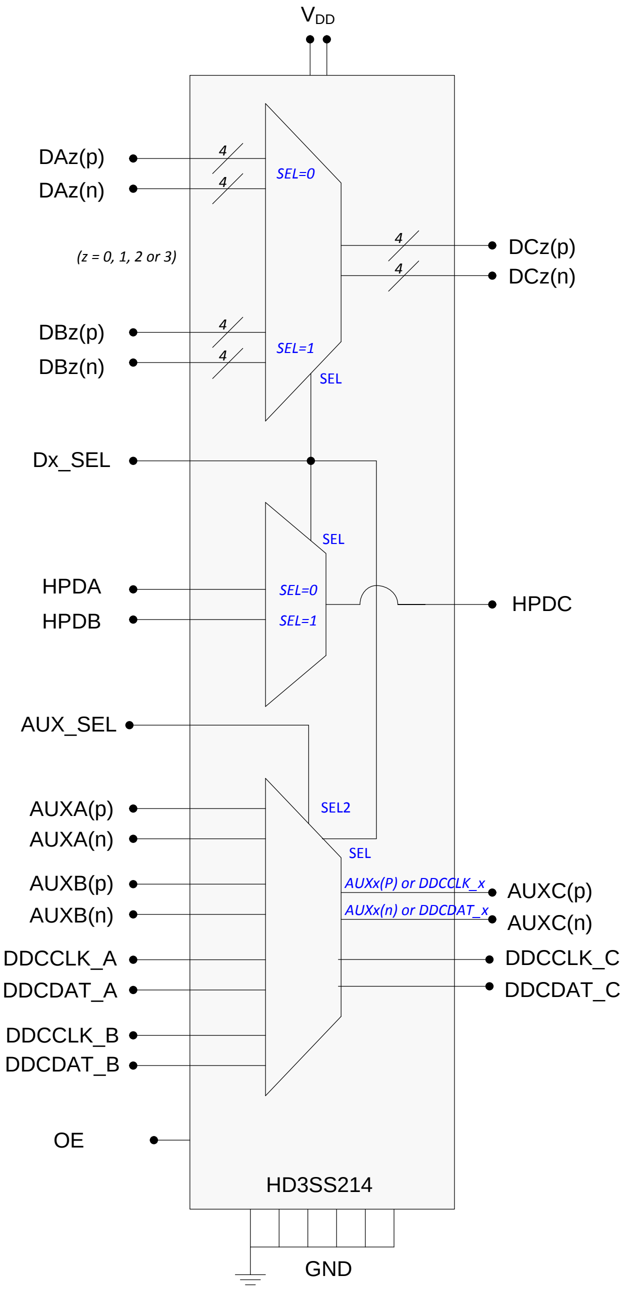
In high-speed applications and data paths, signal integrity is an important concern. The switch offers excellent dynamic performance such as high isolation, crosstalk immunity, and minimal bit-bit skew. These characteristics allow the device to function seamlessly in the system without compromising signal integrity. The 2:1/1:2, mux/de-mux device operates with ports A or B switched to port C, or port C switched to either port A or B. This flexibility allows an application to select between one of two Sources on ports A and B and send the output to the sink on port C. Similarly, a Source on port C can select between one of two Sink devices on ports A and B to send the data.

The HPD and data signals are both switched through the Dx_SEL pin. AUX and DDC are controlled with AUX_SEL and Dx_SEL.

With an OE control pin, the HD3SS214 is operational, with low active current, when this pin is high. When OE is pulled low, the device goes into standby mode and draws very little current in order to save power consumption in the application.

HD3SS214 high speed MUX channels have independent adaptive common mode tracking allowing four data paths to have different common mode voltage, simplifying system implementation and avoid inter-op issues.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Speed Switching

The HD3SS214 supports switching of 8.1 Gbps data rates. The high speed mux is designed with a wide –3dB differential bandwidth of 8 GHz and industry leading dynamic characteristics. All of these attributes help maintain signal integrity in the application. Each high speed port incorporates 20-kΩ pull down resistors that are switched in when the port is not selected and switched out when the port is selected. Additionally, high speed differential pairs at port C have internal 20-kΩ resistor between positive and negative pins

Feature Description (continued)

7.3.2 HPD, AUX, and DDC Switching

HPD, AUX, and DDC switching is supported through the HD3SS214. This enables the device to work in multiple application scenarios within multiple electrical standards. The AUXA/B and DDCA/B lines can both be switched to the AUXC port. This feature supports DP++ or AUX only adapters. For HDMI applications, the DDC channels are switched to the DDC_C port only and the AUX channel can remain active or the end user can make it float.

7.3.3 Output Enable and Power Savings

The HD3SS214 has two power modes, active/normal operating mode, and standby mode. During standby mode, the device consumes very little current to save the maximum power. To enter standby mode, the OE control pin is pulled low and must remain low. For active/normal operation, the OE control pin should be pulled high to VDD through a resistor.

7.4 Device Functional Modes

The HD3SS214 behaves as a two to one or one to two using high bandwidth pass gates. The input ports are selected using the Dx_SEL pin and Dx_SEL pin which are shown in Table 1.

Table 1. AUX/DDC Switch Control Logic(1)

CONTROL LINES		SWITCHED I/O PINS(2)								
AUX_SEL	**Dx_SEL**	**DCz(p) Pin z = 0, 1 ,2 or 3**	**DCz(n) Pin z = 0, 1 ,2 or 3**	**HPDC Pin**	**AUXA**	**AUXB**	**AUXC**	**DDCA**	**DDCB**	**DDCC**
L	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	Z	Z	Z
L	H	DBz(p)	DBz(n)	HPDB	Z	To/From AUXC	To/From AUXB	Z	Z	Z
H	L	DAz(p)	DAz(n)	HPDA	Z	Z	To/From DDCA	To/From AUXC	Z	Z
H	H	DBz(p)	DBz(n)	HPDB	Z	Z	To/From DDCB	Z	To/From AUXC	Z
M(2)	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	To/From DDCC	Z	To/From DDCA
M(2)	H	DBz(p)	DBz(p)	HPDB	Z	To/From AUXC	To/From AUXB	Z	To/From DDCC	To/From DDCB

(1) OE pin - For normal operation, drive OE high. Driving the OE pin low will disable the switch. Note: The ports which are not selected by the control lines will be in high impedance status.
(2) Z = High Impedance

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The HD3SS214 is a 1:2/2:1 DP switch that supports 8.1 Gbps data rates and DP++. This switch is bi-directional, so it can be used to switch two inputs to one output or one input to one of two outputs. In addition to main link switching, this switch also supports AUX and DDC switching, which simplifies DP++ implementation. 3.3 V is used to supply power to the switch.

8.2 Typical Application

8.2.1 Dual GPU With Docking Station Support

Many consumer devices require multiple video sources to be routed to multiple output sinks. One example of these devices is a dual-GPU laptop with docking station support. The laptop has two video sources that can be chosen: one low-power integrated GPU and one high-power discrete GPU. The video stream from one of these sources needs to be routed to one of two outputs: the docking station port or the laptop DisplayPort video port. In order to support this functionality, a high data rate, multi-input/multi-output switch system is required.

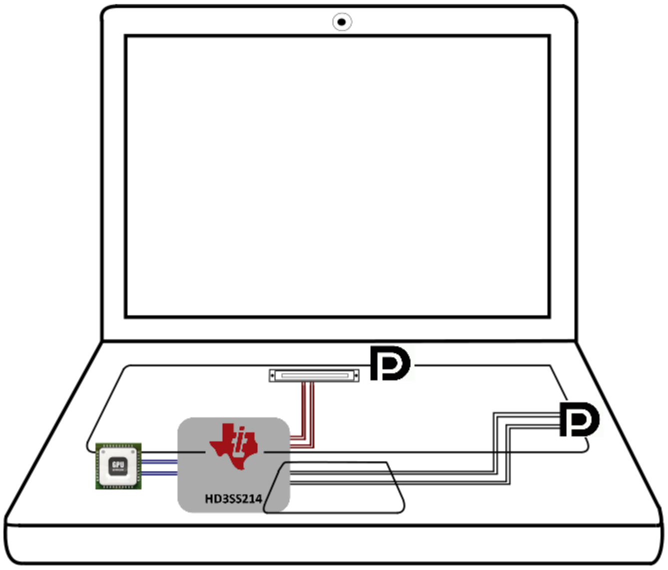


Figure 4. Dual GPU with Docking Station Support

8.2.2 Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
V_{DD}	3.3 V
Source	DP x1
Sink	DP x2
AUX_SEL Level	M
DP++ Support	No

8.2.3 Detailed Design Procedure

8.2.3.1 DP Inputs

The HD3SS214 is used as a 1:2 DP switch, the DCx[p/n] are connected to the GPU; the outputs (DAx[p/n] and DBx[p/n]) are routed to the ++DP connectors of the platform.

NOTE

This application information is only to show the principles of operation of the HD3SS214 and not the requirements of all the implementation. Many implementations will require external circuitry to compensate for signal loss (like a DP re-driver).

8.2.3.2 Source Selection Interface

Two control pins on the HD3SS214 are responsible for selecting the incoming DP signal: Dx_SEL and AUX_SEL. Dx_SEL controls which high speed ports are selected. A low signal on Dx_SEL corresponds to Port A routed to Port C and a high signal corresponds to Port B routed to Port C. A slide switch is used to select the level for this signal. In an embedded application, this switch can be replaced by a GPIO signal from a microcontroller.

AUX channel is controlled by AUX_SEL. This pin configures the switch to route the incoming AUX signal to the outgoing AUX path, when AUX_SEL = 0 the AUXA channel will be routed to AUXC, when AUX_SEL = 1 the AUXB channel will be routed to AUXC. Figure 5 shows the selection circuitry.

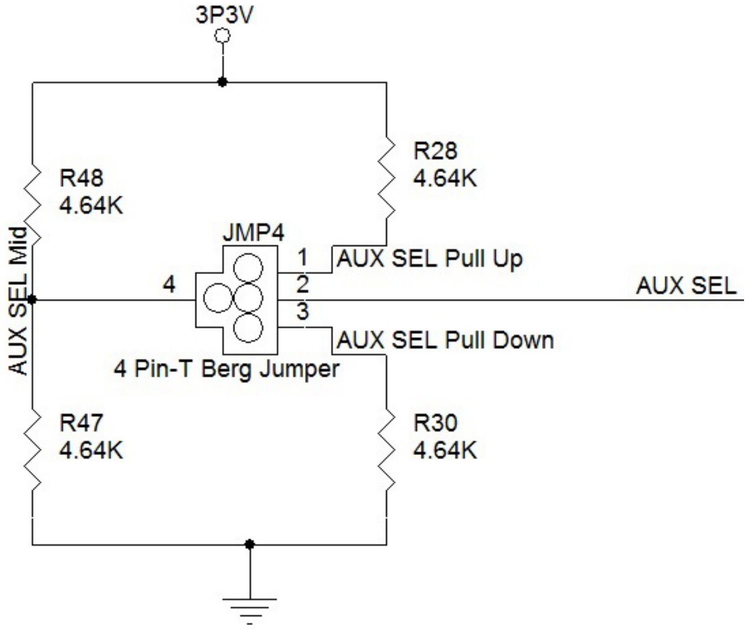


Figure 5. AUX_SEL Schematic

8.2.4 DP++ Support

The HD3SS214 supports DP++ implementations.

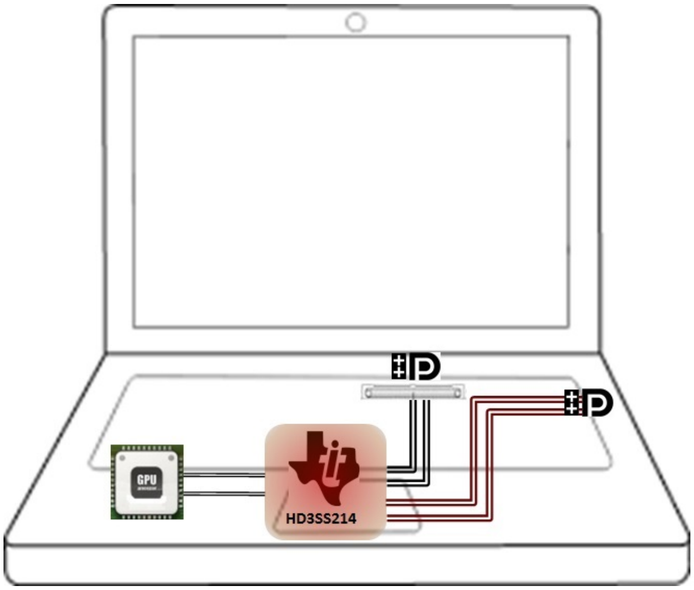


Figure 6. DP++ Docking Station Support

8.2.4.1 *Design Requirements*

For this example, use the parameters shown in Table 3

Table 3. Design Parameters

PARAMETER	VALUE
V_{DD}	3.3 V
Source	DP x1
Sink	DP x2
AUX_SEL Level	M
DP++ Support	Yes

8.2.4.2 *Detailed Design Procedure*

For applications involving DP++ support, following design procedures must be followed.

8.2.4.2.1 AUX and DDC Switching

The HD3SS214 supports DP++ implementations.

According to the DP++ standard, the DP AUX line is repurposed as the DDC line when HDMI signals are being transmitted. Unfortunately, the AUX and DDC signals have very different electrical requirements. AUX is a differential signal that requires AC coupling, while DDC uses I^2C protocol, which needs pull-up resistors. As a result, these signals are electrically incompatible if extra circuitry is not designed to accommodate the signals.

The source selection design block uses conditional pull-up resistors to support AUX and DDC signals on a unified line.Figure 7 illustrates the circuit that was used to enable the signal.

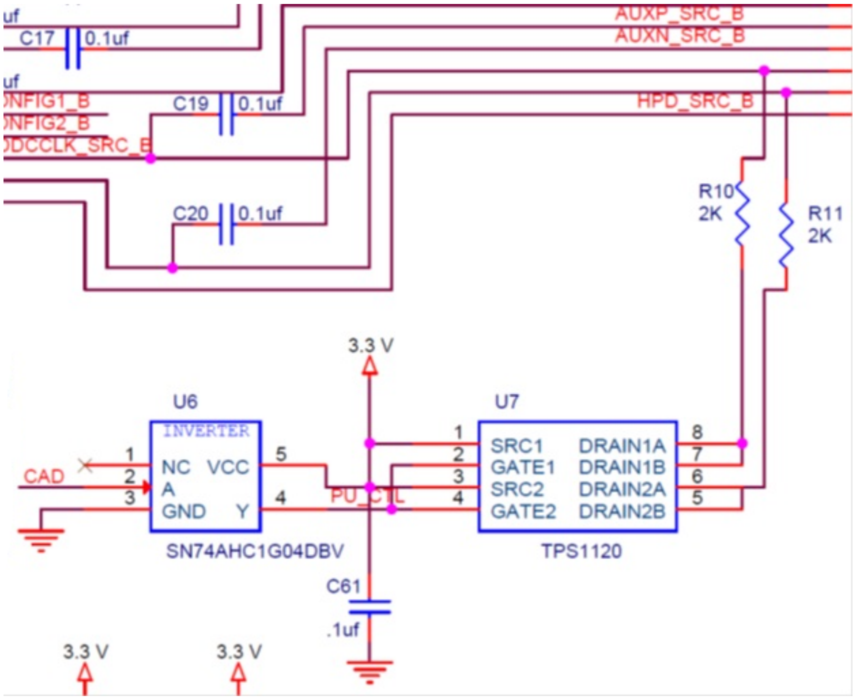


Figure 7. Combined AUX/DDC Circuitry

In this circuit, the unified AUX/DDC lines are split into two branches prior to entering the HD3SS214. One branch is AC coupled and is connected to the AUX inputs of the HD3SS214. The other is connected to the DDC inputs. AUX_SEL is configured so that the HD3SS214 transmits both of these through the switch. A conditional pull-up resistor system is connected to the DDC branch of the line. This resistor system will enable the pull-up resistors on the line only when HDMI/DVI signals are being transmitted, that is, when AUX is transmitting DDC signals. This prevents the AUX signal from being interfered with during standard DP mode and enables I2C DDC signaling during HDMI/DVI mode

The control input for the conditional pull-up circuit is the Cable Adaptor Detect (CAD) signal. When an HDMI or DVI sink is being used, this signal goes high, which indicates that the AUX line must transmit the DDC signal. When a standard DP sink is being used, the CAD signal goes low, indicating that the AUX line is transmitting its normal AUX signal. In this way, the CAD signal indicates when the AUX/DDC lines need pull-up resistors and when they do not.

The conditional pull-up circuit consists of an inverter, a p-type MOSFET, and two pull-up resistors. The FET acts as a switch between the pull-up resistors. When CAD is high (indicating that pull-up resistors are needed), the inverter outputs a low signal, which brings the Vgs of the FET below the FET's threshold voltage. Pulling Vgs below the threshold voltage turns the p-type FET on. When the FET turns on, it connects the AUX line's pull-up resistors to VCC, which enables them.

The chosen inverter is a Texas Instruments SN74AHC1G04 inverter, which has very fast response times and very good electrical characteristics for V_{OH} and V_{OL}. The MOSFET chosen is a Texas Instruments TPS1120 (SLVS080). This device has a convenient dual transistor package, an ideal threshold voltage and very low drain-to-source resistance when on. Together, these two devices have a desirable noise margin of 0.9 V.

8.2.4.2.2 CONFIG1 and CONFIG2 Routing

The HD3SS214 only routes the high speed main link, AUX, and Hot Plug Detect (HPD) lines, which means CONFIG1 and CONFIG2 lines need to be routed externally. This is necessary because these lines are important for DP++ as CONFIG1 carries the CAD signal.

A Texas Instruments TS3USB221 (SCDS263) is used to route these signals. It is a 2:1/1:2 USB switch that operates similarly to the HD3SS214. Each port has two inputs, so it is ideal for the CONFIG signals. SRC_SEL is used to select which source the CONFIG signals are from. The circuit for routing these signals can be seen in Figure 8.

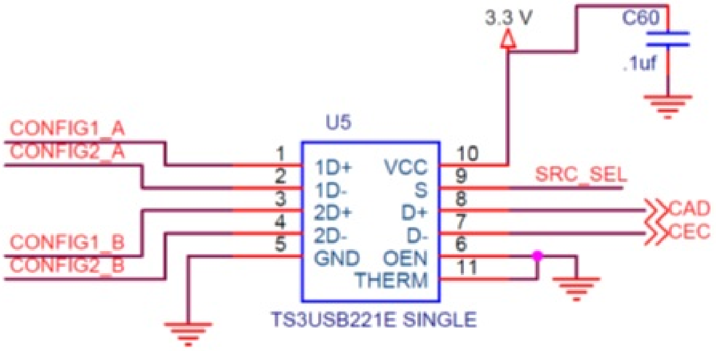


Figure 8. CONFIG Signal Routing

9 Power Supply Recommendations

There is no power supply sequence required for HD3SS214. However, it is recommended that OE is asserted high after device supply VDD is stable and in spec. It is also recommended that ample decoupling capacitors are placed at the device VCC near the pin.

10 Layout

10.1 Layout Guidelines

10.1.1 Layer Stack

Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit.

Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.

Routing the fast-edged control signals on the bottom layer by prevents them from cross-talking into the high-speed signal traces and minimizes EMI.

If the receiver requires a supply voltage different from the one of the repeater, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. Finally, a second power/ground system provides added isolation between the signal layers.

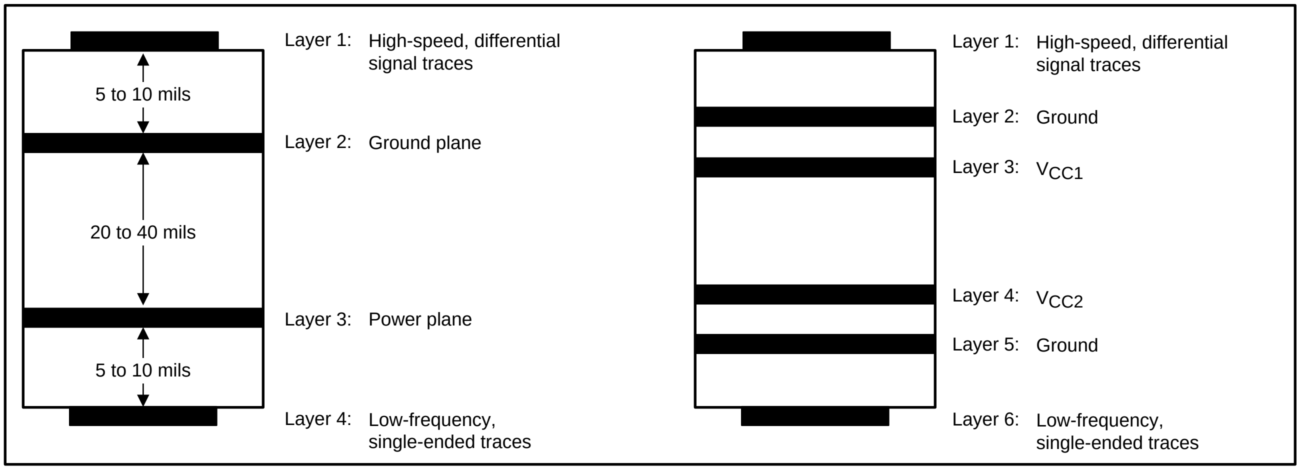


Figure 9. Recommended 4- or 6- Layer (0.062") Stack for a Receiver PCB Design

Layout Guidelines (continued)

10.1.2 Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and lower EMI. Although there seems to be an endless number of precautions to be taken, this section provides only a few main recommendations as layout guidance.

1. Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
2. Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering correction along the signal path. Use chamfered corners with a length-to-trace width ratio of between 3 and 5. The distance between bends should be 8 to 10 times the trace width.
3. Use 45 degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45o bends is seen as a smaller discontinuity.
4. When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.
5. Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.
6. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
7. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
8. Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100 Ω differential impedance. Large vias and pads can cause the impedance to drop below 85 Ω.
9. Use solid power and ground planes for 100 Ω impedance control and minimum power noise.
10. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
11. Keep the trace length between the DisplayPort connector and the DisplayPort device as short as possible to minimize attenuation.
12. Use good DisplayPort connectors whose impedances meet the specifications.
13. Place bulk capacitors (for example, 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
14. Place smaller 0.1 µF or 0.01 µF capacitors at the device.

10.2 Layout Example

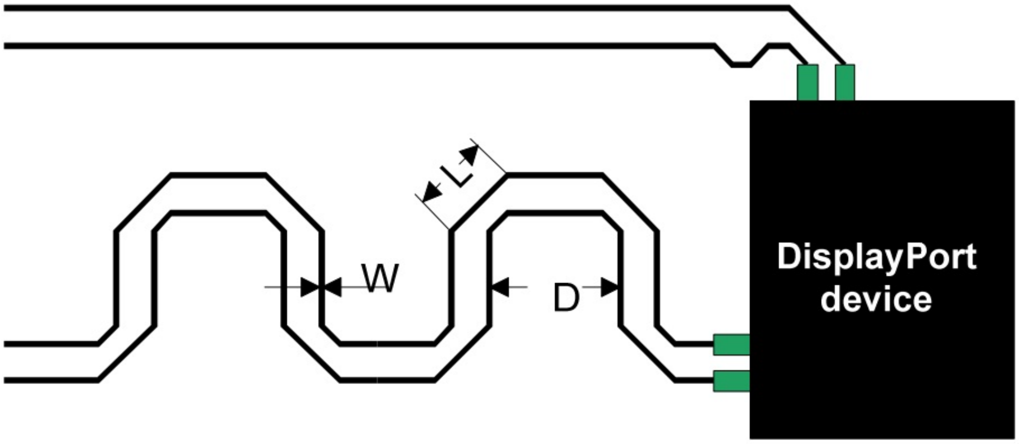


Figure 10. Skew Seduction via Meandering Using Chamfered Corners

Layout Example (continued)

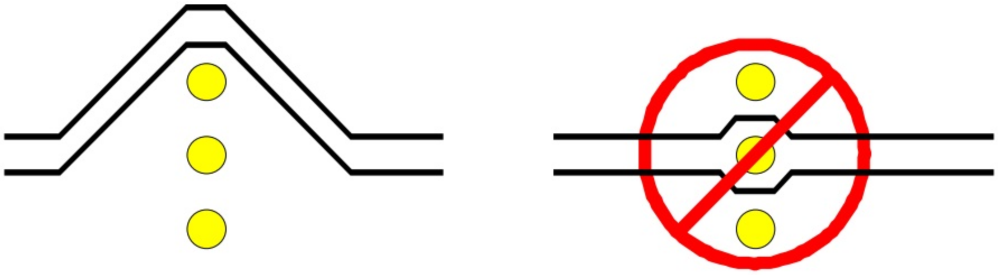


Figure 11. Routing Around an Object

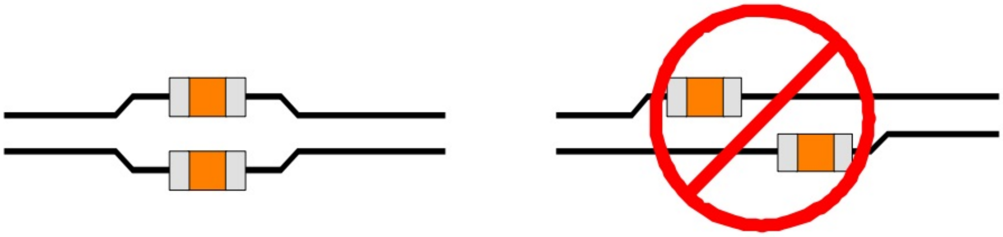


Figure 12. Lumping Discontinuities

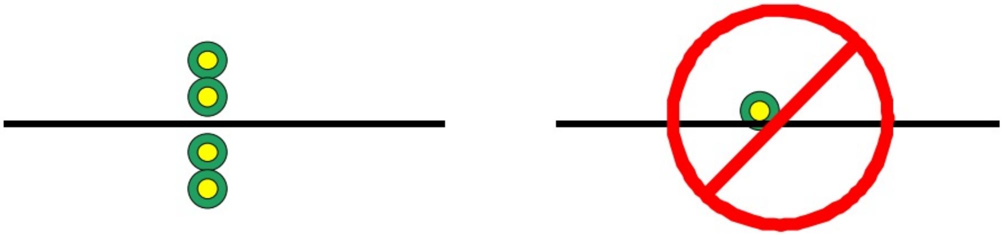


Figure 13. Avoiding via Clearance Sections

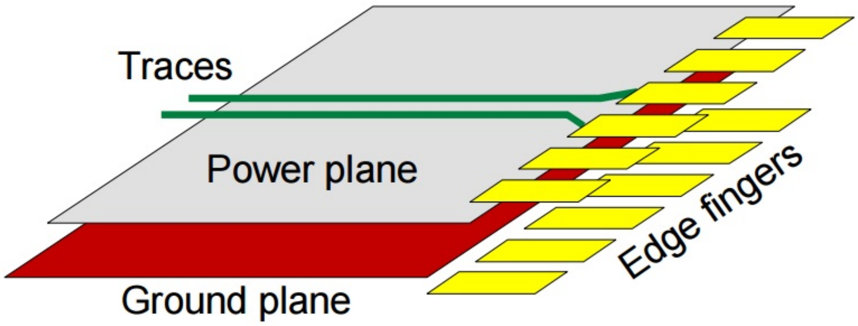


Figure 14. Keeping Planes out of the Area Between Edge-fingers

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

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11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS214IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	50	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS214	Samples
HD3SS214ZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	50	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	HD3SS214	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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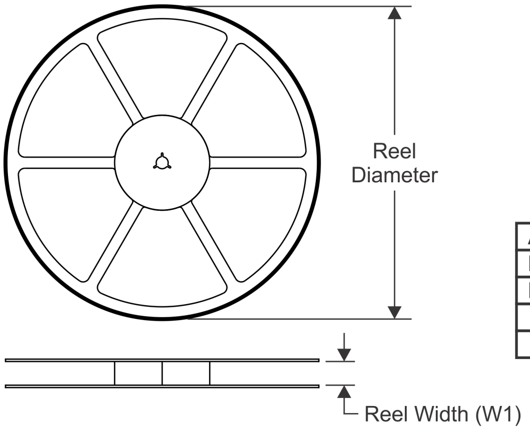
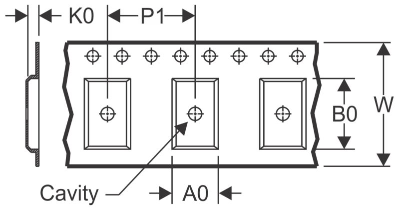
TAPE AND REEL INFORMATION

REEL DIMENSIONS

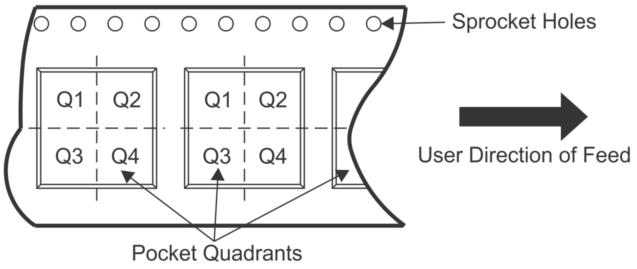


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

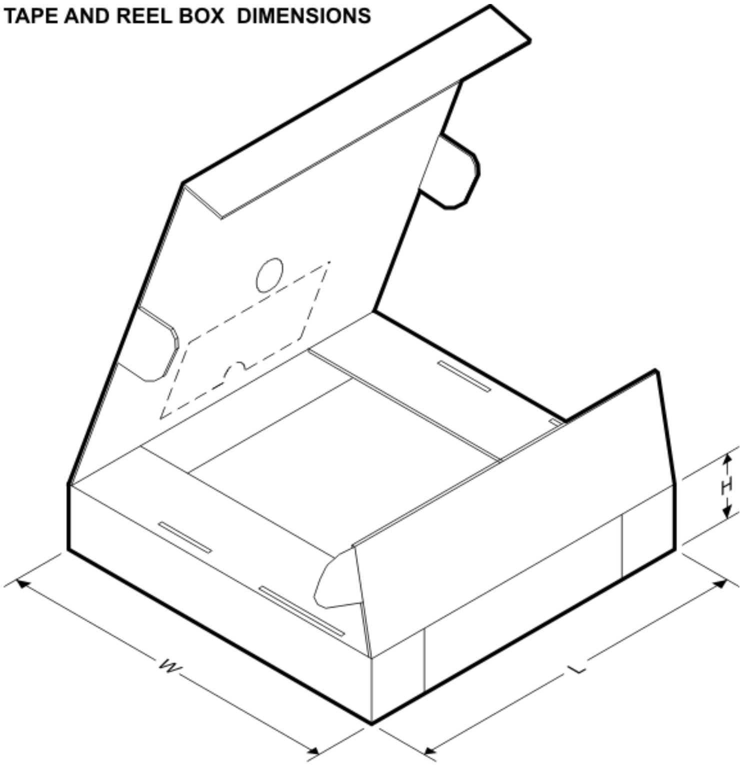
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS214IZQER	BGA MICROSTAR JUNIOR	ZQE	50	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
HD3SS214ZQER	BGA MICROSTAR JUNIOR	ZQE	50	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

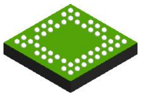
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS214IZQER	BGA MICROSTAR JUNIOR	ZQE	50	2500	336.6	336.6	31.8
HD3SS214ZQER	BGA MICROSTAR JUNIOR	ZQE	50	2500	336.6	336.6	31.8

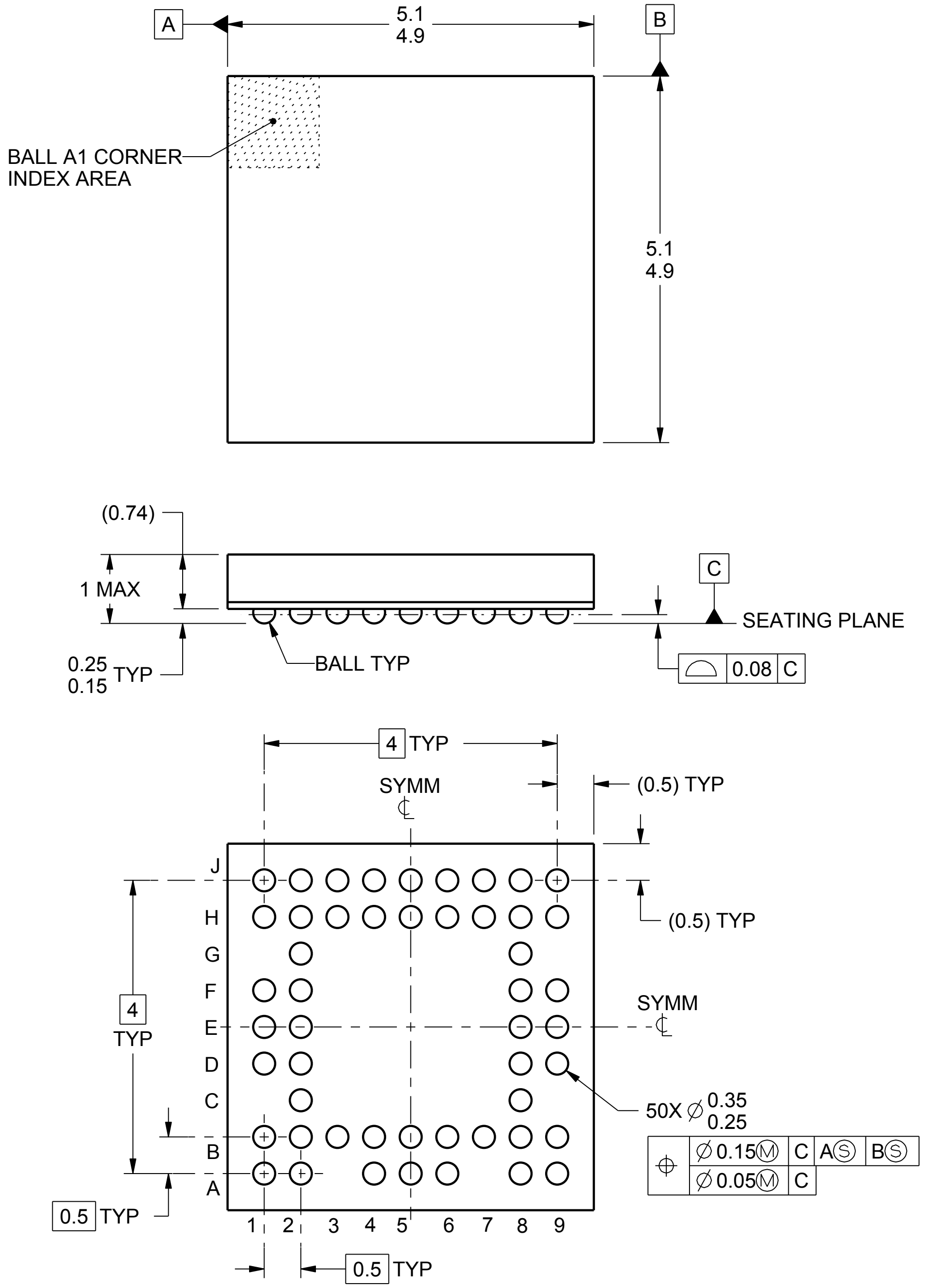
PACKAGE OUTLINE



ZQE0050A

BGA MicroStar Jr ™ - 1 mm max height

PLASTIC BALL GRID ARRAY

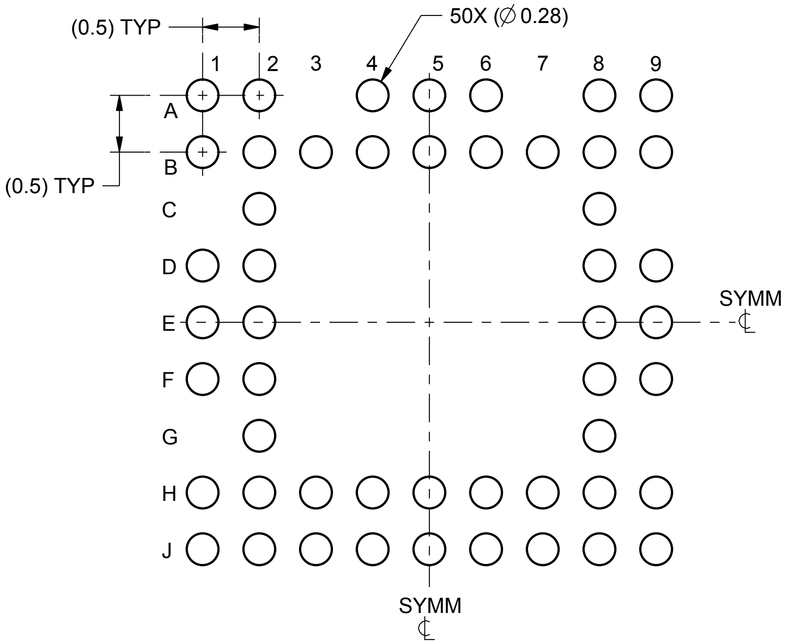


4221625/A 02/2015

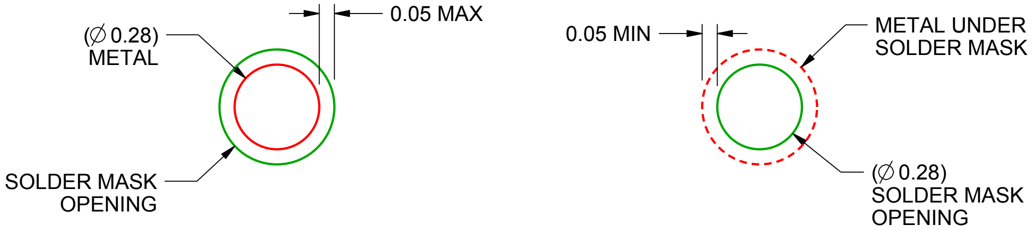
MicroStar Junior is trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-225.



LAND PATTERN EXAMPLE
SCALE:15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

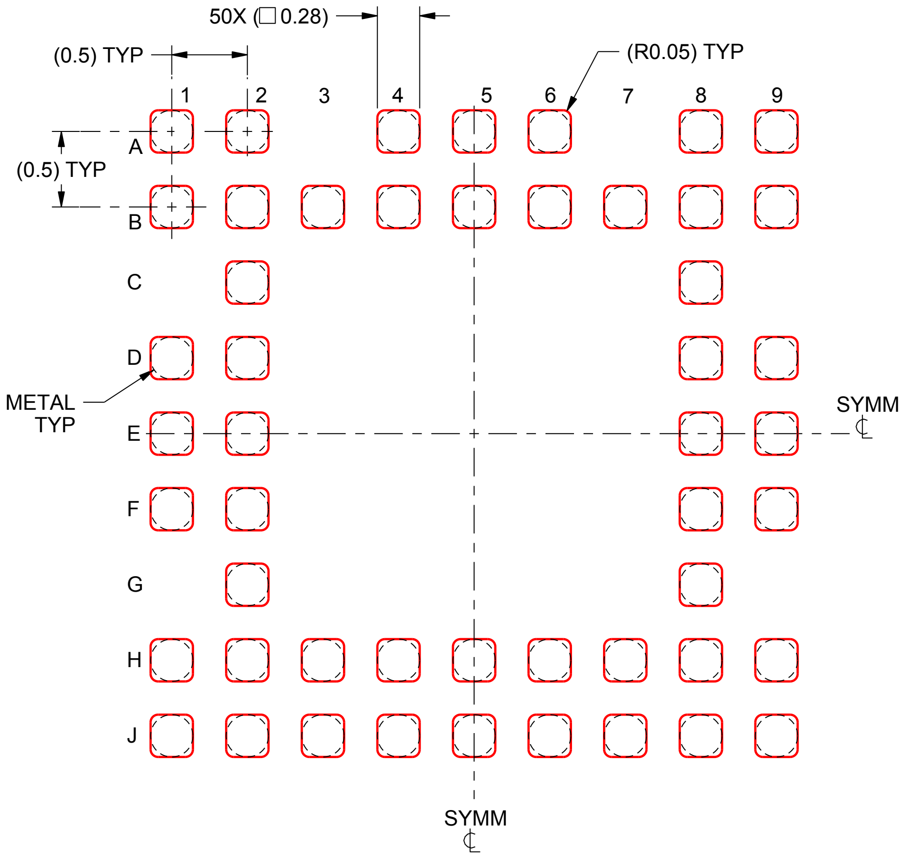
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221625/A 02/2015

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SSYZ015 (www.ti.com/lit/ssyz015).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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