DockPort Controller

Check for Samples: HD3SS2521

FEATURES

- **Ideal for DockPort Applications**
  - **Bi-Directional 2:1 Switch for USB 2.0 (HS/FS/LS) and HPD Signals**
  - **Bi-Directional 2:1 Switch for SuperSpeed USB and DisplayPort Signals**
  - **Integrated DockPort Controller Manages DockPort Detection, Signal Switching and Power Switching**
- **Supports Host-and Dock-side Applications**
- **VCC Operating Range 3.3V ± 10%**
- **SuperSpeed USB I/O Supports Common Mode Voltage from 0V to 2.2V**
- **USB 2.0 I/O Supports Signal Up to 3.6V**
- **Wide –3dB Differential BW on High-bandwidth Path of over 6 GHz**
- **Excellent High-bandwidth Path Dynamic Characteristics on (at 2.5GHz)**
  - **Crosstalk = –39dB**
  - **Isolation = –22dB**
  - **Insertion Loss = –1.2dB**
  - **Return Loss = 12 dB**
  - **Max Bit-Bit Skew = 8 ps**
- **5mm x11mm, 56-Pin WQFN Package (RHU)**
- **ESD**
  - **HBM: 2000V**
  - **CDM: 500V**

APPLICATIONS

- **Desktop PCs**
- **Notebook PCs**
- **Tablets**
- **Docking Station**

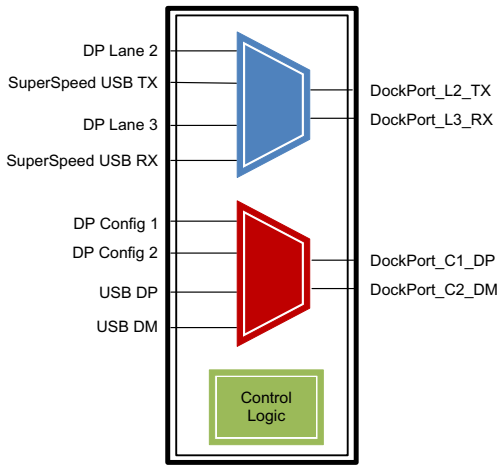


Figure 1. DockPort Functional Diagram

PRODUCT PREVIEW

DESCRIPTION

The HD3SS2521 is an integrated DockPort switch solution. It provides independent 2:1 passive switching for the SuperSpeed USB and Display Port signals as well as for the USB 2.0 (HS/FS/LS) and I2C necessary to support DockPort applications. In addition, a firmware upgradable integrated DockPort controller is provided to manage host and dock side DockPort detection, signal switch and power configuration.

The HD3SS2521 is offered in 56-pin WQFN package and is specified to operate from a single supply voltage of 3.3V over the temperature range of 0°C to 70°C .

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

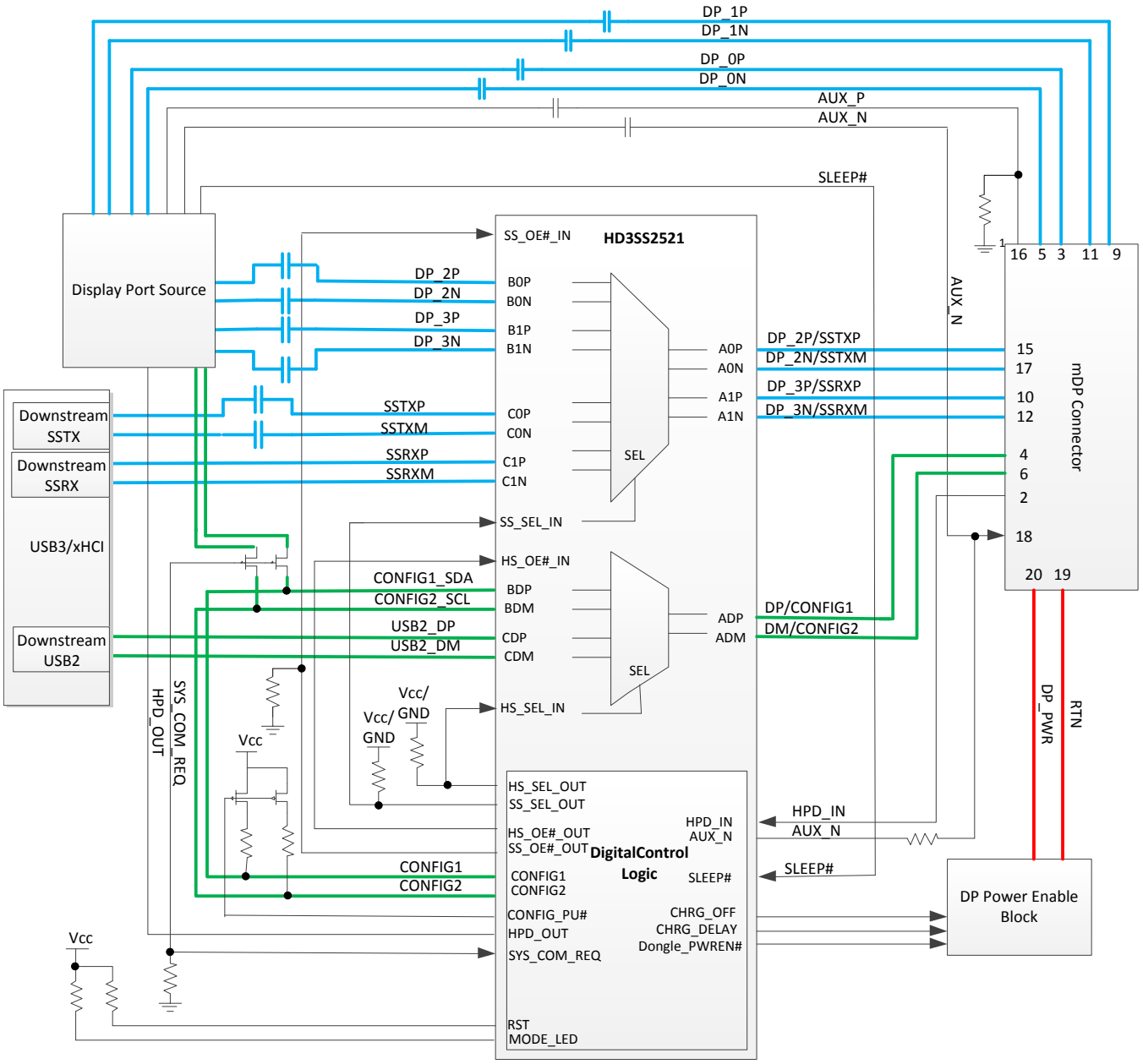
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE
HD3SS2521RHUR	HD3S2521	56-Pin WQFN (Reel Large)
HD3SS2521RHUT	HD3S2521	56-Pin WQFN (Reel Small)

PRODUCT PREVIEW

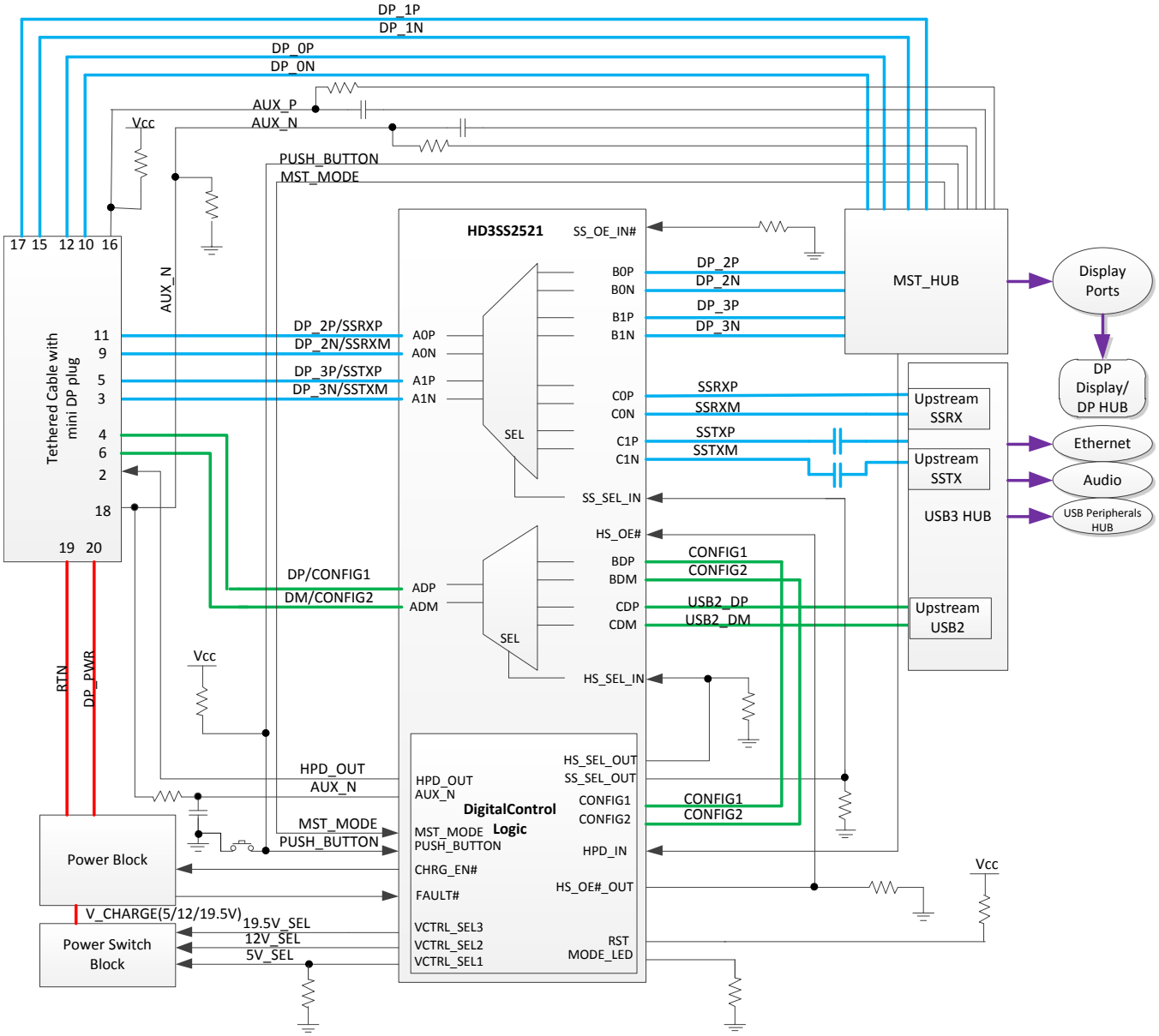
TYPICAL APPLICATION



NOTE: Refer to the implementation guide for details on design considerations and configuration options

Figure 2. DockPort Host Implementation

PRODUCT PREVIEW

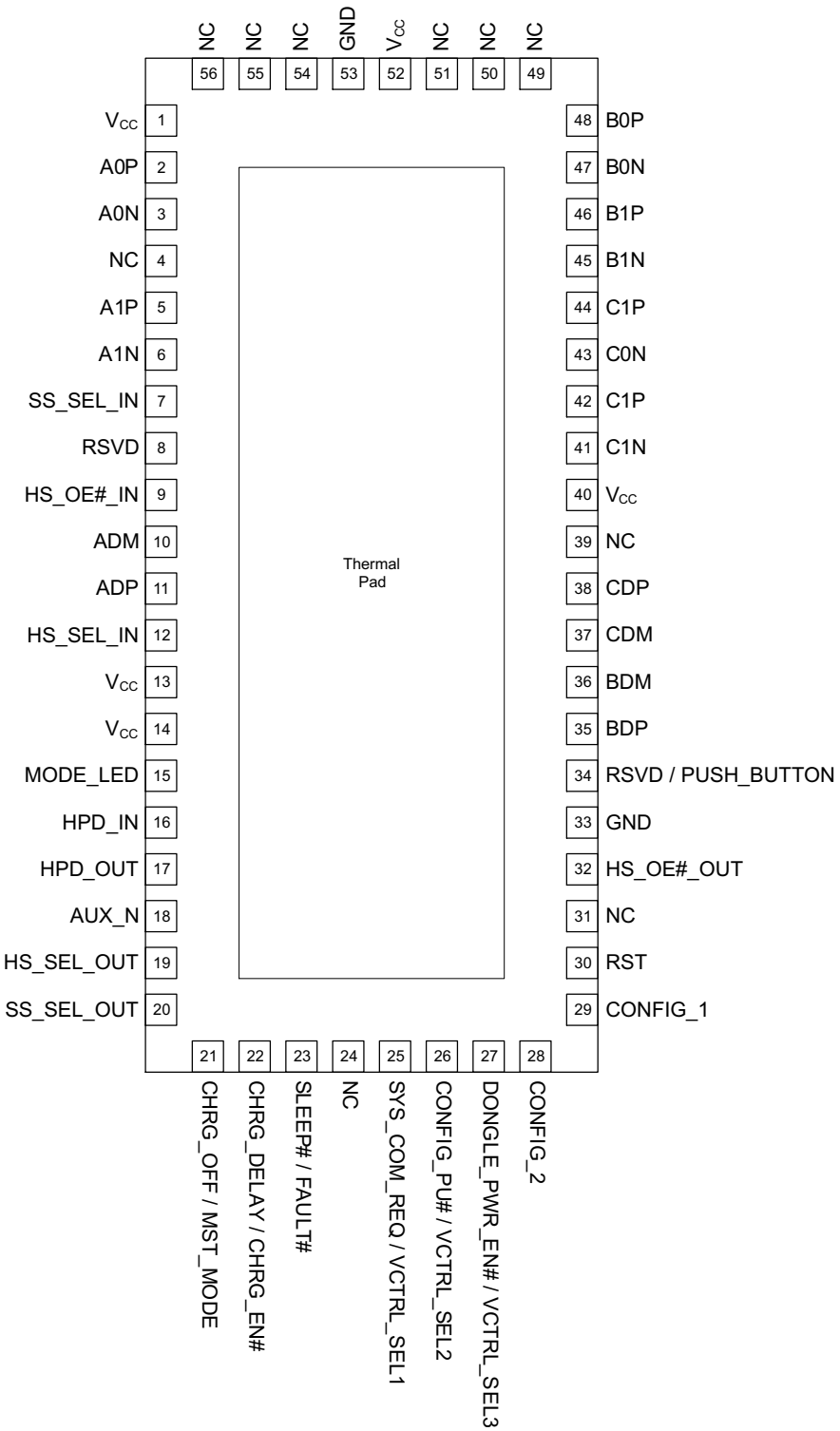


NOTE: Refer to the implementation guide for details on design considerations and configuration options

Figure 3. DockPort Hub Implementation

PRODUCT PREVIEW

RHU PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

PIN FUNCTIONS

PIN	I/O	PIN NAME	DockPort HOST (SIGNAL MUX)	DockPort DEVICE (SIGNAL DE-MUX)	SIGNAL SPEED (MAX)
2	I/O	A0P	DockPort Lane 2, Positive Signal (DockPort cable between DockPort host and DockPort device)		Fast Lane (Up to 5.4Gbps)
3	I/O	A0N	DockPort Lane 2, Negative Signal (DockPort cable between DockPort host and DockPort device)		
5	I/O	A1P	DockPort Lane 3, Positive Signal (DockPort cable between DockPort host and DockPort device)		
6	I/O	A1N	DockPort Lane 3, Negative Signal (DockPort cable between DockPort host and DockPort device)		
48	I/O	B0P	DisplayPort Lane 2, Positive Signal		Fast Lane (Up to 5.4Gbps)
47	I/O	B0N	DisplayPort Lane 2, Negative Signal		
46	I/O	B1P	DisplayPort Lane 3, Positive Signal		
45	I/O	B1N	DisplayPort Lane 3, Negative Signal		
44	I/O	C0P	SuperSpeed USB TX, Positive Signal	SuperSpeed USB RX, Positive Signal	Fast Lane (Up to 5.4Gbps)
43	I/O	C0N	SuperSpeed USB TX, Negative Signal	SuperSpeed USB RX, Negative Signal	
42	I/O	C1P	SuperSpeed USB RX, Positive Signal	SuperSpeed USB TX, Positive Signal	
41	I/O	C1N	SuperSpeed USB RX, Negative Signal	SuperSpeed USB TX, Negative Signal	
11	I/O	ADP	DockPort Config1 (DockPort cable between DockPort host and DockPort device)		Supports High-speed USB
10	I/O	ADM	DockPort Config2 (DockPort cable between DockPort host and DockPort device)		
35	I/O	BDP	CONFIG 1		
36	I/O	BDM	CONFIG 2		
37	I/O	CDP	High-speed USB D+		
38	I/O	CDM	High-speed USB D-		
7	I	SS_SEL_IN	DisplayPort / SuperSpeed USB Mux Select (Connect to SS_SEL_OUT - Pin 20)		
12	I	HS_SEL_IN	DisplayPort / HighSpeed USB Mux Select (Connect to HS_SEL_OUT - Pin 19)		
8	I	RSVD (SS_OE#_IN)	N/C For future compatibility (Connect to RSVD [SS_OE#_OUT] signal - Pin 34)	N/C Requires external 10 kΩ Pull-down.	
9	I	HS_OE#_IN	DisplayPort / HighSpeed USB Mux Enable (Connect to HS_OE#_OUT - Pin 32)		
15	I/O	MODE_LED	This signal is sampled at power on or reset to determine the mode of operation: Pulled High for DockPort host operation. (Optionally through LED for debug purposes)	This signal is sampled at power on or reset to determine the mode of operation: Pulled Low for DockPort hub (dock/dongle) operation. (Optionally through LED for debug purposes)	
16	I	HPD_IN	Hot Plug Detect from DockPort device	Hot Plug Detect from MST Hub/DP Device	
17	O	HPD_OUT	Hot Plug Detect to System Graphics	Hot Plug Detect to DockPort host.	
18	I/O	AUX_N	AUX Negative Pull-Up to DockPort device (Output) This signal indicates a connection event to a DockPort device.	AUX Negative from DockPort host (Input) This signal is used to detect a connection event from a DockPort host.	

PIN FUNCTIONS (continued)

PIN	I/O	PIN NAME	DockPort HOST (SIGNAL MUX)	DockPort DEVICE (SIGNAL DE-MUX)	SIGNAL SPEED (MAX)
19	O	HS_SEL_OUT	DisplayPort / High-speed USB Mux Select (Connect to HS_SEL_IN - Pin 12) This signal in conjunction with SS_SEL_OUT is sampled at power-on or reset to determine the voltage level supplied to a DockPort host and must be strapped to correct logic level for the corresponding voltage level: 5 V, 12 V or 19 V. Refer to the Power Delivery Voltage Selection table for strapping options. After power-on/reset, this signal is driven by DockPort host to select the device operation between DisplayPort and High-speed USB. 0 = DisplayPort 1 = High-speed USB		
20	O	SS_SEL_OUT	DisplayPort / SuperSpeed USB Mux Select (Connect to SS_SEL_IN - Pin 7) This signal in conjunction with HS_SEL_OUT is sampled at power-on or reset to determine the voltage level to be supplied to a DockPort host and must be strapped to correct logic level for the corresponding voltage level: 5 V, 12 V or 19 V. Refer to the Power Delivery Voltage Selection table for strapping options. After power-on/reset, this signal is driven by DockPort host to select the device operation between DisplayPort and SuperSpeed USB. 0 = DisplayPort 1 = SuperSpeed USB		
28	I/O	CONFIG_2	DisplayPort CONFIG2/CEC		
29	I/O	CONFIG_1	DisplayPort CONFIG1/CAD		
21	O	CHRG_OFF	This signal controls the power delivery circuit.	—	
		MST_MODE	—	MST Mode Input from MST HUB which indicates 2/4 DisplayPort lane switch. 0 = 2-lane (external 10 kΩ Pull-down) 1 = 4-lane (external 10 kΩ Pull-up)	
22	O	CHRG_DELAY	This signal controls the power delivery circuit.	—	
		CHRG_EN#	—	This signal is the power delivery enable for a DockPort hub.	
23	I	SLEEP#	Connect to the DockPort host sleep state signal.	—	
		FAULT#	—	Connect to the fault indicator of the power management circuit	
25	I	SYS_COM_REQ	External 100K Pull–down required. This signal is a sampled at power on or reset to determine if the system is in a FW update mode. After power on reset, the signal is used for communication request via a GPIO in a DockPort host for communication request		
	O	VCTRL_SEL1	—	Power enable for 5 V power delivery In additon, this signal is sampled at power on or reset to determine the mode of operation: 0 = DockPort hub (external 10 kΩ Pull-down) 1 = DockPort dongle (external 10 kΩ Pull-up)	

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PIN FUNCTIONS (continued)

PIN	I/O	PIN NAME	DockPort HOST (SIGNAL MUX)	DockPort DEVICE (SIGNAL DE-MUX)	SIGNAL SPEED (MAX)
26	O	CONFIG_PU#	Connect to FET switch to control pull-up option on DisplayPort CONFIG1/CONFIG2 for DockPort communication.	—	
		VCTRL_SEL2	—	Power enable for 12 V power delivery	
27	O	Dongle_PWREN#	Power enable for 5 V DockPort dongle power circuitry	—	
		VCTRL_SEL3	—	Power enable for 19 V power delivery	
34	O	RSVD (SS_OE#_OUT)	N/C For future compatibility (Connect to RSVD [SS_OE#_IN] signal - Pin 8)	—	
	I	PUSH_BUTTON	—	External 5.6 kΩPull-up required. Push button input to DockPort hub and MST HUB for 2-lane/4-lane switching	
32	O	HS_OE#_OUT	DisplayPort / High-speed USB Mux Enable. (Connect to HS_OE#_IN - Pin 9) An external 10 kΩ Pull-down to ground is required.		
30	I/O	RST	Reset		
33 39 53	GND	GND	Connect to Supply Ground		
24 31 49 50 51 54 55 56	NC	NC	No Connect		
1 4 13 14 40 52	Supply	VCC	3.3V Positive power supply voltage		

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Table 1. Power Delivery Voltage Selection

VOLTAGE	HS_SEL_OUT	SS_SEL_OUT
0 V	0	0
12 V	0	1
19 V	1	0
5 V	1	1

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage Range(2)	VCC	–0.3	4	V
Voltage Range	Differential I/O (High bandwidth signal path, AxP/N, BxP/N, CxP/N)	–0.5	4	V
	Differential I/O (Low bandwidth signal path, ADP/M, BDP/M, CDP/M)	-0.5	7	V
	Control Pin and Single Ended I/O	–0.3	V_{CC} + 0.3	V
Electrostatic discharge	Human body model(3)		±2000	V
	Charged-device model(4)		±500	V
Continuous power dissipation		See Thermal Table		

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A

PRODUCT PREVIEW

THERMAL INFORMATION

THERMAL METRIC(1)		HD3SS2521 RHU (56 PIN)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	31.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	15.9	
θ_{JB}	Junction-to-board thermal resistance	8.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	8.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

(Typical values for all parameters are at Vcc = 3.3V and T_A = 25°C. All temperature limits are specified by design)

			MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage	Control/Status Pins	2		V_{CC}	V
V_{IL}	Input low voltage	Control/Status Pins	–0.1		0.8	V
V_{I/O_Diff}	Differential voltage	Switch I/O diff voltage (High-bandwidth path AxP/N, BxP/N, CxP/N)	0		1.8	Vpp
V_{I/O_CM}	Common voltage	Switch I/O common mode voltage (High-bandwidth path AxP/N, BxP/N, CxP/N)	0		2	V
$V_{I/O}$	Input/ouput voltage	Data input/output voltage (Low-bandwidth path ADP/M, BDP/M, CDP/M)	0		5.5	V
T_A	Operating free-air temperature		0		70	°C

ELECTRICAL CHARACTERISTICS – DEVICE PARAMETERS

(under recommended operating conditions)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current	VCC = 3.6V, HS_SEL_IN/SS_SEL_IN = VCC/GND; HS_OE#_IN = GND; Outputs Floating		4.5		mA
AUX_N, CONFIG_1, CONFIG_2, FAULT#, HPD_IN, MODE_LED, PUSH_BUTTON, RST, SLEEP#, SYS_COM_REQ, TEST						
V_{IT+}	Positive-going input threshold voltage		0.45 V_{CC}		0.75 V_{CC}	V
V_{IT-}	Negative-going input threshold voltage		0.25 V_{CC}		0.55 V_{CC}	V
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)	V_{CC} = 3V	0.3		1	V
R_{PULL}	Pullup/pulldown resistor	Pullup: V_{IN} = GND, Pulldown: V_{IN} = V_{CC}, V_{CC} = 3V	20	35	50	kΩ
C_I	Input capacitance	V_{IN} = GND or V_{CC}		5		pF
I_{LK}	High-impedance leakage current	V_{IN} = GND or V_{CC}, V_{CC} = 3V, Pullup/Pulldown disabled			±50	nA
AUX_N, CHRG_DELAY, CHRG_EN, CHRG_OFF, CONFIG_1, CONFIG_2, CONFIG_PU#, Dongle_PWREN#, HPD_OUT, HS_OE#_OUT, HS_SEL_OUT, MODE_LED, MST_MODE, SS_SEL_OUT, RST, TEST, VCTRL_SEL1, VCTRL_SEL2, VCTRL_SEL3						
V_{OH}	High-level ouptut voltage	I_{OHmax} = –6 mA(1)		V_{CC}– 0.3		V
V_{OL}	Low-level ouptut voltage	I_{OLmax} = 6 mA(1)		GND + 0.3		V
SS_SEL_IN						
I_{IH}	Input High Current	V_{CC} = 3.6V, V_{IN} = VCC			95	µA
I_{IL}	Input Low Current	V_{CC} = 3.6V, V_{IN} = GND			1	

(1) The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

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ELECTRICAL CHARACTERISTICS – DEVICE PARAMETERS (continued)

(under recommended operating conditions)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
HS_OE#_IN , HS_SEL_IN						
I_{IH}	Input High Current	V_{CC} = 3.6V, V_{IN} = VCC			1	µA
I_{IL}	Input Low Current	V_{CC} = 3.6V, V_{IN} = GND			1	µA
AxP/N, BxP/N, CxP/N						
I_{LK}	High-impedance leakage current	V_{CC} = 3.6V, V_{IN} = 0V, V_{OUT} = 2V (I_{LK} on open outputs Port B and C)			130	µA
		V_{CC} = 3.6V, V_{IN} = 0V, V_{OUT} = 2V (I_{LK} on open outputs Port A)			4	
ADP/DM, BDP/DM, CDP/DM						
I_{LK}	High-impedance leakage current	V_{CC} = 3.6V, V_{IN} = 0V, V_{OUT} = 0V to 4V, HS_OE#_IN = GND			1	µA

ELECTRICAL CHARACTERISTICS – SIGNAL SWITCH PARAMETERS

(under recommended operating conditions; RL, Rsc = 50Ω, CL = 10pF unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
AxP/N, BxP/N, CxP/N HIGH-BANDWIDTH SIGNAL PATH						
t_{PD}	Switch Propagation Delay	Rsc and RL = 50 Ω, See Figure 5			85	ps
T_{on}	SS_SEL_IN -to-Switch T_{on}	Rsc and RL = 50 Ω, See Figure 4		70	250	ns
T_{off}	SS_SEL_IN -to-Switch T_{off}			70	250	
$T_{SK(O)}$	Inter-Pair Output Skew (CH-CH)	Rsc and RL = 50 Ω, See Figure 5			20	ps
$T_{SK(b-b)}$	Intra-Pair Output Skew (bit-bit)				8	ps
C_{ON}	Outputs ON Capacitance	V_{IN} = 0V, Outputs Open, Switch ON		1.5		pF
C_{OFF}	Outputs OFF Capacitance	V_{IN} = 0V, Outputs Open, Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{CC} = 3.3V, V_{CM} = 0.5V – 1.5V, I_O = –8 mA		5	8	Ω
ΔR_{ON}	On resistance match between channels	V_{CC} = 3.3V; –0.35V ≤ VIN ≤ 1.2V; I_O = –8 mA			2	Ω
	On resistance match between pairs of the same channel				0.7	
R_{FLAT_ON}	On resistance flatness [$R_{ON(MAX)}$ – $R_{ON(MIN)}$]	V_{CC} = 3.3V; –0.35V ≤ V_{IN} ≤ 1.2V			1.15	Ω
RL	Differential Return Loss (VCM = 0V)	f = 2.5 GHz		–12		dB
		f = 4.0 GHz		–11		
X_{TALK}	Differential Crosstalk (VCM = 0V)	f = 2.5 GHz		–39		dB
		f = 4.0 GHz		–35		
O_{IRR}	Differential Off-Isolation (VCM = 0V)	f = 2.5 GHz		–22		dB
		f = 4.0 GHz		–19		
I_L	Differential Insertion Loss (VCM = 0V)	f = 2.5 GHz		–1.1		dB
		f = 4.0 GHz		–1.5		
BW	Bandwidth	At -3 dB		6		GHz
ADP/DM, BDP/DM, CDP/DM SIGNAL PATH						
t_{PD}	Switch Propagation Delay	Rsc and RL = 50 Ω, See Figure 5		250		ps
T_{on}	HS_SEL_IN -to-Switch T_{on}	Rsc and RL = 50 Ω, See Figure 4			30	ps
	HS_OE#_IN -to-Switch T_{on}				17	ns
T_{off}	HS_SEL_IN Toff	Rsc and RL = 50 Ω, See Figure 4			12	ns
	HS_OE#_IN -to-Switch Toff				10	
$T_{SK(O)}$	Inter-Pair Output Skew (CH-CH)	Rsc and RL = 50 Ω, See Figure 5		10	20	ps
$T_{SK(b-b)}$	Intra-Pair Output Skew (bit-bit)			10	20	ps
C_{ON}	Outputs ON Capacitance	V_{IN} = V_{CC} or 0V, Outputs Open, Switch ON		6	7.5	pF

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ELECTRICAL CHARACTERISTICS – SIGNAL SWITCH PARAMETERS (continued)

(under recommended operating conditions; RL, Rsc = 50Ω, CL = 10pF unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
C_{OFF}	Outputs OFF Capacitance	V_{IN} = V_{CC} or 0V, Outputs Open, Switch OFF		3.5	6	pF
R_{ON}	Output ON resistance	V_{CC} = 3V, V_{IN} = 0V, I_O = 30 mA		3	6	Ω
		V_{CC} = 3V, V_{IN} = 2.4V, I_O = –15 mA		3.4	6	
ΔR_{ON}	On resistance match	V_{CC} = 3V, V_{IN} = 0V, I_O = 30 mA		0.2		Ω
		V_{CC} = 3V, V_{IN} = 1.7V, I_O = –15 mA		0.2		
R_{FLAT_ON}	On resistance flatness [$R_{ON(MAX)}$ – $R_{ON(MIN)}$]	V_{CC} = 3V, V_{IN} = 0V, I_O = 30 mA		1		W
		V_{CC} = 3V, V_{IN} = 1.7V, I_O = –15 mA		1		
X_{TALK}	Differential Crosstalk (VCM = 0V)	RL = 50 W, f = 250 MHz		–40		dB
O_{IRR}	Differential Off-Isolation (VCM = 0V)	RL = 50 W, f = 250 MHz		–41		dB
BW	Bandwidth	RL = 50 W		0.9		GHz

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TEST TIMING DIAGRAMS

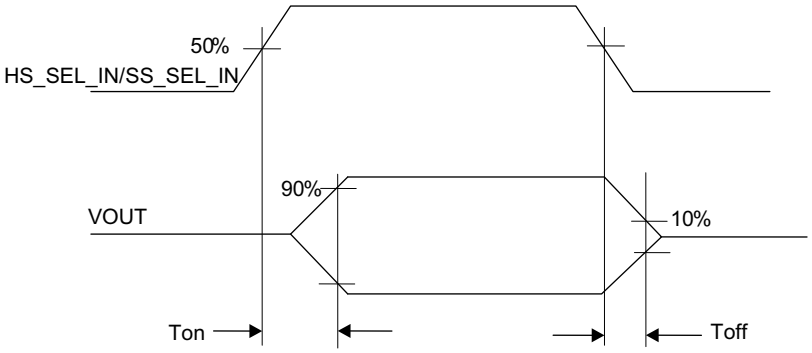
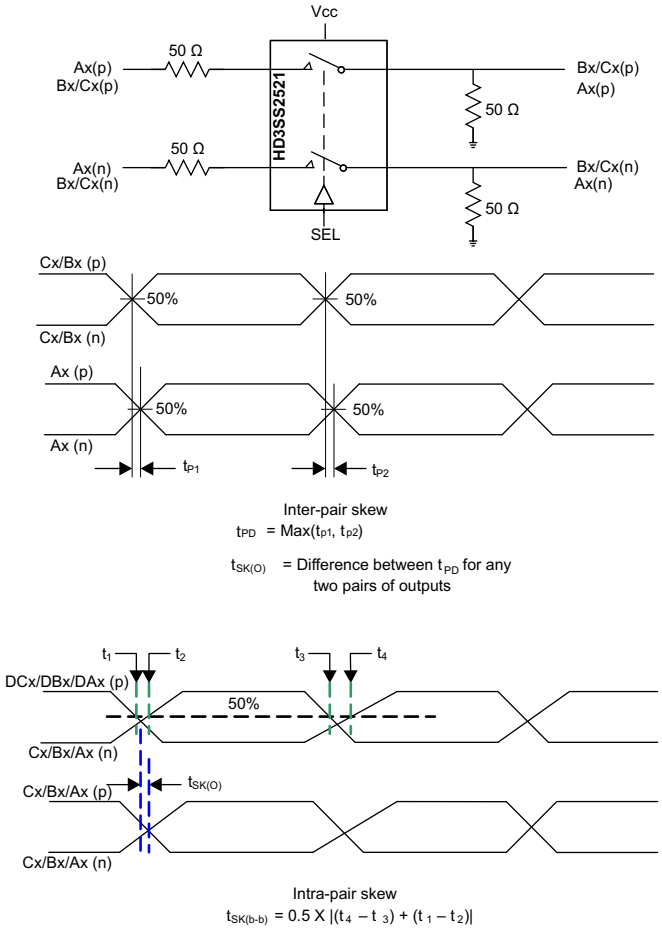


Figure 4. Select to Switch T_{on} and T_{off}



NOTES:

1. Measurements based on an ideal input with zero intra-pair skew on the input, i.e. the input at A to B/C or the input at B/C to A
2. Inter-pair skew is measured from lane to lane on the same channel, e.g. C0 to C1
3. Intra-pair skew is defined as the relative difference from the p and n signals of a single lane

Figure 5. Propagation Delay and Skew

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS2521RHUR	ACTIVE	WQFN	RHU	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 70	HD3S2521	Samples
HD3SS2521RHUT	PREVIEW	WQFN	RHU	56	250	TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

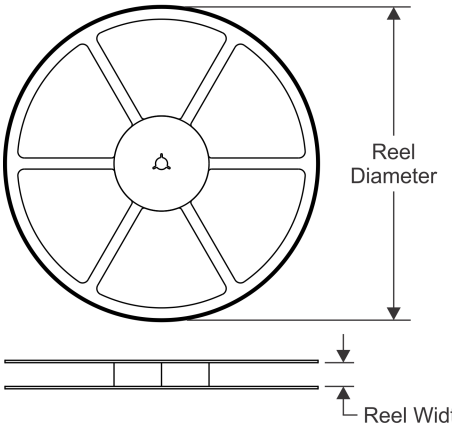
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

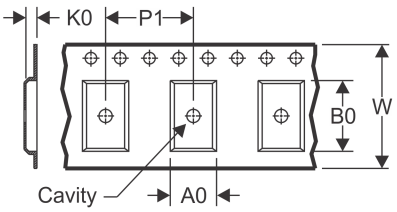
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

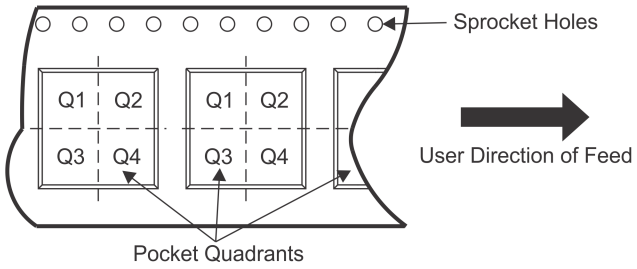


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

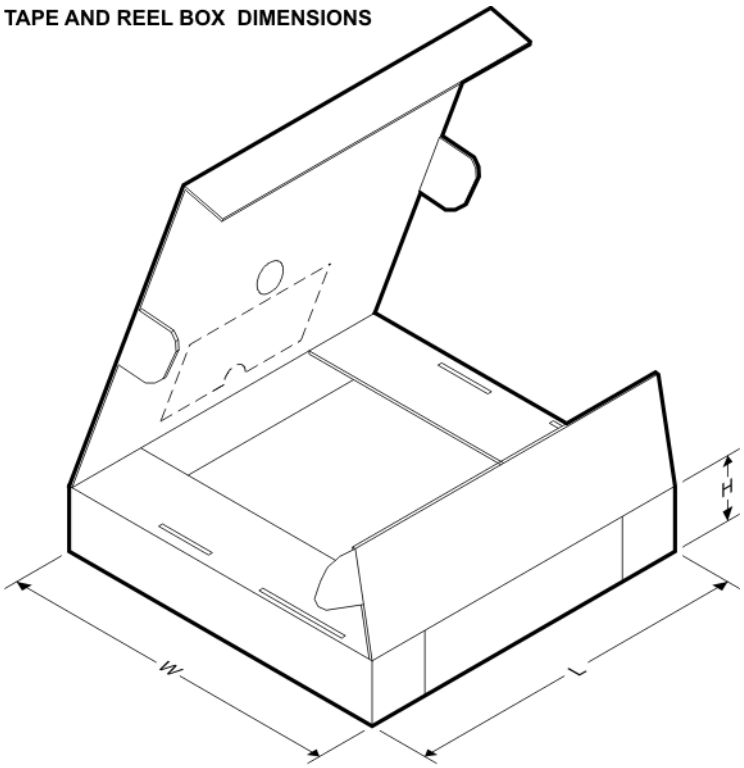
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS2521RHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1

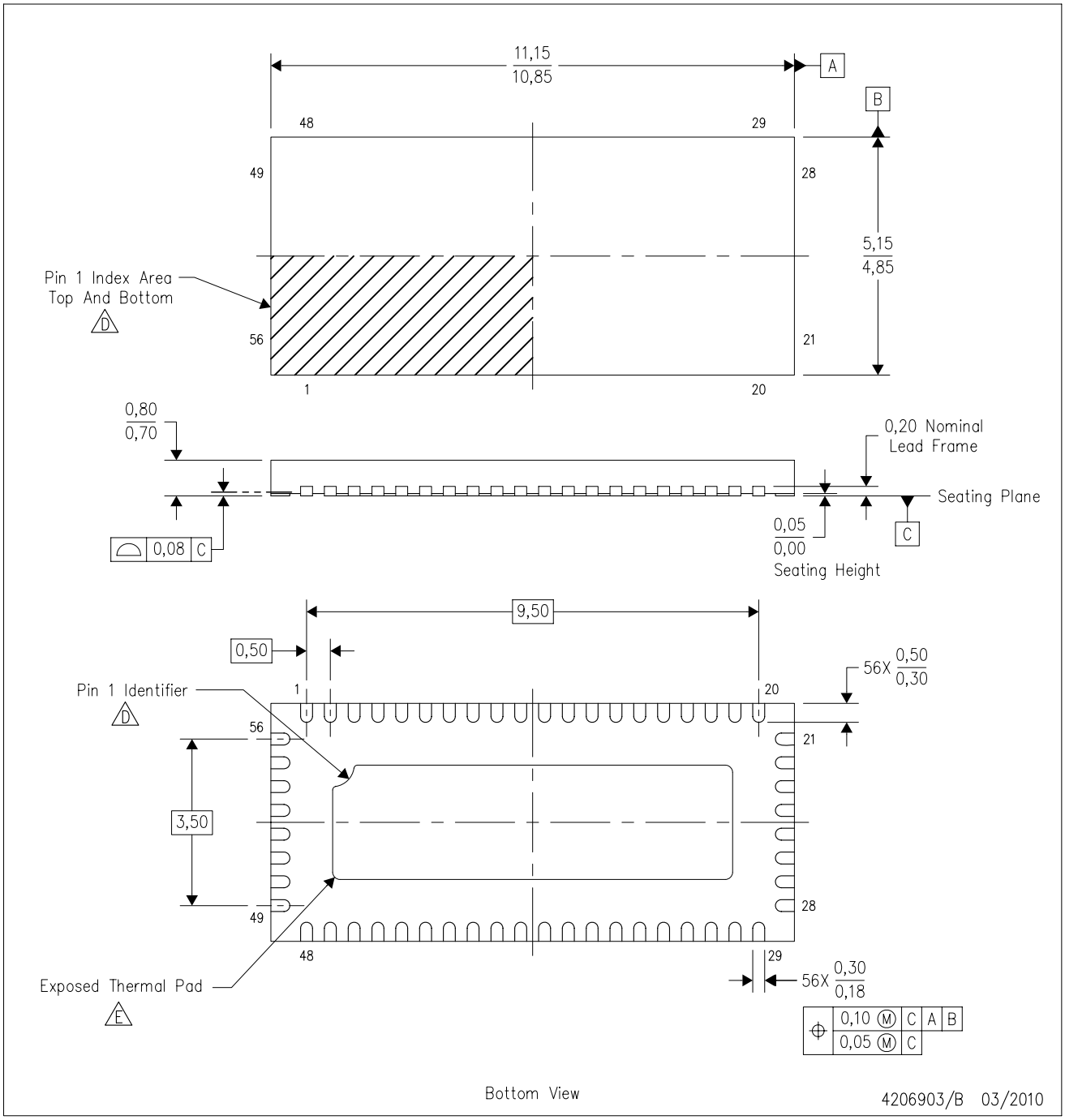
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS2521RHUR	WQFN	RHU	56	2000	367.0	367.0	45.0

RHU (R–PWQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



Notes:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
F. JEDEC MO–220 package registration is pending.

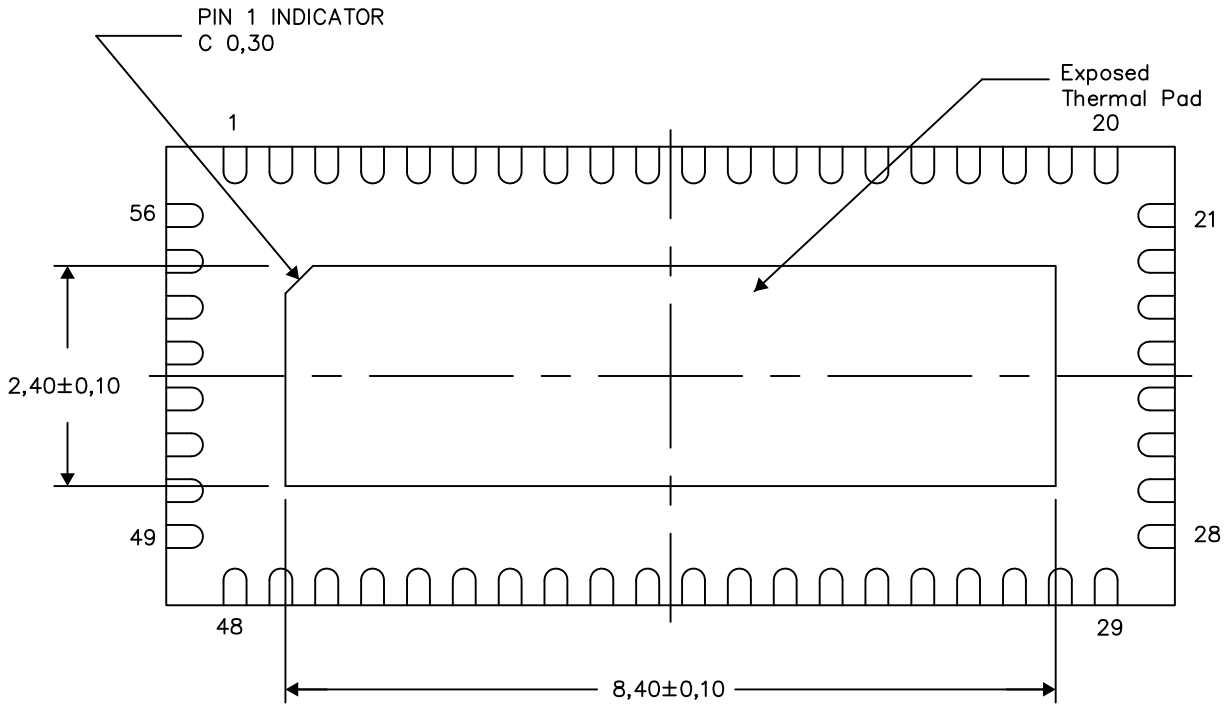
RHU (R–PWQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



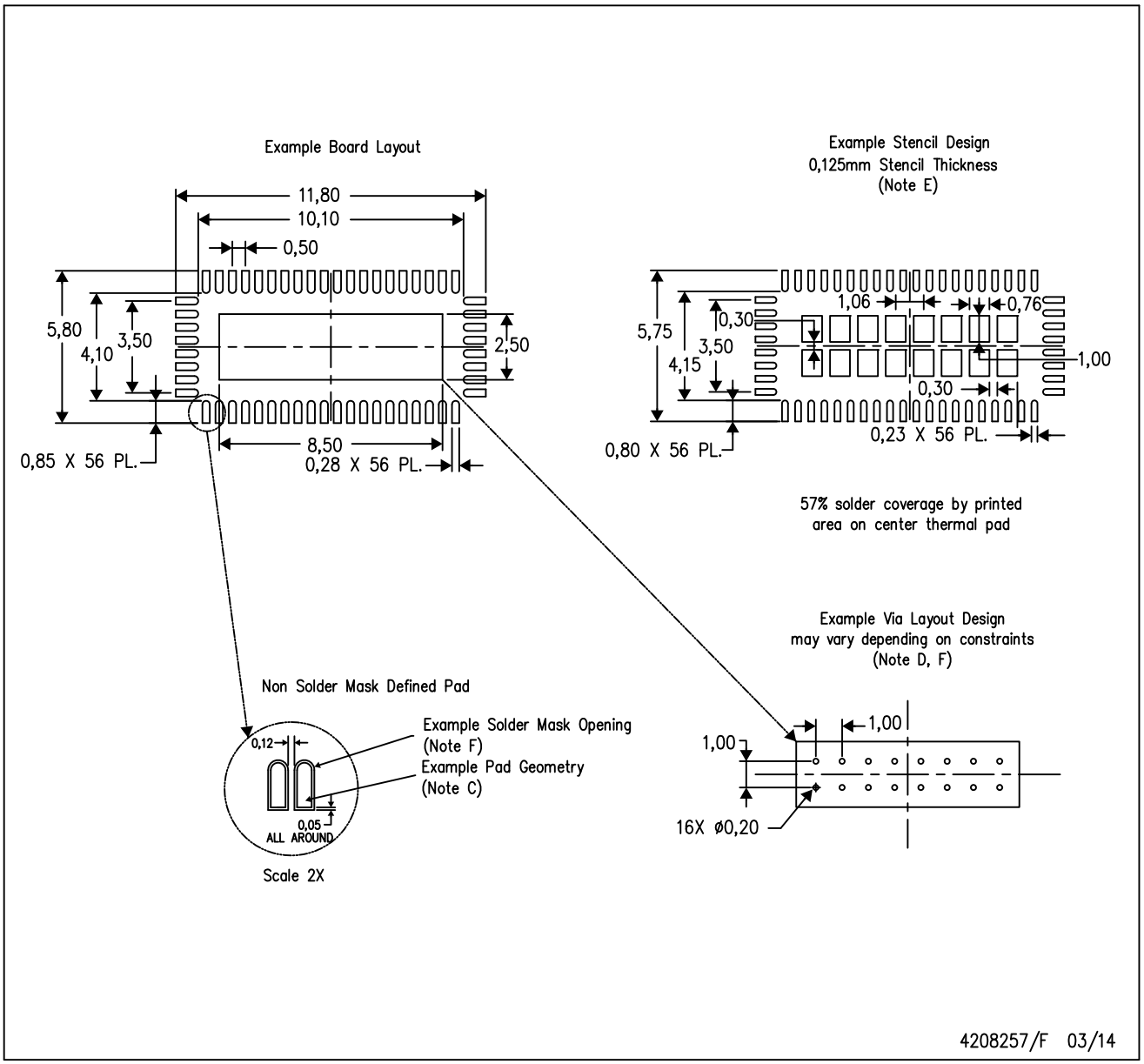
Bottom View

Exposed Thermal Pad Dimensions

4206904/G 03/14

NOTE: All linear dimensions are in millimeters

RHU (R–PWQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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