Preliminary

Document Title

4 Mbit CMOS 3.3 Volt-only Firmware Hub/LPC Flash Memory

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	September 23, 2005	Preliminary

AMIC

A49FL004

4 Mbit CMOS 3.3Volt-only Firmware Hub/LPC Flash Memory

Preliminary

FEATURES

- **Single Power Supply Operation**
  - Low voltage range: 3.0 V - 3.6 V
- **Standard Intel Firmware Hub/LPC Interface**
  - Read compatible to Intel® 82802 Firmware Hub devices
  - Conforms to Intel LPC Interface Specification Revision 1.1
- **Memory Configuration**
  - 512K x 8 (4 Mbit)
- **Block Architecture**
  - Uniform 4 KBytes Sectors
  - Uniform 64 KByte overlay blocks
  - Support full chip erase for Address/Address Multiplexed (A/A Mux) mode
- **Automatic Erase and Program Operation**
  - Build-in automatic program verification for extended product endurance
  - Typical 10 µs/byte programming time
  - Typical x s sector erase time
  - Typical y s block erase time
  - Typical z s chip erase time
- **Two Configurable Interfaces**
  - In-System hardware interface: Auto detection of Firmware Hub (FWH) or Low Pin Count (LPC) Interface for in-system read and write operations
  - Address/Address Multiplexed (A/A Mux) Interface for programming on EPROM Programmers during manufacturing
- **Firmware Hub (FWH)/Low Pin Count (LPC) Mode**
  - 33 MHz synchronous operation with PCI bus
  - 5-signal communication interface for in-system read and write operations
  - Standard SDP Command Set
  - $\overline{\text{Data}}$ Polling and Toggle Bit features
  - Block Locking Register for all blocks
  - Register-based read and write protection for each block
  - 4 ID pins for multiple chips selection
  - 5 GPI pins for General Purpose Input Register
  - $\overline{\text{TBL}}$ pin for hardware write protection to Boot Block
  - $\overline{\text{WP}}$ pin for hardware write protection to whole memory array except Boot Block

- **Address/Address Multiplexed (A/A Mux) Mode**
  - 11-pin multiplexed address and 8-pin data I/O interface
  - Supports fast programming on EPROM programmers
  - Standard SDP Command Set
  - $\overline{\text{Data}}$ Polling and Toggle Bit features
- **Lower Power Consumption**
  - Typical 12mA active read current
  - Typical 17mA program/erase current
- **High Product Endurance**
  - Guarantee 100,000 program/erase cycles per single sector (preliminary)
  - Minimum 20 years data retention
- **Compatible Pin-out and Packaging**
  - 32-pin (8 mm x 14 mm) TSOP
  - 32-pin PLCC
  - Optional lead-free (Pb-free) package
- **Hardware Data Protection**

GENERAL DESCRIPTION

The A49FL004 is a 4 Mbit 3.0 Volt-only Flash Memories used for BIOS storage in PCs and Notebooks. This device is designed to use a single low voltage, ranging from 3.0 Volt to 3.6 Volt, power supply to perform in-system or off-system read, erase and program operations. The device conforms to Intel® Low Pin Count (LPC) Interface specification revision 1.1 and also is compatible with Intel 82802 Firmware Hub (FWH) for most PC and Notebook applications. The A49FL004 supports two configurable interfaces: In-system hardware interface which can automatic detect the FWH or LPC memory cycle for in-system read and write operations, and Address/Address Multiplexed (A/A Mux) interface for fast manufacturing on EPROM Programmers. This device is designed to work with both Intel Family chipset and Non-Intel Family Chipset, it will provide PC and Notebook manufacturers great flexibility and simplicity for design, procurement, and material inventory.

The memory array of A49FL004 is divided into 128 uniform 4 KByte sectors or 8 uniform 64 KByte blocks (sector group - consists of sixteen adjacent sectors). The sector or block erase feature in the A49FL004 allows user to flexibly erase a memory area as 4Kbyte or 64 KByte by one single erase operation without affecting the data in others. The chip erase feature allows the whole memory to be erased in one single erase operation. The device can be programmed on a byte-by-byte basis after performing the erase operation.

The program operation of A49FL004 is executed by issuing the program command code into command register. The internal control logic automatically handles the programming voltage ramp-up and timing. The erase operation of the device is also executed by issuing the sector, block, or chip erase command code into command register. The internal control logic automatically handles the erase voltage ramp-up and timing. The device offer $\overline{\text{Data}}$ Polling and Toggle Bit functions in FWH/LPC and A/A Mux modes, the progress or completion of program and erase operation can be detected by reading the $\overline{\text{Data}}$ Polling on I/O_7 or Toggle Bit on I/O_6.

The A49FL004 has a 64 KByte top boot block. The boot block can be write protected by a hardware method controlled by the $\overline{\text{TBL}}$ pin or a register-based protection turned on/off by the Block Locking Registers (FWH or LPC mode only). The rest of blocks except boot block in the device also can be write protected by $\overline{\text{WP}}$ pin or Block Locking Registers (FWH or LPC mode only).

The A49FL004 is manufactured on AMIC 's advanced nonvolatile technology. The device is offered in 32-pin TSOP and PLCC packages with optional environmental friendly lead-free package.

PIN CONFIGURATIONS

Figure 1: 32-Pin PLCC

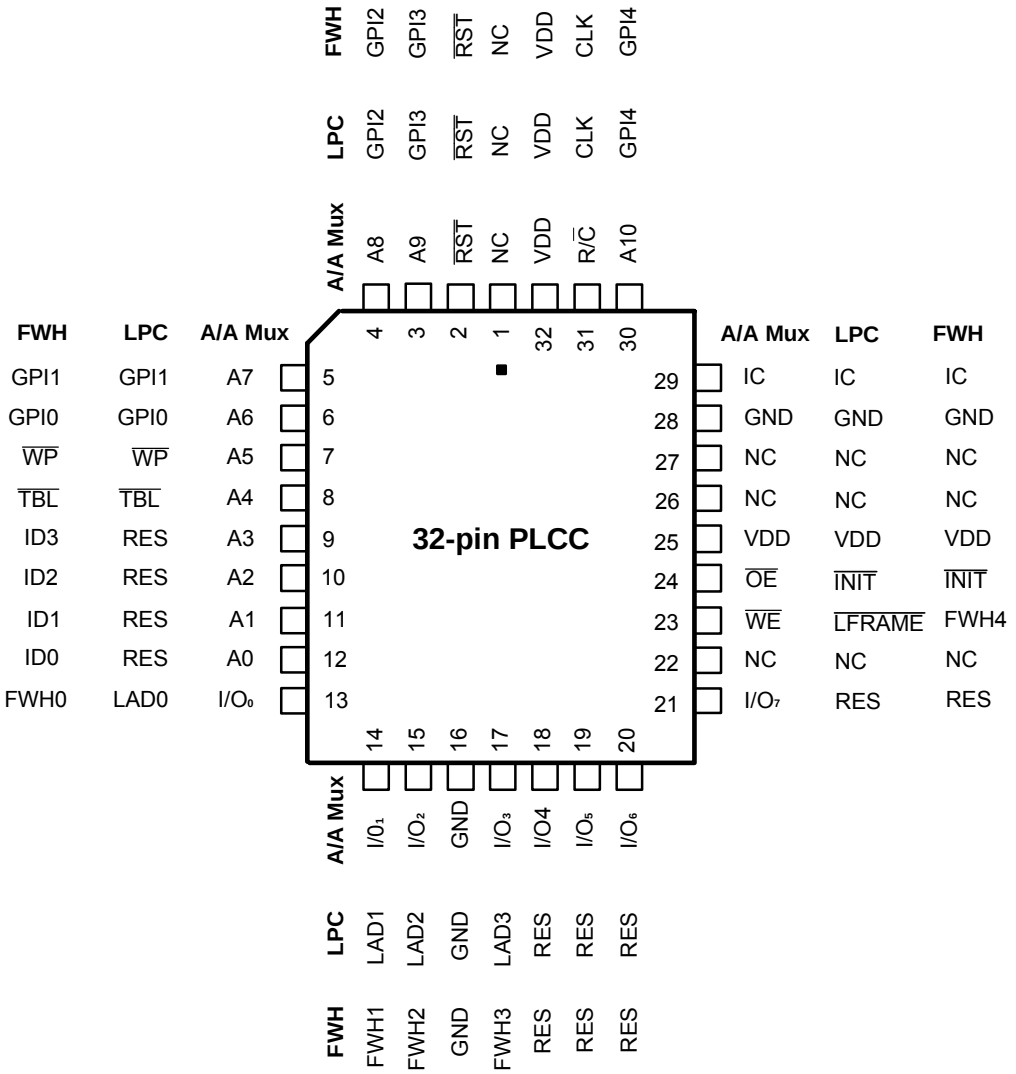


Figure 2: 32-Pin TSOP

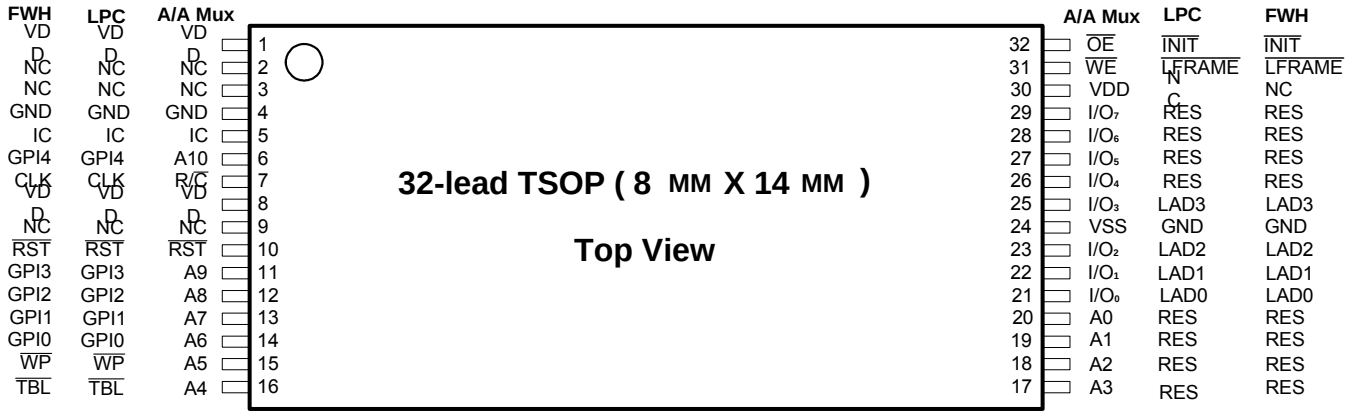


Figure 3: BLOCK DIAGRAM

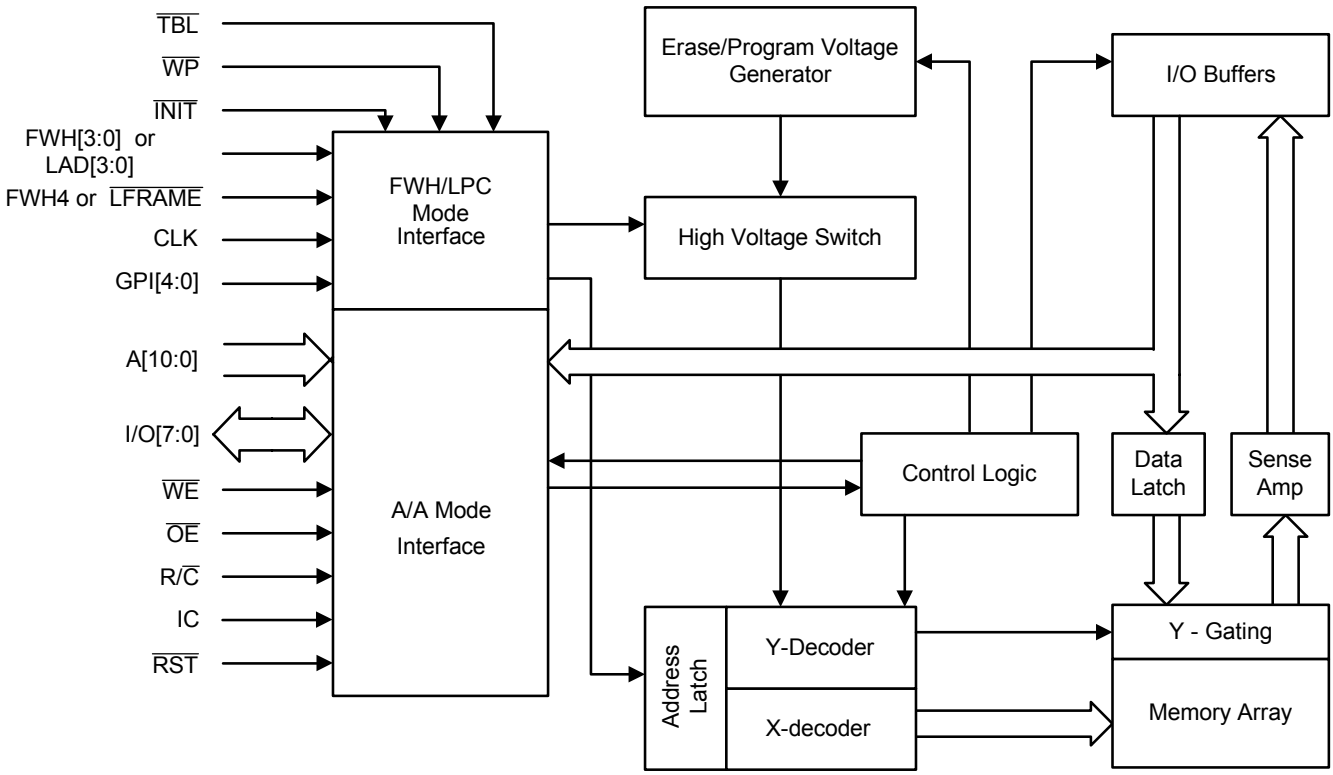


Table 1: Pin Description

Symbol	Type	Interface			Descriptions
		A/A	FWH	LPC	
A[10:0]	IN	X			Addresses Inputs: For inputting the multiplex address in A/A Mux mode. Row and column address are latched during a read or write cycle controlled by R/$\overline{C}$ pin.
I/O[7:0]	I/O	X			Data Inputs/Outputs: Used for A/A Mux mode only, to input command/data during write operation and to output data during Read operation. The data pins float to tri-state when $\overline{OE}$ is high.
$\overline{OE}$	IN	X			Output Enable: Control the device's output buffers during a read cycle. $\overline{OE}$ is a active low.
$\overline{WE}$	IN	X			Write Enable: Active the device for write operation. $\overline{WE}$ is active low.
IC	IN	X	X	X	Interface Configuration Select: This pin determines which mode is selected. When pulls high, the device enters into A/A Mux mode. When pulls low, FWH/LPC mode is selected. This pin must be setup during power-up or system reset, and stays no change during operation. This pin is internally pulled down with a resistor between 20-100 KΩ.
$\overline{INIT}$	IN		X	X	Initialize: This is the second reset pin for in-system use. $\overline{INIT}$ and $\overline{RST}$ pin are internally combined and initialize a device reset when driven low.
ID[3:0]	IN		X		These four pins are part of the mechanism that allows multiple FWH devices to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0]=0000b and it is recommended that all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ.
GPI[4:0]	IN		X	X	FWH/LPC General Purpose Inputs: Used to set the GPI_REG for system design purpose only. The value of GPI_REG can be read through FWH interface. The state of these pins can be read immediately at boot, through FWH/LPC internal registers. These pins should be set at desired state before the start of the PCI clock cycle for read operation and should remain on change until the end of the Read cycle. Unused GPI pins must not be floated.
$\overline{TBL}$	IN		X	X	Top Block Lock: When pulls low, it enables the hardware write protection the state for top boot block. When pulls high, it disables the hardware write protection.
FWH[3:0]	I/O		X		FWH Address and Data: The major I/O pins for transmitting data, address and command code in FWH mode.
CLK	IN		X	X	FWH/LPC Clock: To provide a synchronous clock for FWH and LPC mode operations.
FWH4	IN		X		FWH Input: To indicate the start of a FWH memory cycle operation. Also used to abort a FWH memory cycle in progress.
$\overline{RST}$	IN	X	X	X	Reset: To reset the operation of the device and return to standby mode.
$\overline{WP}$	IN		X	X	Write Protect: When pulls low, it enables the hardware write protection to the memory array except the top boot block. When pulls high, it disables hardware write protection except the top boot block.
R/$\overline{C}$	IN				Row/Column Select: To indicate to the row or column address in A/A Mux mode. When this pin goes low, the row address is latched. When this pin goes high, the column address is latched.
LAD[3:0]	I/O			X	LPC Address and Data: The major i/o pins for transmitting data, addresses and command code in LPC mode.
$\overline{LFRAME}$	IN			X	LPC Frame: To indicate the start of a LPC memory cycle operation. Also used to abort a LPC memory cycle in progress.
RES			X	X	Reserved. Reserved function pins for future use.
VDD		X	X	X	Device power supply.
VSS		X	X	X	Ground.
NC		X	X	X	No Connection.

Notes: IN=Input, I/O=Input/Output.

FWH MODE SELECTION

The A49FL004 can operate in two configurable interfaces: The In-System Hardware interface and Address/Address Multiplexed (A/A Mux) interface controlled by IC pin. If the IC pin is set to logic high (V_{IH}), the devices enter into A/A Mux interface mode. If the IC pin is set logic low (V_{IL}), the device will be in in-system hardware interface mode. During the in-system hardware interface mode, the device can automatically detect the Firmware Hub (FWH) or Low Pin Count (LPC) memory cycle sent from host system and response to the command accordingly. The IC pin must be setup during power-up or system reset, and stays no change during device operation.

When working in-system, typically on a PC or Notebook for Intel Platform, the A49FL004 enters into the FWH mode automatically. The device is configured to interface with its host using Intel's Firmware Hub proprietary protocol. Communication between the host (Intel ICH) and the A49FL004 occurs via the 4-bit I/O communication signal, FWH[3:0] and FWH4. In A/A Mux mode, the device is programmed via 11-bit address A[10:0] and 8-pin data I/O[7:0] interfaces. The address inputs are multiplexed in row and column selected by column the control signal R/$\overline{C}$. The column addresses are mapped to the higher internal addresses, and the row addresses are mapped to the lower internal addresses.

FWH MODE OPERATION

In FWH mode, the A49FL004 is connected through a 5-pin communication interface - FWH[3:0] and FWH4 pins to work with Intel® Family of I/O Controller Hubs (ICH) chipset platforms. The FWH mode also supports JEDEC standard Software Data Protection (SDP) product ID entry, byte program, sector erase, and block erase command sequences. The chip erase command sequence is only available in A/A Mux mode.

The addresses and data are transmitted through the 4-bit FWH[3:0] bus synchronized with the input clock on CLK pin during a FWH memory cycle operation. The address or data on FWH[3:0] bus is latched on the rising edge of the clock. The device enters standby mode when FWH4 is high and no internal operation is in progress. The device is in ready mode when FWH4 is low and no activity is on the bus.

FWH Read Operation

FWH Read Operations read from the memory cells or specific registers in the FWH device. A valid FWH Read operation starts when FWH4 is Low as CLK rises and a START value "1101b" is on FWH[3:0]. Addresses and data are transferred to and from the device decided by a series of "fields". Field sequences and contents are strictly defined for FWH Read Operations. Refer to Table 2 for FWH Read Cycle definition.

FWH Write Operation

FWH Write operations write the FWH Interface or FWH registers. A valid FWH Write operation starts when FWH4 is Low as CLK rises and a START value "1110b" is on FWH[3:0]. Addresses and data are transferred to and from the device decided by a series of "fields". Field sequences and contents are strictly defined for FWH Write operations. Refer to Table 3 for FWH Write Cycle Definition.

FWH Abort Operation

The FWH4 signal indicates the start of a memory cycle or the termination of a cycle in FWH mode. Asserting FWH4 for one or more clock cycle with a valid START value on FWH[3:0] will initiate a memory read or memory write cycle. If the FWH4 is driven low again for one or more clock cycles during this cycle, this cycle will be terminated and the device will wait for the ABORT command "1111b" to release the FWH[3:0] bus. If the abort occurs during the program or erase operation such as checking the operation status with $\overline{\text{Data}}$ Polling (I/O_7) or Toggle Bit (I/O_6) pins, the read status cycle will be aborted but the internal program or erase operation will not be affected. Only the reset operation initiated by $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ pin can terminate the program or erase operation.

Response To Invalid Fields

During FWH operations, the device will not explicitly indicate that it has received invalid field sequences. The response to specific invalid fields or sequences is as follows:

Address out range: The FWH address sequence is 7 fields long (28 bits), but only the last five address fields (20 bits) will be decoded by A49FL004. Address A22 has the special function of directing reads and writes to the flash memory (A22=1) or to the register space (A22=0).

Invalid IMSIZE Field: If the FWH device receives and invalid size field during a Read or Write operation, the device will reset and no operation will be attempted. The A49FL004 will not generate any kind of response in this situation. Invalid size field for a Read/Write cycles are anything but "0000b".

Table 2: FWH Read Cycle

Clock Cycle	Field	FWH[3:0]	Direction	Descriptions
1	START	1101	IN	Start of Cycle: “1101b” to indicate the start of a memory read cycle. FWH4 must be active (low) for the part to respond. Only the last start field (before FWH4 transition high) should be recognized. The start field contents indicate and FWH read cycle.
2	IDSEL	0000 to 1111	IN	ID Select Cycle: Indicates which FWH device should respond. If the IDSEL field matches the value set on ID[3:0] pins, then the particular FWH device will respond to subsequent commands.
3-9	IMADDR	YYYY	IN	Address Cycle: This is the 28-bit memory address. The addressed transfer most-significant nibble first and least-significant nibble last. (i.e., a27-24 on FWH[3:0] first, and A3-A0 on FWH[3:0] last).
10	IMSIZE	0000	IN	Memory Size Cycle: Indicates how many bytes will be or transferred during multi-byte operations. The A49FL004 only support “0000b” for one byte operation.
11	TAR0	1111	IN then Float	Turn-Around cycle 0: The master (Intel ICH) has driven the bus to all”1”s and then float the bus.
12	TAR1	1111 (Float)	Float then OUT	Turn-Around cycle 1: The device takes control of the bus during this cycle.
13	RSYNC	0000 (READY)	OUT	Ready Sync: The FWH device indicates the least-significant nibble of data byte will be ready in next clock cycle.
14-15	DATA	YYYY	OUT	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., $I/O_3 – I/O_0$ on FWH[3:0] first, then $I/O_7 – I/O_4$ on FWH[3:0] last).
16	TAR0	1111	OUT then Float	Turn-Around cycle 0: The FWH device has driven the bus to all “1”s and then float the bus.
17	TAR1	1111 (Float)	Float then IN	Turn-Around cycle 1: The master (Intel ICH) resumes control of the bus during this cycle.

Figure 4: FWH Memory Read Cycle Waveforms

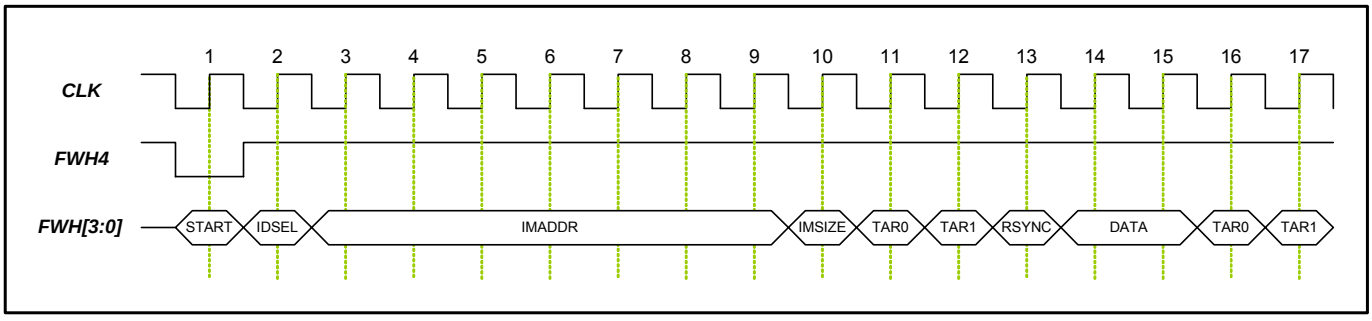
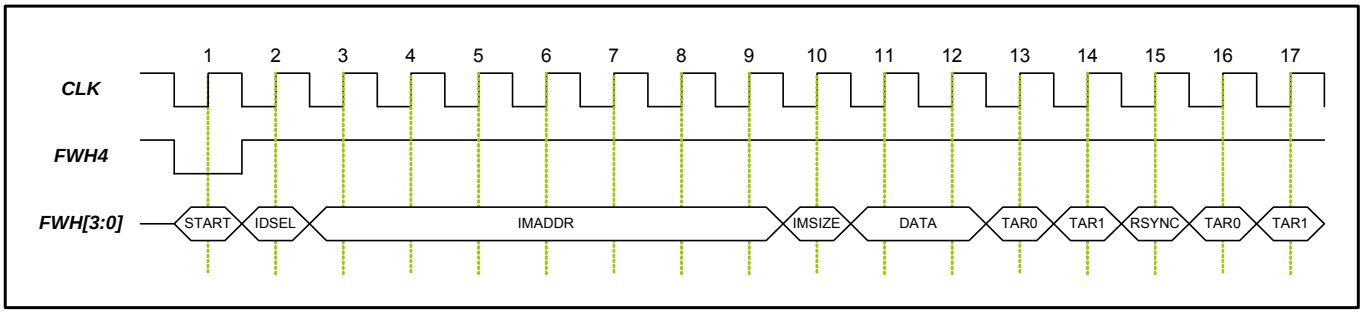


Table 3: FWH Write Cycle

Clock Cycle	Field	FWH[3:0]	Direction	Descriptions
1	START	1101	IN	Start of Cycle: “1101b” to indicate the start of a memory write cycle. FWH4 must be active (low) for the part to respond. Only the last start field (before FWH4 transitioning high) should be recognized. The START field contents indicate an FWH write cycle.
2	IDSEL	0000 to 1111	IN	ID Select Cycle: Indicates which FWH device should respond. If the IDSEL field matches the value set on ID[3:0] pins, then the particular FWH device will respond to subsequent commands.
3-9	IMADDR	YYYY	IN	Address Cycle: This is the 28-bit memory address. The addressed transfer most-significant nibble first and least-significant nibble last. (i.e., a27-24 on FWH[3:0] first, and A3-A0 on FWH[3:0] last).
10	IMSIZE	0000	IN	Memory Size Cycle: Indicates how many bytes will be or transferred during multi-byte operations. The A49FL004 only supports “0000b” for one byte operation.
11-12	DATA	YYYY	IN	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., $I/O_3 – I/O_0$ on FWH[3:0] first, then $I/O_7 – I/O_4$ on FWH[3:0] last).
13	TAR0	1111	IN then Float	Turn-Around cycle 0: The master (Intel ICH) has driven the bus to all”1”s and then float the bus.
14	TAR1	1111 (Float)	Float then OUT	Turn-Around cycle 1: The device takes control of the bus during this cycle.
15	RSYNC	0000 (Ready)	OUT	Ready Sync: The FWH device indicates that it has received the data or command.
16	TAR0	1111	OUT then Float	Turn-Around cycle 0: The FWH device has driven the bus to all “1”s and then float the bus.
17	TAR1	1111 (Float)	Float then IN	Turn-Around cycle 1: The master (Intel ICH) resumes control of the bus during this cycle.

Figure 5: FWH Write Waveforms



LPC MODE SELECTION

The A49FL004 can operate in two configurable interfaces: The In-System Hardware interface and Address/Address Multiplexed (A/A Mux) interface controlled by IC pin. If the IC pin is set to logic high (V_{IH}), the devices enter into A/A Mux interface mode. If the IC pin is set logic low (V_{IL}), the devices will be in in-system hardware interface mode. During the in-system hardware interface mode, the devices can automatically detect the Firmware Hub (FWH) or Low Pin Count (LPC) memory cycle sent from host system and response to the command accordingly. The IC pin must be setup during power-up or system reset, and stays no change during device operation.

When working in-system, typically on a PC or Notebook for non Intel Platform, the A49FL004 is connected to the host system through a 5-pin communication interface operated based on a 33-MHz synchronous clock. The 5-pin interface is defined as LAD[3:0] and $\overline{\text{LFRAME}}$ pins under LPC mode for easy understanding as to those existing compatible products. When working off-system, typically on a EPROM Programmer, the device is operated through 11-pin multiplexed address - A[10:0] and 8-pin data I/O - I/O[7:0] interfaces. The memory addresses of device are input through two bus cycles as row and column addresses controlled by a R/$\overline{\text{C}}$ pin.

LPC MODE OPERATION

In LPC mode, the A49FL004 is connected through a 5-pin communication interface - LAD[3:0] and $\overline{\text{LFRAME}}$ pins to work with non Intel® Family of South Bridge chipset platforms. The LPC mode also supports JEDEC standard Software Data Protection (SDP) product ID entry, byte program, sector erase, and block erase command sequences. The chip erase command sequence is only available in A/A Mux mode.

The addresses and data are transmitted through the 4-bit LAD[3:0] bus synchronized with the input clock on CLK pin during a LAD memory cycle operation. The address or data on LAD[3:0] bus is latched on the rising edge of the clock. The pulse of $\overline{\text{LFRAME}}$ pin is inserted for one clock indicates the start of a LPC memory read or memory write cycle. The address or data on LAD[3:0] is latched on the rising edge of CLK. The device enters standby mode when $\overline{\text{LFRAME}}$ is high and no internal operation is in progress. The device is in ready mode when $\overline{\text{LFRAME}}$ is low and no activity is on the LPC bus.

LPC Mode Memory Read/Write Operation

In LPC mode, the A49FL004 uses the 5-pin LPC interface includes 4-bit LAD[3:0] and $\overline{\text{LFRAME}}$ pins to communicate with the host system. The addresses and data are transmitted through the 4-bit LAD[3:0] bus synchronized with the input clock on CLK pin during a LPC memory cycle operation. The address or data on LAD[3:0] bus is latched on the rising edge of the clock. The pulse of $\overline{\text{LFRAME}}$ signal inserted for one or more clocks indicates the start of a LPC memory read or write cycle.

Once the LPC memory cycle is started, asserted by $\overline{\text{LFRAME}}$, a START value “0000b” is expected by the device as a valid command cycle.

Then a CYCTYPE + DIR value (“010xb” for memory read cycle or “011xb” for memory write cycle) is used to indicates the type of memory cycle. Refer to Table 4 and 5 for LPC Memory Read and Write Cycle Definition.

There are 8 clock fields in a LPC memory cycle that gives a 32 bit memory address A31 - A0 through LAD[3:0] with the most-significant nibble first. The memory space of A49FL004 is mapped directly to top of 4 Gbyte system memory space. See Figure 8 for System Memory Map.

The A49FL004 is mapped to the address location of (FFFFFFFFh - FFF80000h), the A31- A19 must be loaded with “1” to select and activate the device during a LPC memory operation. Only A18 - A0 is used to decode and access the 512 KByte memory.

LPC Abort Operation

The $\overline{\text{LFRAME}}$ is driven low for one or more clock cycles during a LPC cycle, the cycle will be terminated and the device will wait for the ABORT command. The host may drive the LAD[3:0] with “1111b” (ABORT command) to return the device to the ready mode. If abort occurs during a Write operation such as checking the operation status with $\overline{\text{Data}}$ Polling (I/O$_7$) or Toggle Bit (I/O$_6$) pins, the read status cycle will be aborted but the internal program or erase operation will not be affected. In this case, only the reset operation initiated by $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ pin can terminate the write operation.

Response TO Invalid Fields

During LPC operations, the A49FL004 will not explicitly indicate that it has received invalid field sequences. The responses to specific invalid fields or sequence is as follows:

Address out of range: The A49FL004 will only response to address range as specified in Table 9. Address A22 has the special function of directing reads and writes to the flash memory (A22=1) or to the register space (A22=0).

ID mismatch: The A49FL004 will compare ID bits in the address field with the hardware strapping. If there is a mismatch, the device will ignore the cycle.

Table 4: LPC Memory Read Cycle Definition

Clock Cycle	Field	LAD[3:0]	Direction	Descriptions
1	START	0000	IN	Start of Cycle: "0000b" indicates the start of a LPC memory cycle. LFRAME must be active low (low) for the part to respond. Only the last field latched before LFRAME transitions high will be recognized.
2	CYCTYPE + DIR	010x	IN	Cycle Type: Indicates the type of a LPC memory read cycle. CYCTYPE: Bits 3-2 must be "01b" for memory cycle. DIR: Bit 1 = "0b" indicates the type of cycle for Read. Bit 0 is reserved.
3-10	ADDR	YYYY	IN	Address Cycles: This is the 32-bit memory address. The addressed transfer most-significant nibble first and least-significant nibble last. (i.e., a31-28 on LAD[3:0] first, and A3-A0 on LAD[3:0] last).
11	TAR0	1111	IN Then Float	Turn-Around cycle 0: The host has driven the bus to all"1"s and then float the bus.
12	TAR1	1111 (Float)	Float then OUT	Turn-Around cycle 1: The A49FL004 takes control of the bus during this cycle.
13	SYNC	0000	OUT	Sync: The device indicates the least-significant nibble of data byte will be ready in next clock cycle.
14-15	DATA	1111	OUT	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., I/O_3 – I/O_0 on LAD[3:0] first, then I/O_7 – I/O_4 on LAD[3:0] last).
16	TAR0	1111	IN then Float	Turn-Around cycle 0: The host has driven the bus to all "1"s and then float the bus.
17	TAR1	1111 (Float)	Float then OUT	Turn-Around cycle 1: The A49FL004 resumes control of the bus during this cycle.

Figure 6: LPC Single-Byte Read Waveforms

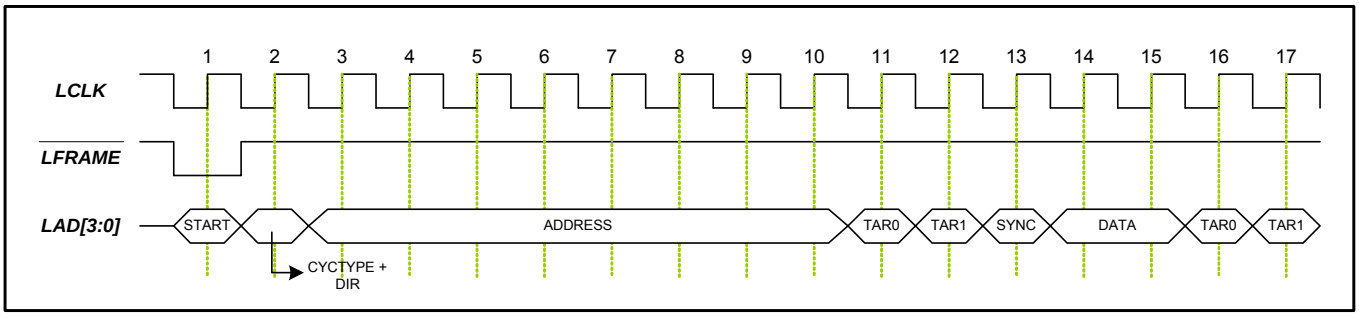
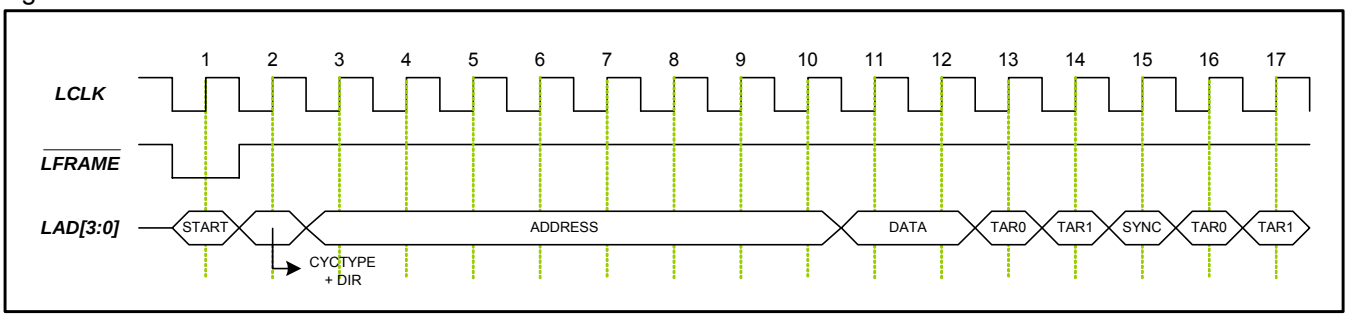


Table 5: LPC Memory Write Cycle Definition

Clock Cycle	Field	LAD[3:0]	Direction	Descriptions
1	START	0000	IN	Start of Cycle: "0000b" to indicate the start of a LPC memory cycle. LFRAME must be active low (low) for the part to respond. Only the last field latched before LFRAME transitions high will be recognized.
2	CYCTYPE + DIR	011x	IN	Cycle Type: Indicates the type of a LPC memory write cycle. CYCTYPE: Bits 3-2 must be "01b" for memory cycle. DIR: Bit 1 = "1b" indicates the type of cycle for Write. Bit 0 is reserved.
3-10	ADDR	YYYY	IN	Address Cycles: This is the 32-bit memory address. The addressed transfer most-significant nibble first and least-significant nibble last. (i.e., a31-28 on LAD[3:0] first, and A3-A0 on LAD[3:0] last).
11-12	DATA	YYYY	IN	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., I/O_3 – I/O_0 on LAD[3:0] first, then I/O_7 – I/O_4 on LAD[3:0] last).
13	TAR0	1111	IN then Float	Turn-Around cycle 0: The host has driven the bus to all"1"s and then float the bus.
14	TAR1	1111 (Float)	Float then OUT	Turn-Around cycle 1: The A49FL004 takes control of the bus during this cycle.
15	SYNC	0000	OUT	Sync: The device indicates the least-significant nibble of data byte will be ready in next clock cycle.
16	TAR0	1111	OUT then Float	Turn-Around cycle 0: The A49FL004 has driven the bus to all "1"s and then float the bus.
17	TAR1	1111 (Float)	Float then IN	Turn-Around cycle 1: The host resumes control of the bus during this cycle.

Figure 7: LPC Write Waveforms



Multiple Device Selection

Multiple A49FL004 devices may be strapped to increase memory densities in a system. The four ID pins, ID[3:0], allow up to 16 devices to be attached to the same bus by using different ID strapping in a system, BIOS support, bus loading, or the attaching bridge may limit this number. The boot device must have an ID of "0000b" (determined by ID[3:0]); subsequent devices use incremental numbering, equal density must be used with multiple devices.

Multiple Device Selection for Firmware Hub Memory Cycle

For Firmware Memory Read/Write cycles, hardware strapping values on ID[3:0] must match the values in IDSEL field. See Table x for multiple device selection configurations. The A49FL004 will compare the IDSEL field with ID[3:0] 's strapping values. If there is a mismatch, the device will ignore the reminder of the cycle.

Table 6: FWH Multiple Device Selection Configuration

Device #	ID[3:0]	IDSEL
0 (Boot Device)	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	1000
9	1001	1001
10	1010	1010
11	1011	1011
12	1100	1100
13	1101	1101
14	1110	1110
15	1111	1111

Multiple Device Selection for LPC Memory Cycle

For LPC Memory Read/Write cycles, ID information is included in the address bits of every cycle. The ID bits in the address field are the reverse of the hardware strapping. See Table x2 for multiple device selection configurations. The A49FL004 will compare these bits with ID[3:0]'s strapping values. If there is a mismatch, the device will ignore the remainder of the cycle.

Table 7: LPC Multiple Device Selection Configuration

Device #	ID[3:0]	Address Range
0 (Boot Device)	0000	1111
1	0001	1110
2	0010	1101
3	0011	1100
4	0100	1011
5	0101	1010
6	0110	1001
7	0111	1000
8	1000	0111
9	1001	0110
10	1010	0101
11	1011	0100
12	1100	0011
13	1101	0010
14	1110	0001
15	1111	0000

Register

The A49FL004 has two registers include the General Purpose Inputs Register (GPI_REG) and Block Locking Register (BL_REG). Both registers are available in FWH and LPC mode only. The GPI_REG can be read at FFBC0100h in the 4 GByte system memory map. The BL_REG can be read through FFBx0002h where x=F-0h. Refer to table 9 for BL_REG.

General Purpose Inputs Register

The A49FL004 contains and 8-bit General Purpose Inputs Register (GPI_REG) available in FWH and LPC modes. Only Bit 4 to Bit 0 are used in the current version, and bit 7 to bit 5 are reserved for the future use. The GPI_REG is a pass-through register with the value set by GPI[4:0] pin during power-up. The GPI_REG is used for the system design purpose only, the device does not use this register. This register is read only and can be read at address location FFBC0100h in the 4 Gbyte system memory map through a memory read cycle. Refer to Table 8 for General Purpose Input Register Definition.

Table 8: General Purpose Inputs Register

Bit	Bit Name	Function	Pin Number	
			32-PLCC	32-TSOP
7:5	-	Reserved	-	-
4	GPI[4]	GPI_REG Bit 4	30	6
3	GPI[3]	GPI_REG Bit 3	3	11
2	GPI[2]	GPI_REG Bit 2	4	12
1	GPI[1]	GPI_REG Bit 1	5	13
0	GPI[0]	GPI_REG Bit 0	6	14

Block Locking Registers

The A49FL004 supports block read-lock, write-lock, and lockdown features through a set of Block Locking Registers. Each memory block has an associated 8-bit read/writable block locking register. Only Bit 2 to Bit 0 are used in current version and Bit 7 to Bit 3 are reserved for future use. The default value of BL_REG is “01h” at power up. The definition of BL_REG is listed in Table 8. The FWH/LPC Register Configuration Map of A49FL004 is shown in Table 9. Unused register will be read as 00h

Table 9: A49FL004 Block Locking Register Address

Memory Address	Mnemonic	Register Name	Protected Block Address Range
FFBF0002h	T_BLOCK_LK	Top Block Lock Register (Block 64)	70000h – 7FFFFh
FFBE0002h	T_MINUS01_LK	Top Block [-1] Lock Register (Block 64)	60000h – 6FFFFh
FFBD0002h	T_MINUS02_LK	Top Block [-2] Lock Register (Block 64)	50000h – 5FFFFh
FFBC0002h	T_MINUS03_LK	Top Block [-3] Lock Register (Block 64)	40000h – 4FFFFh
FFBB0002h	T_MINUS04_LK	Top Block [-4] Lock Register (Block 64)	30000h – 3FFFFh
FFBA0002h	T_MINUS05_LK	Top Block [-5] Lock Register (Block 64)	20000h – 2FFFFh
FFB90002h	T_MINUS06_LK	Top Block [-6] Lock Register (Block 64)	10000h – 1FFFFh
FFB80002h	T_MINUS07_LK	Top Block [-7] Lock Register (Block 64)	00000h – 0FFFFh

Table 10: Block Lock Register Bit Definition

Data	Reserved Bit 7:3	Read-Lock Bit 2	Lock-Down Bit 1	Write-Lock Bit 0	Function
00h	00000	0	0	0	Full Access.
01h	00000	0	0	1	Write locked. Default state at power-up.
02h	00000	0	1	0	Locked open (full access locked down).
03h	00000	0	1	1	Write-locked down.
04h	00000	1	0	0	Read locked.
05h	00000	1	0	1	Read and Write locked.
06h	00000	1	1	0	Read-locked down
07h	00000	1	1	1	Read-locked and Write-locked down

Data	Function
7:3	**Reserved**
2	**Read-Lock** 1 = Prevents read operations in the block where set 0 = Normal operation for reads in the block where clear. This is the default state.
1	**Lock-Down** 1 = Prevents further set or clear operations to the Write-Lock and Read-Lock bits. Lock-Down only can be set but not clear. The block will remain lock-down until reset (with $\overline{RST}$ or $\overline{INIT}$), or until the device is power-on reset. 0 = Normal operation for Write-Lock and Read-Lock bit altering in the block where clear. This is the default state.
0	**Write-Lock** 1 = Prevents program or erase operations in the block where set. This is the default state. 0 = Normal operation for programming and erase in the block where clear.

ADDRESS/ADDRESS MULTIPLEXED (A/A MUX) MODE

Read/Write Operation

The A49FL004 offers a Address/Address Multiplexed (A/A Mux) mode for off-system operation, typically on an EPROM Programmer, similar to a traditional Flash memory except the address input is multiplexed. In the A/A Mux mode, the programmer must drive the $\overline{OE}$ pin to low (V_{IL}) for read or $\overline{WE}$ pins to low for write operation. The devices have no Chip Enable ($\overline{CE}$) pin for chip selection and activation as traditional Flash memory. The R/$\overline{C}$, $\overline{OE}$ and $\overline{WE}$ pins are used to activate the device and control the power.

The 11 multiplex address pins - A[10:0] and a R/$\overline{C}$ pin are used to load the row and column addresses for the target memory location. The row addresses (internal address A10 - A0) are latched on the falling edge of R/$\overline{C}$ pin. The column addresses (internal address A21 - A11) are latched on the rising edge of R/$\overline{C}$ pin. The A49FL004 use A18 - A0 respectively.

During a read operation, the $\overline{OE}$ signal is used to control the output of data to the 8 I/O pins - I/O[7:0]. During a write operation, the $\overline{WE}$ signal is used to latch the input data from I/O[7:0]. See Table 11 for Bus Operation Modes.

Table 11: A/A Mux Mode Operation Selection

Mode	$\overline{RST}$	$\overline{OE}$	$\overline{WE}$	Address	I/O
Read	V_{IH}	V_{IL}	V_{IH}	X (1)	D_{OUT}
Write	V_{IH}	V_{IH}	V_{IL}	X	D_{IN}
Standby	V_{IH}	V_{IH}	V_{IH}	X	High Z
Output Disable	V_{IH}	V_{IH}	X	X	High Z
Reset	V_{IL}	X	X	X	High Z
Product Identification	V_{IH}	V_{IL}	V_{IH}	A2 – A21 = X, A1 = V_{IL}, A0 = V_{IL}, and A1 = V_{IH}, A0 = V_{IH}	Manufacturer ID (2)
				A2 – A21= X, A1 = V_{IL}, A0 = V_{IH}	Device ID

Notes:
1. X can be V_{IL} OR V_{IH}.
2. Refer to Table 12 for the Manufacturer ID and Device ID of devices.

The A49FL004 provides three levels of data protection for the critical BIOS code of PC and Notebook. It includes memory hardware write protection, hardware data protection and software data protection.

Sector-Erase Operation

The A49FL004 contains 128 uniform 4 KByte sectors. A sector erase command is used to erase an individual sector. See Table 11 for Sector/Block Address Table.

In FWH/LPC mode, an erase operation is activated by writing the six-byte command sequence through six consecutive write memory cycles with Sector Erase Command (30h), and sector address (SA) in the last bus cycle.

In A/A Mux mode, an erase operation is activated by writing the six-byte command in six consecutive bus cycles. Pre-programs the sector is not required prior to an erase operation.

Block-Erase Operation

The A49FL004 contains eight uniform 64 KByte blocks. A block erase command is used to erase an individual block. See Table 13 for Sector/Block Address Table.

In FWH/LPC mode, an erase operation is activated by writing the six-byte command sequence through six consecutive write memory cycles with Block Erase Command (50h), and Block address (BA) in the last bus cycle.

In A/A Mux mode, an erase operation is activated by writing the six-byte command in six consecutive bus cycles. Pre-programs the block is not required prior to an erase operation.

Chip-Erase

The entire memory array can be erased by chip erase operation available under the A/A Mux mode operated by EPROM Programmer only. Pre-programs the device is not required prior to the chip erase operation. Chip erase starts immediately after a six-bus-cycle chip erase command sequence. All commands will be ignored once the chip erase operation has started. The $\overline{Data}$ Polling on I/O_7 or Toggle Bit on I/O_6 can be used to detect the progress or completion of erase operation. The device will return back to standby mode after the completion of the chip erase.

Write Operation Status Detection

In program operation, the data is programmed into the devices (to a logical “0”) on a byte-by-byte basis. In FWH and LPC mode, a program operation is activated by writing the three-byte command sequence and program address/data

through four consecutive memory write cycles. In A/A Mux mode, a program operation is activated by writing the three-byte command sequence and program address/data through four consecutive bus cycles.

The row address (A10 - A0) is latched on the falling edge of R/$\overline{C}$ and the column address (A21 - A11) is latched on the rising edge of R/$\overline{C}$. The data is latched on the rising edge of $\overline{WE}$. Once the program operation is started, the internal control logic automatically handles the internal programming voltages and timing.

A data "0" can not be programmed back to a "1". Only erase operation can convert "0"s to "1"s. The $\overline{Data}$ Polling on I/O7 or Toggle Bit on I/O6 can be used to detect when the programming operation is completed in FWH, LPC, and A/A Mux modes.

$\overline{Data}$ Polling (I/O7)

The device provides a $\overline{Data}$ Polling feature to indicate the progress or the completion of a program or erase operation in all modes. During a program operation, an attempt to read the device will result in the complement of the last loaded data on I/O7. Once the program cycle is complete, the true data of the last loaded data is valid on all outputs. During an erase operation, an attempt to read the device will result a "0" on I/O7. After the erase cycle is complete, an attempt to read the device will result a "1" on I/O7.

Toggle Bit (I/O6)

The A49FL004 also provides a Toggle Bit feature to detect the progress or the completion of a program or erase operation. During a program or erase operation, an attempt to read data from the devices will result in I/O6 toggling between "1" and "0". When the program or erase operation is complete, I/O6 will stop toggling and valid data will be read. Toggle bit may be accessed at any time during a program or erase operation.

Data Protection

The device features a software data protection function to protect the device from an unintentional erase or program operation. It is performed by JEDEC standard Software Data Protection (SDP) command sequences. See Table 14 for SDP Command Definition. A program operation is initiated by three memory write cycles of unlock command sequence.
A chip (only available in A/A Mux mode), sector or block erase operation is initiated by six memory write cycles of unlock command sequence. During SDP command sequence, any invalid command or sequence will abort the operation and force the device back to standby mode.

Memory Hardware Write Protection

The A49FL004 has a 64 KByte top boot block. When working in-system, the memory hardware write protection feature can be activated by two control pins - Top Block Lock ($\overline{TBL}$) and Write Protection ($\overline{WP}$) for both FWH and LPC modes. When $\overline{TBL}$ is pulled low (V_{IL}), the boot block is hardware write protected. A sector erase, block erase, or byte program command attempts to erase or program the boot block will be ignored. When $\overline{WP}$ is pulled low (V_{IL}), the Block 0 ~ Block 6 of A49FL004 (except the boot block) are hardware write protected. Any attempt to erase or program a sector or block within this area will be ignored.

Both $\overline{TBL}$ and $\overline{WP}$ pins must be set low (V_{IL}) for protection or high (V_{IH}) for un-protection prior to a program or erase operation. A logic level change on $\overline{TBL}$ or $\overline{WP}$ pin during a program or erase operation may cause unpredictable results.

The $\overline{TBL}$ and $\overline{WP}$ pins work in combination with the block locking registers. When active, these pins write protect the appropriate blocks regardless of the associated block locking registers setting.

Hardware Data Protection

Hardware data protection protects the devices from unintentional erase or program operation. It is performed by the device automatically in the following three ways:

(a) V_{DD} Detection: if V_{DD} is below 1.8 V (typical), the program and erase functions are inhibited.

(b) Write Inhibit Mode: holding any of the signal $\overline{OE}$ low, or $\overline{WE}$ high inhibits a write cycle (A/A Mux mode only).

(c) Noise/Glitch Protection: pulses of less than 5 ns (typical) on the $\overline{WE}$ input will not initiate a write cycle (A/A Mux mode only).

Reset

Any read, program, or erase operation to the devices can be reset by the $\overline{INIT}$ or $\overline{RST}$ pins. $\overline{INIT}$ and $\overline{RST}$ pins are internally hard-wired and have same function to the devices. The $\overline{INIT}$ pin is only available in FWH and LPC modes. The $\overline{RST}$ pin is available in all modes. It is required to drive $\overline{INIT}$ or $\overline{RST}$ pins low during system reset to ensure proper initialization.

During a memory read operation, pulls low the $\overline{INIT}$ or $\overline{RST}$ pin will reset the devices back to standby mode and then the FWH[3:0] of FWH interface or the LAD[3:0] of LPC interface will go to high impedance state. During a program or erase operation, pulls low the $\overline{INIT}$ or $\overline{RST}$ pin will abort the program or erase operation and reset the devices back to standby mode. A reset latency will occur before the devices resume to standby mode when such reset is performed. When a program or erase operation is reset before the completion of such operation, the memory contents of devices may become invalid due to an incomplete program or erase operation.

Product Identification

The product identification mode can be used to read the Manufacturer ID and the Device ID by a software Product ID Entry command in both in-system hardware interface and A/A Mux interface modes. The product identification mode is activated by three-bus-cycle command. Refer to Table 12 for the Manufacturer ID and Device ID of A49FL004 and Table 14 for the SDP Command Definition.

In FWH mode, the product identification can also be read directly at FFBC0000h for Manufacturer ID - "99h" and FFBC0001h for Device ID in the 4 GByte system memory map.

Table 12: Product Identification

Description	Address	Data
Manufacturer ID	00000h	37h
	00003h	7Fh
Device ID A49FL004	00001h	99h

Figure 8: System Memory Map and Device Memory Map for A49FL004

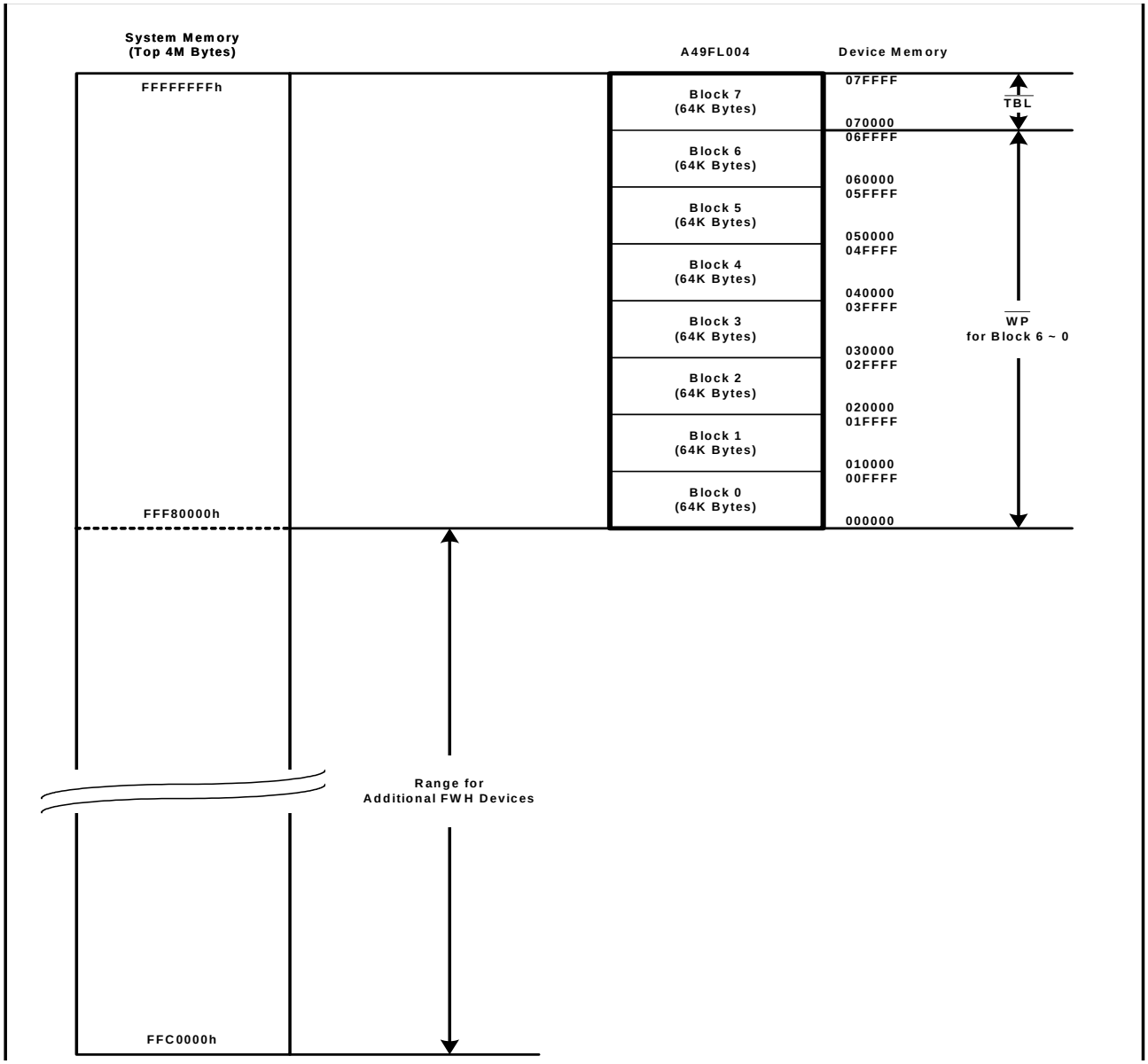


Table 13: Sector/Block Address Table

Hardware	Block	Block Size (Kbytes)	Sector	Sector Size (K bytes)	Sector Number	Address Range
$\overline{TBL}$	Block 7(Boot Block)	64	16	4 Kbytes/Sector	127	7F000h - 7FFFFh
					126	7E000h – 7EFFFh
					125	7D000h – 7DFFFh
					124	7C000h – 7CFFFh
					123	7B000h – 7BFFFh
					122	7A000h – 7AFFFh
					121	79000h – 79FFFh
					120	78000h – 78FFFh
					119	77000h – 77FFFh
					118	76000h – 76FFFh
					117	75000h – 75FFFh
					116	74000h – 74FFFh
					115	73000h - 73FFFh
					114	72000h – 72FFFh
					113	71000h – 71FFFh
					112	70000h - 70FFFh
$\overline{WP}$	Block 6	64	16	4 Kbytes/Sector	111 - 96	60000h - 6FFFFh
	Block 5	64	16	4 Kbytes/Sector	95 - 80	50000h - 5FFFFh
	Block 4	64	16	4 Kbytes/Sector	79 - 64	40000h - 4FFFFh
	Block 3	64	16	4 Kbytes/Sector	63 - 48	30000h - 3FFFFh
	Block 2	64	16	4 Kbytes/Sector	47 - 32	20000h - 2FFFFh
	Block 1	64	16	4 Kbytes/Sector	31 -16	10000h - 1FFFFh
	Block 0	64	16	4 Kbytes/Sector	15 - 0	00000h - 0FFFFh

Table 14: Software Data Protection Command Definition

Command	Bus Cycles	1st Cycle (1)		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr(2)	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Block Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA (4)	50H
Read	1	Addr	DOUT										
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA (3)	30H
Chip Erase (1)	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	Addr	DIN				
Product ID Entry	3	5555H	AAH	2AAAH	55H	5555H	90H						
Product ID Exit (5)	1	XXXXH	F0H										
Product ID Exit (5)	3	5555H	AAH	2AAAH	55H	5555H	F0H						

Notes:
1. Chip erase is available in A/A Mux Mode only.
2. Address A[15:0] is used for SDP command decoding internally and A15 must be “0” in FWH/LPC and A/A Mux modes. AMS - A16 = Don’t care where AMS is the most-significant address of A49FL004.
3. SA = Sector address to be erased.
4. BA = Block address to be erased.
5. Either one of the Product ID Exit command can be used.

DC and AC Operating Range

Range	A49FL004
Operating Temperature	0°C to +70°C
VDD Power Supply	3.0V –3.6V

Table 15: DC Operating Characteristics

Symbol	Parameter	Limits				Test Conditions
		Min	Typ	Max	Units	
I_{CC1}	Vcc Active Read Current (FWH/LPC)		2	15	mA	FWH4 or $\overline{LFRAME}$ = V_{IL}, f = 33MHz, I_{OUT} = 0mA, V_{DD} = $V_{DD\ Max}$
I_{CC2} (2)	Vcc Program/Erase Current		7	20	mA	
I_{SB}	Standby Vcc Current (FWH/LPC Mode)			500	µA	FWH4 or $\overline{LFRAME}$ = V_{IH}, f = 33MHz, V_{DD} = $V_{DD\ Max}$
I_{RY}	Ready Mode Vcc Current (FWH/LPC Mode)			10	mA	FWH4 or $\overline{LFRAME}$ = V_{IL}, f = 33MHz, I_{OUT} = 0mA, V_{DD} = $V_{DD\ Max}$
I_I	Input Leakage Current for IC, ID[3:0] Pins			100	µA	V_{IN} = 0V to V_{DD}, V_{DD} = $V_{DD\ Max}$
I_{LI}	Input Leakage Current			±1	µA	V_{IN} = 0V to V_{DD}, V_{DD} = $V_{DD\ Max}$
I_{LO}	Output Leakage Current			±1	µA	$V_{I/O}$ = 0V to V_{DD}, V_{DD} = $V_{DD\ Max}$
V_{IH}	Input High Voltage	0.7V_{DD}		V_{DD}+0.5	V	
V_{IL}	Input Low Voltage	-0.5		0.3V_{DD}	V	
V_{OL}	Output Low Voltage			0.1V_{DD}	V	I_{OL}= 2.0mA, V_{DD} = $V_{DD\ Min}$
V_{OH}	Output High Voltage	0.9V_{DD}			V	I_{OH} = -100µA, V_{DD} = $V_{DD\ Min}$

Notes:
1. Characterized but not 100% tested.

Table 16: Pin Impedance (V_{DD}=3.3V, T=25°C, f=1MHz)

Parameter	Description	Test Condition	Max
$C_{I/O}$ (1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12pF
C_{IN} (1)	Input Capacitance	V_{IN} = 0V	12pF
L_{PIN} (2)	Pin Inductance		20nH

Notes:
1. These parameters are characterized but not 100% tested.
2. Refer to PCI specification.

Table 17: FWH/LPC Interface Clock Characteristics

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK Cycle Time	30		ns
t_{HIGH}	CLK High Time	11		ns
t_{LOW}	CLK Low Time	11		ns
	CLK Slew Rate (peak-to-peak)	1	4	V/ns
	$\overline{INIT}$ or $\overline{RST}$ Slew Rate	50		mV/ns

Table 18: FWH/LPC Memory Read/Write Operations Characteristics

Symbol	Parameter	Min	Max	Units
t_{CYC}	Clock Cycle Time	30		ns
t_{SU}	Input Set Up Time	7		ns
t_H	Input Hold Time	0		ns
t_{VAL}	Clock to Data Out	2	11	ns
t_{ON}	Clock to Active Time (Float to Active Delay)	2		ns
t_{OFF}	Clock to Inactive Time (Active to Float Delay)		28	ns

Table 19: FWH/LPC Interface Measurement Condition Parameters

Symbol	Value	Units
V_{TH}[4]	0.6 V_{DD}	V
V_{TL}[1]	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}[1]	0.4 V_{DD}	V
Input Signal Edge Rate	1V/ns	

Notes: The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive that this. V_{MAX} specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.

Figure 9: Input Timing Parameters

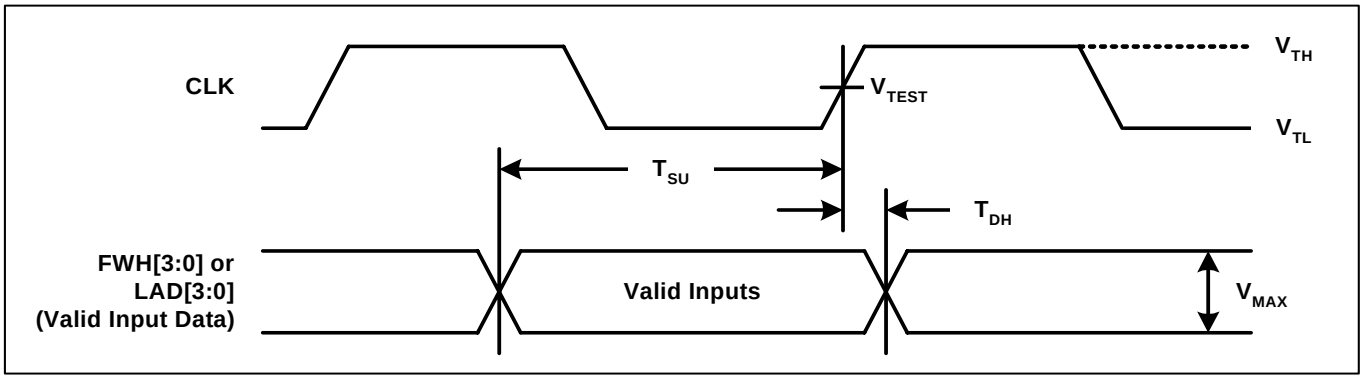


Figure 10: Output Timing Parameters

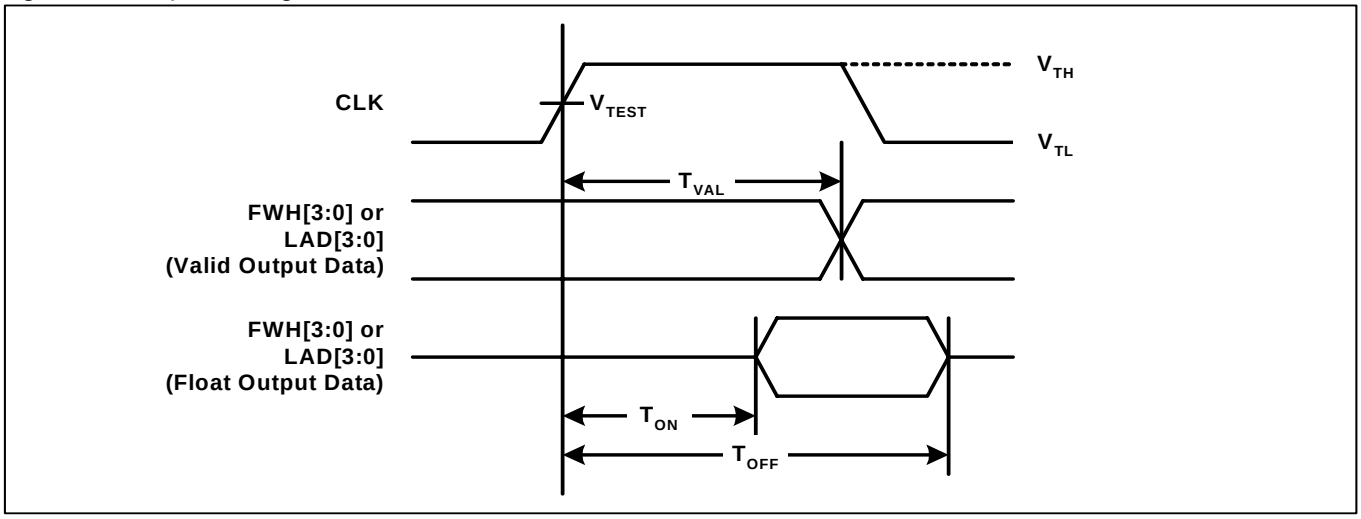


Table 20: FWH/LPC Interface AC Input/Output Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{OH} (AC)	Switching Current High	$0 < V_{OUT} \le 0.3V_{DD}$	$-12\ V_{DD}$		mA
		$0.3V_{DD} < V_{OUT} \le 0.9V_{DD}$	$-17.1(V_{DD}-V_{OUT})$		mA
		$0.7V_{DD} < V_{OUT} \le V_{DD}$		Equation C (1)	mA
	(Test Point)	$V_{OUT} = 0.7V_{DD}$		$-32\ V_{DD}$	
I_{OL} (AC)	Switching Current Low	$V_{DD} > V_{OUT} \ge 0.6V_{DD}$	$16V_{DD}$		mA
		$0.6V_{DD} > V_{OUT} > 0.1V_{DD}$	$-17.1(V_{DD} - V_{OUT})$		mA
		$0.18V_{DD} > V_{OUT} > 0$		Equation D (1)	mA
	(Test Point)	$V_{OUT}=0.18V_{DD}$		$38V_{DD}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25+(V_{IN}+1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{DD}+4 > V_{IN} > V_{DD}+1$	$25+(V_{IN}-V_{DD}-1)/0.015$		mA
slewr (2)	Output Rise Slew Rate	$0.2V_{DD}$-$0.6V_{DD}$ load	1	4	V/ns
slewf (2)	Output Fall Slew Rate	$0.6V_{DD}$-$0.2V_{DD}$ load	1	4	V/ns

Notes:
1. See PCI specification.
2. PCI specification output load is used.

Table 21: FWH Mode Interface Reset Timing Parameters, V_{DD}=3.0-3.6V

Symbol	Parameter	Min	Max	Units
t_{PRST}	Reset Active Time to Vcc Stable	1		ms
t_{KRST}	Reset Active Time to Clock Stable	100		µs
t_{RSTP}	Reset Pulse Width	100		ns
t_{RSTF}	Reset Active to Output Float Delay		50	ns
t_{RST} (1)	Reset Inactive Time to Input Active	1		ns

Note:
There will be an 10 µs reset latency if a reset procedure is performed during a programming or erase operation.

Figure 11: Reset Timing Diagram

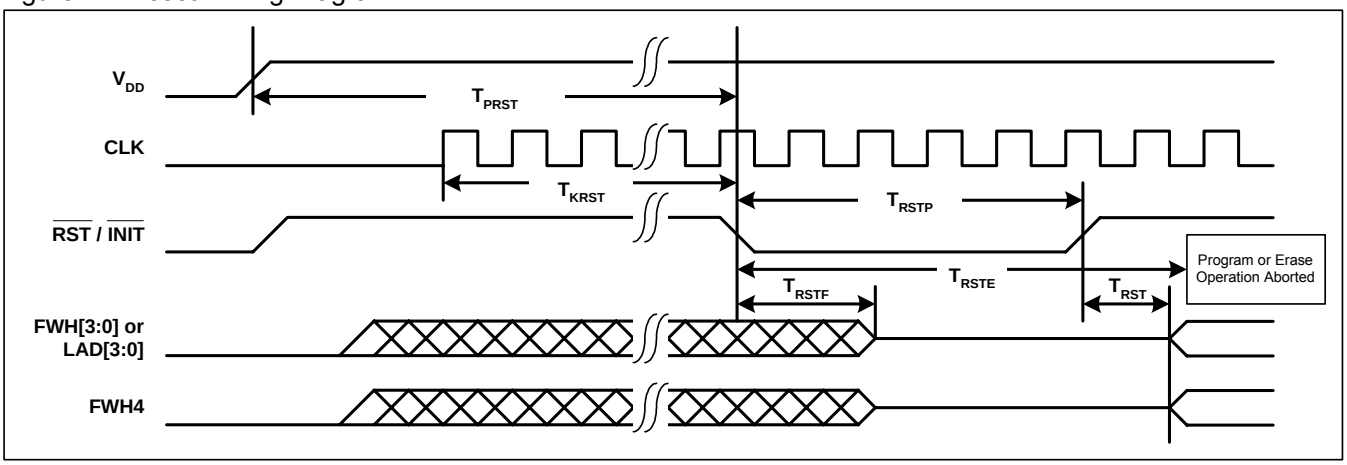
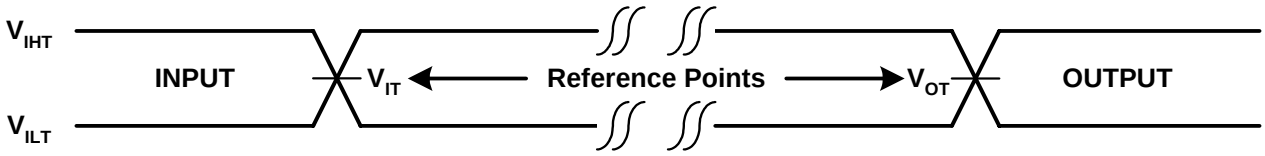


Figure 12: A/A Mux Mode AC Input/Output Reference Waveforms

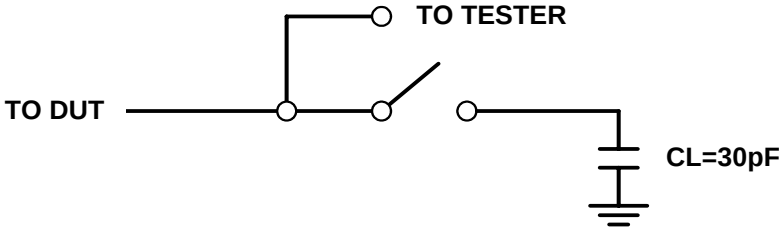


AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic HIGH and V_{ILT} ($0.1V_{DD}$) for a logic LOW. Measurement reference points for inputs and outputs are V_{IT} ($0.5V_{DD}$) and V_{OT} ($0.5V_{DD}$). Input rise and fall times (10% <-> 90%) are < 5ns

Note:

V_{IT}: V_{INPUT} Test
V_{OT}: V_{OUTPUT} Test
V_{IHT}: V_{INPUT} HIGH Test
V_{ILT}: V_{INPUT} LOW Test

Figure 13: A/A Mux Mode Test Load Condition



A/A MUX MODE AC CHARACTERISTICS

Table 22: A/A Mux Mode Read Operations Characteristics

Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	270		ns
t_{RST}	$\overline{RST}$ High to Row Address Setup Time	1		ms
t_{AS}	R/$\overline{C}$ Address Set-up Time	45		ns
t_{AH}	R/$\overline{C}$ Address Hold Time	45		ns
t_{AA}	Address to Output Delay		120	ns
t_{OE}	$\overline{OE}$ to Output Delay		50	ns
t_{DF}	$\overline{OE}$ Output High Z	0	30	ns
t_{VCS}	V_{DD} Setup Time	50		µs
t_{OH}	Output Hold from $\overline{OE}$ or Address, whichever occurred first	0		ns

Table 21: A/A Mux Write (Program/Erase) Operations Characteristics

Symbol	Parameter	Min	Max	Units
t_{RST}	$\overline{RST}$ High to Row Address Setup Time	1		ms
t_{AS}	R/$\overline{C}$ Address Setup Time	50		ns
t_{AH}	R/$\overline{C}$ Address Hold Time	50		ns
t_{CWH}	R/$\overline{C}$ to $\overline{WE}$ High Time	50		ns
t_{OES}	$\overline{OE}$ High Setup Time	20		ns
t_{OEH}	$\overline{OE}$ High Hold Time	20		ns
t_{WP}	Write Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ Pulse Width High	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	5		ns
t_{BP}	Byte Programming Time		40	µs
t_{EC}	Chip, Sector or Block Erase Cycle Time		80	ms
t_{VCS}	V_{DD} Setup Time	50		µs

Figure 14: A/A Mux Mode Read Cycle Timing Diagram

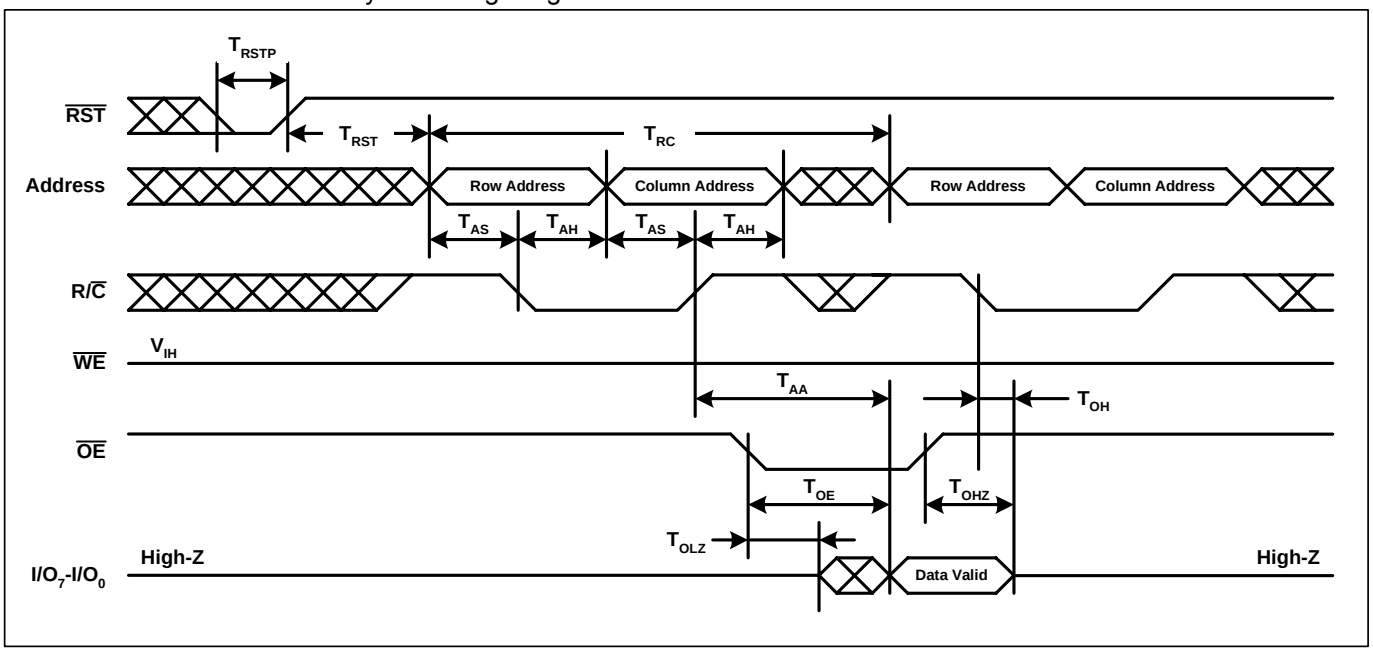


Figure 15: A/A Mux Mode Write Cycle Timing Diagram

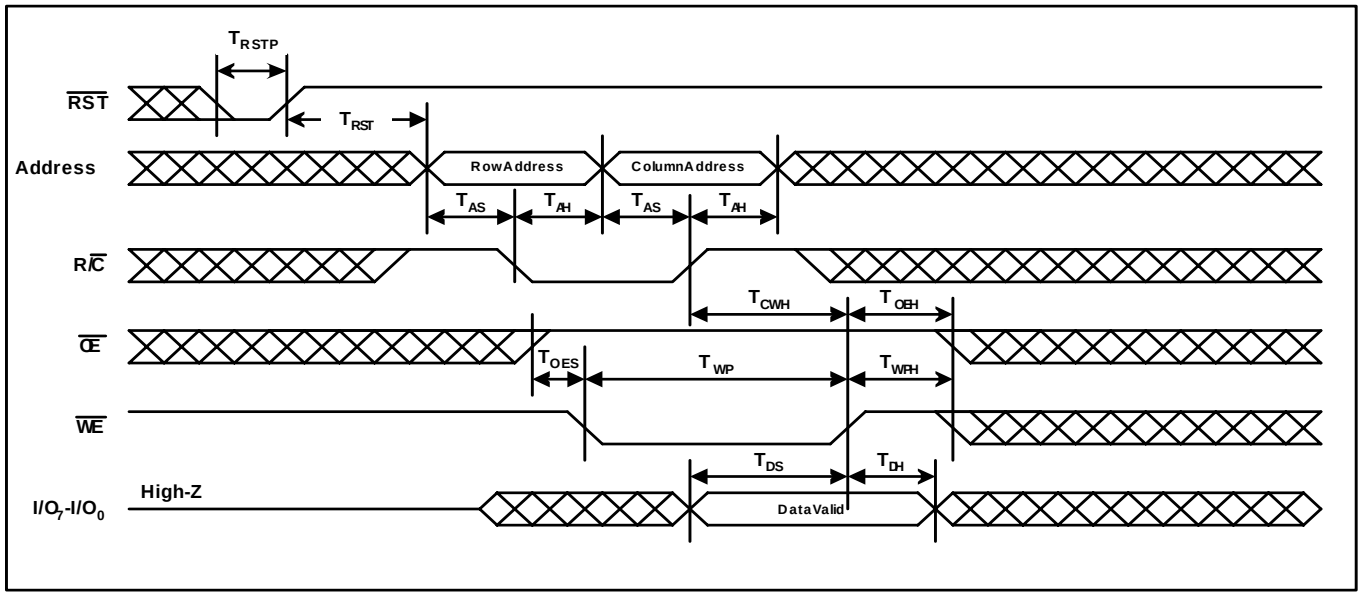


Figure 16: A/A Mux Mode Data# Polling Timing Diagram

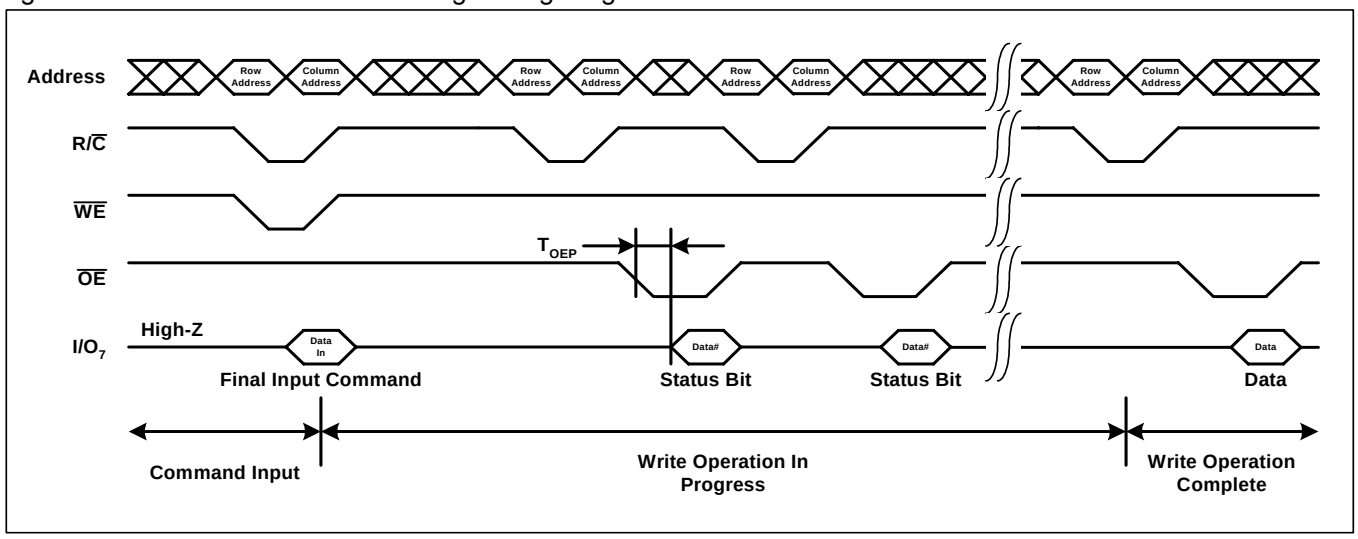


Figure 17: A/A Mux Mode Toggle Bit Timing Diagram

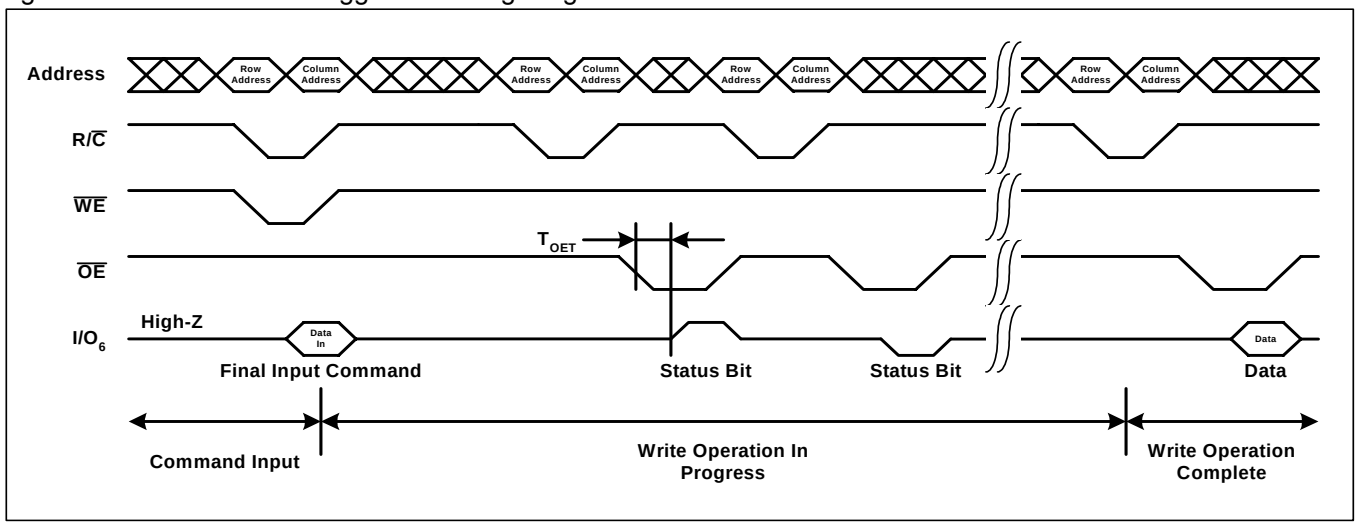


Figure 18: A/A Mux Mode Byte Program Timing Diagram

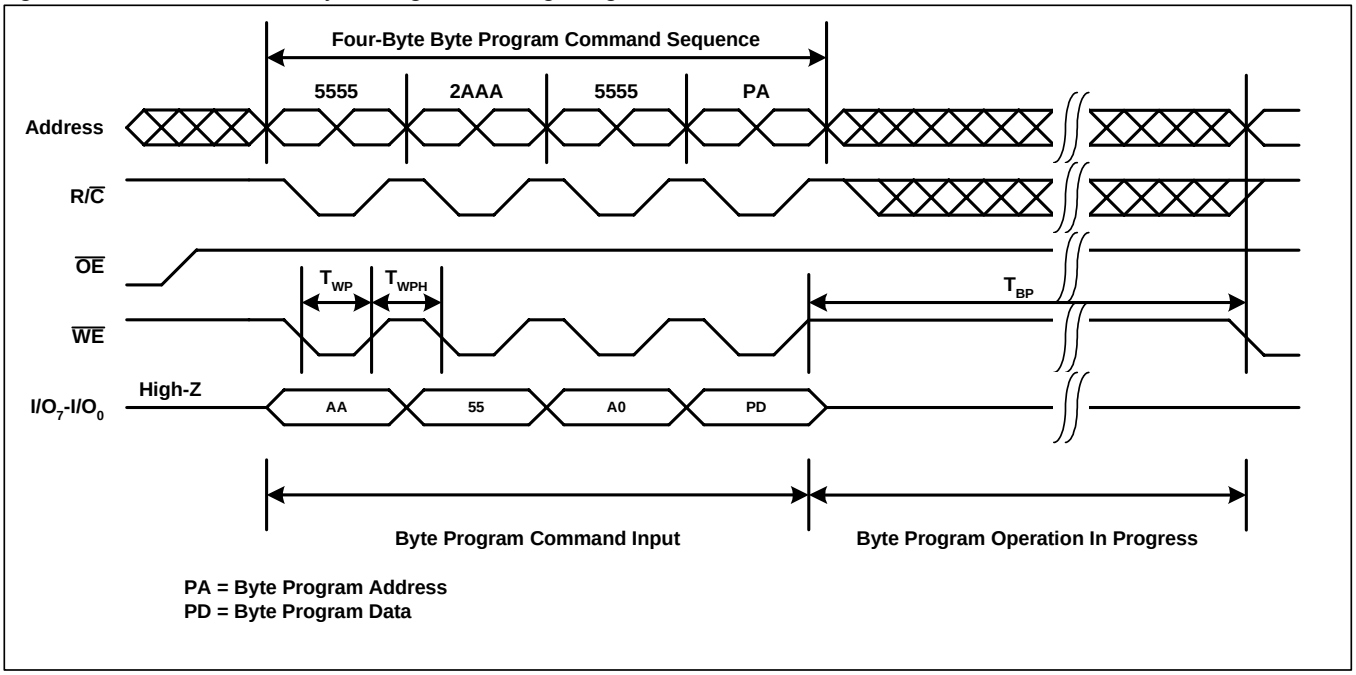


Figure 19: A/A Mux Mode Block Erase Timing Diagram

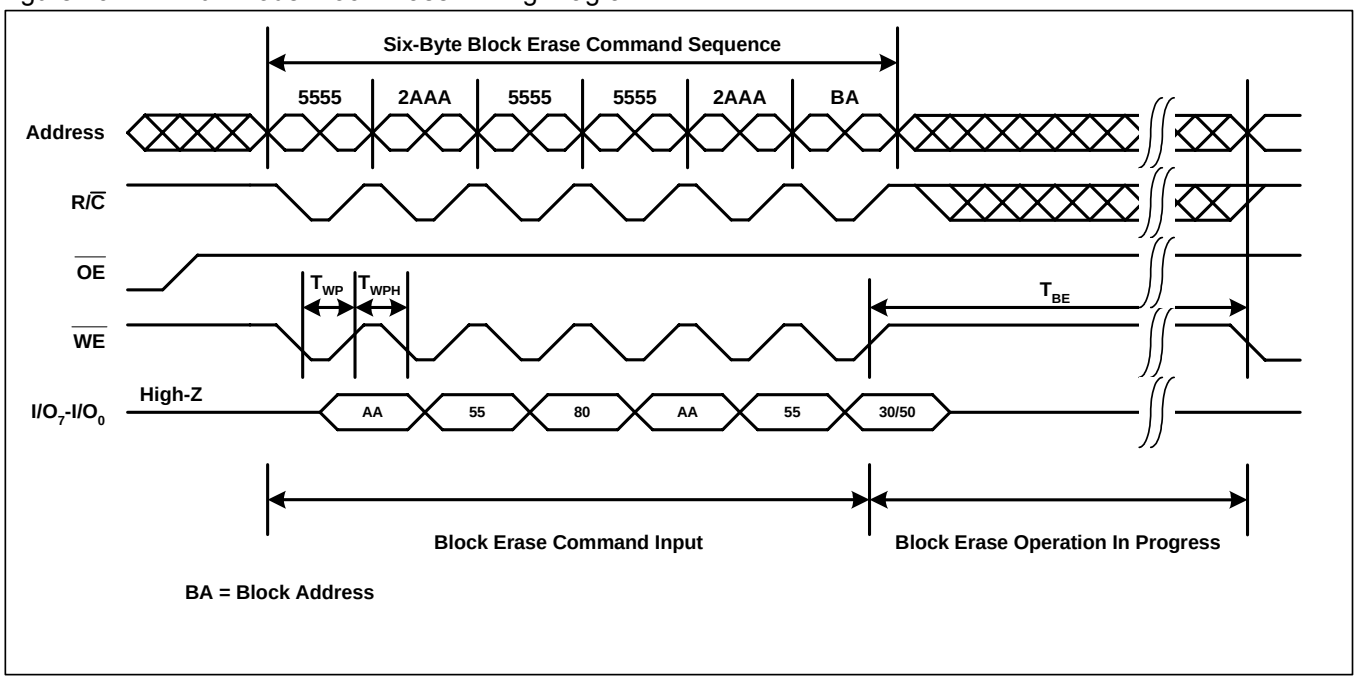


Figure 20: A/A Mux Mode Chip Erase Timing Diagram

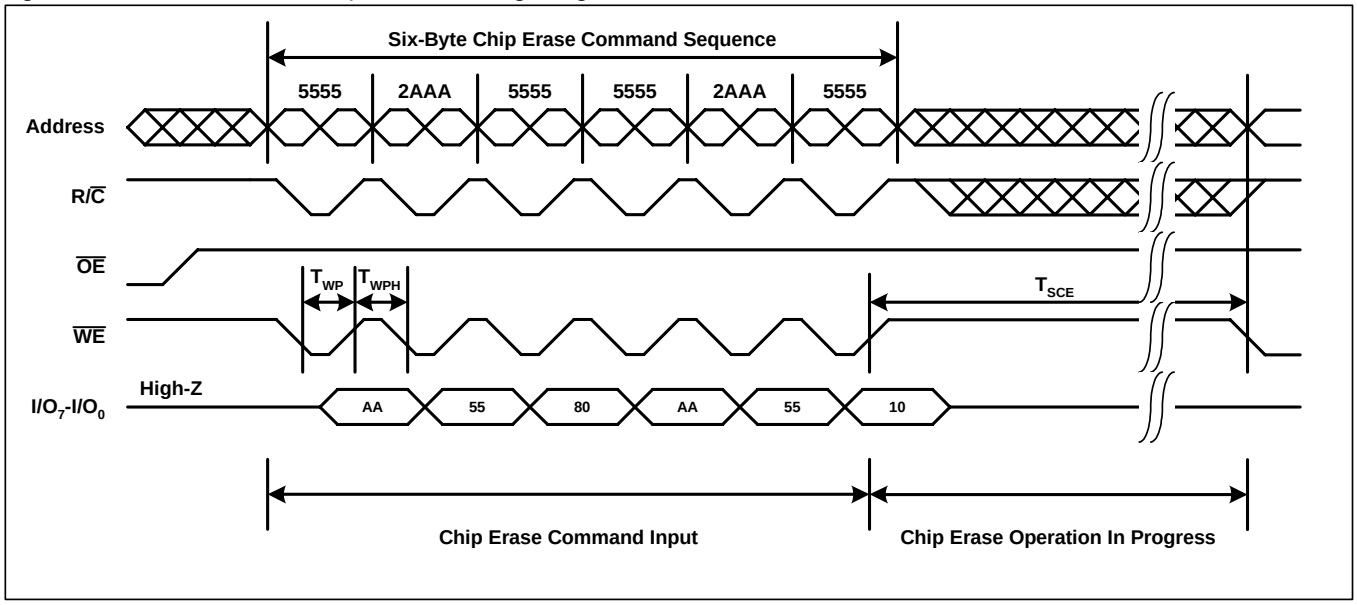


Figure 21: A/A Mux Mode Product ID Entry and Read Timing Diagram

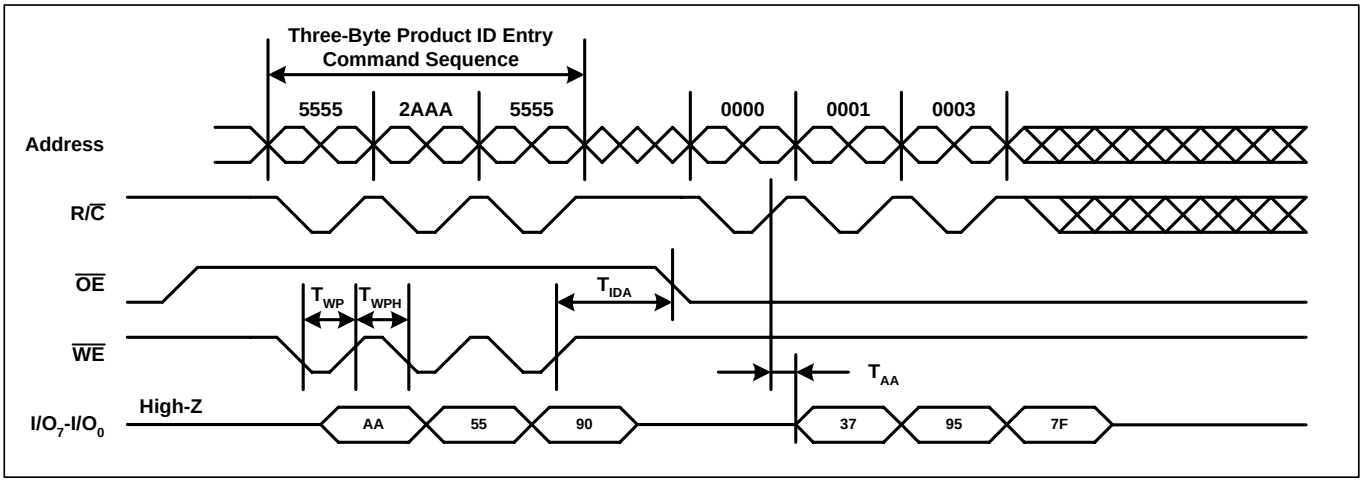


Figure 22: A/A Mux Mode Product ID Exit and Reset Timing Diagram

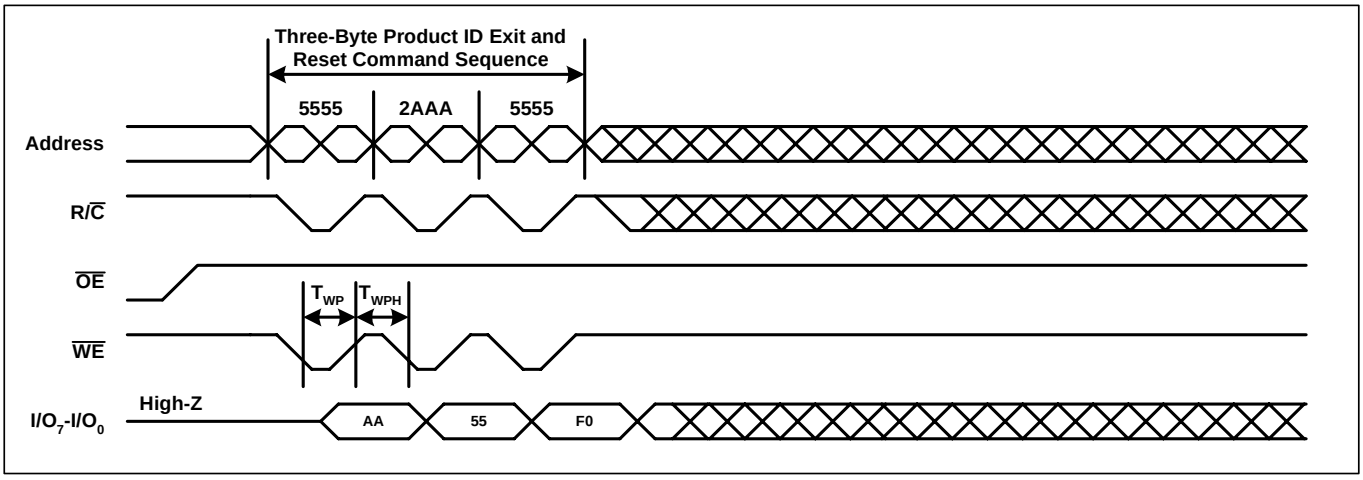


Figure 23: Automatic Byte Program Algorithm

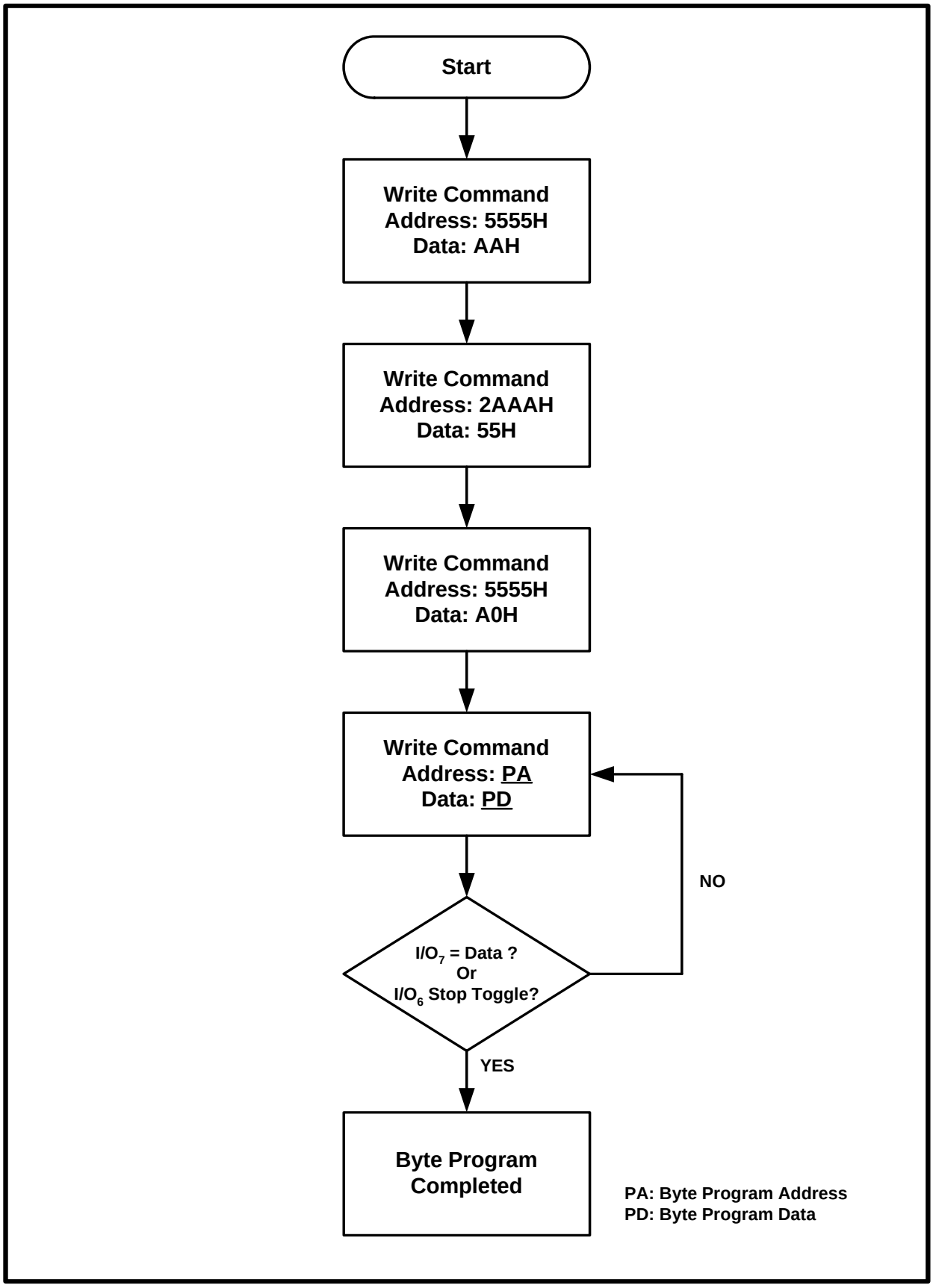


Figure 24: Automatic Block Erase Algorithm

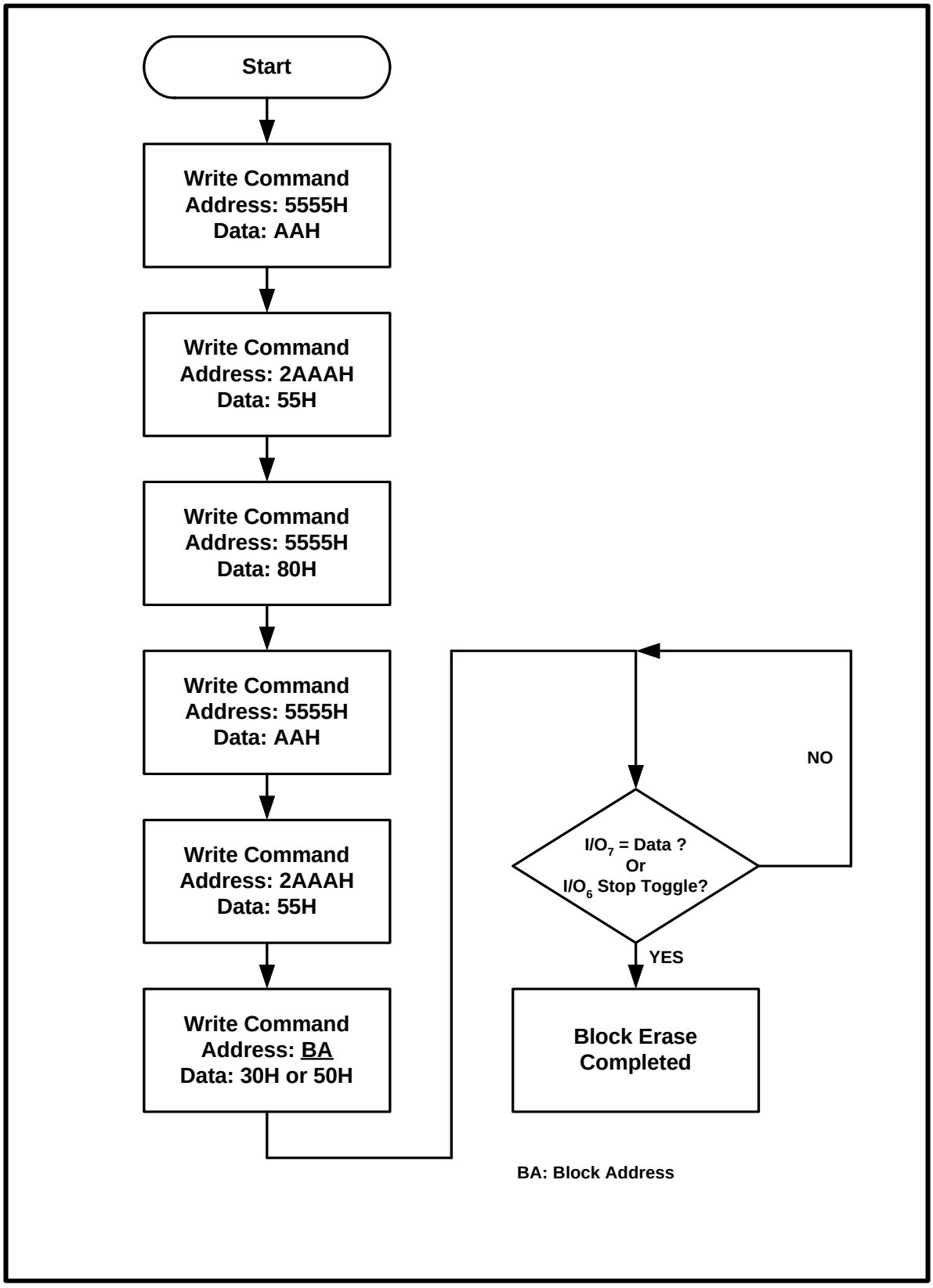


Figure 25: Automatic Chip Erase Algorithm

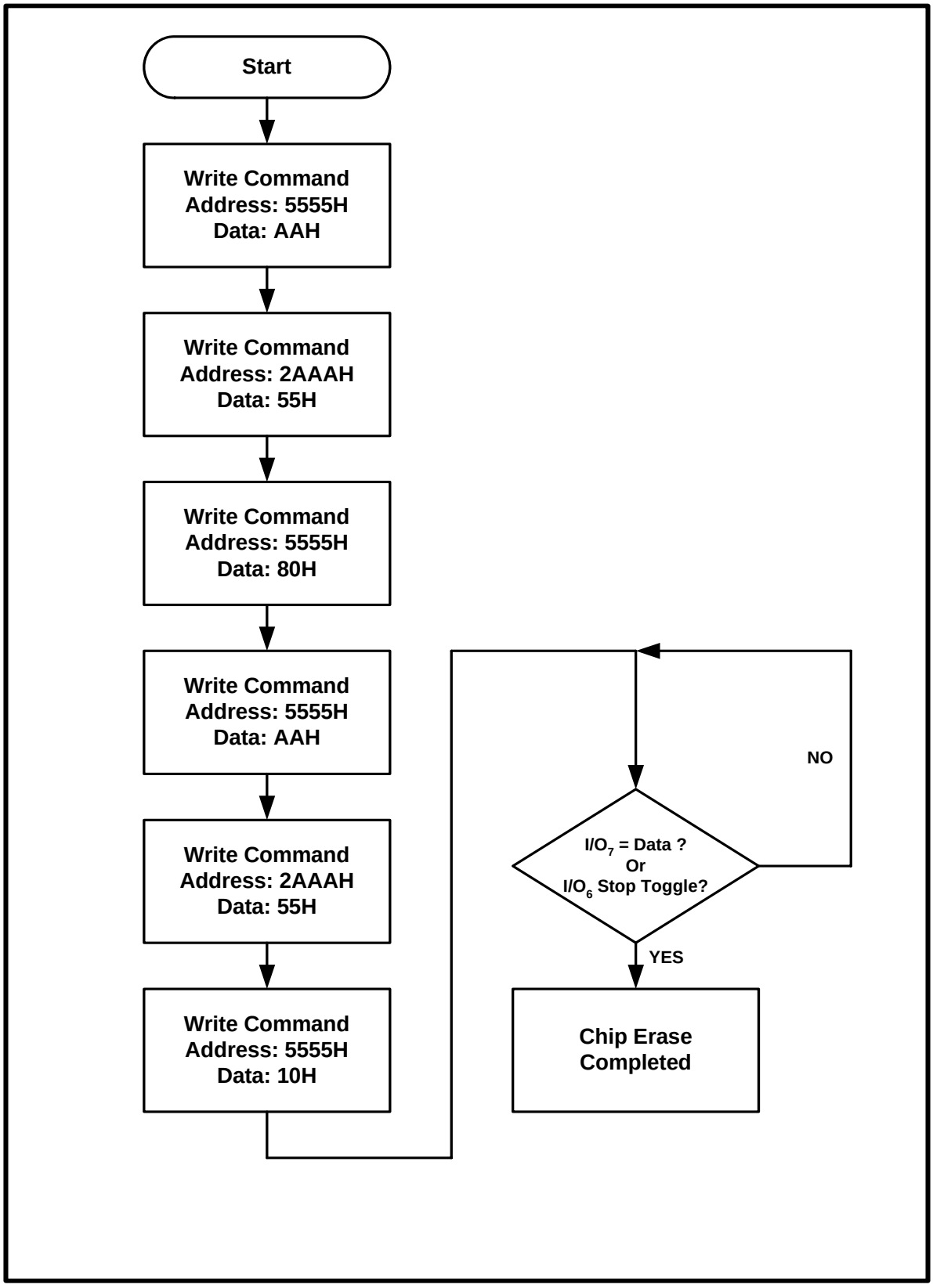
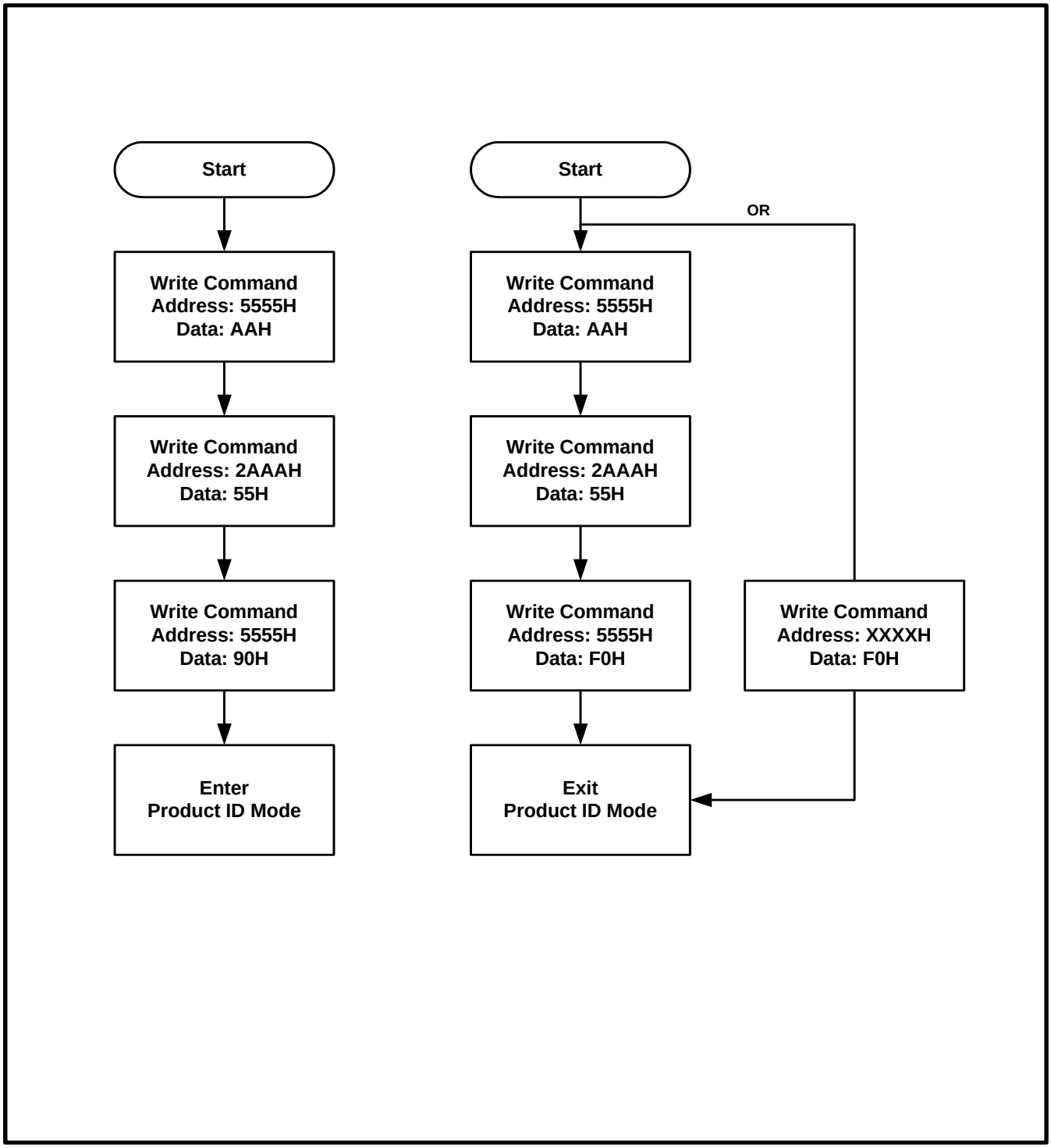
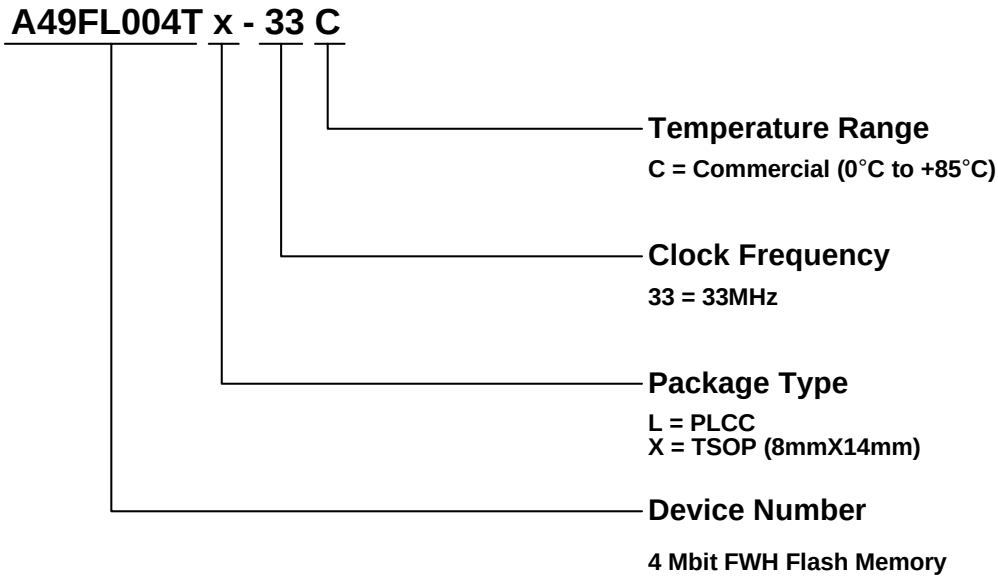


Figure 26: Product ID Command Flowchart



Ordering Information

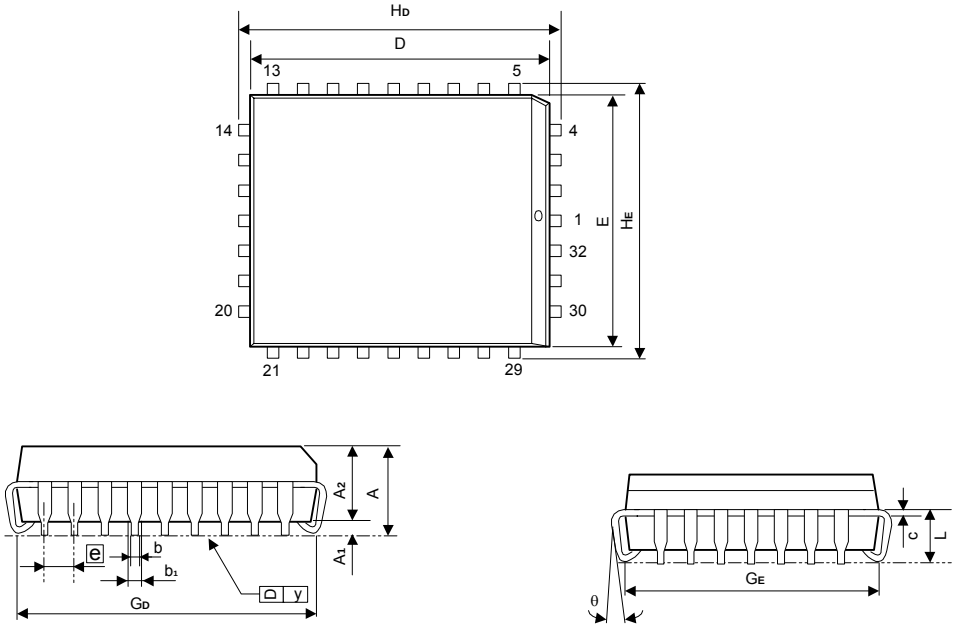


Part No.	Clock Frequency (MHz)	Boot Block Location	Temperature Range	Package Type
A49FL004TL-33	33	Top	0°C to +85°C	32-pin PLCC
A49FL004TL-33F		Top	0°C to +85°C	32-pin Pb-Free PLCC
A49FL004TX-33		Top	0°C to +85°C	32-pin TSOP (8mm X 14 mm)
A49FL004TX-33F		Top	0°C to +85°C	32-pin Pb-Free TSOP (8mm X 14 mm)

Package Information

PLCC 32L Outline Dimension

unit: inches/mm

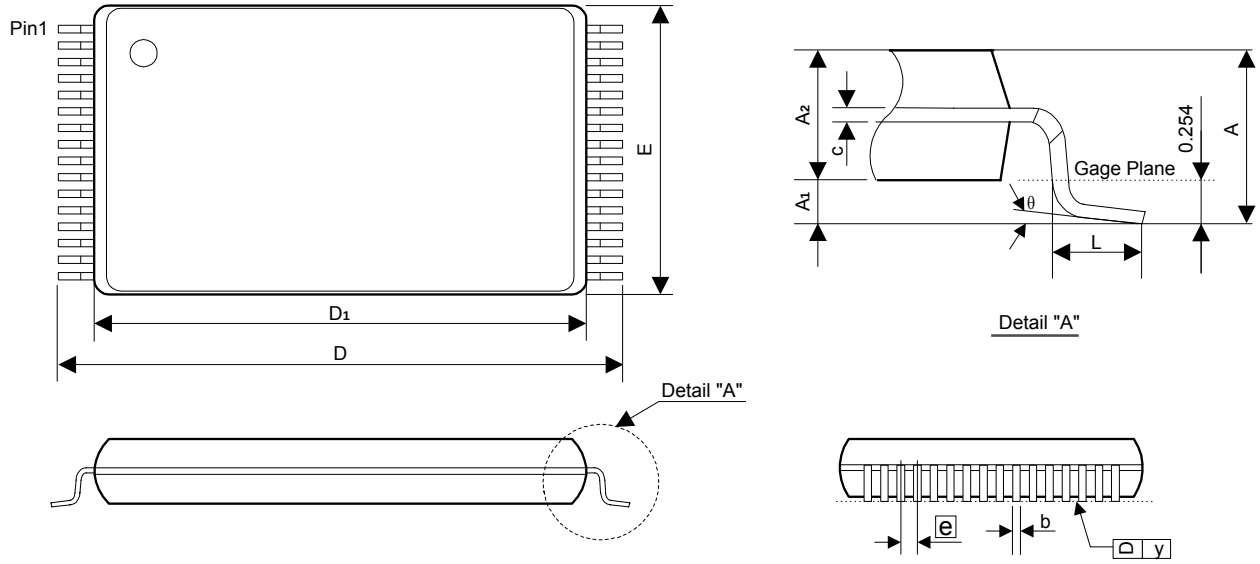


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.134	-	-	3.40
A_1	0.0185	-	-	0.47	-	-
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
C	0.008	0.010	0.014	0.20	0.254	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	-	-	0.003	-	-	0.075
θ	0°	-	10°	0°	-	10°

Notes:
1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Package Information

TSOP 32L TYPE I (8 X 14mm) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.0067	0.0087	0.0106	0.17	0.22	0.27
c	0.004	-	0.0083	0.10	-	0.21
E	0.311	0.315	0.319	7.90	8.00	8.10
e	-	0.0197	-	-	0.50	-
D	0.543	0.551	0.559	13.80	14.00	14.20
D_1	0.484	0.488	0.492	12.30	12.40	12.50
L	0.020	0.024	0.028	0.50	0.60	0.70
y	0.000	-	0.003	0.00	-	0.076
θ	0°	3°	5°	0°	3°	5°

Notes:
1. Dimension E does not include mold flash.
2. Dimension D_1 does not include interlead flash.
2. Dimension b does not include dambar protrusion.