Features

General

- High-performance, Low-power secureAVR[™] RISC Architecture
 - 133 Powerful Instructions (Most Executed in a Single Clock Cycle)
 - Linear Addressing of up to 8M Bytes of Code and up to 16M Bytes of Data
- Low-power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 6000V
- Operating Ranges: from 2.7V to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications; PC Industry Compatible
- Available in Wafers, Modules and Industry-standard Packages

Memory

- 192K Bytes of ROM Program Memory
- 72K Bytes of EEPROM, Including 128-byte OTP Area and 384-byte Bit-addressable Area
 - 1 to 128-byte Program/Erase
 - 1 ms Program, 1 ms Erase
 - Typically More than 500,000 Write/Erase Cycles at a Temperature of 25°C
 - 10 Years Data Retention
- · 4K Bytes of RAM

Peripherals

- ISO 7816 Controller
 - Up to 625 kbps at 5 MHz
 - Compliant with T = 0 and T = 1 Protocols
- Programmable Internal Oscillator (Up to 20 MHz on ROM)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 8-vector Interrupt Controller
- Hardware DES and Triple DES DPA Resistant
- Checksum Accelerator
- CRC 16 Engine (Compliant with ISO/IEC 3309)
- 8-bit GF(2ⁿ) Multiplier
- Crypto-coprocessor (Pre-programmed Functions for Cryptography and Authentication Including RSA, DSA, Key Generation, ECC)

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Temperature Monitor
- Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)

Development Tools

- Voyager Emulation Platform (ATV2 Advanced) to Support Software Development
- IAR Systems C-Spy® Debugger or AVR Studio, Version 4.7 or Later
- Software Libraries and Application Notes



Secure Microcontroller for Smart Cards

AT90SC 19272RC

Summary



Rev. 1592AS-SMIC-25Jun03



Description

The AT90SC19272RC is a low-power, high-performance, 8-/16-bit microcontroller, based on the secureAVR RISC architecture, with ROM program memory, EEPROM data memory and a crypto-coprocessor. By executing powerful instructions in a single clock cycle, the AT90SC19272RC achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

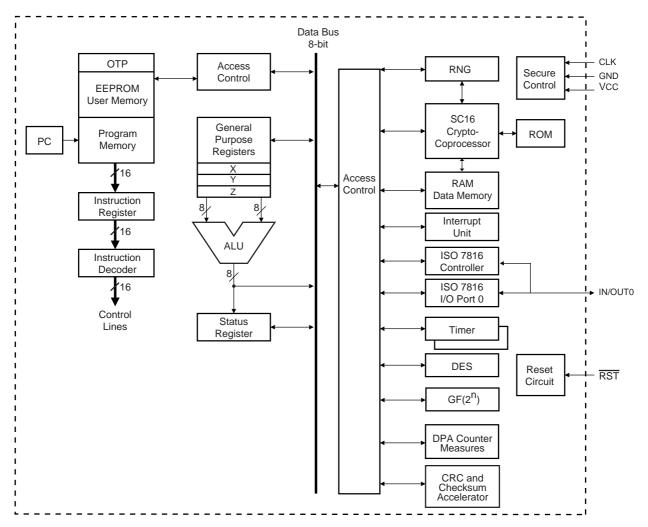
The AT90SC19272RC uses secureAVR architecture that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data, and also provides a number of new functional and security features.

The crypto engine featured in the AT90SC series is the SC16, a 16-bit processor dedicated to performing fast encryption and authentication functions.

Additional security features include power, frequency and temperature protection logic, logical scrambling on program data and addresses, power analysis countermeasures, and memory accesses controlled by a supervisor mode.

A block diagram of the AT90SC19272RC is shown in Figure 1.

Figure 1. AT90SC19272RC secureAVR Enhanced RISC Architecture





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