Features

- Maximum Supply Voltage 40V
- One Programmable/Adjustable Boost Converter
- Two Programmable Buck Converters
- One Programmable Linear Regulator
- OTP Customer Mode
- 16-bit Serial Interface
- Two ISO9141 Interfaces (One Interface Programmable to LIN Functionality)
- Watchdog
- Various Diagnosis Functions
- 5 Voltage Sources Tailored to Resistor Measurement
- Charge Pump
- Small, 44-pin Package
- ESD Protection Against 2kV and 4kV

Airbag Power Supply IC

ATA6264

Preliminary

1. Description

With the introduction of the ATA6264, Atmel® introduces a new generation of airbag power supplies for future airbag systems tailored to the needs of the automotive industry. It is designed in Atmel's 0.8 micron BCDMOS technology. ATA6264 contains all the necessary blocks to supply the microcontroller, the firing capacitors, and peripheral components of the airbag system. The power supply specifically fulfills the power requirements of dual-voltage microcontrollers used in modern ECUs. The integrated watchdog and diagnosis blocks additionally support the safety aspects. The 8-MHz 16-bit SPI enables a high communication speed. Despite the high-level functionality, ATA6264 comes in a space-saving QFP44 package.

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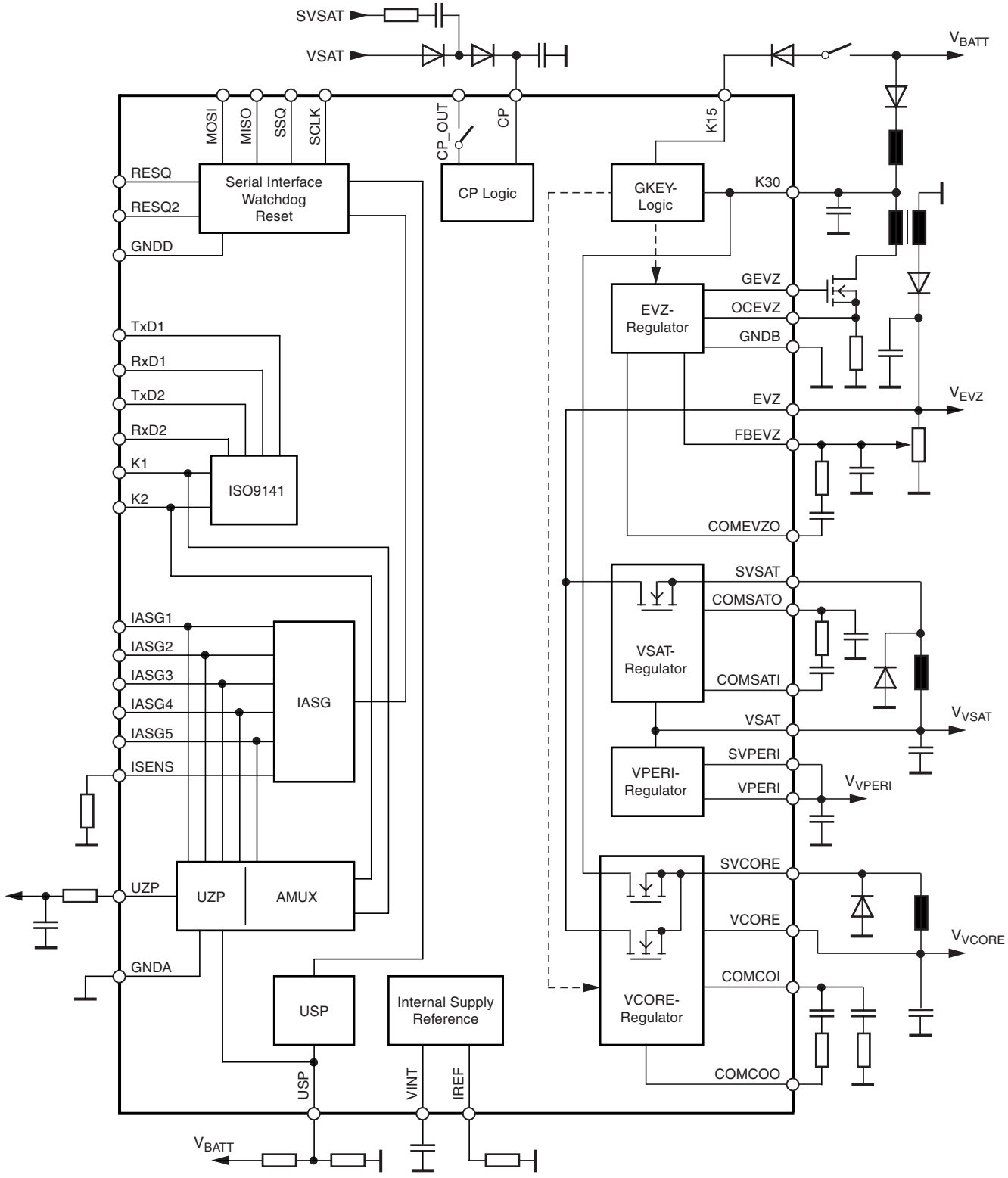
Figure 1-1. Block Diagram



1.1 Block Description

1.1.1 Integrated Boost Converter EVZ

With an external n-channel FET, the integrated boost converter EVZ provides 3 different voltages adjustable via the serial interface for the energy reserve and firing capacitors. Two voltages are fixed values; one voltage can be adjusted using an external resistive divider.

1.1.2 Integrated Buck Converter VSAT

The integrated buck converter VSAT is a fully integrated step-down converter supplied by the boost converter, EVZ, and providing 7.8V, 9.1V, or 10.4V. The user can program the voltage via an OTP system.

1.1.3 Integrated Buck Converter VCORE

The integrated buck converter VCORE is a fully integrated step-down converter supplied either by the boost converter, EVZ, or by the battery, and providing 1.88V, 2.5V, or 5V. The user can program the voltage via an OTP system.

1.1.4 Linear Regulator VPERI

The linear regulator, VPERI, is supplied from the buck converter VSAT and provides an accurate voltage of 3.3V ±3% or 5V ±4% as a supply for sensitive elements such as sensors and ADC references with the current capability of 100 mA. The user can program the voltage via an OTP system. With a sophisticated power-sequencing concept of VCORE and VPERI, ATA6264 supports dual-voltage-supply microcontrollers, so that under all conditions the voltage difference between the two linear regulator voltages never drops below a defined value. This measure guarantees the safe operation of the system.

1.1.5 Blocks Included

- A general purpose comparator USP, for, for example, low battery voltage detection
- A band gap as reference for all internal voltages and currents
- Two ISO9141 interfaces, one of which is configurable via OTP in accordance with the LIN specification
- Five constant voltage sources with current-to-voltage mirrors used for resistance measurements, such as buckle switch detection in the range from –0.5 mA to –40 mA
- An AMUX block with push-pull buffer stage provides the output of all analog values such as voltage sources, low voltage detection, or the chip temperature for continuous diagnosis
- A 16-bit serial interface for the communication with the microcontroller which includes a 16-bit shift register, a 16-bit latch, and a decoder-logic block
- A watchdog to monitor the microcontroller and to generate reset signals in the case of failure
- Internal oscillator generates internal clock signals
- GKEY function to control the main switch of the ECU via a logic signal

2. Pin Configuration

Figure 2-1. Pinning QFP44

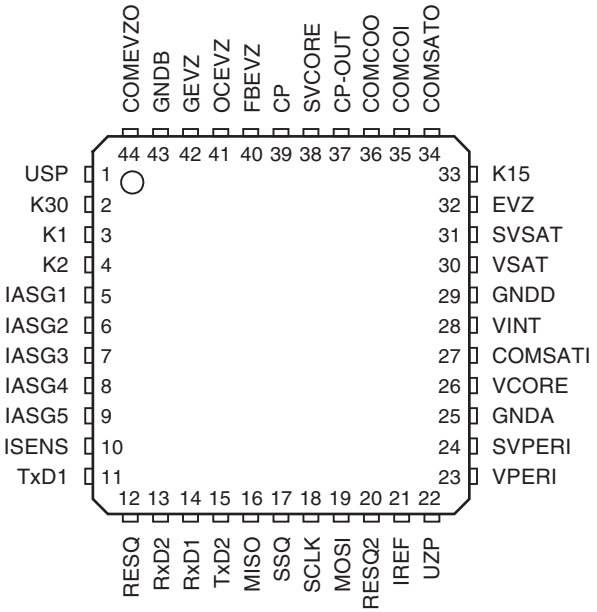


Table 2-1. Pin Description

Pin	Symbol	Function
1	USP	Comparator input
2	K30	Continuous connection to the car battery
3	K1	Bus line of 1st ISO9141 interface
4	K2	Bus line of 2nd ISO9141 interface
5	IASG1	Output of voltage source 1
6	IASG2	Output of voltage source 2
7	IASG3	Output of voltage source 3
8	IASG4	Output of voltage source 4
9	IASG5	Output of voltage source 5
10	ISENS	Output of the current mirror from the IASGx interface
11	TXD1	Data input of the 1st ISO9141 interface
12	RESQ	Reset output
13	RXD2	Data output of the 2nd ISO9141 interface
14	RXD1	Data output of the 1st ISO9141 interface
15	TXD2	Data input of the 2nd ISO9141 interface
16	MISO	Data output of the serial interface
17	SSQ	Chip select of the serial interface
18	SCLK	Clock input of the serial interface
19	MOSI	Data input of the serial Interface
20	RESQ2	Redundant reset output
21	IREF	Connection for the external reference resistor
22	UZP	Analog measurement output

Table 2-1. Pin Description

Pin	Symbol	Function
23	VPERI	Input for the VPERI regulator, internally used VPERI supply
24	SVPERI	Output of VPERI regulator power transistor
25	GNDA	Analog GND
26	VCORE	Input for VCORE regulator
27	COMSATI	Input of the VSAT externally compensated error amplifier
28	VINT	Output of internal supply voltage
29	GNDD	Digital GND
30	VSAT	Input for VSAT regulator, internally used VSAT supply
31	SVSAT	Output of VSAT regulator power transistor
32	EVZ	Input for EVZ regulator, internally used EVZ supply
33	K15	Connection to car battery via the ignition key
34	COMSATO	Output of the VSAT externally compensated error amplifier
35	COMCOI	Input of the VCORE externally compensated error amplifier
36	COMCOO	Output of the VCORE externally compensated error amplifier
37	CP-OUT	Switchable output of charge pump voltage
38	SVCORE	Output of VCORE regulator power transistor
39	CP	Charge pump output
40	FBEVZ	Input for external resistor divider to adjust EVZ voltage
41	OCEVZ	Input for overcurrent measurement of the EVZ regulator
42	GEVZ	Gate driver output for the external FET of the EVZ regulator
43	GNDB	GND connection of all power stages
44	COMEVZO	Output of the EVZ externally compensated error amplifier

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
All voltages are referenced to an ideal ground level of an ECU connected to the GNDA, GNDB and GNDD pins.

Parameters	Remark	Minimum	Maximum	Unit
Voltage at pins, connected directly or indirectly to the car battery (K30, K15, USP)	Any combination of one or more pins applied with any voltage between the limits K30 and K15 connected via diode to V_{Batt}. USP connected via minimum 5 kΩ to V_{Batt} (maximum reverse current 5 mA).	–0.3	+45	V
Voltage at pins, connected directly or indirectly to the car battery (K1, K2)	Any combination of one or more pins applied with any voltage between the limits	–25	+45	V
Voltage at pins, connected directly or indirectly to the car battery (IASG1, IASG2, IASG3, IASG4, IASG5)	Any combination of one or more pins applied with any voltage between the limits	Voltage necessary to drive –40 mA stored in 20 µH	45	V
Voltage at ECU internal pins (FBEVZ, EVZ, VSAT)	Any combination of one or more pins applied with any voltage between the limits	–0.3	+45	V
Maximum rate of change at pin VSAT			1	V/µs
Voltage at ECU internal pins (SVSAT, SVCORE)	Any combination of one or more pins applied with any voltage between the limits	–1	+45	V
Voltage at ECU internal pins (CP, CP-OUT)	Any combination of one or more pins applied with any voltage between the limits	–0.3	+56	V
Voltage at ECU internal pins (GEVZ, OCEVZ)	Any combination of one or more pins applied with any voltage between the limits	–0.3	+10	V
Voltage at ECU internal pins (COMEVZO, COMSATO, COMSATI, VPERI, SVPERI, VCORE, COMCOI, COMCOO, IREF, UZP, ISENS, RXD1, TXD1, RXD2, TXD2, RESQ, RESQ2, MISO, MOSI, SSQ, SCLK, VINT)	These voltages can be applied in any combination with any voltage between the limits	–0.3	+7	V
Current at logic pins	Connected to voltages outside of maximum voltage ratings via resistor	–3	+3	mA
ESD classification at pins connected to devices outside the ECU (K30, K15) Human body model (HBM)	 HBM AEC Q100-002	 ±4000		V

3. Absolute Maximum Ratings (Continued)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
All voltages are referenced to an ideal ground level of an ECU connected to the GNDA, GNDB and GNDD pins.

Parameters	Remark	Minimum	Maximum	Unit
ESD classification at pins connected to devices outside the ECU (IASG1 to IASG5)				
Human body model (HBM)	HBM AEC Q100-002	±3000		V
ESD classification at pins connected to devices outside the ECU (K1 and K2)				
Human body model (HBM)	HBM AEC Q100-002	±2500		V
General ESD classification for all other pins				
Human body model (HBM)	HBM AEC Q100-002	±1500		V
Charged device model (CDM) – no corner pins	CDM ESD STM5.3.1-1999	±500		V
Charged device model (CDM) – corner pins		±750		V

4. Functional Range

Within the functional range, the ATA6264 works as specified. All voltages are referenced to the ideal ground level of an ECU connected to the GNDA, GNDB and GNDD pins.

At the beginning of each specification table, supply voltage and temperature conditions are described.

Table 4-1. Electrical Characteristics – Functional Range

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Voltage on pins K30, K15, USP				–0.3		+40	V	
1.1a	Voltage on pins K1, K2				–25		+40	V	
1.2	Rate of supply voltage rise (K30, K15, K1, K2)						50	V/µs	
1.3	Supply voltage EVZ				–0.3		+40	V	
1.4	Supply voltage VSAT				–0.3		+14	V	
1.5	Supply voltages VCORE, VPERI				–0.3		+5.5	V	
1.6	Supply voltage CP, CP-OUT				–0.3		+50	V	
1.7	Voltage on digital I/O pins				–0.3		+5.5	V	
1.8	Voltage on pins SVSAT, SVCORE				–1.0		+40	V	
1.9	Voltage on pins UZP, ISENS, COMCOI, COMCOO, COMSATO, COMSATI, COMEVZO, FBEVZ, IREF, VINT				–0.3		+5.5	V	
1.10	Voltage on pins GEVZ, OCEVZ				–0.3		+10	V	
1.11	Voltage on pin SVPERI				–0.3		+6	V	
1.12	Voltage on pins IASGx (x = 1 to 5)				Voltage necessary to drive –40 mA stored in 20 µH		40	V	
1.14	Temperatures: Operating ambient temperature range Operating junction temperature range Storage ambient/junction temperature range				 – 40 – 40 – 55		 + 90 +150 +105	 °C °C °C	
1.15	Thermal resistance junction ambient						60	K/W	
1.16	Substrate current which can be drawn without disturbances to upper defined blocks/functions(1)				–40			mA	

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. No substrate current occurs at pins K1, K2 down to V_{K1}, V_{K2} > –25V

4.1 Protection Against Substrate Currents

Due to the fact that the ATA6264 is connected to the wiring harness and to components outside of the ECU, negative voltages at the following pins might occur:

- IASG interface: IASG1, IASG2, IASG3, IASG4, IASG5
- USP comparator: USP

If substrate currents occur, it is guaranteed by design that no disturbance and malfunction of the following blocks and functions will happen:

- No disturbance of RESET block.
- No voltage changes of any regulators outside of their tolerances.
- No impact on digital circuitry (for example, changes of latches, status register, etc.)
- No latch up of any circuitry

5. Supply Currents

A minimum current has to flow into each pin for proper functioning of the IC.

Table 5-1. Electrical Characteristics – Supply currents

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.1	Supply current at K30	Standby mode: 0V = V_{K30} = 18V, V_{K15} = 3V and KEYLATCH = OFF	K30	I_{K30}	0		50	µA	A
2.1a	Supply current at K30	Standby mode: 18V < V_{K30} = 40V, V_{K15} = 3V and KEYLATCH = OFF	K30	I_{K30}	0		5	mA	A
2.1b	Supply current at K30	Startup mode: 0V < V_{K30} = 18V, V_{K15} > 4.15V or KEYLATCH = ON, V_{EVZ} = 0V, C_{CP} = 47 nF	K30	I_{K30}	0		7	mA	A
2.1c	Supply current at K30	Startup mode: 18V < V_{K30} = 40V V_{K15} > 4.15V or KEYLATCH = ON V_{EVZ} = 0V, C_{CP} = 47 nF	K30	I_{K30}	0		10	mA	A
2.1d	Supply current at K30	Normal mode: 0V < V_{K30} = 18V, V_{EVZ} > V_{K30}, V_{K15} > 4V or KEYLATCH = ON, SVCORE open, AMUX Measurement K30 active	K30	I_{K30}	0		6.5	mA	A
2.1e	Supply current at K30	Normal mode: 18V < V_{K30} = 40V, V_{EVZ} > V_{K30}, V_{K15} > 4.15V or KEYLATCH = ON, SVCORE open, AMUX Measurement K30 active	K30	I_{K30}	0		10	mA	A
2.2	Supply current at EVZ	Startup mode: 0V < V_{EVZ} = 40V, V_{SAT} = V_{PERI} = V_{CORE} = 0V, V_{K30} > 5V, V_{K15} > 4.15V, SVCORE and SVSAT open	EVZ	I_{EVZ}	0		5	mA	A
2.2a	Supply current at EVZ	Normal mode: 0V < V_{EVZ} = 40V, V_{PERI} and V_{CORE} > Reset Threshold, V_{EVZ} > V_{K30}, V_{SAT} = 10V, V_{K30} > 5V, V_{K15} > 4.15V, SVCORE and SVSAT open, AMUX Measurement EVZ active	EVZ	I_{EVZ}	0		6	mA	A
2.2b	Supply current at EVZ	Autonomous mode: 0V < V_{EVZ} = 40V, V_{PERI} and V_{CORE} > Reset Threshold, V_{EVZ} > V_{K30}, V_{SAT} = 10V, V_{K30} < 3.85V, V_{K15} < 3V, SVCORE and SVSAT open, AMUX Measurement EVZ active	EVZ	I_{EVZ}	0		10	mA	A
2.3	Supply current at VSAT	0V < V_{SAT} = 14V, SVPERI open, AMUX measurement VSAT active	VSAT	I_{VSAT}	0		1.5	mA	A
2.4	Supply current at VPERI	0V < V_{PERI} = 5.3V, AMUX measurement VPERI active	VPERI	I_{VPERI}	–0.2		2.2	mA	A
2.5	Supply current at VCORE	0V < V_{CORE} = 5.3V, AMUX measurement VCORE active	VCORE	I_{VCORE}	–0.45		1	mA	A

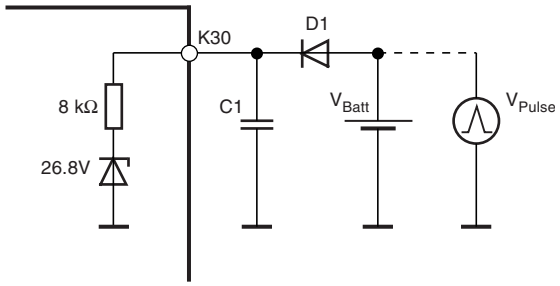
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

5.1 Discharger Circuit

Applications using the ATA6264 usually use a reverse polarity protection diode (D1 in Figure 5-1) in the power supply to prevent any damage if the wrong polarity is applied to V_{K30}. Unfortunately, this method includes some risk as can be seen in the following description:

During *Standby mode* (V_{K15} < 3V and KEYLATCH = OFF) the IC consumes only a low current, I_{K30}. Any peaks on the supply voltage (V_{Pulse} in Figure 5-1) will gradually charge the blocking capacitor (C1). D1 prevents the capacitor from being discharged via the power supply and the very small quiescent current via the IC can also be neglected. This means that during long periods of Standby mode, the IC's supply voltage could increase continuously until finally the maximum supply voltage limit would be exceeded and the IC could be damaged. ATA6264 therefore features a discharger circuit which avoids such unwanted effects. If V_{K30} exceeds a threshold value of approximately 26.8V, the blocking capacitor is discharged via an integrated resistor until V_{K30} again falls below the threshold.

Figure 5-1. Discharger Circuit



5.2 Initial Programming of the ATA6264

The ATA6264 supports different output voltages at the VSAT, VPERI and the VCORE regulators. In addition, different modes at the ISO9141 interfaces can be adjusted at the initial programming (IP). The memory cells are one-time programmable (OTP) and cannot be changed after the IP (default values are "0"). In general, the IP is done after mounting the ATA6264 on the PCB with an in-circuit tester. The programming voltage of 11.7V has to be applied on pin VSAT. It is also possible to use the VSAT regulator as the programming voltage because VSAT is programmed to 11.7V (±0.5V) as long as the Test mode is entered and the lock bit is not set. To ensure proper programming of the ATA6264, at least a 10-µF electrolytic cap and a 100-nF ceramic cap have to be applied at pin VSAT.

The following settings can be made at the initial programming:

MSBit							LSBit
VR1	VR2	VR3	VR4	EXT	ISO/LIN	Parity	Lock bit

Table 5-2. Initial Programming Settings

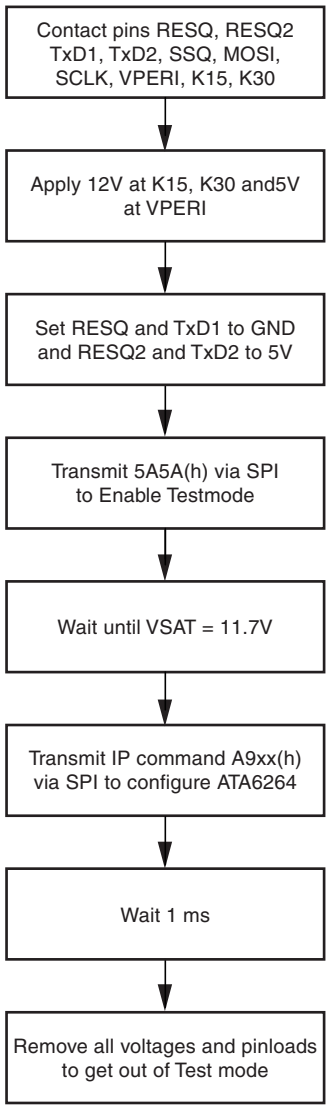
VR1	VR2	VR3	VR4	VCORE	VPERI	VSAT
0	0	0	0	All regulators deactivated (default)		
0	0	0	1	1.88V	3.3V	7.8V
0	0	1	0	1.88V	3.3V	9.1V
0	0	1	1	1.88V	3.3V	10.4V
0	1	0	0	2.5V	3.3V	7.8V
0	1	0	1	2.5V	3.3V	9.1V
0	1	1	0	2.5V	3.3V	10.4V
0	1	1	1	1.88V	5V	7.8V
1	0	0	0	1.88V	5V	9.1V
1	0	0	1	1.88V	5V	10.4V
1	0	1	0	2.5V	5V	7.8V
1	0	1	1	2.5V	5V	9.1V
1	1	0	0	2.5V	5V	10.4V
1	1	0	1	5V	5V	7.8V
1	1	1	0	5V	5V	9.1V
1	1	1	1	5V	5V	10.4V

	Set to 0	Set to 1
EXT	No external transistor at VPERI (default)	External transistor at VPERI applied

	Set to 0	Set to 1
ISO/LIN	ISO9141 mode is activated at K1 (default)	LIN mode is activated at K1

The IP data is valid only if the parity is odd. If the IP data is not valid, or if the lock bit is not set, the programming will not be executed.

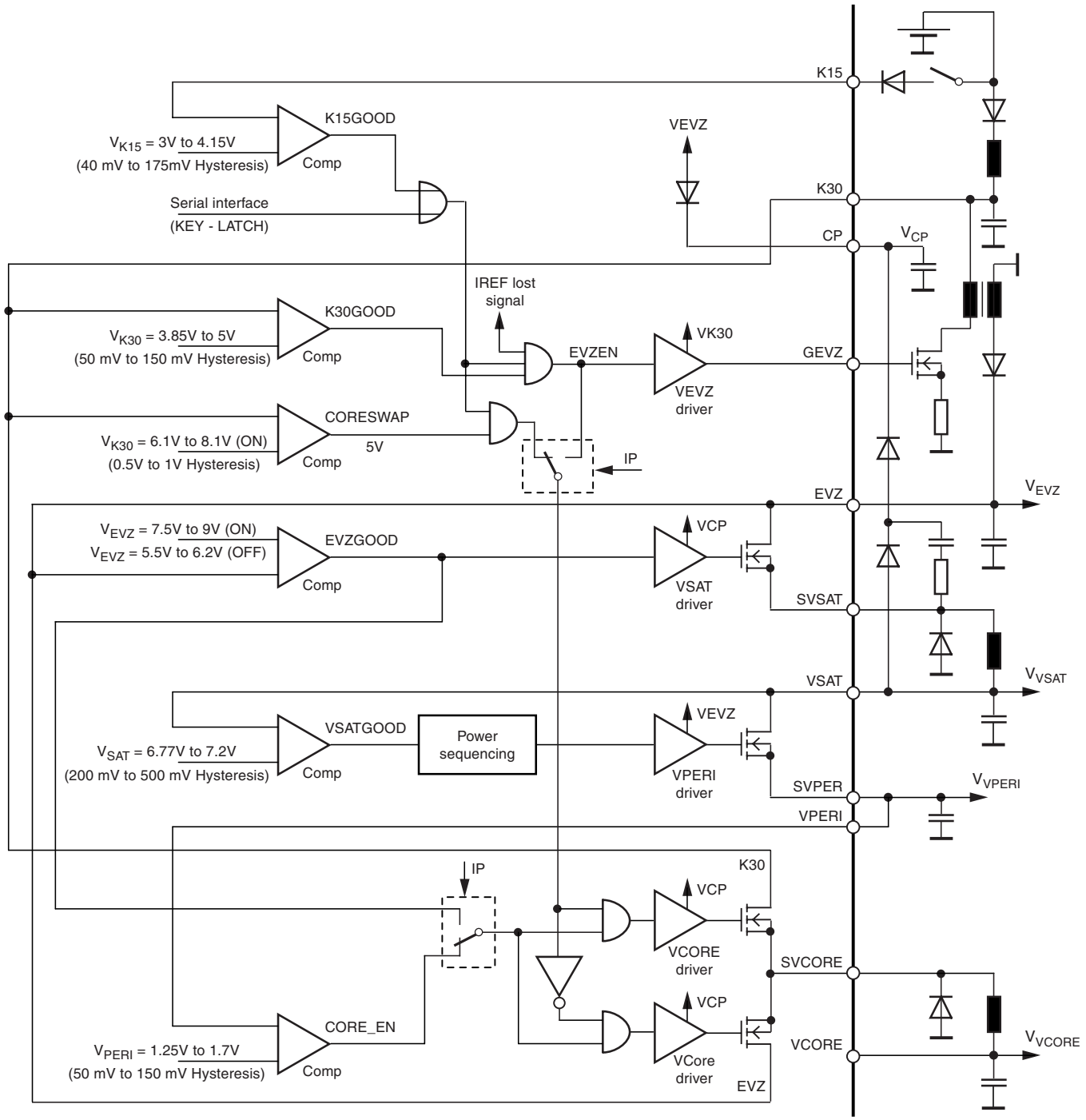
Figure 5-2. Programming Sequence



5.3 Start-up and Power-down Procedure

The ATA6264 is powered via the pin K30 (battery voltage) and via a diode or a resistor it is connected to the ignition key line K15. In order to detect an interruption on one of these pins correctly, resistors are implemented at these pins. Normally, the main supply pin of ATA6264 is pin K30. In the case of a missing or a too-low voltage at pin K30, the whole IC is supplied from the backup power supply capacitor hooked up to pin EVZ.

Figure 5-3. Block Diagram Start-up and Power-down Procedure



Depending on the initial programming of the ATA6264, the start-up procedure takes place in different phases.

5.3.1 Start-up Procedure if V_{VCORE} is Programmed to Be 5V or 2.5V

Phase1: After switching on the ignition key, K15 voltage will apply at pin K15. If, in addition, the voltage at pin K30 is larger than 3.85V to 5V, the EVZ regulator will be enabled. The signal K15GOOD can be replaced by the serial interface command KEYLATCH which can be set via the serial interface.

Phase2: If V_{EVZ} is larger than 7.5V to 9V the VSAT regulator starts operating and the VCORE regulator will be enabled.

Phase3: After V_{VSAT} has reached 6.77V to 7.2V, the VPERI regulator starts working. The VCORE regulator starts operating depending on the charge pump voltage.

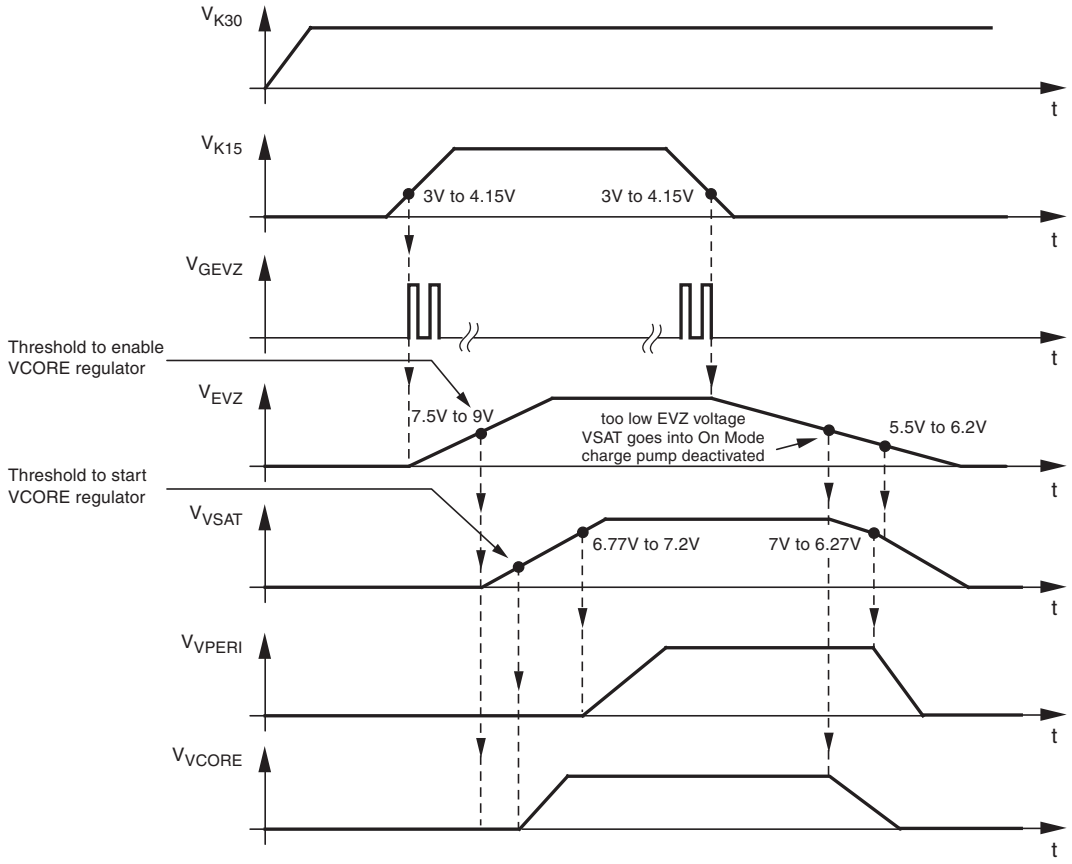
5.3.2 The Power-down Procedure Takes Place in Different Phases

Phase1: If the ignition key is switched off, K15 voltage will vanish at pin K15. If the serial interface command KEYLATCH is not set, the EVZ regulator stops working. The external charge pump is still working because EVZ is above VSAT and the VSAT regulator is not in *Permanent-on mode*. The charge-pump voltage still supplies the VSAT regulator and the VCORE regulator. Because the EVZ regulator stops working, VCORE will be switched to EVZ.

Phase2: The EVZ capacitor will be discharged, and as soon as the voltage at pin VSAT drops to low, the VSAT regulator will go into Permanent-on mode. If VSAT reaches Permanent-on mode, the external charge pump stops working and the VSAT voltage falls analog to the EVZ voltage. If the voltage at VSAT is below 6.27V to 7V, the VPERI regulator will be switched off. Depending on the charge-pump voltage, the VCORE regulator stops working.

Phase3: When the voltage at the EVZ capacitor gets to be lower than 5.5V to 6.2V, VSAT is switched off.

Figure 5-4. Start-Up and Power-Down Procedure if V_{VCORE} Programmed to Be 5V or 2.5V



5.3.3 Start-up Procedure if V_{VCORE} Programmed to Be 1.88V

Phase1: After switching on the ignition key, the K15 voltage will appear at pin K15. If, in addition, the voltage at pin K30 is larger than 3.85V to 5V, the EVZ regulator will be enabled. The signal K15GOOD can be replaced by the serial interface command KEYLATCH which can be set by the serial interface.

Phase2: If VEVZ is larger than 7.5V to 9V, the VSAT regulator starts operating.

Phase3: After VVSAT has reached 6.77V to 7.2V, the VPERI regulator starts working.

Phase4: If VVPERI is higher than 1.25V to 1.7V, the VCORE regulator will be enabled.

5.3.4 The Power-down Procedure for V_{VCORE} is Programmed to be 1.88V

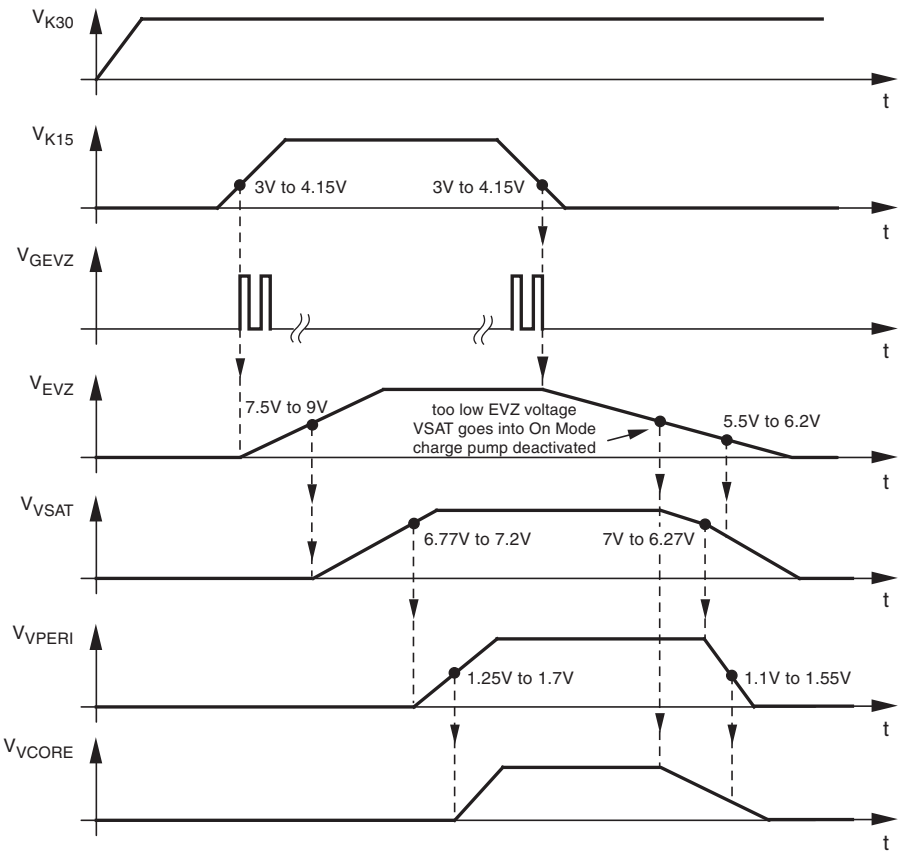
Phase1: If the ignition key is switched off, the K15 voltage will vanish at pin K15. If the serial interface command KEYLATCH is not set, the EVZ regulator stops working. The external charge pump is still working because EVZ is above VSAT and the VSAT regulator is not in the Permanent-on mode. The charge-pump voltage still supplies the VSAT regulator and the VCORE regulator. Because the EVZ regulator stops working, VCORE will be switched to EVZ.

Phase2: The EVZ capacitor will be discharged, and as soon as the voltage at pin VSAT drops too low, the VSAT regulator will go into Permanent-on mode. If VSAT reaches Permanent-on mode, the external charge pump stops working and the VSAT voltage falls analog to the EVZ voltage. If the voltage at VSAT is below 6.27V to 7V, the VPERI regulator will be switched off. Depending on the charge-pump voltage, the VCORE regulator stops working. The power sequencing function for the VPERI regulator is still active and guarantees a maximum voltage difference between VPERI and VCORE of 2.8V

Phase3: After VVPERI becomes lower than 1.1V to 1.55V, the VCORE regulator has to stop working.

Phase4: When the voltage at the EVZ capacitor is lower than 5.5V to 6.2V, VSAT is switched off.

Figure 5-5. Start-up and Power-down Procedure if V_{VCORE} Programmed to Be 1.88V



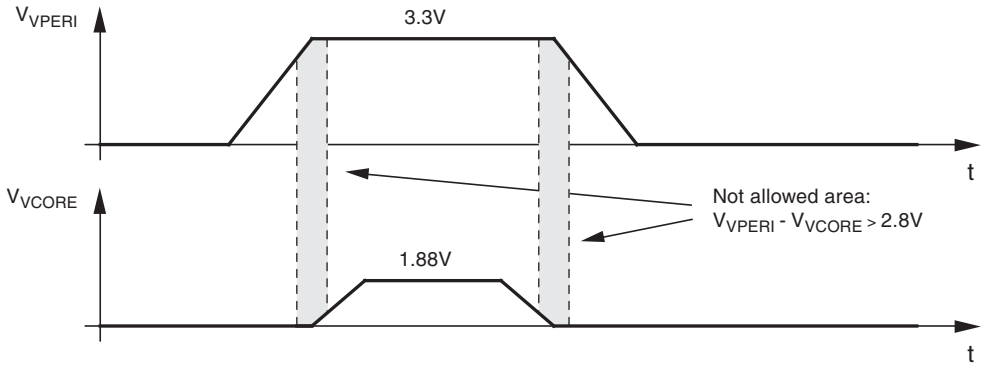
6. Power Supply Sequencing

(Only active when initial programming sets V_{VCORE} = 1.88V and V_{VPERI} = 3.3V)

In order to meet the requirements of several dual-voltage-supply microcontrollers, a power-sequencing function is implemented. The ATA6264 ensures that the voltage difference VPERI – VCORE will not exceed 2.8V.

The voltage difference between VPERI and VCORE is monitored. In error cases, for example, if the VCORE regulator does not start to work, the difference may rise above the 2.8V threshold. In this case, the VPERI regulator is switched off before reaching this level and switched on again if the voltage difference drops below a hysteresis value.

Figure 6-1. Example for Incorrect Ramp Up



Necessary for operation:
V_{EVZ} = 0V to 40V, V_{INT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{K30}, V_{VSAT}, V_{VPERI} and V_{VCORE} are within functional range limits, T_j = –40°C to 150°C

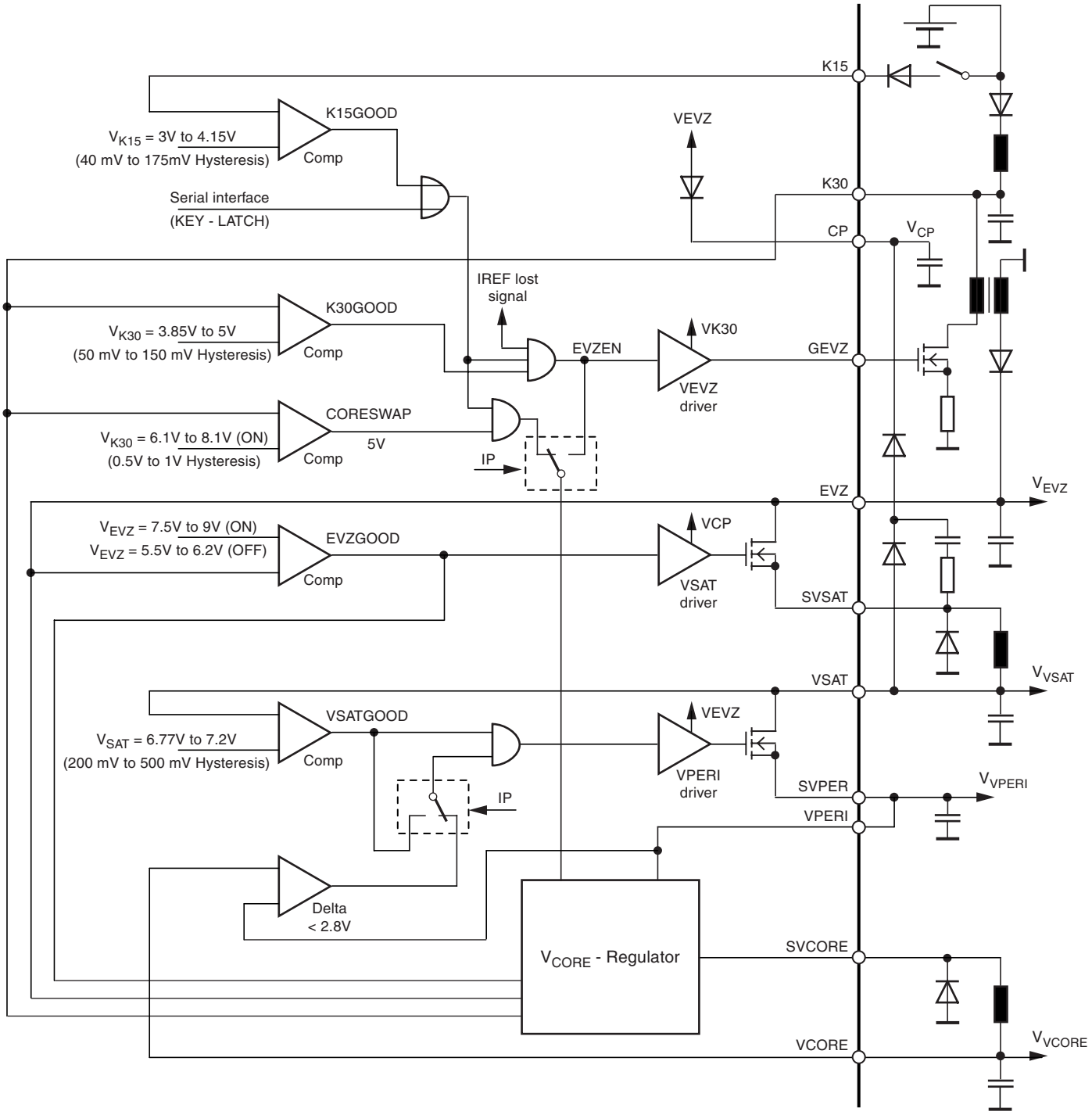
Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 6-1. Electrical Characteristics – Power Supply Sequencing

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
5.1	Maximum voltage difference $V_{VPERI} – V_{VCORE}$		VPERI, VCORE	$V_{VPERI} – V_{VCORE}$	0		2.8	V	A
5.2a	Voltage level $V_{VPERI} – V_{VCORE}$ to switch off VPERI regulator		VPERI, VCORE	$V_{VPERI} – V_{VCORE}$	2.3		2.8	V	A
5.2b	Hysteresis for $V_{VPERI} – V_{VCORE}$ to enable VPERI regulator			V_{HYS}			100	mV	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 6-2. Block Diagram Power Supply Sequencing

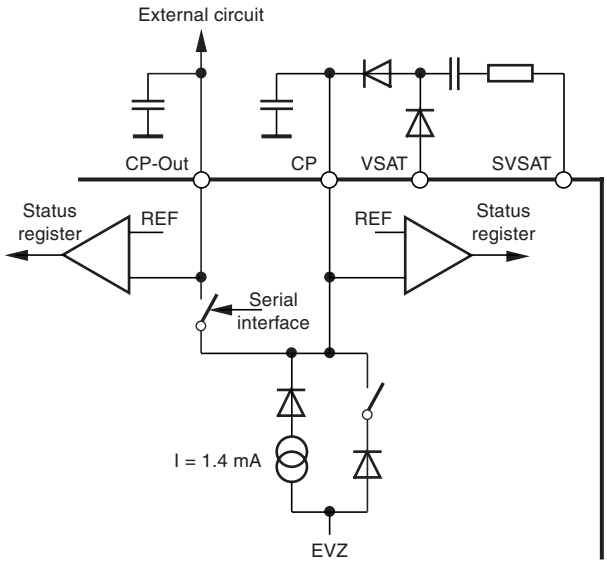


7. Charge Pump

To supply the VSAT and VCORE drivers, an external charge pump is provided. Both FETs[1] are driven by the high charge pump voltage V_{CP} to ensure that they can be switched to a low-ohmic state. For correct function of the charge pump, an external capacitor of C = 47 nF has to be connected to pin SVSAT, and another of C = 100 nF to pin CP. A double diode has to be implemented for proper function of the charge pump. An external series resistor is recommended to suppress spikes during switching of the SVSAT. The CP block is supplied by EVZ and VSAT voltage and starts to operate as soon as the thresholds for VK15, K30 and EVZ are achieved. An additional start-up circuitry is implemented to support the VSAT driver during the start-up phase, thus enabling a reliable system startup.

The charge pump has an output CP-OUT to supply the external circuitry, and can be switched via the SPI. It is capable of 250 µA.

Figure 7-1. Block Diagram Charge Pump



Note: 1. Connected to the drivers (see Figure 5-3)

Necessary for operation:
V_{EVZ} = 5.5V to 40V or V_{K30} = 5.5V to 40V, V_{K15} > 3V, V_{VINT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{VSAT}, V_{VPERI} and V_{VCORE} are within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 7-1. Electrical Characteristics – Charge Pump

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
6.11	Supply current at pin CP	CP off, supply of internal circuitry	CP	I_{CP}	0		50	µA	A
6.12	Time between wrong CP-OUT voltage and valid data in status register		CP-OUT	t_d	0		50	µs	A
6.13	Current limitation at pin CP-OUT		CP-OUT	I_{CP-OUT}	–0.8		–4.2	mA	A
6.14	Voltage difference $V_{CP} – V_{EVZ}$ for detecting wrong CP	Note: Threshold is in the range of 5V to 7V	CP	V_{Diff}			5	V	A
6.15	Time between wrong CP voltage and valid data in status register		CP	t_d	0		50	µs	A
6.16	Voltage difference $V_{CP-OUT} – V_{EVZ}$ for detecting wrong CP-OUT	Note: Threshold is in the range of 5V to 7V	CP-OUT	V_{Diff}			5	V	A
6.17	Voltage at pin CP	V_{EVZ} = 5.5V to 40V, $V_{K30} < V_{EVZ}$ $I_{CP} + I_{CP\_Out}$ = –100 µA (current consumption of V_{SAT} and V_{CORE} have to be added)	CP	V_{CP}	V_{EVZ} + 7		V_{EVZ} + 11	V	A
6.18	Voltage at pin CP	V_{EVZ} = 5.5V to 40V, $V_{K30} < V_{EVZ}$ $I_{CP} + I_{CP\_Out}$ = –100 µA (current consumption of V_{SAT} and V_{CORE} have to be added)	CP	V_{CP}	V_{K30} + 7		V_{K30} + 11	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. GKEY Function

The GKEY function is used to enable or disable the ECU via a powerless signal. If the voltage at pin K15 is larger than 3V to 4.15V, the charge pump and the EVZ regulator (for correct EVZ function, the K30 pin has to be connected to the battery) will start operating. If the K15 pin is open, an internal pull-down resistor of approximately 220 kΩ discharges the pin. A logical connection between the voltage at the K15 pin, a serial-interface-driven latch command, and the K30 voltage determines the EVZ Enable signal. In order to achieve the *Switch Function* of the GKEY function, a transformer has to be used.

Table 8-1. Overview of the Start-up Conditions

V_{K30}	V_{K15}	Serial-interface-driven Latch (Default: "0" = OFF)	EVZ Regulator
Low[1)]	x	x	Disabled
High[2)]	High[3)]	x	Enabled
High[2)]	x	1	Enabled

Note:
1. Less than the value shown in number 7.3 of Table 8-2 on page 23
2. Greater than the value shown in number 7.3 of Table 8-2 on page 23
3. Greater than the value shown in number 7.1 of Table 8-2 on page 23

Figure 8-1. Application With Low-current Switch (GKEY Function Used)

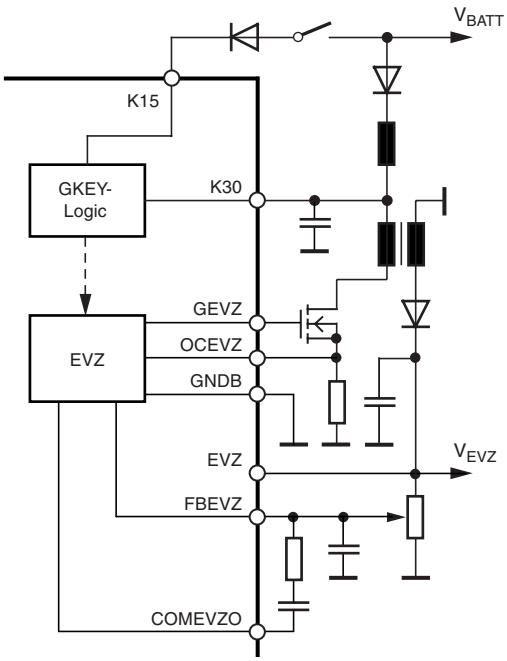
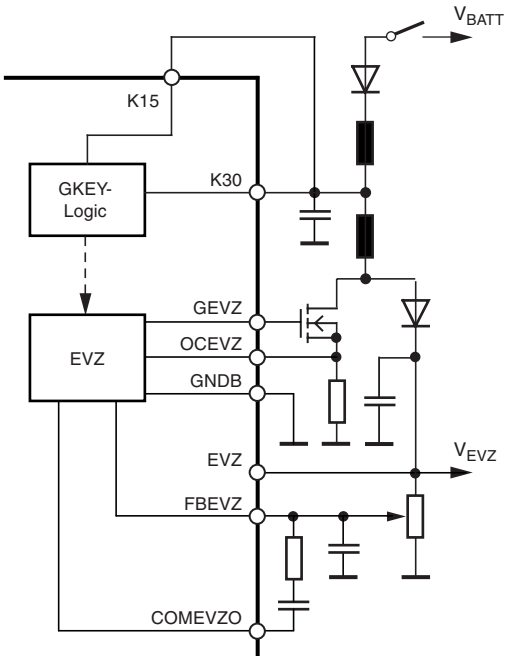


Figure 8-2. Application With High Current Switch (GKEY Function Not Used)



Necessary for operation:
V_{K15} = 3V to 40V, V_{K30} = 3.85V to 40V

Operating conditions of all other supply pins:
V_{EVZ}, V_{SAT}, V_{PERI} and V_{CORE} are within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 8-2. Electrical Characteristics – GKEY Function

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
7.1	Voltage level at K15 to enable the EVZ regulator	V_{K15} increasing, V_{K30} > 5V	K15	V_{K15}	3		4.15	V	A
7.2	Hysteresis at K15 to disable the EVZ regulator		K15	V_{K15}	40		175	mV	A
7.3	Voltage level at K30 to enable the EVZ regulator	V_{K30} increasing, V_{K15} > 4.15V	K30	V_{K30}	3.85		5	V	A
7.4	Hysteresis at K30 to disable the EVZ regulator		K30	V_{K30}	50		150	mV	A
7.5	Pull-down resistor at K15		K15	R_{K15}	70		365	kΩ	A
7.6	Pull-down resistor at K30		K30	R_{K30}	320		1700	kΩ	A
7.7	Current at K15	0V ≤ V_{K15} ≤ 40V, AMUX measurement EVZ active	K15	I_{K15}	0		1.1	mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. EVZ Step-up Regulator

A boost converter generates the supply voltage for energy reserve and firing capacitors in the system. Using a voltage divider at pin FBEVZ, this voltage can be adjusted between 15V and 40V. Thus, high-voltage charged capacitors will be used to supply the whole system during the stand-alone time (for example, broken K30 line after a crash). The step-up regulator has to start running as soon as a certain threshold voltage at the K15 pin is exceeded. The regulator has to stop running again if the voltage at the K15 pin falls below a voltage level (or voltage at pin K30 is missing, see Section 5.3 ”Start-up and Power-down Procedure” on page 14).

An inductor is PWM-switched by an external n-channel power FET with a fixed frequency of 100 kHz. A driver stage for the external FET is integrated into the ATA6264. The current limitation of the external FET is implemented by using an external resistor in series between the source connection of the external FET and GND, sensing the voltage drop at this resistor via the pins OCEVZ and GNDA.

The reference section provides a reference voltage of 1.24V for the regulation loop. An error amplifier compares the reference voltage with the feedback signal, which is provided either from two different serial-interface-programmable internal dividers (VEVZ1 = 22V, VEVZ2 = 31.5V) or an external voltage divider network (VEVZExt). These dividers determine the output voltage EVZ.

Figure 9-1. EVZ Regulator With External Divider

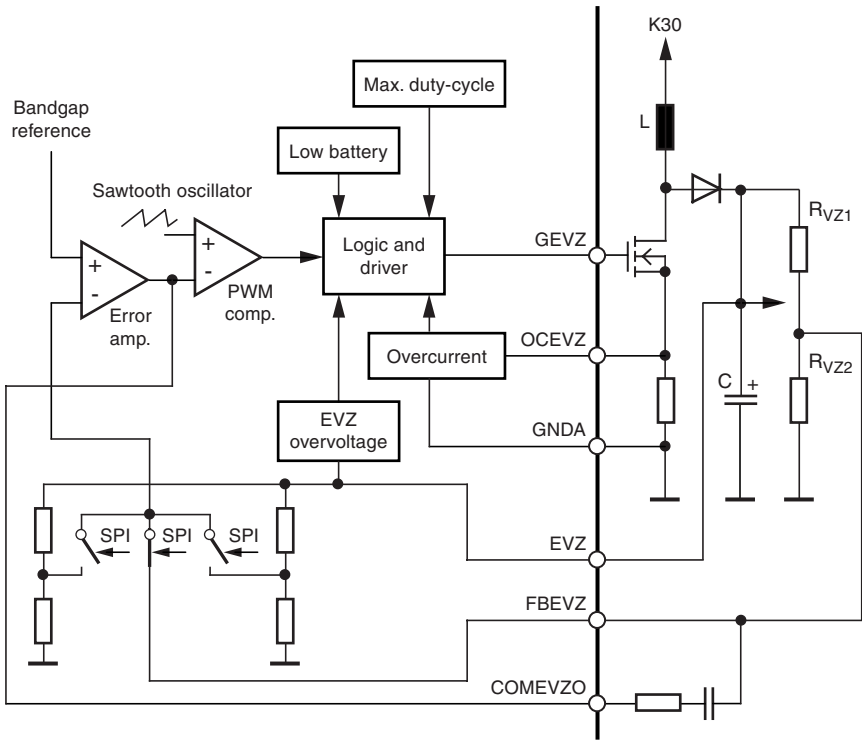
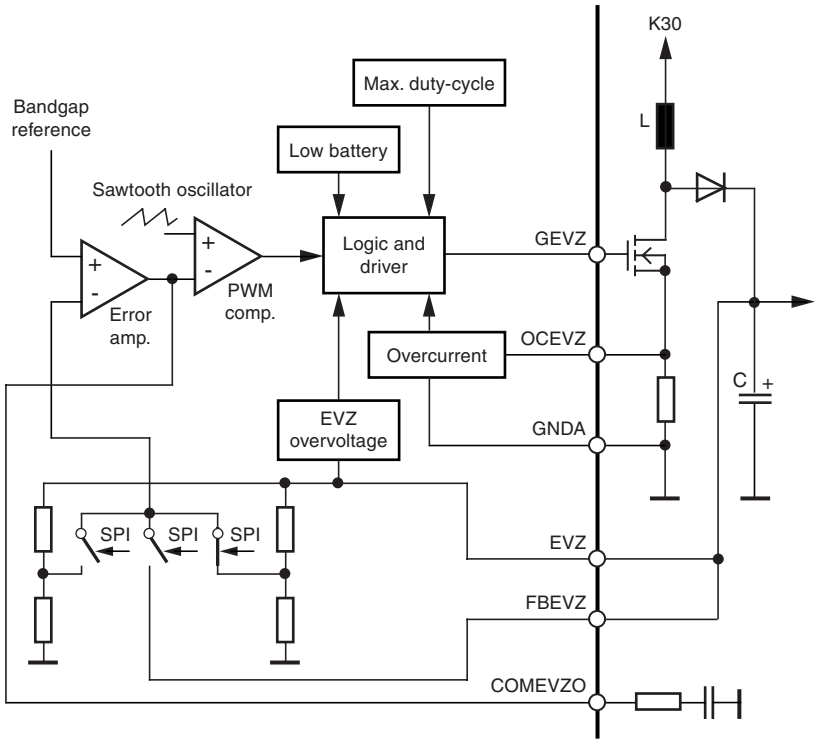


Figure 9-2. EVZ Regulator With Internal Divider



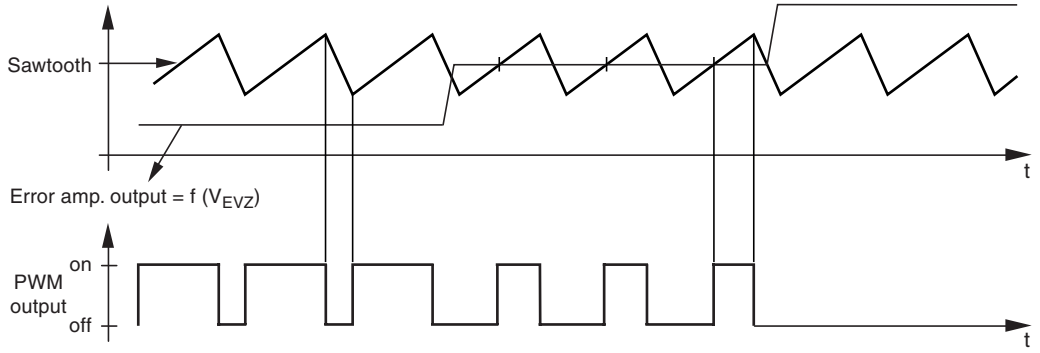
A draft formula for calculating the EVZ voltage, which is programmed by the external voltage divider network at pin FBEVZ, is:

$$V_{EVZ} = V_{REF} \times \frac{R_{VZ1} + R_{VZ2}}{R_{VZ2}}$$

The pins EVZ and FBEVZ have to be shorted in applications without an external divider in order to ensure a safe operation of the ATA6264 in the case of an EVZ-pin fault. If the voltage at pin FBEVZ is larger than the voltage at pin EVZ, the ATA6264 switches the feedback path automatically to pin FBEVZ. The remaining voltage at FBEVZ causes the regulator to switch off.

The output of the error amplifier is compared with a periodic linear ramp of a saw-tooth generator by the PWM comparator. A logic signal with variable pulse width is generated, which controls the PWM frequency of the external FET. A maximum duty cycle is determined by the duration of the falling ramp of the saw-tooth oscillator. The saw-tooth generator is controlled by the internal 100-kHz oscillator.

Figure 9-3. Functional Principle of the EVZ Regulator



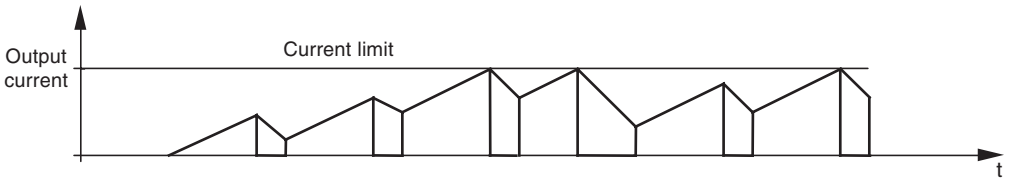
The output transistor conduction is suppressed immediately if the current through the power FET exceeds a certain level, determined by the voltage drop across an external resistor in the range of 0.2Ω. The ATA6264 itself will see a voltage at the OCEVZ pin. If this voltage exceeds typically 0.5V, the output transistor conduction has to be suppressed.

The external FET also has to be switched off if a low battery voltage at K30 or overvoltage on pin EVZ is detected. Multiple output pulses at pin GEVZ during one oscillator period are suppressed by internal logic.

In the default state - for example, before the minimum input voltage for starting the regulator has been reached - the external transistor is switched off.

During startup, the voltage on pin EVZ is too low and the PWM comparator requires a duty cycle of more than 90%. Due to an increasing inductance current, after several periods the overcurrent sensor becomes active and reduces the maximum duty cycle to improve magnetic energy transfer.

Figure 9-4. Output Current During Start-up



A capacitance of 10 mF or more may be applied at pin EVZ. The equivalent series resistance (ESR) should have a value of less than 0.5Ω

After power-on, the default state of the internal dividers should always be the low EVZ voltage divider.

The voltage at pin GNDA is compared with the voltage at pin GNDD, and if GNDA is not connected, bit b6 of the APACE status register is set. Pin GNDB is also compared with pin GNDD. Pin GNDB not being connected will also result in bit b6 being set, and, additionally, in the EVZ regulator being switched off.

Necessary for operation:
V_{K15} = 3V to 40V, V_{K30} = 5V to 40V, C_{GEVZ} = 200 pF to 2 nF, V_{INT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{SAT}, V_{PERI} and V_{CORE} are within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 9-1. Electrical Characteristics – EVZ Step-up Regulator

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
8.1	Switching frequency	$V_{K30} \geq 8V$ or $V_{EVZ} \geq 8V$ (after startup)	GEVZ	f_{GEVZ}	–5%	100	+5%	kHz	A
8.2	Switching frequency	$4V < V_{K30} < 8V$ or $4V < V_{EVZ} < 8V$ (after startup)	GEVZ	f_{GEVZ}	–10%	100	+10%	kHz	A
8.3	Voltage level at K15 to start the EVZ regulator	See number 7.1 of Table 8-2 on page 23							A
8.4	Hysteresis at K15 to stop the EVZ regulator	See number 7.2 of Table 8-2 on page 23							A
8.5	Voltage level at K30 to start the EVZ regulator	See number 7.3 of Table 8-2 on page 23							A
8.6	Hysteresis at K30 to stop the EVZ regulator	See number 7.4 of Table 8-2 on page 23							A
8.7	Voltage at pin GEVZ to switch through the external driver	$V_{K30} \geq 3.85V$ to 5V (ON threshold)	GEVZ	V_{GEVZ}	V_{K30} – 0.5V		V_{K30}	V	A
8.8	Voltage at pin GEVZ to switch through the external driver	$V_{K30} \geq 7V$	GEVZ	V_{GEVZ}	6		10	V	A
8.9	Driving current at pin GEVZ to switch through the external driver	$V_{GEVZ} \leq 5V$	GEVZ	I_{GEVZ}	–600		–80	mA	A
8.10	Gate charge delivered to the external FET	$V_{GEVZ} = 5V$	GEVZ	Q_{GEVZ}	10			nC	D
8.11	Gate charge delivered to the external FET	$V_{GEVZ} = 10V$	GEVZ	Q_{GEVZ}	20			nC	D
8.12	Pull-down resistor at pin GEVZ		GEVZ	R_{GEVZ}	20		50	kΩ	A
8.13	R_{Dson} of dynamic sinking transistor at GEVZ		GEVZ	R_{GEVZ}			28	Ω	A
8.15	Voltage between pins OCEVZ and GND to detect overcurrent		OCEVZ	V_{OCEVZ}	0.475		0.525	V	A
8.16	Maximum switch duty cycle	$V_{K30} \geq 8V$ or $V_{EVZ} \geq 8V$ (after startup) $V_{EVZ} \geq 8V$	GEVZ	D_{GEVZ}	87.5	90	92.5	%	A
8.17	Maximum switch duty cycle	$4V < V_{K30} < 8V$ or $4V < V_{EVZ} < 8V$ (after startup)	GEVZ	D_{GEVZ}	75	90	92.5	%	A
8.18	Minimum switch duty cycle		GEVZ	D_{GEVZ}			0	%	A
8.19	Overvoltage at pin EVZ to switch off the regulator	V_{EVZExt} programmed (via external divider)	VEVZ	V_{EVZ}	40.5		46.2	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 9-1. Electrical Characteristics (Continued)– EVZ Step-up Regulator

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
8.19a	Overvoltage at pin EVZ to switch off the regulator	V_{EVZ1} programmed	VEVZ	V_{EVZ}	25		28.5	V	A
8.19b	Overvoltage at pin EVZ to switch off the regulator	V_{EVZ2} programmed	VEVZ	V_{EVZ}	35		39.5	V	A
8.20	Overvoltage switch-off time	Time between reaching overvoltage and reaching 90% of the value at numbers 8.7 and 8.8 of Table 9-1 on page 27	GEVZ	t_{offov}			200	ns	D
8.21	Overcurrent switch-off time	Time between reaching overcurrent and reaching 90% of the value at numbers 8.7 and 8.8 of Table 9-1 on page 27	GEVZ	t_{offoc}			500	ns	A
8.22	Switch-on delay time for the boost converter output stage		GEVZ	t_{don}	50		250	ns	A
8.23	Switch-on rise time for the boost converter output stage	Time between 0.5V and 4.5V at GEVZ, C_{GEVZ} = 2 nF	GEVZ	t_{ron}	10		200	ns	A
8.24	Switch-off delay time for the boost converter output stage		GEVZ	t_{doff}	50		150	ns	A
8.25	Switch-off fall time for the boost converter output stage	Time between 4.5V and 0.5V at GEVZ, C_{GEVZ} = 2 nF	GEVZ	t_{foff}	10		100	ns	A
8.26	Leakage current at pin OCEVZ		OCEVZ	I_{OCEVZ}	–10		+10	µA	A
8.27	Leakage current at pin FBEVZ		FBEVZ	I_{OCEVZ}	–10		+10	µA	A
8.28	Switch-on threshold via FBEVZ	Band-gap tolerance included	FBEVZ	V_{FBEVZ}	1.20	1.24		V	A
8.29	Switch-on threshold via FBEVZ	Band-gap tolerance included	FBEVZ	V_{FBEVZ}		1.24	1.28	V	A
8.30	V_{EVZ} voltage #1 set by SPI	V_{EVZ1} programmed, Band-gap tolerance included	EVZ	V_{EVZ1}	20		23	V	A
8.31	V_{EVZ} voltage #2 set by SPI	V_{EVZ2} programmed, Band-gap tolerance included	EVZ	V_{EVZ2}	28.6		33	V	A
8.31a	Temperature shutdown activation			T_{off}	155		185	°C	B
8.31b	Hysteresis for reactivation of GEVZ			T_{hys}	5		25	K	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 9-1. Electrical Characteristics (Continued)– EVZ Step-up Regulator

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
Error Amplifier									
8.32	Output current at pin COMEVZO sinking to low		COMEVZO	$I_{COMEVZO}$	0.4		3	mA	A
8.33	Output current at pin COMEVZO driving to high		COMEVZO	$I_{COMEVZO}$	–1000		–150	µA	A
8.34	Input offset voltage				–10		+10	mV	D
8.35	DC open-loop gain				70			dB	D
8.36	Unity-gain bandwidth				2			MHz	D
8.37	Output voltage low on pin COMEVZO	$I_{COMEVZO}$ = 100 µA	COMEVZO	$V_{COMEVZO}$	0		0.2	V	A
8.38	Output voltage high on pin COMEVZO	$I_{COMEVZO}$ = –100 µA	COMEVZO	$V_{COMEVZO}$	VINT – 0.3V		VINT	V	A
GNDA/GNDB Disconnect									
8.40	GNDA lost detection	$V_{GNDA} – V_{GNDD}$	GNDA	V_{GNDA}	0.2		0.4	V	A
8.41	Delay for GNDA lost detection		GNDA	td	10		50	µs	A
8.42	GNDB lost detection	$V_{GNDB} – V_{GNDD}$	GNDB	V_{GNDB}	0.2		0.4	V	A

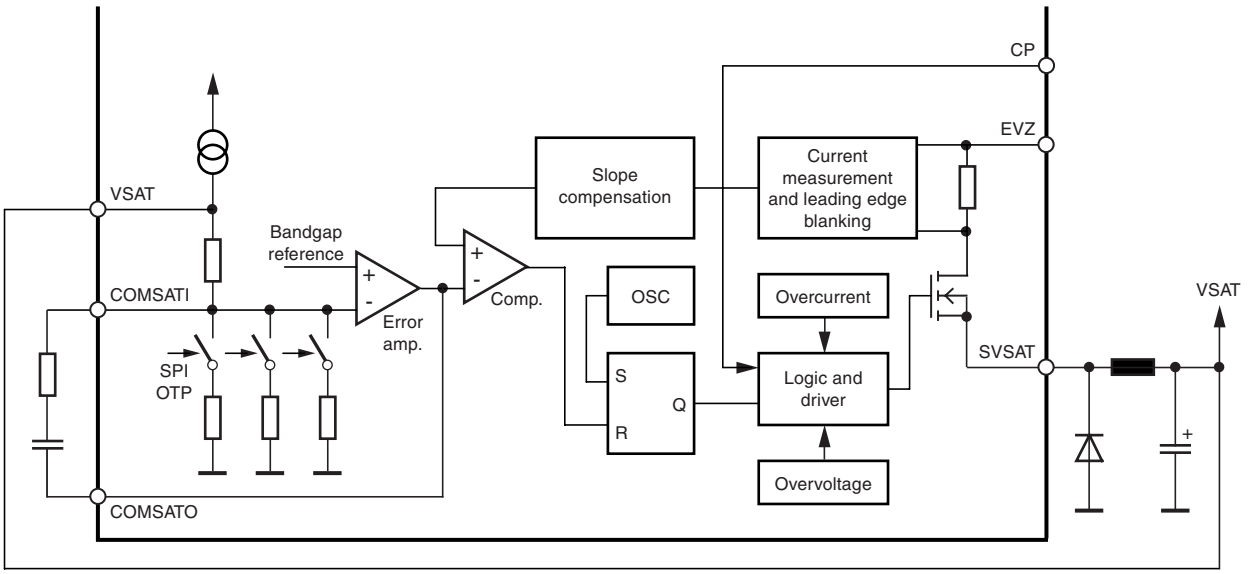
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

10. VSAT Power Supply

A stabilized VSAT supply is realized by a buck converter. An external inductance is PWM-switched with a frequency of 200 kHz via an internal high-side DMOS power transistor. The VSAT power supply is connected to the boost converter output (EVZ), and uses the stored energy of the boost converter capacitor if the voltage at K30 is missing. The regulator uses both current and voltage feedback. The basis for the regulation loop is a temperature-compensated band-gap reference voltage, which is compared with the internally divided output voltage VSAT. The error amplifier output is applied to the inverting input of a comparator, the current feedback is connected with the positive input. The PWM flip-flop (which is set every 5 µs by the oscillator) is reset if the current feedback reaches the error amplifier level. In order to adjust the compensation of the regulation loop and therefore improve the behavior in case of load changes in continuous-mode operation, pin COMSATO has to be connected to COMSATI via a compensation network. Because of the fact that current-mode-controlled converters exhibit sub-harmonic oscillations when operating at duty cycles higher than 50%, a slope compensation (which adds an artificial ramp to the comparator) is implemented. If the regulator input voltage at pin EVZ is too low, the regulator switches to a duty cycle of 100% (Permanent-on mode).

The VSAT voltage can be programmed via the serial interface to one of three different voltage values during initial programming.

Figure 10-1. Functional Principle of the VSAT Regulator



The duration of the output transistor conduction depends on the VSAT level and current feedback. Conduction is suppressed immediately if the current through the output transistor exceeds 850 mA typically. A logic circuit disables, in the case of short spikes, multiple-pulse operation during one oscillating period. If pin VSAT is open (VSAT loss), an internal current source connected to a higher voltage than VSAT acts as pull-up for this pin, to prevent the VSAT voltage from rising up to EVZ. In order to ensure the gate voltage for the output transistor, the driver stage is supplied by the charge pump (pin CP).

Necessary for operation:
V_{EVZ} = 5.5V to 40V, $V_{CP} > V_{EVZ}$ + 7V, V_{INT} = 3.7V to 5.45V

Operating conditions of all other supply pins:
V_{K30}, V_{PERI} and V_{CORE} are within functional range limits, T_j = –40°C to +150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 10-1. Electrical Characteristics – VSAT Power Supply

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
9.1	V_{EVZ} voltage for the buck converter to start running		EVZ	V_{EVZ}	7.5		9	V	A
9.2	V_{EVZ} voltage for the buck converter to stop		EVZ	V_{EVZ}	5.5		6.2	V	A
9.3	Regulator switch-on time via pin EVZ		SVSAT	t_{SVSAT}	0		20	µs	A
9.4	Regulator switch-off time via pin EVZ		SVSAT	t_{SVSAT}	0		5	µs	A
9.5	Regulator switching frequency	$V_{EVZ} \geq 8V$	SVSAT	f_{SVSAT}	–5%	200	+5%	kHz	A
9.5a	Regulator switching frequency	$5.5V > V_{EVZ} \geq 8V$	SVSAT	f_{SVSAT}	–10%	200	+10%	kHz	A
9.6	Output current limit		SVSAT	I_{SVSAT}	0.8		1	A	A
9.7	R_{Dson} of output transistor		SVSAT	R_{SVSAT}			1	Ω	A
9.8	Output voltage #1 only at V_{PERI} = 3.3V	Band-gap tolerance included	VSAT	V_{VSAT1}	–4%	7.8	+4%	V	A
9.9	Output voltage #2	V_{VSAT2} programmed, Band-gap tolerance included	VSAT	V_{VSAT2}	–4%	9.1	+4%	V	A
9.10	Output voltage #3	V_{VSAT3} programmed, Band-gap tolerance included	VSAT	V_{VSAT3}	–4%	10.4	+4%	V	A
9.11	Output transistor switch-on time	Time between reaching $0.1 \times (V_{EVZmax} - V_{SVSATmin})$ and $0.9 \times (V_{EVZmax} - V_{SVSATmin})$					150	ns	A
9.12	Output transistor switch-on time	Time between reaching $0.9 \times (V_{EVZmax} - V_{SVSATmin})$ and $0.1 \times (V_{EVZmax} - V_{SVSATmin})$					150	ns	A
9.13	Overvoltage switching off the regulator		VSAT	V_{VSAT}			$1.1 \times V_{SATX}$	V	A
9.14	Overvoltage switch-on time	Time between reaching overvoltage and reaching 90% of V_{SVSAT} maximum under on condition	SVSAT	$t_{SVSAToff}$	0		0.4	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Depending on implementation of slope compensation; sub-harmonics must be prevented
2. The value of the minimum load current must be higher than the internal pull-up current at pin VSAT to ensure proper function of the regulator

Table 10-1. Electrical Characteristics (Continued)– VSAT Power Supply

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
9.15	Overcurrent switch-on time	Time between reaching overcurrent and reaching 90% of V_{SVSAT} maximum under on condition	SVSAT	$t_{SVSAToff}$	0		0.5	µs	A
9.16	Leakage current at pin SVSAT	Output transistor off	SVSAT	I_{SVSAT}	–10		+10	µA	A
Error Amplifier									
9.17	Maximum output current at pin COMSATO sinking to low		COMSATO	$I_{COMSATO}$	200		3000	µA	A
9.18	Maximum output current at pin COMSATO sourcing to high		COMSATO	$I_{COMSATO}$	–165		–85	µA	A
9.19	Input impedance at pin COMSATI		COMSATI	$R_{COMSATI}$	9		23	kΩ	A
9.20	Input offset voltage				–10		+10	mV	D
9.21	DC open-loop gain				70			dB	D
9.22	Unity-gain bandwidth				2			MHz	D
9.23	Output voltage low	$I_{COMSATO}$ = 165 µA	COMSATO	$V_{COMSATO}$	0		0.3	V	A
9.24	Output voltage high	$I_{COMSATO}$ = –85 µA	COMSATO	$V_{COMSATO}$	V_{VINT} – 0.6V		V_{VINT}	V	A
9.25	Leading-edge blanking time			t_{blank}	150		200	ns	D
9.26	Slope of artificial ramp for slope compensation			dV/dt	150(1)		240(1)	mV/µs	D
9.27	VSAT loss detection threshold(2)			I_{Load}	0		1.5	mA	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

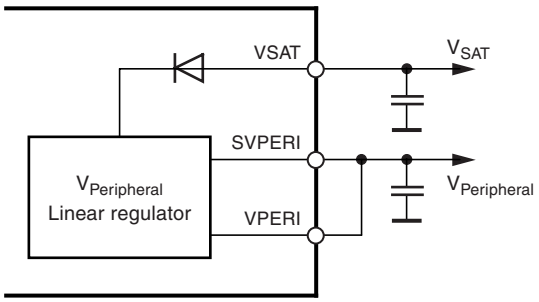
Notes: 1. Depending on implementation of slope compensation; sub-harmonics must be prevented

2. The value of the minimum load current must be higher than the internal pull-up current at pin VSAT to ensure proper function of the regulator

11. VPERI Power Supply

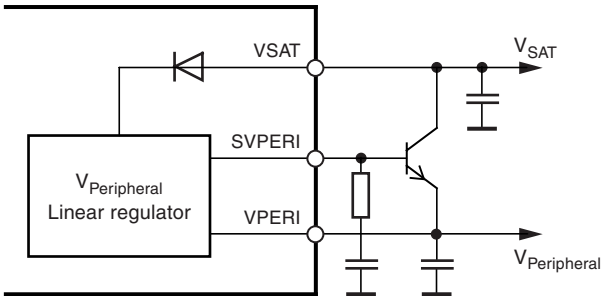
With the V_{PERI} regulator a stabilized and ripple-free voltage is generated out of the VSAT supply voltage. This voltage is intended to be used for sensitive components, for example, sensors or reference inputs of A/D converters from microcontrollers. For this reason, a linear regulator is implemented to guarantee high ripple rejection and a precise voltage. The regulator output is short-circuit protected by an overcurrent protection. If pin VPERI is disconnected, the regulator is switched off and RESQ/RESQ2 are set to low.

Figure 11-1. Functional Principle of the $V_{Peripheral}$ Regulator



If a higher current capability of the regulator is requested or if the power dissipation of the linear regulator is too high, an external transistor can boost the regulator.

Figure 11-2. Functional Principle of the VPERI Regulator With External Boost Transistor



The VPERI voltage can be programmed via the serial interface to one of two different voltage values during initial programming.

Necessary for operation:
V_{SAT} > 7.5V, V_{INT} = 3.7V to 5.47V, V_{CORE} < V_{PERI} + 0.3V

Operating conditions of all other supply pins:
V_{K30}, V_{EVZ} and V_{CORE} are within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 11-1. Electrical Characteristics – VPERI Power Supply

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
10.1	Voltage level at VSAT to enable VPERI regulator		VSAT	V_{VSAT}	6.77		7.2	V	A
10.2	Hysteresis at VSAT to disable VPERI regulator		VSAT	V_{VSAT}	0.2		0.5	V	A
10.3	Output voltage #1	V_{VPERI1} programmed, band-gap tolerance included	VPERI	V_{VPERI}	–3.6%	5	+4%	V	A
10.4	Output voltage #2	V_{VPERI2} programmed, band-gap tolerance included	VPERI	V_{VPERI}	–4%	3.3	+3%	V	A
10.5	Output current	V_{VSAT} = 7.5V to 12.5V	VPERI	I_{VPERI}	–100			mA	A
10.6	Short-circuit current		VPERI	I_{VPERI}	–200		–110	mA	A
10.7	Line regulation	V_{VSAT} = 8V to 12.5V I_{PERI} = –1 mA to –100 mA (I_{PERI} is constant during measurement)	VPERI	V_{VPERI}	–10		+10	mV	A
10.8	Load regulation	V_{SAT} = 8V to 12.5V (V_{VSAT} is constant during measurement) I_{PERI} = –1 mA to –100 mA	VPERI	V_{VPERI}	–10		+10	mV	A
10.10	Supply voltage rejection	I_{PERI} = –100 mA, f = 100 kHz – 20 MHz, C_{PERI} = 47 µF + 100 nF (ceramic)			40			dB	D

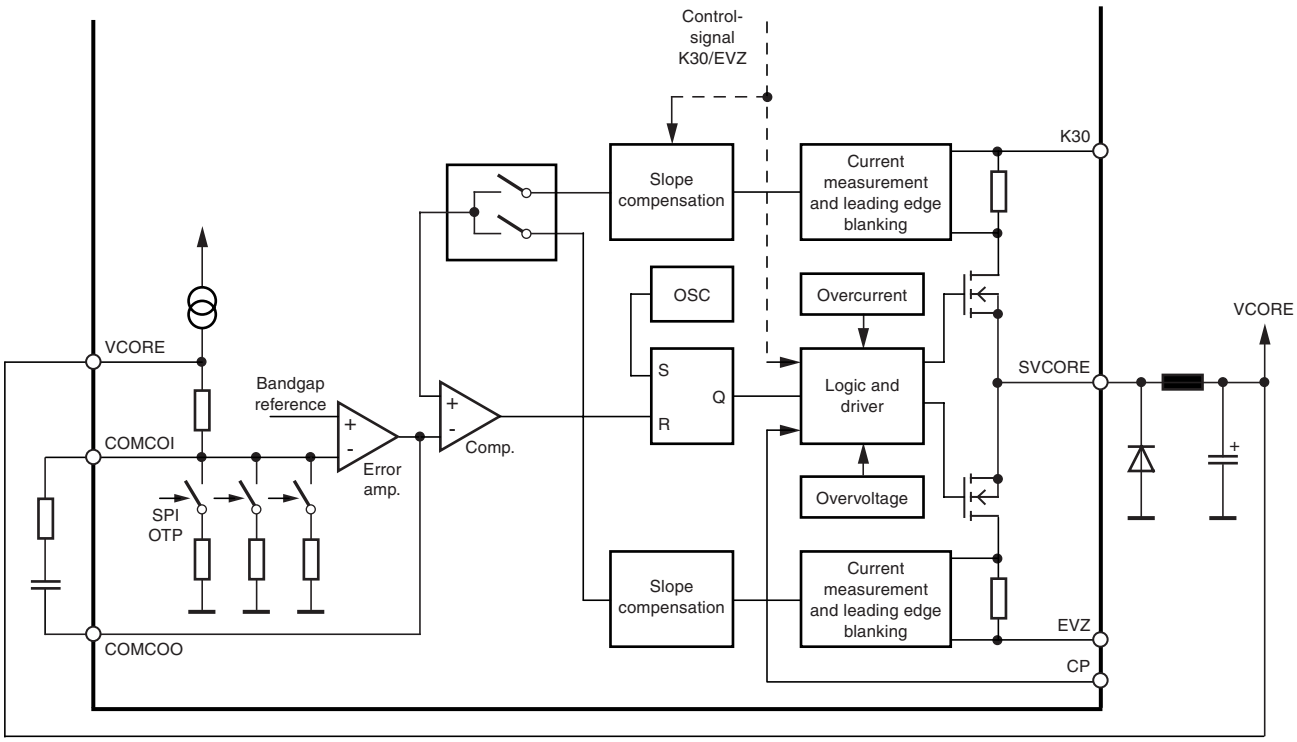
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

12. VCORE Power Supply

The voltage of the VCORE regulator is generated out of the K30 voltage using a step-down regulator as long as the K30 voltage is available. During times when K30 is not present (power-down or stand-alone time), the VCORE regulator is supplied out of VEVZ. Depending on the initial programming, the supply switch signal is derived from the CORESWAP comparator or the EVZEN comparator. The VCORE voltage can be programmed via the serial interface to 3 different voltage values during initial programming. In the case of short spikes, a logic circuit disables multiple-pulse operation during one oscillating period. The regulator uses both current and voltage feedback. In the following cases, the output transistor of the regulator is switched off at once and may be switched on again with the beginning of the next clock period:

1. If the current through the transistor exceeds the output current limit value, the transistor is switched off immediately.
2. If overvoltage is detected at the pin VCORE, the transistor is switched off immediately.
3. If the feedback voltage at the pin VCORE is missing (disconnected pin), the regulator is switched off.

Figure 12-1. Functional Principle of the VCORE Regulator



In order to trim the compensation of the regulation loop and to improve the behavior at load changes, pin COMCOO has to be connected to COMCOI via a compensation network. Because of the fact that current-mode-controlled converters exhibit sub-harmonic oscillations when operating at duty cycles larger than 50%, a slope compensation (which adds an artificial ramp to the comparator) is implemented. If the regulator input voltage at pin EVZ or pin K30 is too low, the regulator switches to a duty cycle of 100% (Permanent-on mode). Backward feeding of EVZ and K30 is avoided. In order to ensure the gate voltage for the output transistors of the regulator, the driver stages are supplied by the charge pump (pin CP).

Necessary for operation:
V_{EVZ} = 5.5V to 40V or V_{K30} = 5.5V to 40V, $V_{CP} > V_{EVZ} + 7V$ or $V_{CP} > V_{K30} + 7V$,
$V_{PERI} > V_{CORE} - 0.3V$, V_{INT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{SAT} is within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 12-1. Electrical Characteristics – VCORE Power Supply

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
11.1	V_{EVZ} voltage for the VCORE regulator to start running	Initial programming: V_{VCORE} = 5V or 2.5V	EVZ	V_{EVZ}	7.5		9	V	A
11.1a	V_{VPERI} voltage for the VCORE regulator to start running	Initial programming: V_{VCORE} = 1.88V	VPERI	V_{VPERI}	1.25		1.7	V	A
11.2	V_{EVZ} voltage for the VCORE regulator to stop running	Initial programming: V_{VCORE} = 5V or 2.5V	EVZ	V_{EVZ}	5.5		6.2	V	A
11.2a	Hysteresis at VPERI for the VCORE regulator to stop running	Initial programming: V_{VCORE} = 1.88V	VPERI	V_{HYS}	50		150	mV	A
11.3	Switch-on time via pin EVZ		SVCORE	t_{SVCORE}	0		20	µs	A
11.4	Switch-off time via pin EVZ		SVCORE	t_{SVCORE}	0		10	µs	A
11.5	Regulator switching frequency	See numbers 8.1 and 8.2 of Table 9-1 on page 27	SVCORE	f_{SVCORE}					A
11.6	Output current limit		SVCORE	I_{SVCORE}	0.7		0.9	A	A
11.7	R_{Dson} of output transistor		SVCORE	R_{SVCORE}			1.2	Ω	A
11.8	Output voltage #1	V_{VCORE1} programmed, band-gap tolerance included	VCORE	V_{VCORE1}	–4%	5.0	+4%	V	A
11.9	Output voltage #2	V_{VCORE2} programmed, band-gap tolerance included	VCORE	V_{VCORE2}	–4%	2.5	+4%	V	A
11.10	Output voltage #3	V_{VCORE3} programmed, band-gap tolerance included	VCORE	V_{VCORE3}	–4%	1.88	+4%	V	A
11.11	Output transistor switch-on time	Time between reaching $0.1 \times (V_{K30max} - V_{VCOREmin})$ and $0.9 \times (V_{K30max} - V_{VCOREmin})$ or $0.1 \times (V_{EVZmax} - V_{VCOREmin})$ and $0.9 \times (V_{EVZmax} - V_{VCOREmin})$	SVORE	$t_{SVCOREon}$			150	ns	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Depending on implementation of slope compensation, sub-harmonics have to be prevented.
2. The value of the minimum load current must be higher than the internal pull-up current at pin VCORE to ensure proper function of the regulator.

Table 12-1. Electrical Characteristics (Continued)– VCORE Power Supply

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
11.12	Output transistor switch-off time	Time between reaching $0.1 \times (V_{K30max} - V_{VCOREmin})$ and $0.9 \times (V_{K30max} - V_{VCOREmin})$ or $0.1 \times (V_{EVZmax} - V_{VCOREmin})$ and $0.9 \times (V_{EVZmax} - V_{VCOREmin})$	SVCORE	$t_{SVCOREoff}$			150	ns	A
11.13	Overvoltage at pin VCORE for switching off the regulator and setting pin RESQ to low (VCORE is set to 5V)	See numbers 14.6 and 14.6a of Table 15-2 on page 45							
11.13a	Overvoltage at pin VCORE for switching off the regulator and setting pin RESQ to low (VCORE is set to 2.5V)	See numbers 14.7 and 14.7a of Table 15-2 on page 45							
11.13b	Overvoltage at pin VCORE for switching off the regulator and setting pin RESQ to low (VCORE is set to 1.8V)	See numbers 14.8 and 14.8a of Table 15-2 on page 45							
11.14	Overvoltage switch-off time	Time between reaching overvoltage and reaching 90% of V_{SCORE} maximum under on condition	SVORE	$t_{SVCOREoff}$	0		0.4	µs	A
11.15	Overcurrent switch-off time	Time between reaching overcurrent and reaching 90% of V_{SCORE} maximum under on condition	SVCORE	$t_{SVCOREoff}$	0		0.5	µs	A
11.16	Leakage current at pin SVCORE	Output transistor off	SVCORE	I_{SVCORE}	–10		10	µA	A
Error Amplifier									
11.17	Maximum output current at pin COMCOO sinking to low		COMCOO	I_{COMCOO}	200		3000	µA	A
11.18	Maximum output current at pin COMCOO sourcing to high		COMCOO	I_{COMCOO}	–165		–85	µA	A
11.19	Input impedance at pin COMCOI	V_{CORE} = 1.88V V_{CORE} = 2.5V/5V	COMCOI	R_{COMCOI}	7.5 13		18 27	kΩ kΩ	A
11.20	Input offset voltage				–10		10	mV	D
11.21	DC open loop gain				70			dB	D
11.22	Unity-gain bandwidth				2			MHz	D
11.23	Output voltage low at pin COMCOO	I_{COMCOO} = 165 µA	COMSATO	$V_{COMSATO}$	0		0.3	V	A
11.24	Output voltage high at pin COMCOO	I_{COMCOO} = –85 µA	COMSATO	$V_{COMSATO}$	VINT – 0.6		VINT	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Depending on implementation of slope compensation, sub-harmonics have to be prevented.
2. The value of the minimum load current must be higher than the internal pull-up current at pin VCORE to ensure proper function of the regulator.

Table 12-1. Electrical Characteristics (Continued)– VCORE Power Supply

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
11.25	Leading-edge blanking time			t_{blank}	150		200	ns	D
11.26	Slope of artificial ramp for slope compensation			dV/dt	80(1)		150(1)	mV/µs	D
11.27	Voltage level at K30 to switch VCORE supply from EVZ to K30 (V_{VCORE} = 1.8V or 2.5V programmed)	V_{K30} increasing See number 7.3 of Table 8-2 on page 23							A
11.28	Hysteresis at K30 to switch VCORE supply from K30 to EVZ (V_{VCORE} = 1.8V or 2.5V programmed)	V_{K30} decreasing See number 7.4 of Table 8-2 on page 23							A
11.29	Voltage level at K30 to switch VCORE supply from EVZ to K30 (V_{VCORE} = 5V programmed)	V_{K30} increasing	K30	V_{K30}	6.1		8.1	V	A
11.30	Hysteresis at K30 to switch VCORE supply from K30 to EVZ (V_{VCORE} = 5V programmed)	V_{K30} decreasing	K30	V_{K30}	0.5		1	V	A
11.31	Time to switch VCORE supply from EVZ to K30 or K30 to EVZ		SVCORE	t_{switch}	0		7.6	µs	D
11.32	VCORE loss-detection threshold(2)		VCORE	I_{Load}	0		1	mA	D

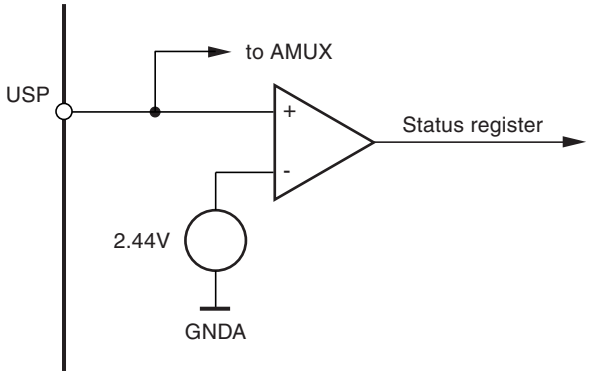
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Depending on implementation of slope compensation, sub-harmonics have to be prevented.
2. The value of the minimum load current must be higher than the internal pull-up current at pin VCORE to ensure proper function of the regulator.

13. USP Comparator for General Purpose

The USP comparator is used for general purposes, for example, low battery detection. An external resistive voltage divider provides the input signal for pin USP. A missing USP connection or V_{USP} < 2.44V sets the status register bit b7 to low. During normal operation (V_{USP} > 2.44V) the status register bit b7 stays high.

Figure 13-1. Functional Principle of the USP Comparator



Necessary for operation:
V_{EVZ} = 5.5V to 40V, V_{PERI} > reset threshold, V_{CORE} > reset threshold, V_{INT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{SAT} and V_{K30} are within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 13-1. Electrical Characteristics – USP Comparator for General Purpose

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
12.1	Input current at pin USP	V_{USP} = 2.44V	USP	I_{USP}	–2.5		+2.5	µA	A
12.2	Input current at pin USP	V_{USP} = 0 to 40V	USP	I_{USP}	–2.5		+2.5	µA	A
12.3	Threshold voltage at pin USP	Trigger voltage for status register bit 7= high with increasing V_{USP}	USP	V_{USP}	2.44 ±5%			V	A
12.4	De-glitching time			$t_{deglitch}$	20		60	µs	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

14. Reference Voltage and Reference Current Generation

The pin IREF is an output derived directly from the chip's internal reference voltage. This reference source is a band gap. All internally used precise voltages are derived from this band-gap voltage. At pin IREF a reference resistor of 12.4 kΩ has to be applied, providing a reference current. All internally used precise currents are derived from this current. In case of a missing resistor at IREF, the regulators will stop. The power-sequencing block still operates as specified.

A defect of the band-gap reference source can be detected by a microcontroller by comparing the voltage at IREF with the voltage at pin VINT (Internal 5V supply), because V_{VINT} is derived from a different band gap.

Table 14-1. Truth Table for VINT

State	K30GOOD (V_{K30} > 4.2V to 5V)	K15GOOD (V_{K15} > 3V to 4V)	V_{EVZ}	V_{VINT}
1	Low	Low	0	OFF
2	High	Low	0	OFF
3	Low	High	0	OFF
4	High	High	$V_{EVZ} < V_{K30}$	ON (Supply: K30)
5	Low	Low	$V_{EVZ} > 5.5V$	ON (Supply: EVZ) – only valid if VINT was already enabled via state #4
6	High	Low	$V_{EVZ} > 5.5V$	ON (Supply: EVZ) – only valid if VINT was already enabled via state #4
7	Low	High	$V_{EVZ} > 5.5V$	ON (Supply: EVZ) – only valid if VINT was already enabled via state #4
8	High	High	$V_{EVZ} > V_{K30}$	ON (Supply: K30)

Necessary for operation:
V_{EVZ} = 5.5V to 40V or V_{K30} = 3.85V to 40V

Operating conditions of all other supply pins:
V_{SAT}, V_{PERI} and V_{CORE} are within functional range limits, T_j = –40°C to +150°C

Other pins:
As defined in Section 4. "Functional Range" on page 8.

Table 14-2. Electrical Characteristics – Reference Voltage and Reference Current Generation

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
13.1	Reference voltage V_{IREF}		IREF	V_{IREF}	1.24 ± 4%			V	A
13.2	Reference current IREF		IREF	I_{IREF}	100 ± 4%			µA	A
13.3a	Voltage at VINT	$V_{K30} > V_{EVZ}$ V_{K30} = VK30GOOD to 5V	VINT	V_{VINT}	3.35		5.47	V	A
13.3b	Voltage at VINT	$V_{K30} > V_{EVZ}$, V_{K30} = 5V to 6V	VINT	V_{VINT}	3.7		5.47	V	A
13.3c	Voltage at VINT	$V_{K30} > V_{EVZ}$, V_{K30} = 6V	IREF	V_{IREF}	4.2		5.47	V	A
13.3d	Voltage at VINT	$V_{EVZ} > V_{K30}$ V_{K30} = 0V, V_{EVZ} > 6V	IREF	V_{IREF}	4.2		5.47	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Reset Function (Pin RESQ and Pin RESQ2)

Pins RESQ and RESQ2 are low-active digital outputs of the ATA6264, which provide a digital “low” signal in the case of a missing or incorrect watchdog transmission or in the case of improper VEVZ, VPERI or VCORE voltage.

The voltage at pin RESQ depends on the proper voltages at pins EVZ, VCORE, and VPERI. The RESQ signal will be set to high after a 16-ms delay as soon as the VCORE reset threshold and the VPERI reset threshold and the EVZ reset threshold (signal EVZGOOD = high) have been reached. If the watchdog circuitry does not detect a valid watchdog trigger, the RESQ signal is set to low again. If the watchdog was triggered successfully, RESQ stays high and RESQ2 is also set to high.

In the case that an overvoltage at VCORE or VPERI is detected, the voltages at pins RESQ and RESQ2 are set to low.

Figure 15-1. Functional Principle of RESQ, RESQ2

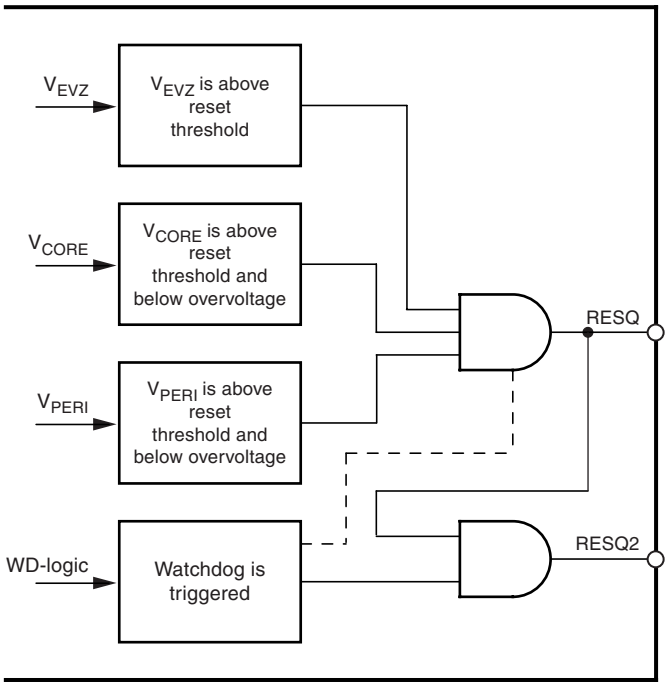
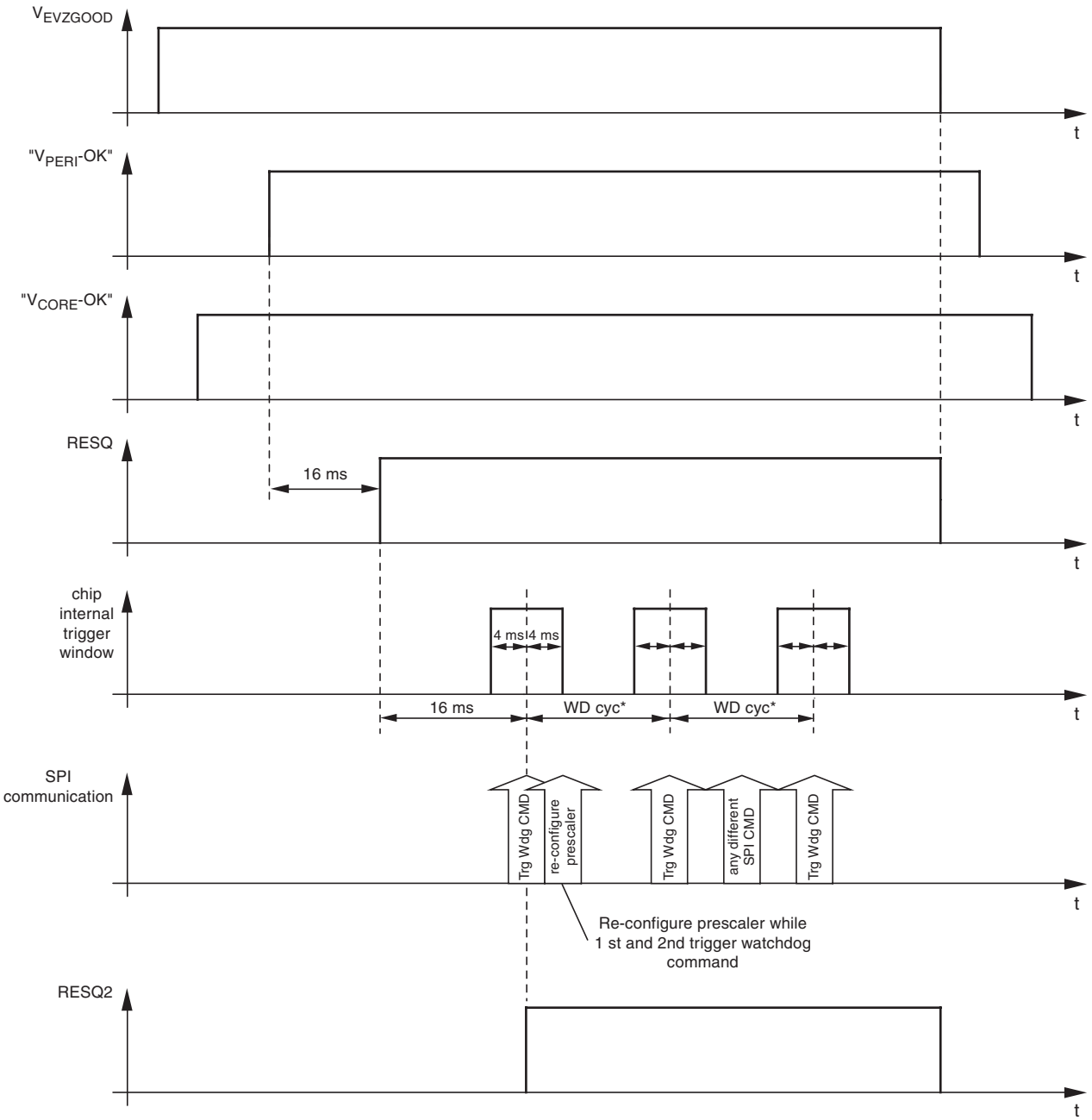


Figure 15-2. Functional Principle of RESQ, RESQ2

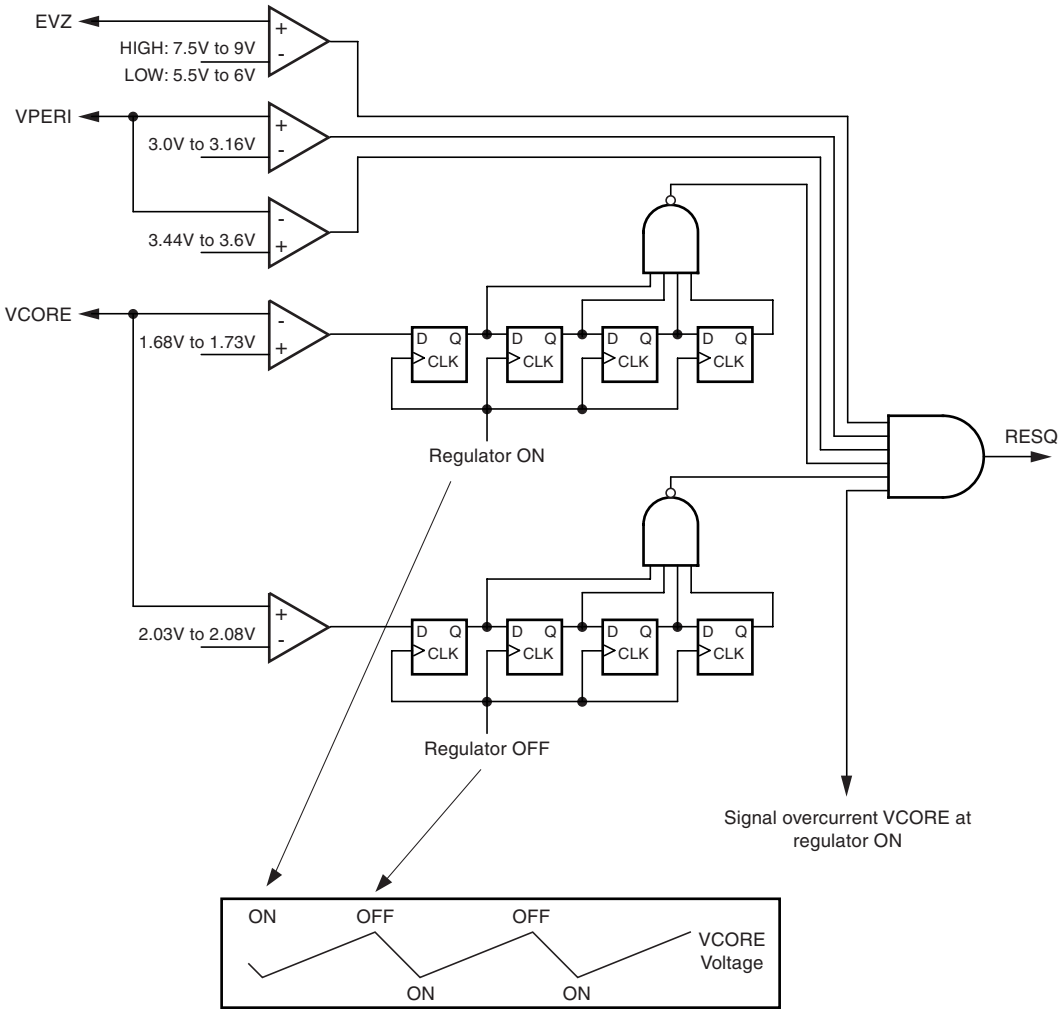


* Watchdog cycle, see pages 48 and 49

The RESQ2 signal results from a logical AND of the Reset signal and an OK signal from the watchdog circuitry, so RESQ2 will go high after the watchdog triggers correctly.

RESQ and RESQ2 have to be set to low if V_{VPERI} or V_{EVZ} are below the specified threshold. VCORE is designed as an essential supply for a microcontroller core, and therefore special *supervisor circuits* for this regulator will affect the signals at pin RESQ and RESQ2 such that both outputs are set to low if the voltage at pin VCORE spends more than 4 regulator cycles in an overvoltage or undervoltage condition at their corresponding switching marks. In addition, a detected overcurrent signal during switch-on gives information about regulator problems, and results in a low-level signal for RESQ/RESQ2.

Figure 15-3. Functional Principle of the Supervisor Circuit for VCORE Monitoring (Values are Valid for V_{VCORE} = 1.88V and V_{VPERI} = 3.3V)



If the watchdog is triggered incorrectly, RESQ and RESQ2 are set to low as well. Voltage spikes on EVZ smaller than or equal to 10 µs to 20 µs do not influence the RESQ or RESQ2 pins.

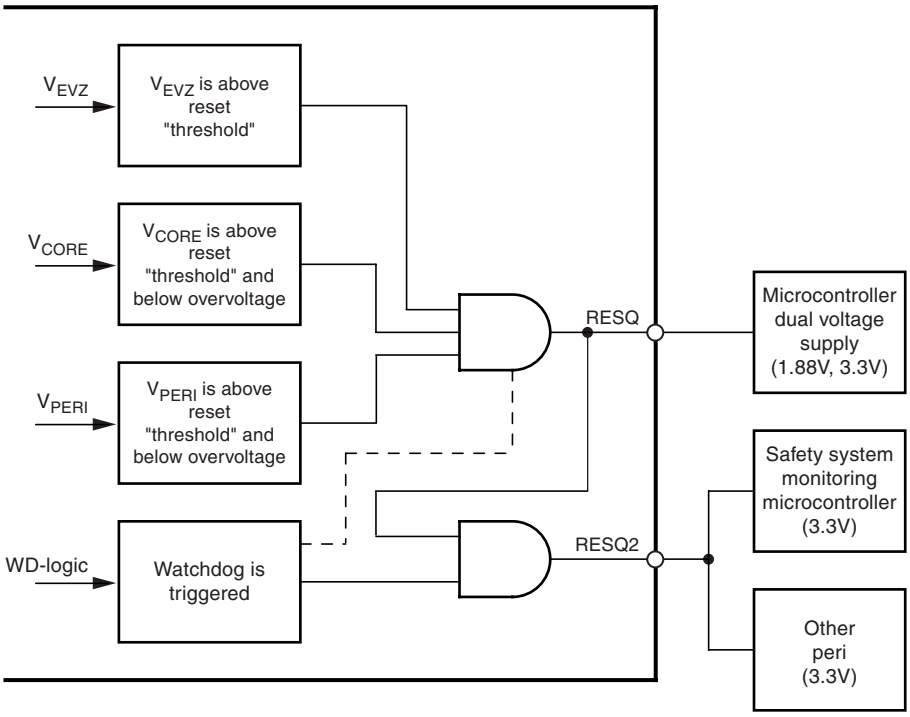
If the ATA6264 internal supply voltage (VINT) is below its proper value, RESQ and RESQ2 are also set to low.

For all voltages at VPERI below the reset threshold, pins RESQ and RESQ2 are switched to low. Both pins deliver a valid low until VPERI goes lower than 1V.

Table 15-1. Reset Truth Table

VPERI	VCORE	VEVZ	WATCHDOG	RESQ	RESQ2
< 1V	X	X	X	Undefined (low via resistor)	Undefined (low via resistor)
1V to V_{VPERI} = OK	X	X	X	Low	Low
> V_{VPERI} = OK	V_{VCORE} = Not OK	X	X	Low	Low
	V_{VCORE} = OK	EVZGOOD = high (V_{EVZ} = OK)	After startup (no trigger has occurred)	High	Low
			Correctly triggered (trigger occurred 1st time)	High	Low -> high
			Correctly triggered	High	High
			Incorrectly triggered	High -> low	High -> low
	X	EVZGOOD = low (V_{EVZ} = Not OK)	X	Low	Low

Figure 15-4. Application Example



Necessary for operation:
V_{EVZ} = 5.5V to 40V, V_{PERI} = 1V to 5.5V, V_{INT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{K30}, V_{SAT}, and V_{CORE} are within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. "Functional Range" on page 8.

Table 15-2. Electrical Characteristics – Reset Function (Pin RESQ and Pin RESQ2)

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
14.1	RESQ and RESQ2 high level	I_{RESQ}, I_{RESQ2} = –200 µA to 0 µA	RESQ RESQ2	V_{RESQ} V_{RESQ2}	V_{VPERI} – 0.8		V_{VPERI}	V	A
14.2	RESQ and RESQ2 low level	I_{RESQ}, I_{RESQ2} = 0 mA to 2 mA	RESQ RESQ2	V_{RESQ} V_{RESQ2}	0		0.4	V	A
14.3	Reset threshold at pin VCORE	V_{VCORE} is set to 5V	VCORE	V_{VCORE}	4.5		5.03	V	A
14.3a	Voltage difference V_{VCORE} – reset threshold at VCORE (see number 14.3)	V_{VCORE} is set to 5V	VCORE	dV_{VCORE}	0.17		0.7	V	A
14.4	Reset threshold at pin VCORE	V_{VCORE} is set to 2.5V	VCORE	V_{VCORE}	2.25		2.5	V	A
14.4a	Voltage difference V_{VCORE} – reset threshold at VCORE (see number 14.4)	V_{VCORE} is set to 2.5V	VCORE	dV_{VCORE}	0.1		0.35	V	A
14.5	Reset threshold at pin VCORE	V_{VCORE} is set to 1.88V	VCORE	V_{VCORE}	1.68		1.8852	V	A
14.5a	Voltage difference V_{VCORE} – reset threshold at VCORE (see number 14.5)	V_{VCORE} is set to 1.88V	VCORE	dV_{VCORE}	0.07		0.275	V	A
14.6	Overvoltage at pin V_{CORE} to switch off the regulator and set RESQ to low	V_{VCORE} is set to 5V	VCORE	V_{VCORE}	4.97		5.5	V	A
14.6a	Voltage difference reset threshold at VCORE (see number 14.6) – V_{VCORE}	V_{VCORE} is set to 5V	VCORE	dV_{VCORE}	0.17		0.7	V	A
14.7	Overvoltage at pin V_{CORE} to switch off the regulator and set RESQ to low	V_{VCORE} is set to 2.5V	VCORE	V_{VCORE}	2.5		2.8	V	A
14.7a	Voltage difference reset threshold at VCORE (see number 14.7) – V_{VCORE}	V_{VCORE} is set to 2.5V	VCORE	dV_{VCORE}	0.1		0.35	V	A
14.8	Overvoltage at pin VCORE to switch off the regulator and set RESQ to low	V_{VCORE} is set to 1.88V	VCORE	V_{VCORE}	1.8748		2.11	V	A
14.8a	Voltage difference reset threshold at VCORE (see number 14.8) – V_{VCORE}	V_{VCORE} is set to 1.88V	VCORE	dV_{VCORE}	0.07		0.275	V	A
14.9	Reset threshold at pin VPERI	V_{VPERI} is set to 5V	VPERI	V_{VPERI}	4.5		4.82	V	A
14.10	Reset threshold at pin VPERI	V_{VPERI} is set to 3.3V	VPERI	V_{VPERI}	2.94		3.16	V	A
14.11	Overvoltage at pin VPERI to set RESQ to low	V_{VPERI} is set to 5V	VPERI	V_{VPERI}	5.2		5.51	V	A
14.12	Overvoltage at pin VPERI to set RESQ to low	V_{VPERI} is set to 3.3V	VPERI	V_{VPERI}	3.4		3.63	V	A
14.13	Threshold for signal EVZGOOD = OK	V_{EVZ} rising	EVZ	V_{EVZ}	7.5		9	V	A
14.14	Threshold for signal EVZGOOD = Not OK	V_{EVZ} falling	EVZ	V_{EVZ}	5.5		6.2	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 15-2. Electrical Characteristics (Continued)– Reset Function (Pin RESQ and Pin RESQ2)

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
14.15	Delay time for RESQ and RESQ2 to switch to low after reaching the reset threshold of V_{EVZ}		RESQ RESQ2	t_{RESQ} t_{RESQ2}	10		20	µs	A
14.16	Pull-down current at pin RESQ	RESQ is switched to low (V_{RESQ} = 0.4V), $1V \le V_{VPERI} < 5.5V$	RESQ	I_{RESQ}	1		2	mA	A
14.17	Pull-down current at pin RESQ2	RESQ2 is switched to low (V_{RESQ} = 0.4V), $1V \le V_{VPERI} < 5.5V$	RESQ2	I_{RESQ2}	1		2	mA	A
14.18	Pull-down resistor at pin RESQ, RESQ2		RESQ RESQ2	R_{RESQ} R_{RESQ2}	0.5		1.5	MΩ	D
14.19	Output current high side RESQ, RESQ2	RESQ, RESQ2 are switched to high, V_{RESQ}, V_{RESQ2} = 0V	RESQ RESQ2	I_{RESQ} I_{RESQ2}	–550		–250	µA	A
14.20	Output current low side RESQ, RESQ2	RESQ, RESQ2 are switched to high, V_{RESQ}, V_{RESQ2} = V_{VPERI}	RESQ RESQ2	I_{RESQ} I_{RESQ2}	4		10	mA	A
14.21	Rise time RESQ, RESQ2	30-pF external capacitive load	RESQ RESQ2	t_{RESQ} t_{RESQ2}			4.0	µs	A
14.22	Fall time RESQ, RESQ2	30-pF external capacitive load	RESQ RESQ2	t_{RESQ} t_{RESQ2}			0.5	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

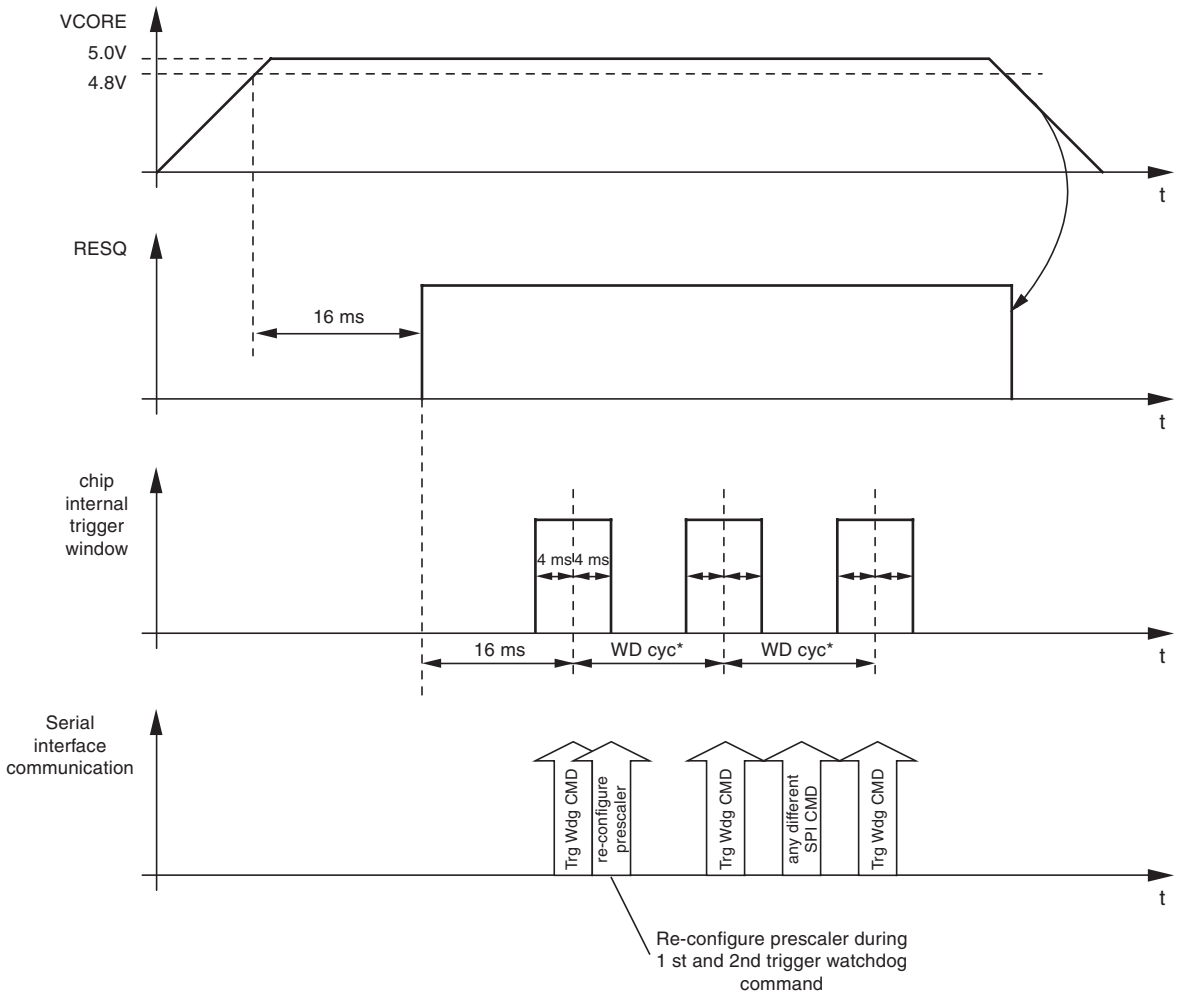
16. Watchdog Function

To verify the proper function of the microcontroller, watchdog logic is included. As the ATA6264 is powered up, the RESQ2 signal stays low until the first valid watchdog trigger is detected.

Features:

- Watchdog trigger has to be done via the serial interface
- In case of a watchdog-trigger mismatch, the ATA6264 is set into its default state (latches, MISO status, etc.) and RESQ is set to low.
- Watchdog has to be triggered cyclically (prescaler for repetition time is set via serial interface command). Default: 16-ms repetition time

Figure 16-1. Watchdog Trigger Functional Principle



* Watchdog cycle, see pages 48 and 49

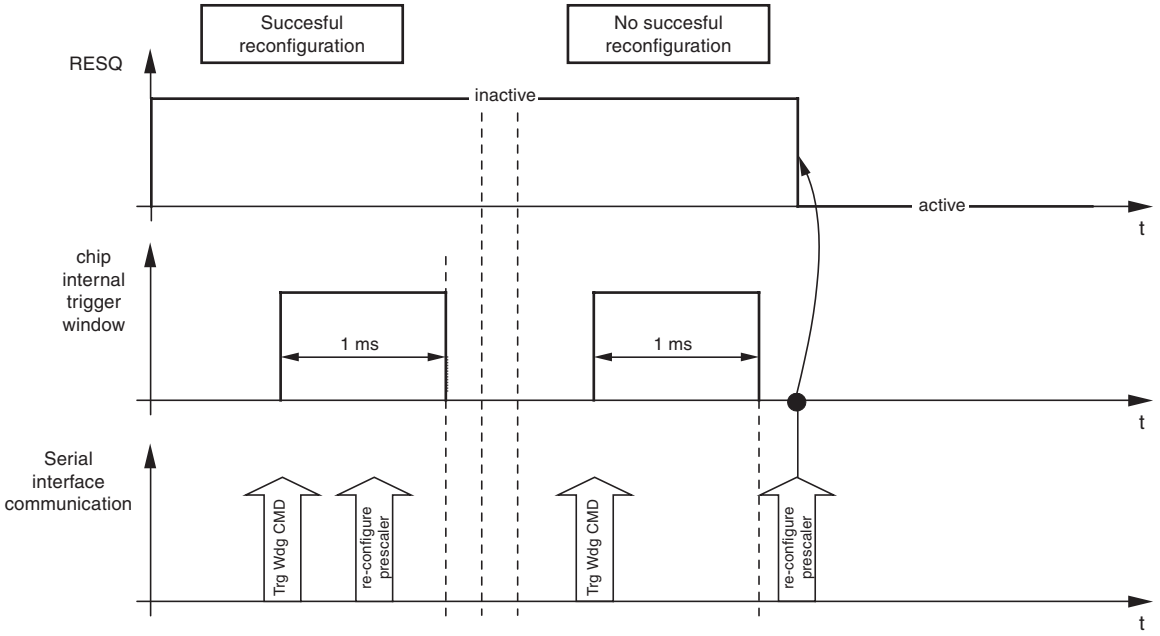
Requirements for successful trigger:

- Minimum one valid different serial interface command between two trigger watchdog commands is necessary. Exception: First trigger watchdog command need not be preceded by a different serial interface command.
- Cyclic repetition for the trigger watchdog command within ±25% tolerance is necessary.

Incorrect trigger causes RESQ active.
The prescaler will be set to its default value with RESQ = low

Initial phase:
Timing for the first trigger watchdog is fixed to 16 ms after RESQ changes from low to high (trigger window ±25% means ±4-ms trigger window for first trigger watchdog command). After the first watchdog trigger, the prescaler can be reconfigured within a specified time window (< 1 ms). Only one configuration command is allowed in this time window. For watchdog trigger handling, the Serial Interface Reconfigure command can be chosen as a different serial interface command. Any further configuration inside or outside this time window will cause an immediate reset via RESQ.

Figure 16-2. Reconfiguration Prescaler Functional Principle



The trigger watchdog cycle can be set to the following retrigger times:

- 4 ms
- 8 ms
- 16 ms (default)
- 32 ms
- 64 ms
- 128 ms

Cyclic phase:
Between two trigger commands a different SPI command must be seen by the SPI decoder

Figure 16-3. Watchdog Trigger Functional Principle (Successful Watchdog Trigger)

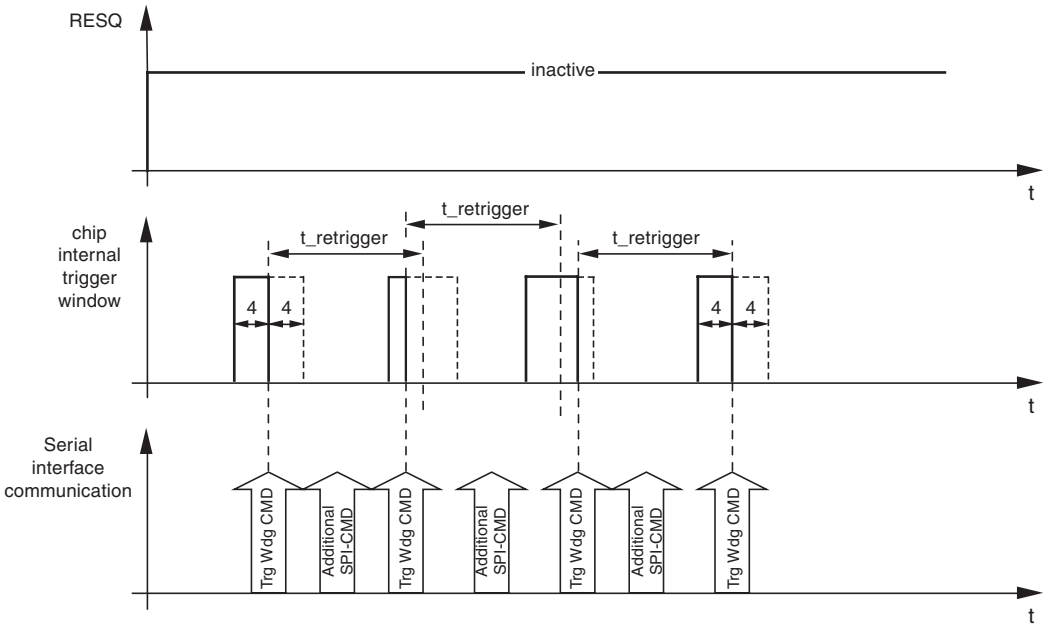
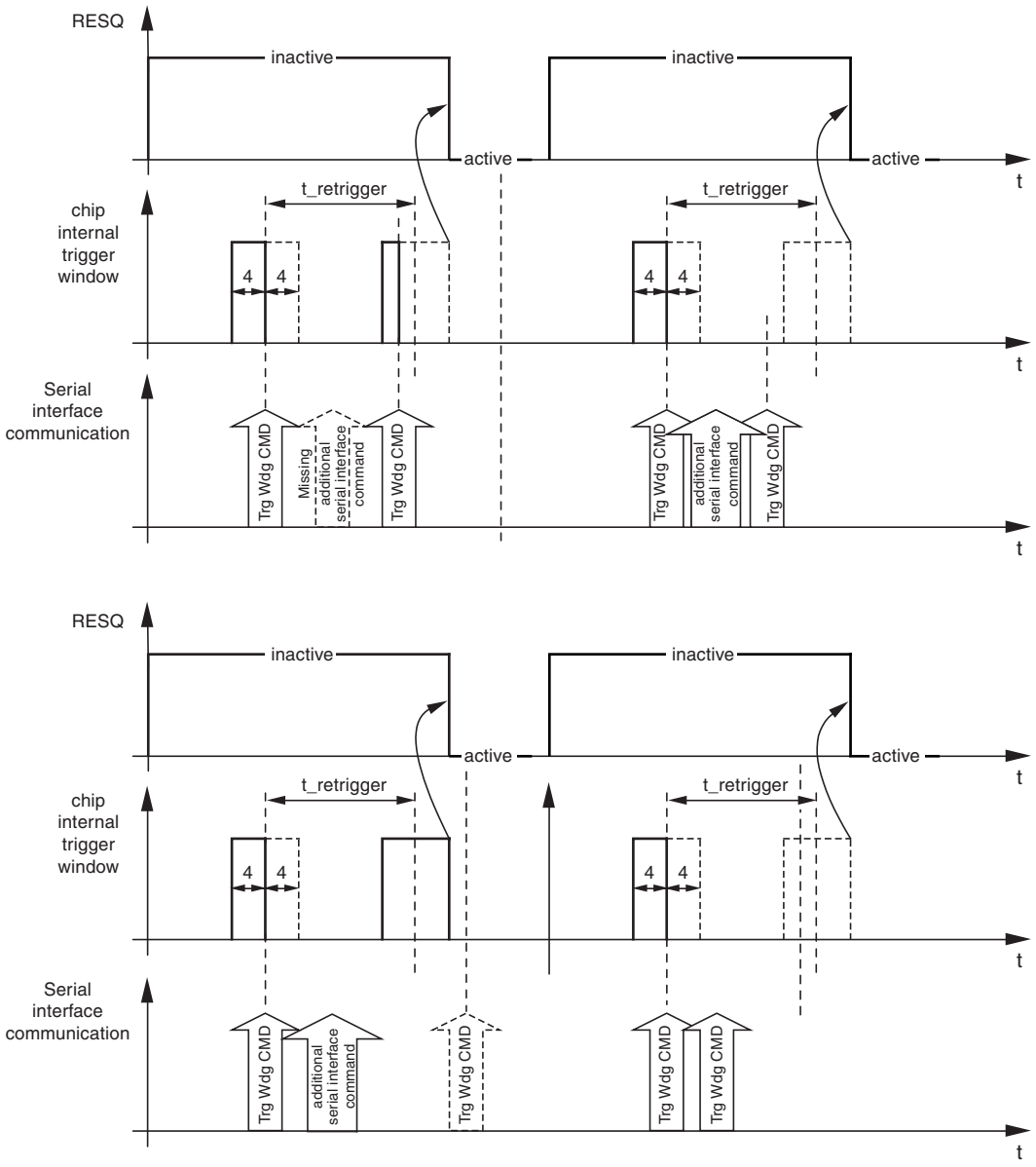


Figure 16-4. Watchdog Trigger Functional Principle (Unsuccessful Watchdog Trigger)



Configuration of watchdog trigger:

For the configuration of the watchdog prescaler, a special serial interface command is necessary.

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Configure prescaler	**0**	**1**	**1**	**0**	0	0	0	0	1	1	1	1	0	a	b	c	60F*x*

Note: a, b, and c to be set as defined in Table 16-1

Table 16-1. Watchdog Prescaler Command

Selection Bits			Retrigger Time (ms)
a	b	c	
0	0	0	Set to default (16 ms)
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	Set to default (16 ms)

The status of the watchdog prescaler is indicated in the status register.

Necessary for operation:
V_{PERI} > Reset threshold, V_{CORE} > Reset threshold

Operating conditions of all other supply pins:
V_{K30}, V_{EVZ} and V_{VSAT} are within functional range limits, T_j = –40°C to 150°C

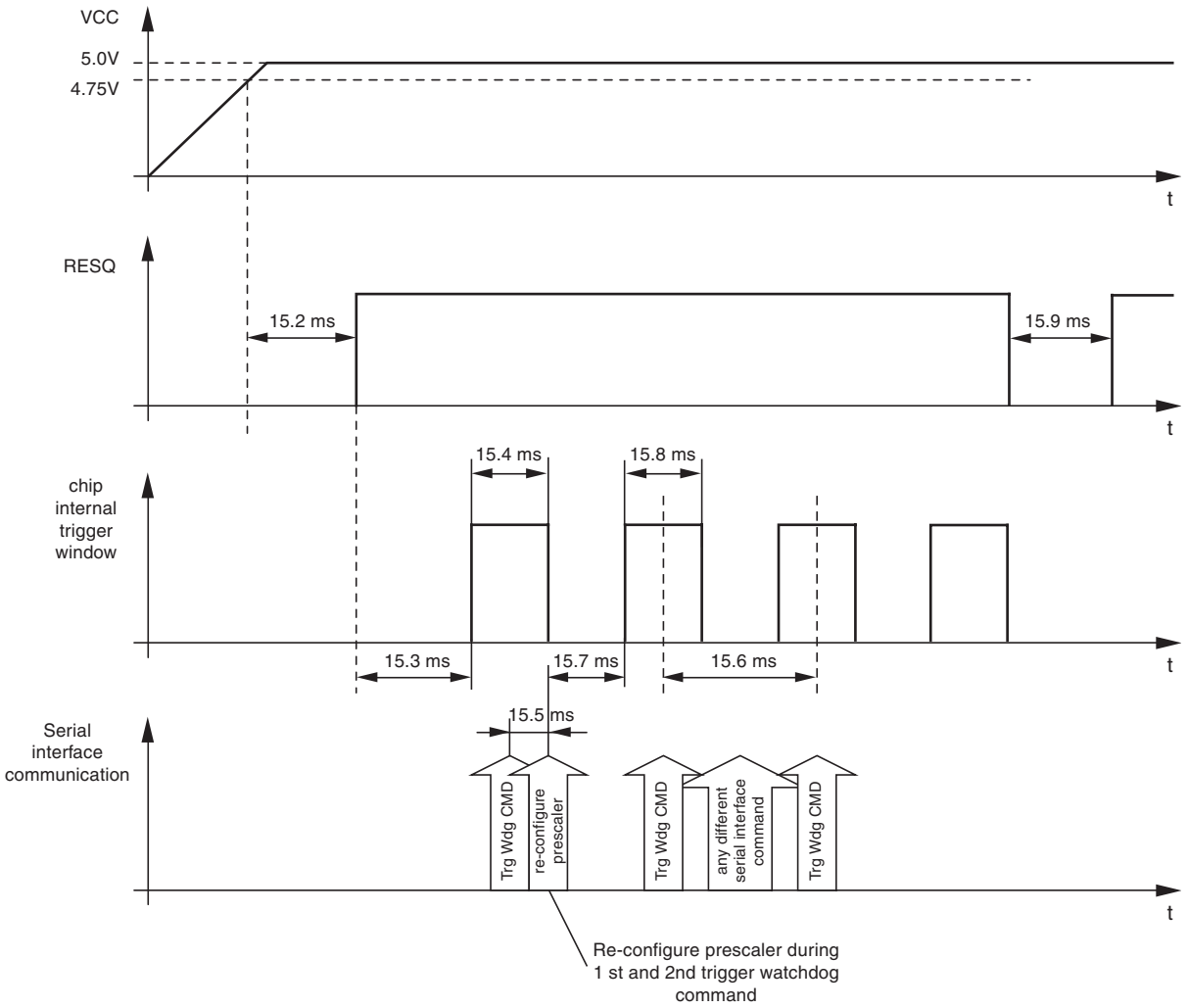
Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 16-2. Electrical Characteristics – Watchdog Function

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
15.1	Oscillator frequency			f_{os}	–5%	100	+5%	kHz	A
15.2	Power-up extension of RESQ signal		RESQ	t_{RESQ}	16		16	$\frac{100}{f_{os}}$	A
15.3	Start of first watchdog trigger window after rising edge at RESQ			t	12		12	$\frac{100}{f_{os}}$	A
15.4	Maximum width of first watchdog-trigger window			t	8		8	$\frac{100}{f_{os}}$	A
15.5	Maximum time for prescaler configuration after first watchdog-trigger command			t	1		1	$\frac{100}{f_{os}}$	A
15.6	Programmed watchdog cycle	t_{WD} as set by prescaler (default 16 ms)			t_{WD}		t_{WD}		A
15.7	Start of programmed watchdog window				75% × t_{WD}		75% × t_{WD}		A
15.8	Max. programmed window duration				50% × t_{WD}		50% × t_{WD}		A
15.9	Time for RESQ = low after watchdog timeout	(Missing watchdog trigger)	RESQ	t	16		16	$\frac{100}{f_{os}}$	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

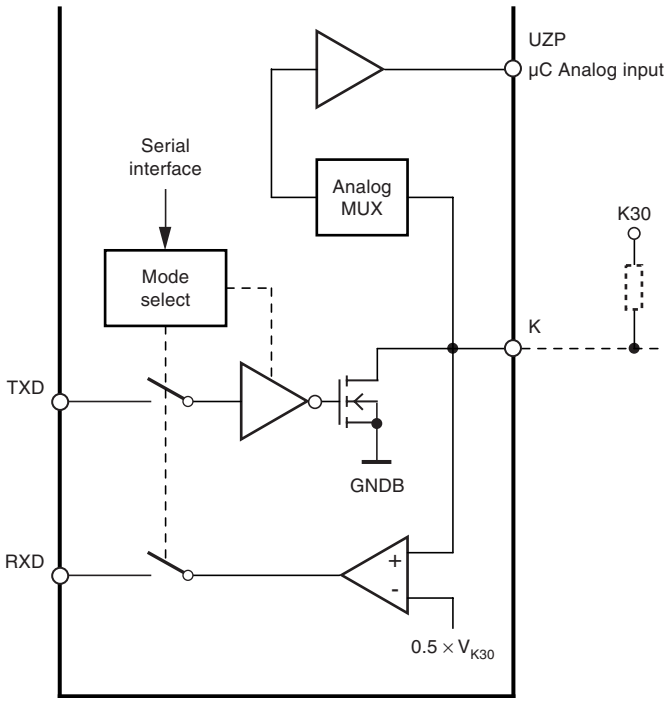
Figure 16-5. Watchdog Trigger



17. LIN/ISO 9141 Interfaces

The ATA6264 includes two complete ISO 9141 interfaces. Interface #1 is controlled via the pins RxD1 and TxD1, interface #2 is controlled via the pins RxD2 and TxD2. In order to support both ISO9141 and LIN bus requirements, interface #1 can be configured during initial programming. In applications where one or both ISO9141 interfaces are not needed, the output transistors of K1 and K2 may be used as simple low-side transistors, switched on or off by the serial interface. In this mode, a diagnosis of the pins K1 and K2 via the analog multiplexer is possible. The K1 and K2 outputs include an internal current limitation and overtemperature protection circuit.

Figure 17-1. Functional Principle of the LIN/ISO 9141 Interfaces



Necessary for operation:
V_{EVZ} = 9V to 40V, V_{K30} = 5.5V to 40V, V_{VPERI} > Reset threshold, V_{VCORE} > Reset threshold, V_{VINT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{VSAT} is within functional range limits, T_j = –40°C to +150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 17-1. Electrical Characteristics – LIN/ISO 9141 Interfaces

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
General (Valid for All Modes)									
16.1	Pull-up current to VPERI at pin TxD_x	(x = 1, 2)	TxD_x	I_{TxDx}	–35	–50	–65	µA	A
16.2	K_x input receiver low	(x = 1, 2)	K_x	V_{Kx}	0		$0.4 \times V_{K30}$	V	A
16.3	K_x input receiver high	(x = 1, 2)	K_x	V_{Kx}	$0.6 \times V_{K30}$		V_{K30}	V	A
16.4	K_x input receiver threshold	(x = 1, 2)	K_x	V_{Kx}		V_{K30} / 2		V	A
16.5	K_x input receiver hysteresis	(x = 1, 2)	K_x	V_{Kx}	$0.07 \times V_{K30}$		$0.2 \times V_{K30}$	V	A
16.6	K_x output sink current	(x = 1, 2), K output voltage 1.5V	K_x	I_{Kx}	35			mA	A
16.7	K_x output voltage drop	(x = 1, 2), I_{Kx} = 0 mA to 40 mA	K_x	V_{Kx}			1.7	V	A
16.8	K_x output capacitance	(x = 1, 2), capacitance between Kx and GNDB	K_x	C_{Kx}			10	pF	D
16.9	K_x output current limitation	(x = 1, 2)	K_x	I_{Kx}	50		100	mA	A
16.10	K_x leakage current	(x = 1, 2), output driver deactivated	K_x	I_{Kx}	–10		+10	µA	A
16.11	RxD_x voltage drop high side	(x = 1, 2), with I_{RxDx} = 0 µA to –500 µA	RxD_x	V_{RxDx}	V_{VPERI} – 0.8		V_{VPERI}	V	A
16.12	RxD_x voltage drop low side	(x = 1, 2), I_{RxDx} = 0 mA to 1mA	RxD_x	V_{RxDx}	0		0.4	V	A
16.13	RxD_x high-side output current	(x = 1, 2), V_{RxDx} = 0V	RxD_x	I_{RxDx}	–1.1		–0.2	mA	A
16.14	RxD_x low-side output current	(x = 1, 2), $V_{RxDx} = V_{VPERI}$	RxD_x	I_{RxDx}	1		4	mA	A
16.15	RxD_x output rise time	(x = 1, 2), 30-pF external load	RxD_x	t_{RxDx}			1	µs	A
16.16	RxD_x output fall time	(x = 1, 2), 30-pF external load	RxD_x	t_{RxDx}			1	µs	A
16.17	TxD_x input-voltage high-level threshold	(V_{PERI} = 5V), (x = 1, 2)	TxD_x	V_{TxDx}	$0.5 \times V_{VPERI}$		V_{VPERI} + 0.3V	V	A
16.18	TxD_x input-voltage high-level threshold	(V_{PERI} = 3.3V), (x = 1, 2)	TxD_x	V_{TxDx}	$0.6 \times V_{PERI}$		V_{PERI} + 0.3V	V	A
16.19	TxD_x input-voltage low level	(V_{PERI} = 3.3V), (x = 1, 2)	TxD_x	V_{TxDx}			$0.2 \times V_{VPERI}$	V	A
16.20	TxD_x input-voltage hysteresis	(x = 1, 2)	TxD_x	V_{TxDx}	100		550	mV	A
16.21	TxD_x input capacitance	(x = 1, 2)	TxD_x	C_{TxDx}			5	pF	D
16.22	K_x thermal shutdown	(x = 1, 2)		T_{JKx}	155		185	°C	B
16.22a	K_x thermal-shutdown hysteresis	(x=1, 2)		DT_{JKx}	5		25	K	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 17-1. Electrical Characteristics (Continued)– LIN/ISO 9141 Interfaces

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
ISO 9141 Mode									
16.23	Maximum baud rate		K_x	f_{Kx}	62.5			kBd	A
16.24	Propagation delay TxD_x = low to K_x = low	(x = 1, 2), measured from TxD_x H to L to $K_x = 0.9 \times V_{K30}$ R_{Kx} = 510Ω to K30, C_{Kx} = 470 pF to GNDB	K_x	t_{PDtL}			1	µs	A
16.25	Propagation delay TxD_x = high to Kx = high	(x = 1, 2), measured from TxD_x L to H to $K_x = 0.1 \times V_{K30}$ R_{Kx} = 510Ω to K30, C_{Kx} = 470 pF to GNDB	K_x	t_{PDtH}			1	µs	A
16.26	K_x rise time	(x = 1, 2), measured from $0.1 \times V_{K30}$ to $0.9 \times V_{K30}$ R_{Kx} = 510Ω to K30, C_{Kx} = 470 pF to GNDB	K_x	t_{Krise}			3	µs	A
16.27	K_x fall time	(x = 1, 2), measured from $0.9 \times V_{K30}$ to $0.1 \times V_{K30}$ R_{Kx} = 510Ω to K30, C_{Kx} = 470 pF to GNDB	K_x	t_{Kfall}			3	µs	A
16.28	Propagation delay K_x = low to RxD_x = low	(x = 1, 2), measured from $K_x = 0.4 \times V_{K30}$ to RxD_x = H to L	K_x	t_{PDkL}			4	µs	A
16.29	Propagation delay K_x = high to RxD_x = high	(x = 1, 2), from $K_x = 0.6 \times V_{K30}$ to xD_x = L to H	K_x	t_{PDkH}			4	µs	A
16.30	Symmetry of transmitter delay	(x = 1, 2), $t_{SYM\_Tx} = (t_{PDtL} + t_{Kfall}) - (t_{PDtH} + t_{Krise})$	K_x	t_{SYM_Tx}	–1		1	µs	A
16.31	Symmetry of receiver propagation delay	(x = 1, 2), $t_{SYM\_Rx} = t_{PDkL} - t_{PDkH}$	K_x	t_{SYM_Rx}	–1		1	µs	A
LIN Bus Mode (Necessary for Operation: V_{K30} = 8V to 18V)									
16.32	Slew rate for rising and falling edge	Measured between high level = $0.8 \times V_{K30}$ and low level = $0.2 \times V_{K30}$, R_{K1} = 1 kΩ to K30, C_{K1} = 3.3 nF to GNDB	K_1	dV_{K1}/dt	1		3	V/µs	A
16.33	Maximum baud rate		K_1	t_{Kx}	20			kBd	A
16.34	Propagation delay TxD_1 low to K_1 = low	Measured from TxD_1 H-> L to $K_1 = 0.9 \times V_{K30}$ R_{K1} = 1 kΩ to K30, C_{K1} = 3.3 nF to GNDB	K_1	t_{PDtL}			2.5	µs	A
16.35	Propagation delay TxD_1 high to K_1 = high	Measured from TxD_1 L to H to $K_1 = 0.1 \times V_{K30}$ R_{K1} = 1 kΩ to K30, C_{K1} = 3.3 nF to GNDB	K_1	t_{PDtH}			2.5	µs	A
16.36	Propagation delay K_1 low to RxD_1 = low	Measured from $K_1 = 0.4 \times V_{K30}$ to RxD_1 = H to L	K_1	t_{PDkL}			4	µs	A

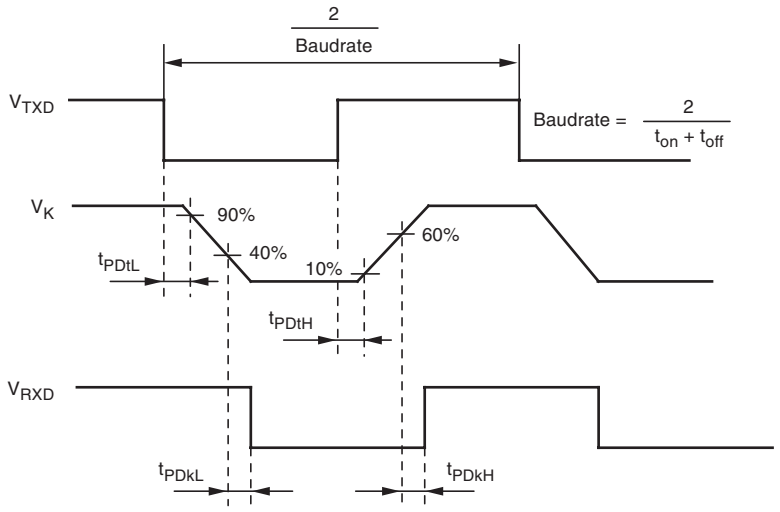
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 17-1. Electrical Characteristics (Continued)– LIN/ISO 9141 Interfaces

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
16.37	Propagation delay K_1 high to RxD_1 = high	Measured from $K_1 = 0.6 \times V_{K30}$ to RxD_1 = L to H	K_1	t_{PDkH}			4	µs	A
16.38	Symmetry of transmitter delay	$t_{SYM\_T1} = t_{PDtL} - t_{PDtH}$	K_1	t_{SYM_T1}	–1		1	µs	A
16.39	Symmetry of receiver propagation delay	$t_{SYM\_R1} = t_{PDkL} - t_{PDkH}$	K_1	t_{SYM_R1}	–1		1	µs	A
LS Driver Mode									
16.40	K_x output voltage drop	I_{Kx} = 40 mA I_{Kx} = 20 mA	K_x	V_{Kx}			1.7 1.2	V	A
16.41	K_x switch-on delay	(x = 1, 2), measured from rising edge of SSQ to V_{Kx} = 16.40V, R_{Kx} = 250Ω to K30, C_{Kx} = 3.3 nF to GNDB	K_x	t_{Kx}			50	µs	A
16.42	K_x switch-off delay	(x = 1, 2), measured from rising edge of SSQ to $V_{Kx} = 0.9 \times V_{K30}$, R_{Kx} = 250Ω to K30, C_{Kx} = 3.3 nF to GNDB	K_x	t_{Kx}			10	µs	A
16.43	K_x leakage current	(x = 1, 2), output driver deactivated, AMUX measurement activated and deactivated K30 = 5.5V to 15V K30 > 15V to 25V K30 > 25V to 40V	K_x	I_{Kx}	 –10 –10 –10		 +100 +160 +260	 µA µA µA	 A A A
16.44	K_x leakage current	(x = 1, 2), output driver deactivated, AMUX measurement deactivated K30 = 5.5V to 40V K_x = –25V	K_x	I_{Kx}	–150		+10	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 17-2. Timing LIN/ISO 9141 Interface



18. Voltage/Current Sources ($IASG_x$ Sources)

For a variable resistance measurement and especially for buckle-switch detection, five constant voltage sources, switchable between two different voltages (V1 and V2) are implemented. The current delivered by these voltage sources is mirrored by a factor of 1 / 10 or 1 / 15 to the pin ISENS and causes a voltage drop at the external resistor connected to this pin. This voltage drop can be measured at pin UZP by choosing the corresponding AMUX command. The external resistor at pin $IASG_x$ can be calculated using the following formulas:

$$R_{IASGx} = \frac{R_{ISENS}}{10} \times \frac{V_{V1} - V_{V2}}{V_{ISENS1} - V_{ISENS2}} \text{ or}$$

$$R_{IASGx} = \frac{R_{ISENS}}{15} \times \frac{V_{V1} - V_{V2}}{V_{ISENS1} - V_{ISENS2}}$$

The current through pin $IASG_x$ is internally limited to a value between I_{IASGx} = –150 mA and –50 mA. If the voltage at pin ISENS becomes higher than V_{VPERI}, the voltage at pin IASG and, consequently, the current at pin $IASG_x$ is reduced until $V_{ISENS} = V_{VPERI}$. This function can be used to reduce the current limitation of pin $IASG_x$ to values lower than the internal limit by choosing an adequate external resistor at pin ISENS. In this case, the maximum current through pin $IASG_x$ can be calculated as:

$$I_{IASGxlim} = 10 \times \frac{V_{VPERI}}{R_{ISENS}} \text{ or}$$

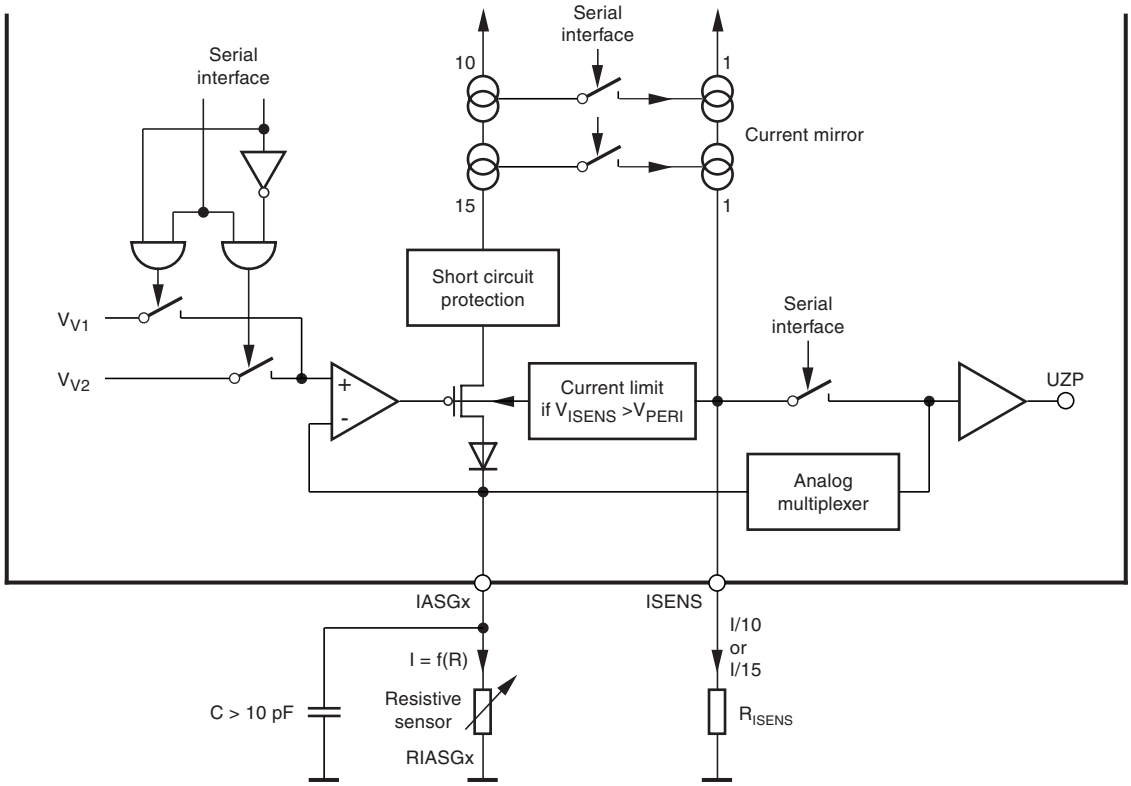
$$I_{IASGxlim} = 15 \times \frac{V_{VPERI}}{R_{ISENS}}$$

For high accuracy, the IASGx current needs to be between 0.5 mA and 40 mA, and the maximum ISENS voltage must be < V_{PERI} – 40%. Under a clamping condition, the voltage at pin ISENS is clamped to V_{PERI} + 5%. Calculation of the resistor at pin ISENS:

$$RSENS = 0.96 \times V_{PERI} \times \frac{CR1}{I_{ASGmax}}$$

In applications with one or more unused IASG channels, the IASG pins can be used as measurement inputs. The five IASG pins are connected to the analog multiplexer block via different dividers. Voltages applied to these IASG pins can be measured at the UZP pin, selected via SPI commands.

Figure 18-1. Functional Principle of the IASG Interface



Necessary for operation:

V_{VCORE} and V_{VPERI} > Reset threshold, V_{EVZ} = 9V to 40V for operation with IASGx switched to 5V

V_{VCORE} and V_{VPERI} > Reset threshold, V_{EVZ} = 15V to 40V for operation with IASGx switched to 10V

V_{INT} = 3.7V to 5.47V, $V_{CP} > V_{EVZ} + 7V$

Operating conditions of all other supply pins:

V_{K30} and V_{VSAT} are within functional range limits, T_j = –40°C to 150°C

Other pins:

As defined in Section 4. "Functional Range" on page 8, $C_{IASGx} \geq 10$ nF and $825\Omega \geq R_{ISENS} \geq 5\ k\Omega$

Table 18-1. Electrical Characteristics – Voltage/Current Sources ($IASG_x$ Sources)

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
17.1	Output voltage (V1)	(x = 1 to 5), –40 mA < I_{IASGx} < –0.5 mA $V_{ISENS} = 0.96 \times V_{VPERI}$	$IASG_x$	$V1_{IASGx}$	–6%	10	+6%	V	A
17.2	Output voltage (V2)	(x = 1 to 5), –40 mA < I_{IASGx} < –0.5 mA $V_{ISENS} = 0.96 \times V_{VPERI}$ $IASG_x$ switched to 5V V_{EVZ} > 11V	$IASG_x$	$V2_{IASGx}$	–6%	5	+6%	V	A
17.2a	Output voltage (V2)	(x = 1 to 5), –25 mA < I_{IASGx} < –0.5 mA $V_{ISENS} = 0.96 \times V_{VPERI}$ $IASG_x$ switched to 5V V_{EVZ} > 9V to 11V	$IASG_x$	$V2_{IASGx}$	–6%	5	+6%	V	A
17.3	Output voltage overshoot at IASGx due to regulator characteristic	(x = 1 to 5) when IASG = 5V when IASG = 10V	$IASG_x$	ΔV_{IASGx}			5.9 11.3	V V	A A
17.4	Maximum duration of voltage overshoot at IASGx	(x = 1 to 5), with V_{IASGx} = 10V / 0.5 mA < R_{LOAD} < V_{IASGx} = 5V / 40 mA	$IASG_x$	t_{IASGx}			30	µs	A
17.5	Linear range for current mirror at IASGx	(x = 1 to 5), 0V = $V_{ISENS} = 0.96 \times V_{PERI}$	$IASG_x$	I_{IASGx}	–40		–0.5	mA	A
17.6	Internal current limitation at $IASG_x$	(x = 1 to 5)	$IASG_x$	I_{IASGx}	–150		–50	mA	A
17.7	Current ratio #1	(x = 1 to 5), $CR_{1x} = I_{IASGx} / I_{ISENS}$ 0V = $V_{ISENS} = 0.96 \times V_{VPERI}$ –40 mA < I_{IASGx}< –0.5mA	$IASG_x$	CR_{1x}	–3%	9.9	+3%		A
17.8	Current ratio #2	(x = 1 to 5), $CR_{2x} = I_{IASGx} / I_{ISENS}$ 0V = $V_{ISENS} = 0.96 \times V_{VPERI}$ –40 mA < I_{IASGx} < –0.5 mA	$IASG_x$	CR_{2x}	–3%	14.9	+3%		A
17.9	Settling time	(x = 1 to 5), R_{IASGx} = 250Ω, no capacitive load at IASGx	ISENSE	t_{ISENSE}	0		50	µs	A
17.10	Switch-on delay	(x = 1 to 5) Measured from rising edge of SSQ to $V_{IASGx} = 0.1 \times V_{IASGx}$ R_{IASGx} = 250Ω, no capacitive load at IASGx	$IASG_x$	t_{IASGx}	0		50	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 18-1. Electrical Characteristics (Continued)– Voltage/Current Sources ($IASG_x$ Sources)

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
17.11	Output voltage clamping ($V_{ISENS} \leq V_{VPERI}$)	$I_{IASGx} > CR_Y \times V_{VPERI} / R_{ISENS}$ (x = 1 to 5), (Y = 1, 2) ($V_{ISENS} \leq V_{VPERI}$ regulator active)	ISENSE	V_{ISENSE}	$0.96 \times V_{VPERI}$		$1.05 \times V_{VPERI}$	V	A
17.12	ISENS leakage current	V_{ISENS} = 0V to $0.96 \times V_{VPERI}$	ISENSE	I_{ISENSE}	–1.6		+1.6	µA	A
17.13	IASGx leakage current	(x = 1 to 5) IASGx channel deactivated, $0V < V_{IASGx} < V_{EVZ}$	$IASG_x$	I_{IASGx}	–1.6		+1.6	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

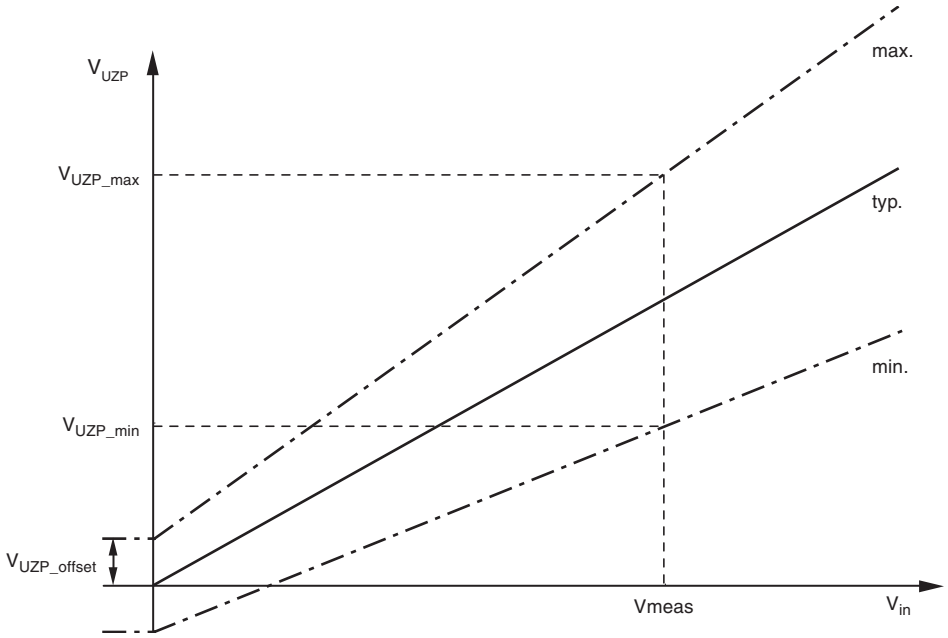
19. AMUX (Analog Multiplexer for Voltage Measurements)

Various voltages and the chip temperature inside of the ATA6264 can be measured at the analog measurement output UZP. Different voltage dividers ensure that the values of the measured voltages at UZP are in the range of 0V to V_{PERI}. To select a specific measurement, a serial interface command has to be sent to the ATA6264.

For the list of measurable voltages and temperatures, refer to Section 22. ”Serial Interface Commands” on page 68. The overall accuracy of the measurement part inside the ATA6264 can be calculated using the following formula:

$$V_{UZP} = \left[\frac{V_{meas}}{ratio \pm ratio\ tolerance}\right] \pm V_{UZPoffset}$$

Figure 19-1. AMUX Tolerances



In order to describe the behavior of the whole measurement properly, the tolerance of the voltage-divider ratio (ratio tolerance) and the offset tolerance of the UZP buffer ($V_{UZPoffset}$) are defined in separate points. The UZP buffer is defined in the following section.

Necessary for operation:
V_{EVZ} = 8V to 40V or V_{CP} = 10V to 50V, V_{VINT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{K30}, V_{VSAT}, V_{VPERI} and V_{VCORE} are within functional range limits, T_j = –40°C to +150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 19-1. Electrical Characteristics – AMUX (Analog Multiplexer for Voltage Measurements)

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
18.1	Output offset error	Has to be calculated from the values of the differential measurement	UZP	$V_{UZPoffset}$	–5		+15	mV	A
18.2	Ratio V_{K15} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.05 ± 4% 6.05 ± 2.3%				A A
18.2a	Ratio V_{K15} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.12 ± 6% 9.12 ± 2.3%				A A
18.3	Ratio V_{K30} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.04 ± 6% 6.04 ± 2.3%				A A
18.3a	Ratio V_{K30} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.11 ± 6% 9.11 ± 2.3%				A A
18.4	Ratio V_{EVZ} / V_{UZP}	For V_{VPERI} = 5V	UZP	Ratio	9.9 ± 2.3%				A
18.4a	Ratio V_{EVZ} / V_{UZP}	For V_{VPERI} = 3.3V	UZP	Ratio	14.78 ± 2.6%				A
18.5	Ratio V_{SAT} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.05 ± 6% 6.05 ± 2.3%				A A
18.5a	Ratio V_{SAT} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.12 ± 6% 9.12 ± 2.3%				A A
18.6	Ratio V_{VCORE} / V_{UZP}	For V_{VPERI} = V_{VCORE} = 5V	UZP	Ratio	2 ± 2.3%				A
18.6a	Ratio V_{VCORE} / V_{UZP}	For V_{VPERI} > V_{VCORE}	UZP	Ratio	0.995 ± 1%				A
18.7	Ratio V_{ISENS} / V_{UZP}	V_{VPERI} – 0.2V ≥ V_{ISENS} ≥ 0.2V	UZP	Ratio	0.992 ± 1%				A
18.8	Ratio V_{K1} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.06 ± 3.5% 6.06 ± 2.3%				A A
18.8a	Ratio V_{K1} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.16 ± 3.5% 9.16 ± 2.3%				A A
18.9	Ratio V_{K2} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.06 ± 3.5% 6.06 ± 2.3%				A A
18.9a	Ratio V_{K2} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.16 ± 3.5% 9.16 ± 2.3%				A A
18.10	Ratio V_{IASG1} / V_{UZP}	For V_{VPERI} = 5V	UZP	Ratio	10 ± 3%				A
18.10a	Ratio V_{IASG1} / V_{UZP}	For V_{VPERI} = 3.3V	UZP	Ratio	14.75 ± 3%				A
18.11	Ratio V_{IASG2} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.04 ± 6% 6.04 ± 2.3%				A A
18.11a	Ratio V_{IASG2} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.11 ± 6% 9.11 ± 2.3%				A A
18.12	Ratio V_{IASG3} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.04 ± 6% 6.04 ± 2.3%				A A
18.12a	Ratio V_{IASG3} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.11 ± 6% 9.11± 2.3%				A A
18.13	Ratio V_{IASG4} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.04 ± 6% 6.04 ± 2.3%				A A
18.13a	Ratio V_{IASG4} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.11 ± 6% 9.11 ± 2.3%				A A
18.14	Ratio V_{IASG5} / V_{UZP}		UZP	Ratio	0.995 ± 1%				A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 19-1. Electrical Characteristics (Continued)– AMUX (Analog Multiplexer for Voltage Measurements)

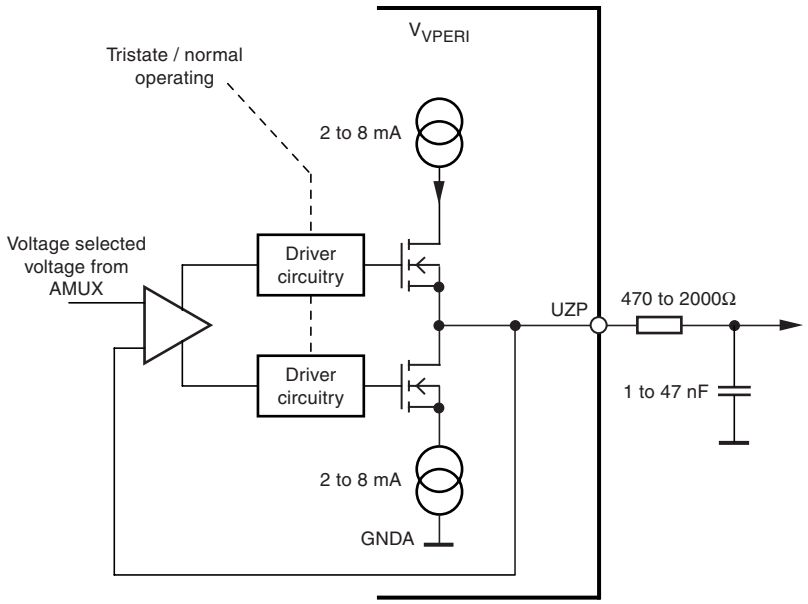
No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
18.15	Ratio V_{USP} / V_{UZP}	For V_{VPERI} = 5V (1.5V to 3V) For V_{VPERI} = 5V (> 3V to 25V)	UZP	Ratio	6.02 ± 6% 6.02 ± 2.3%				A A
18.15a	Ratio V_{USP} / V_{UZP}	For V_{VPERI} = 3.3V (1.5V to 3V) For V_{VPERI} = 3.3V (> 3V to 25V)	UZP	Ratio	9.07 ± 6% 9.07 ± 2.3%				A A
Special Measurement (For Detection of Band-gap Defect)									
18.16	Ratio V_{VINT} / V_{UZP}		UZP	Ratio	3.99 ± 2.6%				A
18.17	Voltage 0.9 × V_{VPERI} switched to V_{UZP}		UZP	Ratio	(0.9 × V_{VPERI}) ± 2%				A
18.18	Voltage 0.1 × V_{VPERI} switched to V_{UZP}		UZP	Ratio	(0.1 × V_{VPERI}) ± 2%				A
18.19	Input voltage range for proper function of 10 or 14.6 divider			V_{Input}	6		40	V	A
18.20	Input voltage range for proper function of 6 or 9.1 divider			V_{Input}	1.5		25	V	A
18.21	Input voltage range for proper function of 4 and 2 divider			V_{Input}	4		6	V	A
18.22	Input voltage range for proper function of 1 buffer			V_{Input}	0.2		V_{VPERI} – 0.2	V	A
18.23	Ratio V_{REF} / V_{UZP}				–2%	1	0%		A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

20. UZP Buffer

The pin UZP is an analog output pin of the ATA6264. The UZP buffer is realized as a tristate output with the ability to drive to VPERI as well as to GNDA. The selected measurement result is given to the pin UZP as long as no new measurement is selected or the tristate command has been sent. Driver capability is typically 4 mA.

Figure 20-1. Functional Principle of the UZP Buffer



Necessary for operation:
V_{PERI} > Reset threshold, V_{CP} = 10V to 50V, V_{VINT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{K30}, V_{EVZ}, V_{VSAT} and V_{VCORE} are within functional range limits, T_J = –40°C to +150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 20-1. Electrical Characteristics – UZP Buffer

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
19.1	Output current high side, driving current with measurement activated	V_{UZP} = 0V, UZP connected to GND	UZP	I_{UZP}	–8		–2	mA	A
19.2	Output current low side, sink current with measurement activated	$V_{UZP} = V_{VPERI}$ UZP connected to GND	UZP	I_{UZP}	2		8	mA	A
19.3	Output settling time	Measured from rising edge of SSQ to 90% of V_{UZP}, no load at pin UZP	UZP	t_{UZP}			10	µs	A
19.4	Output settling time	Load 2 kΩ/22 nF low-pass filter connected to pin UZP, measured from rising edge of SSQ to 90% of $V_{Low\ pass\ filter\ out}$	UZP	t_{UZP}			250	µs	A
19.5	Output resistance		UZP	R_{UZP}			100	Ω	A
19.6	Linear measurement range		UZP	V_{UZP}	0.2		V_{VPERI} – 0.2	V	A
19.7	Maximum output voltage	V_{IASG5} switched via AMUX to UZP, V_{IASG5} = 6V	UZP	V_{UZP}	V_{VPERI} – 50 mV		V_{VPERI} + 50 mV	V	A
19.8	Output leakage current	V_{UZP} = 0V to V_{VPERI}, UZP buffer in tristate mode	UZP	I_{UZP}	–5		+5	µA	A
19.9	Output capacitance	UZP buffer in tristate mode	UZP	C_{UZP}	0		10	pF	D
19.10	Time to switch to tristate mode	Measured from rising edge of SSQ to I_{leak} within tolerance	UZP	t_{UZP}			3	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

21. Chip Temperature Measurement

A serial interface command allows measuring a chip-temperature–dependent voltage which is generated by two diodes connected in series. Three 2-diode sensors are connected in parallel and located in the following blocks: VPERI, VCORE, and VSAT. The diodes are supplied by a temperature-constant current source, the voltage drop of the diodes is switched via AMUX to pin UZP. If the overtemperature level is exceeded, bit a7 in the status register is set to “1”.

Necessary for operation:
V_{INT} = 3.7V to 5.47V

Operating conditions of all other supply pins:
V_{K30}, V_{EVZ}, V_{VSAT}, V_{VPERI} and V_{VCORE} are within functional range limits, T_j = –40°C to 150°C

Other pins:
As defined in Section 4. ”Functional Range” on page 8.

Table 21-1. Electrical Characteristics – Chip Temperature Measurement

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
20.1	Temperature coefficient of chip-temperature sensor	Chip temperature switched via AMUX to UZP	UZP	V_{UZP}	–4	–3.6	–3.2	mV/K	D
20.2	Output voltage temperature sensor	Chip temperature switched via AMUX to UZP, T_J = 25°C	UZP	V_{UZP}	1.29		1.54	V	A
20.3	Threshold overtemperature detection	If overtemperature is detected, voltage drops by 35 mV	UZP	V_{UZP}	155		185	°C	B
20.3a	Hysteresis for overtemperature detection		UZP	V_{UZP}	5		25	K	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

22. Serial Interface Commands

22.1 Overview

All functions of the ATA6264 are triggered by 16-bit serial interface commands. Some of these commands are latched because their actions have to continue for a longer time. Other commands have to be executed as long as no other command is received via the serial interface.

The pin SSQ (low active) is used to select the ATA6264. If pin SSQ is inactive (high), the output pin MISO is disabled (tristate) and the signals at the pins SCLK and MOSI are ignored and do not affect the data in the serial interface register.

With the falling edge at pin SSQ, the ATA6264 response on the previous command is latched in the ATA6264 status register and, after a short delay time, the signal at pin MISO is valid. With the rising edge at pin SCLK, the data at pin MOSI is shifted into the serial interface input register and the next bit of the status register is shifted to pin MISO. A command received at pin MOSI is valid and will be executed if the number of rising edges at pin SCLK was exactly 16 during data transmission; otherwise, the received signal will be ignored.

The *slave select pin,* SSQ, allows the individual selection of different slave SPI devices. Slave devices that are not selected do not interfere with SPI bus activities. To ensure deactivation of the device in case of an open SSQ pin, an internal current source is implemented to drive the SSQ pin to high level (VPERI).

All commands, independent of their function, consist of 16 bits. The serial interface includes a 16-bit input shift register, 16-bit latches, and a decoder logic block for the generation of the SPI command signals.

To suppress data transfer errors in the case of spikes or glitches on the clock signal, a 16-clock-cycle counter is provided. Only after 16 clock cycles does the rising edge of SSQ cause an internal signal *latch enable*, which transfers the data from the shift register to the 16-bit latch. The data word is decoded to address the correct functional block.

Table 22-1. Electrical Characteristics – Serial Interface Commands

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
21.1	SSQ to SCLK rising-edge isolation		SCLK	t_{iso}	100			ns	A(3)
21.2	SSQ lag time		SSQ	t_{lag}	100			ns	A(3)
21.3	Fall time		SSQ, SCLK, MOSI	t_f			20	ns	A(3)
21.3a	Fall time	(2)	MISO	t_f			20	ns	A
21.4	Rise time		SSQ, SCLK, MOSI	t_r			20	ns	A(3)
21.4a	Rise time	(2)	MISO	t_r			20	ns	A
21.5	Data set-up time		MOSI	t_{su}	20			ns	A(3)
21.6	Data hold time		MOSI	t_{hold}	20			ns	A(3)

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note:
1. Voltage levels for serial interface timing measurements: High level = 0.7 × V_{VPERI}, low level = 0.2 × V_{VPERI}
2. Timing specified with a 100-pF external load at pin MISO
3. System requirement

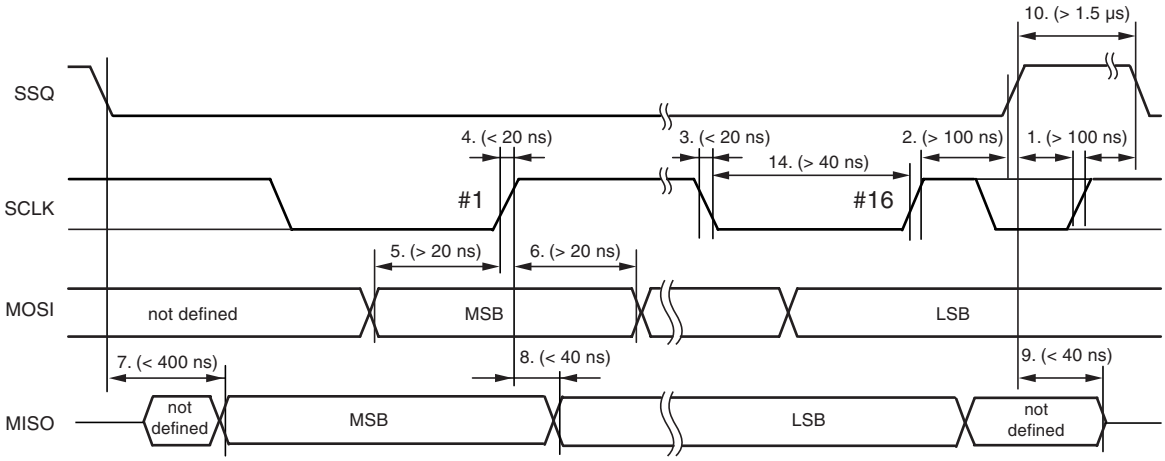
Table 22-1. Electrical Characteristics (Continued)– Serial Interface Commands

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ.	Max.	Unit	Type*
21.7	Time from SSQ falling edge to MISO MSB valid	(2)	MISO	$t_{MISOMSB\_V}$	0		400	ns	A
21.8	Time from SCLK rising edge to MISO valid	(2)	MISO	t_{MISOV}	0		40	ns	A
21.9	Time from SSQ rising edge to MISO tristate condition	(2)	MISO	$t_{MISOhiZ}$	0		40	ns	A
21.10	No-data time between serial interface commands			t_{nodata}	1.5			µs	A(3)
21.11	Clock frequency		CLK	f_{SCLK}	0		8	MHz	A(3)
21.12	Pull-up current VPERI		SSQ	R_{pu_SSQ}	–95		–45	µA	A
21.13	Pull-up current VPERI		SCLK	R_{pu_SCLK}	–95		–45	µA	A
21.14	SCLK high/low time		SCLK	t_{CL}	40			ns	A(3)
21.15	Input voltage high level		SSQ, SCLK, MOSI	V_H			$0.5 \times V_{VPERI}$		A
21.16	Input voltage low level		SSQ, SCLK, MOSI	V_L	$0.25 \times V_{VPERI}$				A
21.17	Input voltage hysteresis		SCLK	V_{HYS}	50		250	mV	A
21.18	Output voltage high level	I_{MISO} = –1 mA to 0 mA	MISO	V_H	$V_{VPERI} - 0.8$		V_{VPERI}	V	A
21.19	Output voltage low level	I_{MISO} = 0 mA to 1 mA	MISO	V_L	0		0.4	V	A
21.20	Output current high level driven to short circuit	V_{VPERI} = 5V	MISO	I_{MISO}	–47		–10	mA	A
21.21	Output current low level sinking from VPERI level	V_{VPERI} = 5V	MISO	I_{MISO}	6		45	mA	A
21.22	Input capacitance		SSQ, SCLK, MOSI	C_{IN}			10	pF	D
21.23	Output capacitance	Switched-off condition	MISO	C_{MISO}			10	pF	D
21.24	Leakage current	Switched-off condition	MISO	I_{MISO}	–10		+10	µA	A
21.25	Number of clock cycles to be detected between falling and rising edge of SSQ, to set error signal in status register to “0”				16		16		A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Voltage levels for serial interface timing measurements: High level = $0.7 \times V_{VPERI}$, low level = $0.2 \times V_{VPERI}$
2. Timing specified with a 100-pF external load at pin MISO
3. System requirement

Figure 22-1. Timing Serial Interface



22.2 Set Commands

After a reset due to the watchdog or undervoltage, all internal control registers and decoded signals are set to their default values.

Table 22-2. Set of Serial Interface Commands

Command	Latch	Hex	Description	MSByte								LSByte							
				7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
				Command								Option and Data							
NOP	No	0000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Key latch	Yes	3xxx	See Table 22-3 on page 71	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x
Watchdog	No	6xxx	See Table 22-4 on page 71	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x
Switch commands	Yes	9xxx	See Table 22-5 on page 71	1	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x
Initial programming	N/A	Axxx	See Table 22-6 on page 72	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x
Diagnosis	No	Cxxx	See Table 22-7 on page 72	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x
IASG	No	Fxxx	See Table 22-8 on page 73	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x
Test mode 1	No	55AA		0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
Test mode 2	No	AA55		1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
Test mode 3	No	5500		0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
Test-mode enable	No	5A5A		0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0

Serial interface commands other than those listed in Table 22-2 on page 70 lead to an interruption of measurements via AMUX, cause pin UZP to be switched to tristate, and IASG sources to be deactivated. The status of the latches does not change.

Table 22-3. Key Latch Commands

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Key latch set	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFF
Key latch reset (default)	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	3000

Table 22-4. Watchdog Commands

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Trigger watchdog	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0	1	6A55
Configure prescaler	0	1	1	0	0	0	0	0	1	1	1	1	0	a	b	c	60Fx

Table 22-5. Switch Commands

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Enable EVZ switching	1	0	0	1	1	0	1	0	0	1	0	1	1	0	1	0	9A5A
EVZ switched to 33V	1	0	0	1	0	0	1	1	0	0	0	0	1	1	1	1	930F
EVZ switched to 23V (default)	1	0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	93F0
EVZ switched to external divider	1	0	0	1	0	0	1	1	1	0	0	1	0	1	1	0	9396
CP-OUT switched to high-ohmic state (default)	1	0	0	1	0	1	1	0	0	0	0	0	1	1	1	1	960F
CP-OUT switched to low-impedance state	1	0	0	1	0	1	1	0	1	1	1	1	0	0	0	0	96F0
K1 interface works as ISO9141 or LIN interface (depending on ISO/LIN bit of initial programming) (default)	1	0	0	1	1	0	0	1	1	1	1	1	0	0	0	0	99F0
K1 interface works in LS driver mode	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	99FF
K1 switched to high-ohmic state (default)	1	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	9CF0
K1 switched to low-impedance state	1	0	0	1	1	1	0	0	1	1	1	1	1	1	1	1	9CFF
K2 interface works as ISO9141 interface (default)	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	9900
K2 interface works in LS driver mode	1	0	0	1	1	0	0	1	0	0	0	0	1	1	1	1	990F
K2 switched to high-ohmic state (default)	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	9C00
K2 switched to low-impedance state	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	9C0F

Because the K1 and K2 interfaces are by default switched to ISO (LIN) mode, the commands 9CF0, 9CFF, 9C00, and 9C0F default to invalid commands.

Table 22-6. Initial Programming (IP Command)

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Write data to IP register	1	0	1	0	1	0	0	1	x	x	x	x	x	x	x	x	A9xx

The initial programming command is only available in Test mode. For more information about the programming flow and the register contents, see Section 5.2 ”Initial Programming of the ATA6264” on page 11.

Table 22-7. Diagnosis Commands

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Set UZP to tristate mode and switch off all measurements	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C000
Switch V_{EVZ} via AMUX to UZP	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	1	CA31
Switch V_{VSAT} via AMUX to UZP	1	1	0	0	1	0	1	0	0	0	1	1	0	0	1	0	CA32
Switch 90% × V_{VPERI} via AMUX to UZP	1	1	0	0	1	0	1	0	0	0	1	1	0	1	0	0	CA34
Switch 10% × V_{VPERI} via AMUX to UZP	1	1	0	0	1	0	1	0	0	0	1	1	1	0	0	0	CA38
Switch V_{VCORE} via AMUX to UZP	1	1	0	0	1	0	1	0	0	1	1	0	0	0	0	1	CA61
Switch V_{K15} via AMUX to UZP	1	1	0	0	1	0	1	0	0	1	1	0	0	0	1	0	CA62
Switch V_{K30} via AMUX to UZP	1	1	0	0	1	0	1	0	0	1	1	0	0	1	0	0	CA64
Switch V_{IREF} via AMUX to UZP	1	1	0	0	1	0	1	0	0	1	1	0	1	0	0	0	CA68
Switch V_{IASG1} via AMUX to UZP	1	1	0	0	1	0	1	0	1	0	0	1	0	0	1	0	CA92
Switch V_{IASG2} via AMUX to UZP	1	1	0	0	1	0	1	0	1	0	0	1	0	1	0	0	CA94
Switch V_{IASG3} via AMUX to UZP	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0	0	CA98
Switch V_{IASG4} via AMUX to UZP	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	1	CAC1
Switch V_{IASG5} via AMUX to UZP	1	1	0	0	1	0	1	0	1	1	0	0	0	0	1	0	CAC2
Switch V_{USP} via AMUX to UZP	1	1	0	0	1	0	1	0	1	1	0	0	0	1	0	0	CAC4
Switch V_{K1} via AMUX to UZP	1	1	0	0	1	0	1	0	1	1	0	0	1	0	0	0	CAC8
Switch V_{K2} via AMUX to UZP	1	1	0	0	1	0	1	0	1	1	1	0	0	0	0	1	CAE1

Note: 1. UZP voltage will be influenced by the USP voltage

Table 22-7. Diagnosis Commands (Continued)

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Switch V_{VINT} via AMUX to UZP	1	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0	CAE2
Switch voltage at chip-temperature sensor via AMUX to UZP	1	1	0	0	1	0	1	0	1	1	1	0	0	1	0	0	CAE4(1)

Note: 1. UZP voltage will be influenced by the USP voltage

Because the diagnosis commands are non-latching commands, any new serial interface commands, except watchdog triggering (6A55) and the Kx switching commands (9Cxx), interrupt the diagnosis.

Table 22-8. IASG Commands

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
IASGx switched to 10V (mirror factor 10:1)	1	1	1	1	0	a	b	c	0	0	1	1	0	0	1	1	Fx33
IASGx switched to 10V (mirror factor 15:1)	1	1	1	1	0	a	b	c	0	0	1	1	1	1	0	0	Fx3C
IASGx switched to 5V (mirror factor 10:1)	1	1	1	1	0	a	b	c	1	1	0	0	0	0	1	1	FxC3
IASGx switched to 5V (mirror factor15:1)	1	1	1	1	0	a	b	c	1	1	0	0	1	1	0	0	FxCC

Note: a, b, and c represent the IASG number in binary format; only 001 = IASG1, 010 = IASG2, 011 = IASG3, 100 = IASG4, and 101 = IASG5 are valid commands

Table 22-9. Example

Description	MSByte								LSByte								Hex Code
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
IASG1 switched to 10V (mirror factor 10:1)	1	1	1	1	0	0	0	1	0	0	1	1	0	0	1	1	F133
IASG5 switched to 5V (mirror factor 15:1)	1	1	1	1	0	1	0	1	1	1	0	0	1	1	0	0	F5CC

Because the IASG commands are non-latching commands, any new serial interface command, except watchdog triggering (6A55) and the Kx switching commands (9Cxx), interrupts the IASG function.

22.3 Serial Interface Status Register

For all serial interface commands except the test-mode commands (55AAh, AA55h, 5500h), the ATA6264 status is available at the MISO line. For the status register a 16-bit structure is used, one bit for each information.

Table 22-10. Status Register

Byte A								Byte B							
MSBit							LSBit	MSBit							LSBit
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0

Table 22-11. Information Provided by the Itemized Bits of the Status Register

Bit	Set To	Information
a7	High	Chip temperature reports overtemperature
	Low	Chip temperature reports normal temperature
a6	High	Overtemperature at K1 output
	Low	Normal temperature at K1 output
a5	High	Overtemperature at K2 output
	Low	Normal temperature at K2 output
a4	High	Latch for GKEY function is set
	Low	Latch for GKEY function is not set
a3	High	EVZ switched to 33V, EVZ switched to external divider
	Low	EVZ switched to 23V
a2	High	CP-OUT switch is low impedance
	Low	CP-OUT switch is high ohmic
a1	High	CP-OUT voltage too low
	Low	CP-OUT voltage is in correct voltage range
a0	High	CP voltage too low
	Low	CP voltage is in correct voltage range
b7	High	Voltage at pin USP above detection threshold
	Low	Voltage at pin USP below detection threshold
b6	High	GNDA or GNDB disconnected
	Low	GNDA and GNDB connected
b5	High	Previously sent serial interface command was invalid (default after power-on reset)
	Low	Previously sent serial interface command was valid
b4	High	Error during last serial interface transmission (default after power-on reset)
	Low	No error during last serial interface transmission
b3	High	IC is in Test mode
	Low	IC is in Normal mode
b2		Reflects bit b2 of the watchdog prescaler
b1		Reflects bit b1 of the watchdog prescaler
b0		Reflects bit b0 of the watchdog prescaler

The overtemperature bits a5, a6 and a7 are latched when overtemperature is detected. These bits will be reset with the next SPI command, unless overtemperature still exists.

In the case of a reset, bits b4 and b5 are not set to their default state. These bits show the status before reset so that the microcontroller can detect whether or not the ATA6264 is in power-up state.

Table 22-12. Test Command Issued via the MISO line as a Result of the Test Mode Commands

Description	Command	MISO Answer																Hex Code
Test mode 1	55AA	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	AA55
Test mode 2	AA55	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	55AA
Test mode 3	5500	0	0	0	0	0	0	0	1	a	b	c	d	e	f	g	h	01xx

Note: a, b, c, d, e, f, g, h represent the contents of the Initial Programming Register

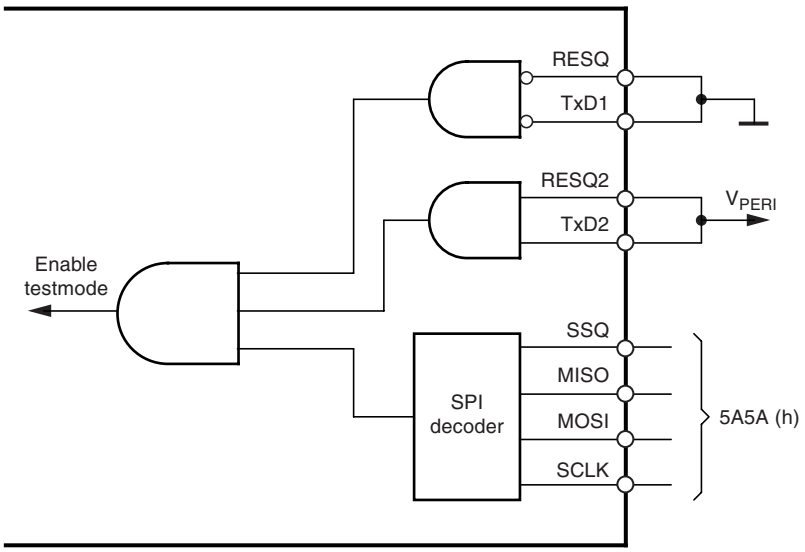
23. Test Mode

For better testability of the ATA6264, a test mode is implemented. This mode is activated if the pins RESQ and TxD1 are connected to GND, the pins RESQ2 and TxD2 are connected to VPERI, and the serial interface command 5A5Ah is sent to the ATA6264. Test mode is latched as long as the ATA6264 is powered (V_{K30} > 4.2V to 5V and V_{K15} > 3V to 4V). In Test mode the watchdog is disabled, which means that RESQ and RESQ2 depend on the voltage levels of the pins VCORE, VPERI and EVZ. In order to provide the programming voltage at VSAT for the initial programming, V_{VSAT} is set to 12.5V (±0.5V) in Test mode if the lock bit is not set.

After a reset, Test mode is disabled (default).

The following serial interface commands are used for the ATA6264 supplier test: E6B5(h) and E6BA(h).

Figure 23-1. How to Enable Test Mode



24. Application Circuits

Figure 24-1. Overview of a Typical Airbag System

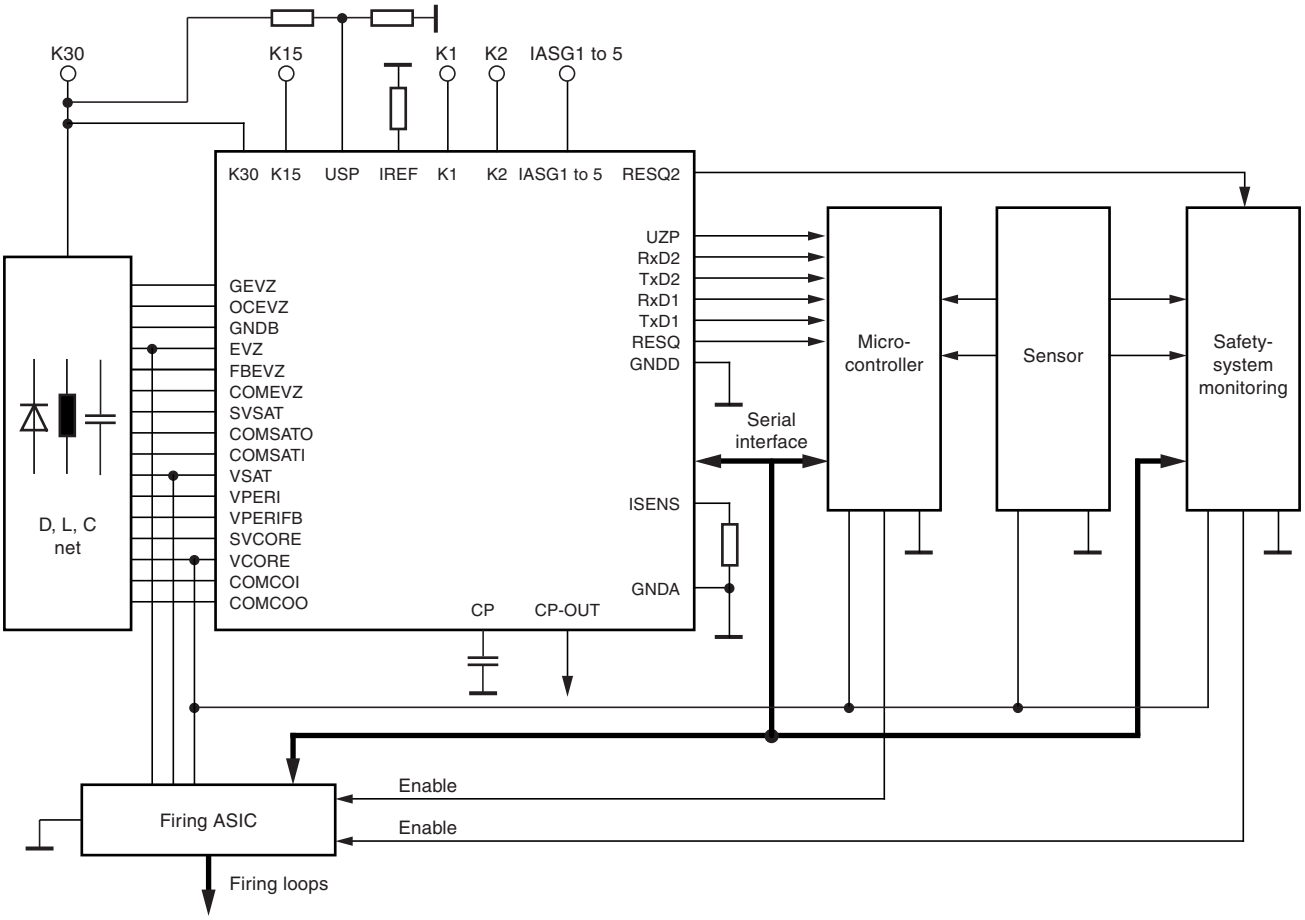
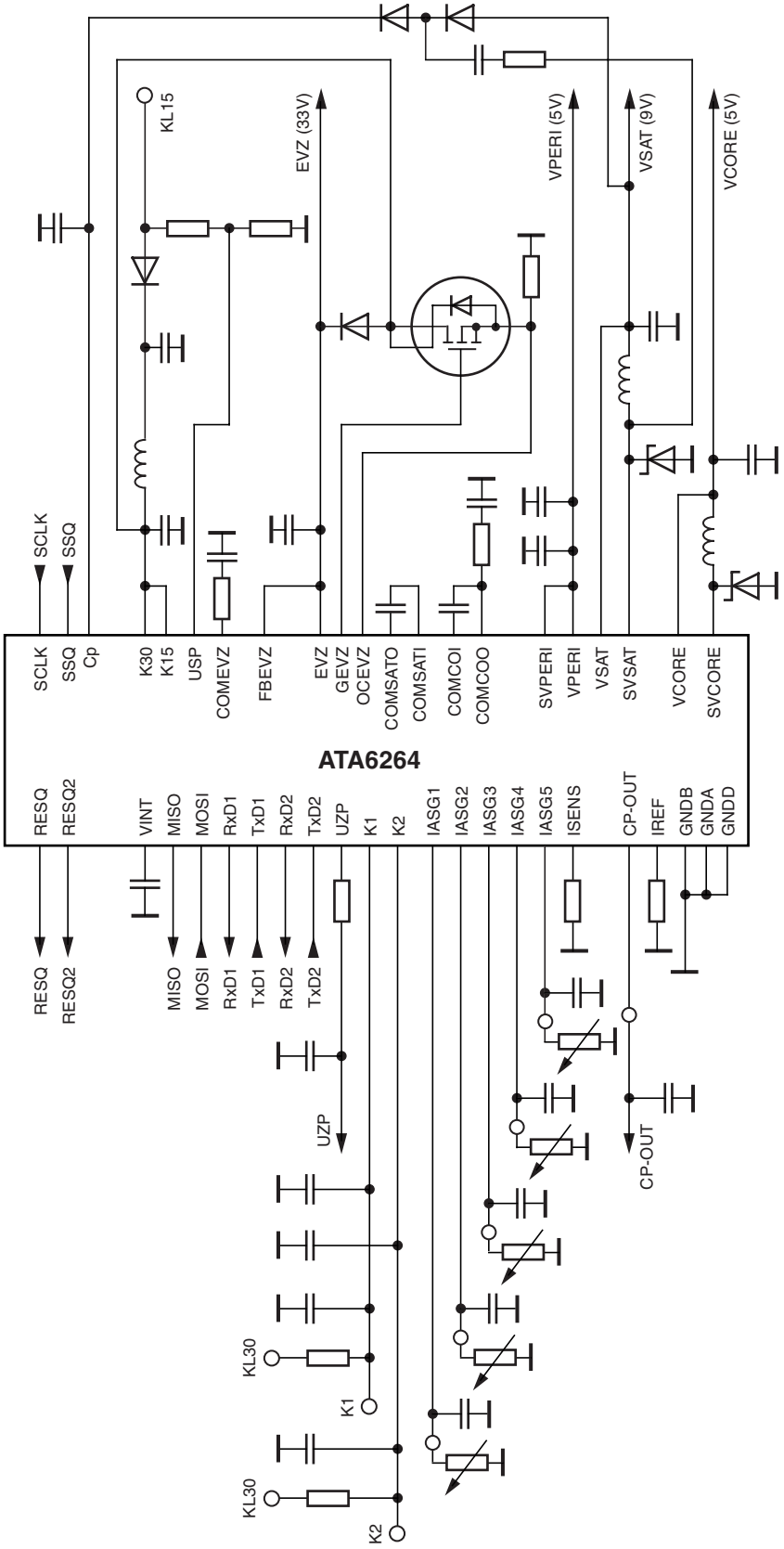


Figure 24-2. Typical Application Circuit



25. Ordering Information

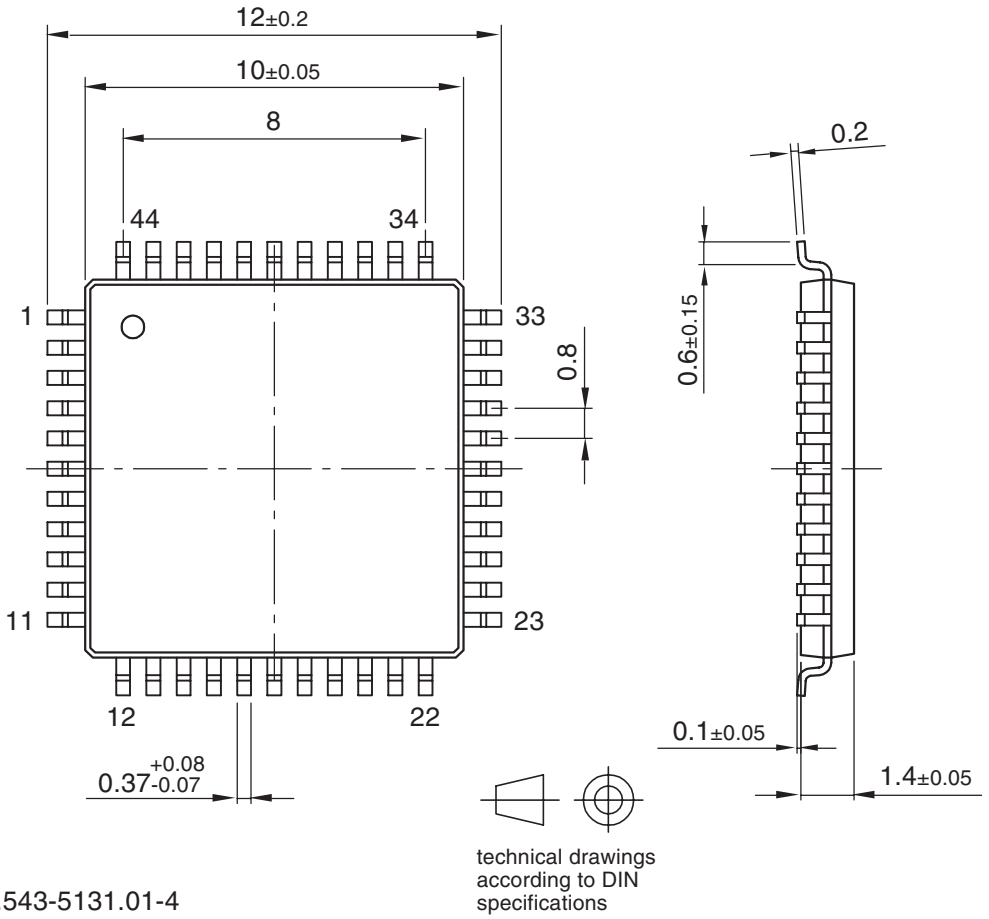
Extended Type Number	Package	Remarks
ATA6264-ALTW	P-TQFP44	Tray
ATA6264-ALQW	P-TQFP44	Taped and reeled

26. Package Information

Package: P-TQFP 44

(acc. JEDEC OUTLINE No. MO-112)

Dimensions in mm



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27. Table of Contents

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