Data Book

AU9340
USB Memory Stick Card Reader Controller Chip
Technical Reference Manual

Product Specification

Official Release

Revision 1.00

Public **Mar 2003**

Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision / Model	Description
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Contact Information:

Web site: http://www.alcormicro.com/

Product URL: http://www.alcormicro.com/product_au9340.htm

Taiwan
Alcor Micro Corp.
4F, No 200 Kang Chien Rd., Nei Hu,
Taipei, Taiwan, R.O.C.
Phone: 886-2-8751-1984
Fax: 886-2-2659-7723

Santa Clara Office
2901 Tasman Drive, Suite 206
Santa Clara, CA 95054
USA
Phone: (408) 845-9300
Fax: (408) 845-9086

Los Angeles Office
9400 Seventh St., Bldg. A2
Rancho Cucamonga, CA 91730
USA
Phone: (909) 483-9900
Fax: (909) 944-0464

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1.0 Introduction

1.1 Description

The AU9340 is a single chip integrated USB Memory Stick (MS) card reader controller. The AU9340 enabled Memory Stick card reader to be used as a removable storage disk in enormous data exchange applications between PC and PC or PC and various consumer electronic appliances.

The AU9340 reads digital data saved on memory stick while users manipulating electronic devices such as digital cameras, MP3 players, PDAs and mobile phones… etc. By the AU9340, users can transfer information such as data, graphics, texts or digital images from one electronic device to another quickly and easily. With AU9340, users' knowledge will be further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows 2000/XP and Mac OS X.

By integrating of various analog components, the AU9340 is the most powerful and most effective solution for Memory Stick card .

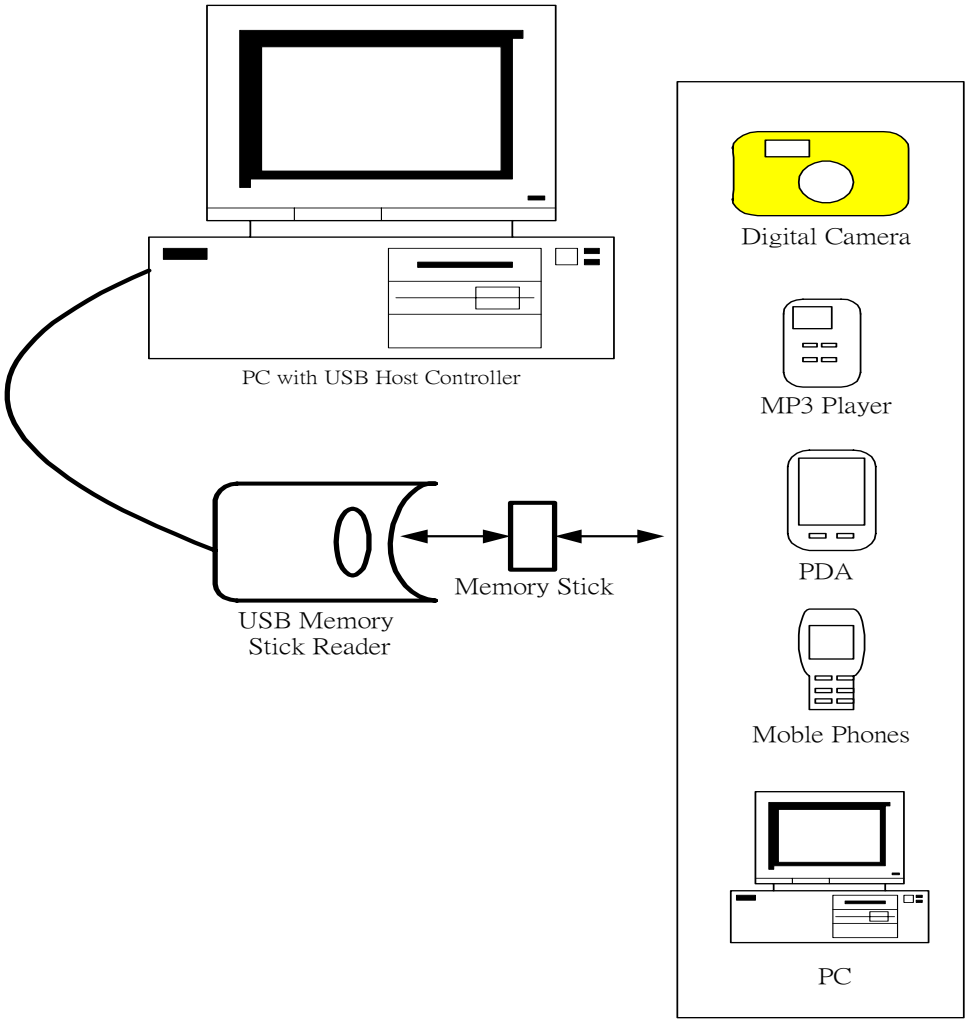
1.2 Features

- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Fully compliant with Memory Stick (MS) v1.3 Specification.
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac OS 9.1, and Mac OS X. Windows 98 is supported by mass storage class driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation.
- Dedicated hardware engine for MS bus operation, average throughput over 1MB/sec for read, 680KB/sec for write operation.
- Support multiple sectors transfer up to 128MB to optimize performance
- Support optional external EEPROM for USB VID, PID and string customization
- Capable of handling 8 sets of built-in PID, VID and strings to minimize inventory control and improve lead production lead time
- LED for bus activity indication.
- Integrated power switch and power management circuit to meet USB 500uA power consumption during suspend with MS card in the slot.
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- 28-pin SSOP package

2.0 Application Block Diagram

Following is the application diagram of a typical memory stick card reader. By connecting the reader to a PC through USB bus, the AU9340 is acting as a bridge between the flash memory card from digital camera, MP3 player, PDA or mobile phone and PC.

Figure 2.1 Block Diagram



3.0 Pin Assignment

The AU9340 is packed in 28-SSOP form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail

Figure 3.1 Pin Assignment Diagram

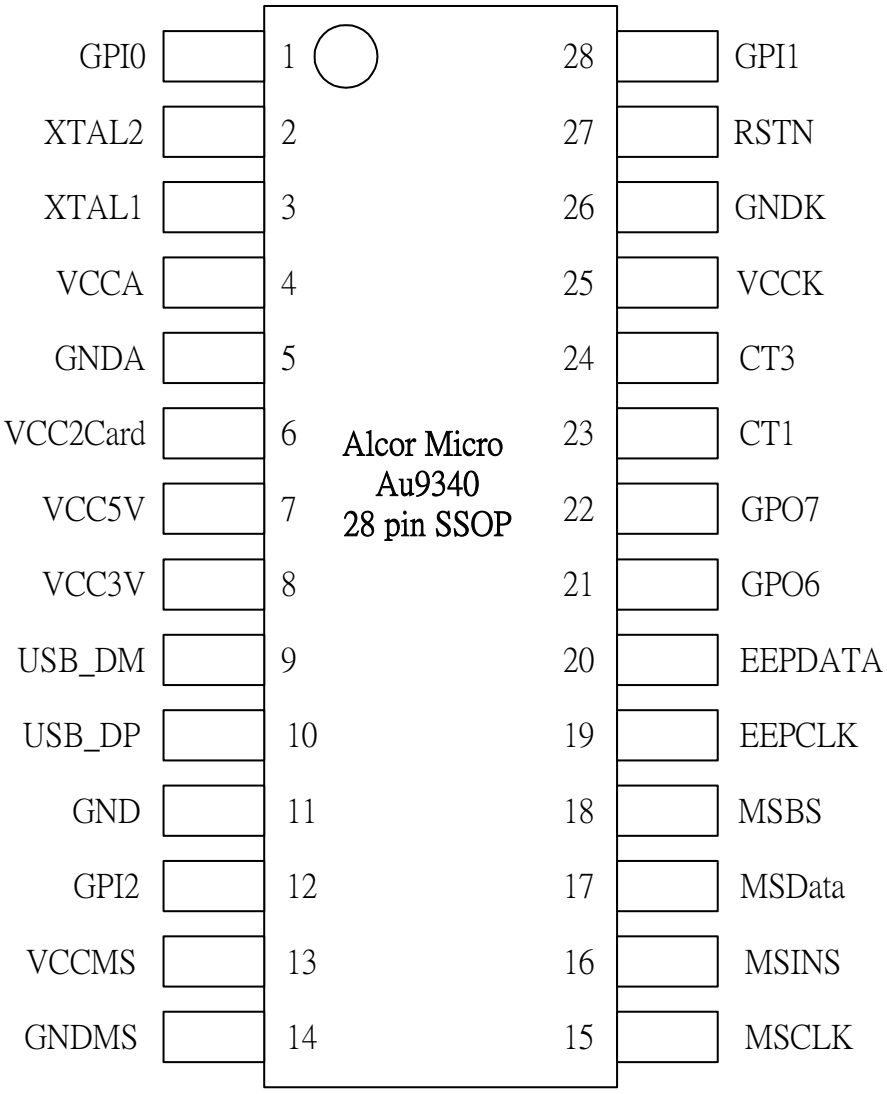


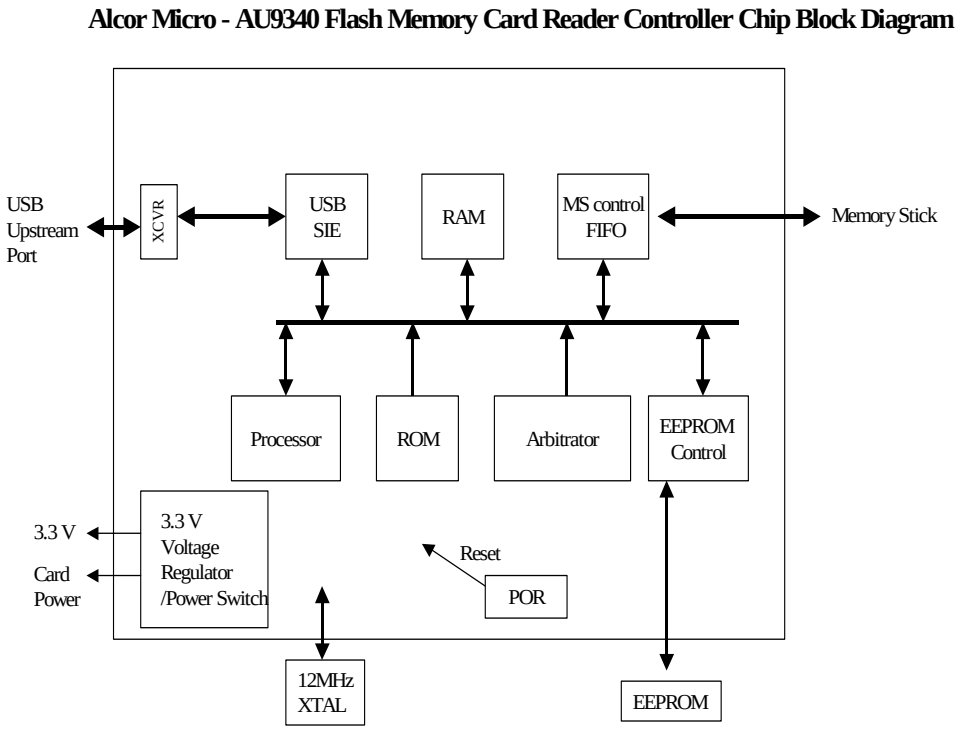
Table 3.1 Pin Descriptions

PIN	Name	Input/Output	Description
1	GPI0	Input	Internal ROM selection, Connect to GND or VCC
2	XTAL2	Output	Crystal Oscillator Output (12 MHz)
3	XTAL1	Input	Crystal Oscillator Input (12 MHz)
4	VCCA	Power	Analog 3.3 Input
5	GNDA	GND	Ground
6	VCC2Card	Output	Power to MS Card
7	VCC5V	Power	5V power supply
8	VCC3V	Power	Regulator 3.3V output for VCCA and VCCK.
9	USB_DM	Input/Output	USB D-
10	USB_DP	Input/Output	USB D+
11	GND	GND	Ground
12	GPI2	Input	Internal ROM selection, Connect to GND or VCC
13	VCCMS	Input	InPut VCC3V to MS Power
14	GNDMS	Input	InPut Ground to MS Power Ground
15	MSCLK	Output	Connect to MS Card SCLK. #8
16	MSINS	Input	Connect to MS Card INS Pin #6
17	MSData	Input/Output	Connect to MS Card Data Pin #4
18	MSBS	Output	Connect to MS Card BS Pin #2
19	EEPCLK	Input	EEPROM clock
20	EEPDATA	Input	EEPROM data
21	GPO6	Output	NC
22	GPO7	Output	Connect to LED
23	CT1	Input	Connect to GND
24	CT3	Input	Connect to Ground
25	VCCK	Power	3.3 Core Voltage Input
26	GNDK	GND	Ground
27	RSTN	Input	Connect to VCC3
28	GPI1	Input	Internal ROM selection, Connect to GND or VCC

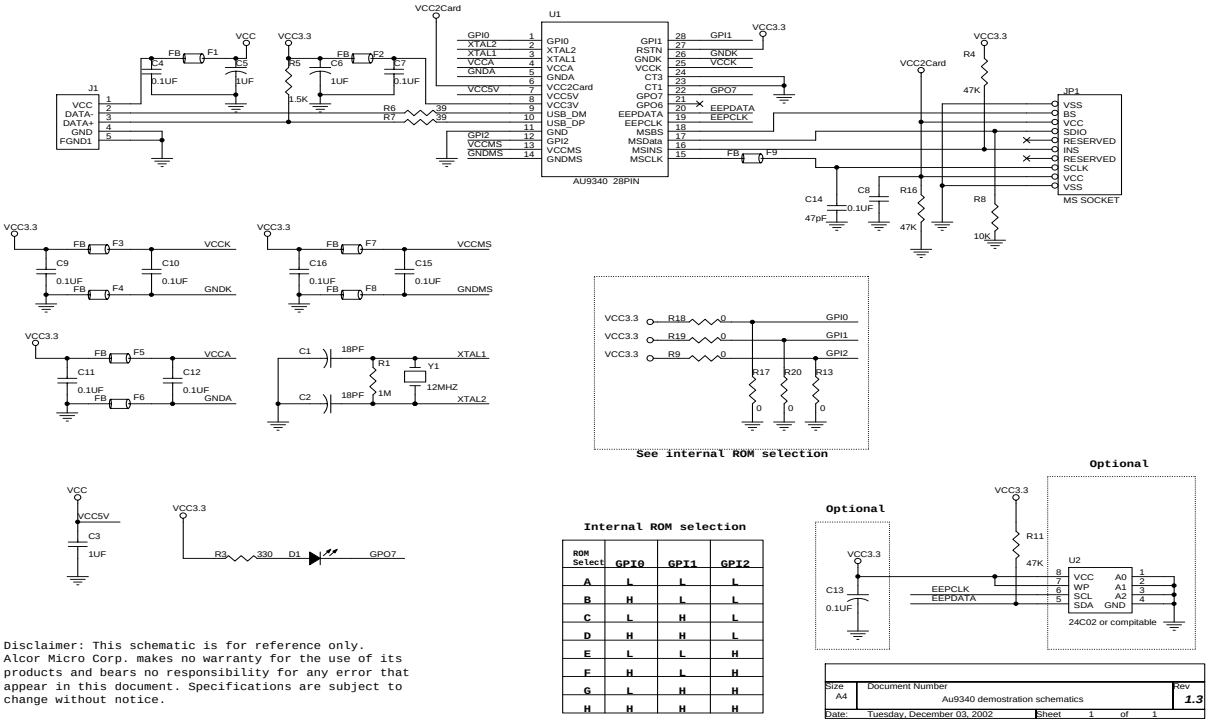
4.0 System Architecture and Reference Design

4.1 AU9340 Block Diagram

Figure 4.1 AU9340 Block Diagram



4.2 Sample Schematics



Internal ROM selection

ROM Select	GPI0	GPI1	GPI2
A	L	L	L
B	H	L	L
C	L	H	L
D	H	H	L
E	L	L	H
F	H	L	H
G	L	H	H
H	H	H	H

Size	Document Number	Rev
A4	Au9340 demostration schematics	1.3
Date: Tuesday, December 03, 2002	Sheet 1 of 1	

5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to 6.0	V
V_{IN}	Input Voltage	-0.3 to VCC+0.3	V
V_{OUT}	Output Voltage	-0.3 to VCC+0.3	V
T_{STG}	Storage Temperature	-40 to 125	°C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	-5		85	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	μA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	μA
I_{OZ}	Tri-state leakage current		-10		10	μA
C_{IN}	Input capacitance			4		ρF
C_{OUT}	Output capacitance			4		ρF
C_{BID}	Bi-directional buffer capacitance			4		ρF

5.4 DC Electrical Characteristics for 5 volts operation

Table 5.4 DC Electrical Characteristics for 5 volts operation

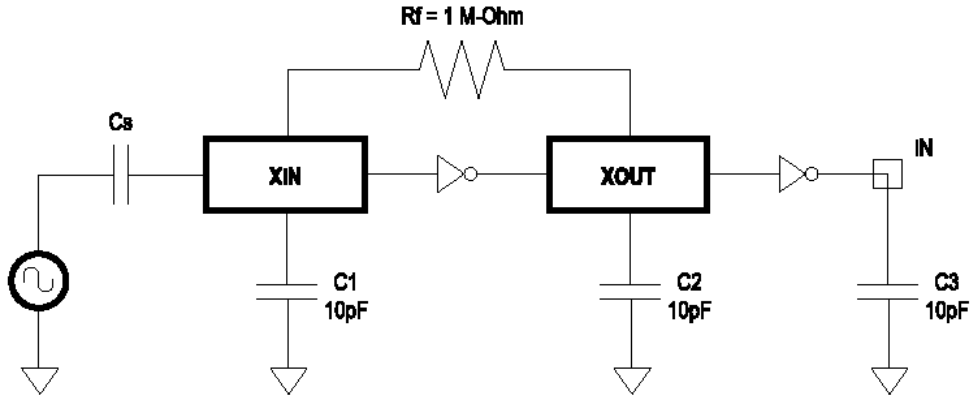
(Under Recommended Operating Conditions and V_{CC}=4.5v ~ 5.5v , Tj= -40°C to + 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IL}	Input Low Voltage	CMOS			0.3*V_{CC}	V
V_{IL}	Schmitt input Low Voltage	TTL		1.10		V
V_{IL}	Schmitt input Low V oltage	CMOS		1.84		V
V_{IH}	Input High Voltage	TTL	2.2			V
V_{IH}	Input Hight Voltage	CMOS	0.7*V_{CC}			V
V_{IH}	Schmitt input High Voltage	TTL		1.87		V
V_{IH}	Schmitt input High Voltage	CMOS		3.22		V
V_{OL}	Output low voltage	I_{OL}=2, 4, 8, 12, 16, 24 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2, 4, 8, 12, 16, 24 mA	3.5			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		50		KΩ

5.5 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.

Figure 5.1 Crystal Oscillator Circuit Setup for Characterization



5.6 USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

Table 5.5 USB Transceiver Characteristics

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

Table 5.6 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	Vi<0		-50	mA
V_I	DC input voltage	Note 3	-0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5	Vcc +0.5	V
I_{OK}	DC output diode current	Vo> Vcc or Vo<0		+/-50	mA
V_O	DC output voltage	Note 3	-0.5	Vcc +0.5	V
I_O	DC output source sink current for VP/VM and RCV pins	Vo=0 to Vcc		+/-15	mA
I_O	DC output source or sink current for D+/D- pins	Vo= 0 to Vcc		+/-50	mA
I_{CC}, I_{GND}	DC Vcc or GND current			+/-100	mA
T_{STO}	Storage temperature range		-60	+150	°C
P_{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

Table 5.7 DC Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS -40°C to +85°C			UNIT
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.6V (Note 3)	0.3	0.4	0.5	V
VIH	HIGH level input	Vcc=3.0V to 3.6V (Note 3)		1.5	2.0	V
VIL	LOW level input	Vcc=3.0V to 3.6V (Note 3)	0.8	1.1		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA	2.2 2.4 2.8	2.7		V
VOL	LOW level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply current	Vcc=3.6V VI=Vcc or GND Io=0		330	600	µA
Isup	Supply current in suspend	Vcc=3.6V VI=Vcc or GND Io=0			70	µA
IFS	Active supply current (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply current (Low Speed)	Vcc=3.3V		2		mA
ILeak	Input leakage current	Vcc=3.6V VI=5.5V or GND, not for I/O Pins		+/-0.1	+/-0.5	µA
IOFF	3-state output OFF-state current	Vi=Vih or ViL; Vo=Vcc or GND			+/-10	µA

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

GND=0V, t_R = t_F =3.0 ns; C_L =50 pF; RL=500 Ohms

Table 5.8 AC Electrical Characteristics

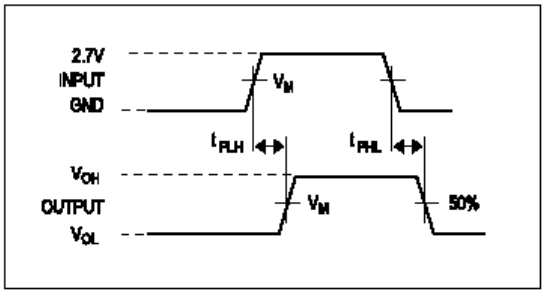
SYMBOL	PARAMETER	WAVEFORM	LIMITS (T_{AMB})					UNIT
			0°C to +25°C			0°C to +70°C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup for SPEED	5	0					ns
Vcr	Crossover point[1]	3	1.3		2.0	1.3	2.0	V

NOTES:

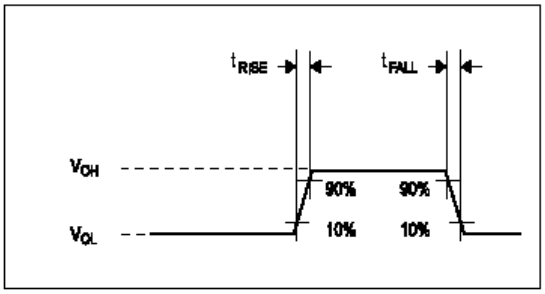
1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 50 pF capacitance.

Figure 5.2 Electrical Characteristics Diagram

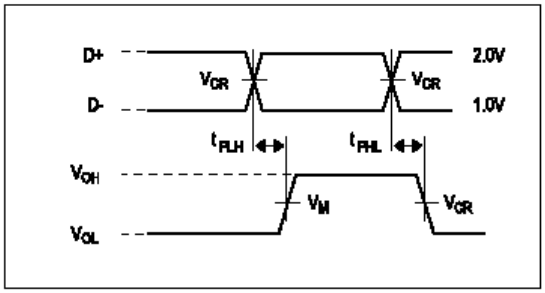
AC WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



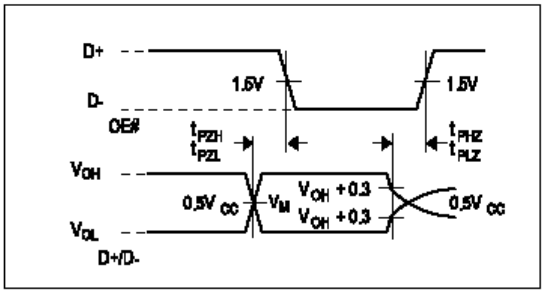
AC WAVEFORM 2.
RISE AND FALL TIMES



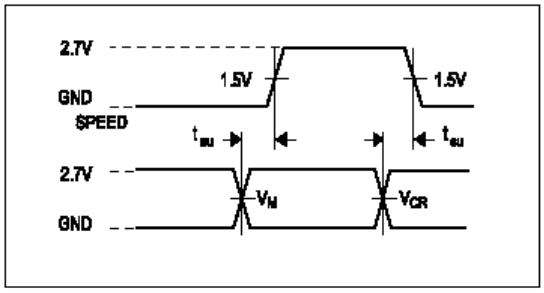
AC WAVEFORM 3.
D+/D- TO RCV



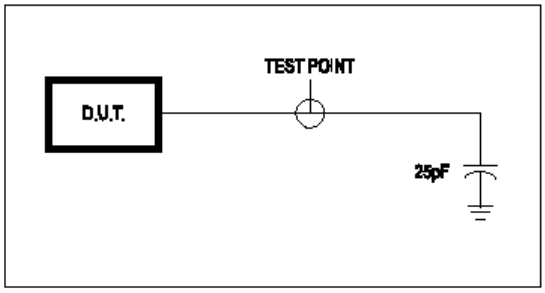
AC WAVEFORM 4.
OE# TO D/+/D-



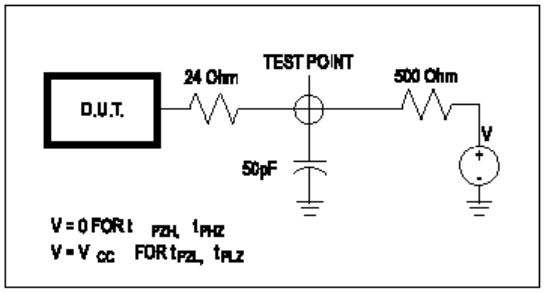
AC WAVEFORM 5.
SETUP FOR SPEED



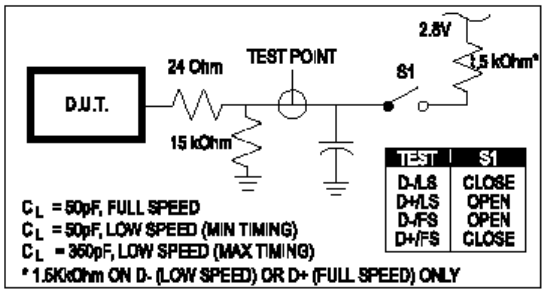
TEST CIRCUIT 1.
LOAD FOR VM/VP AND RCV



TEST CIRCUIT 2.
LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.
LOAD FOR D+/D-



5.7 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test circuit & condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

Table 5.9 ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	6000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

5.8 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

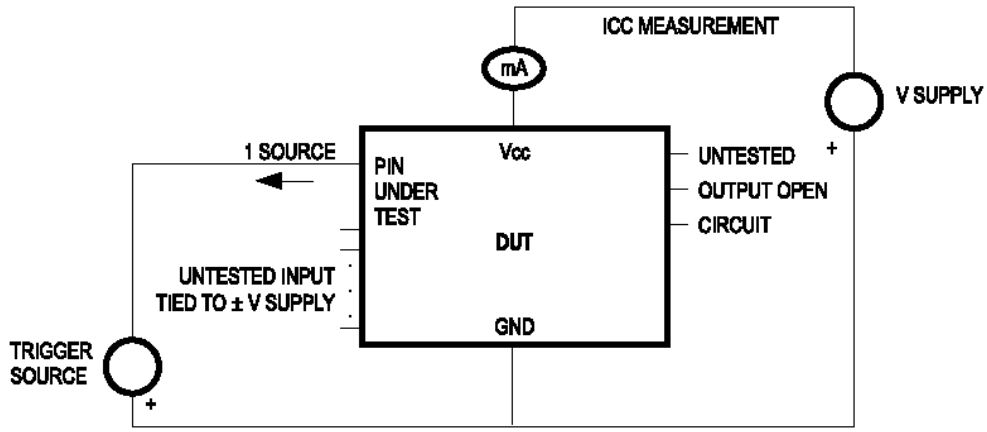
Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

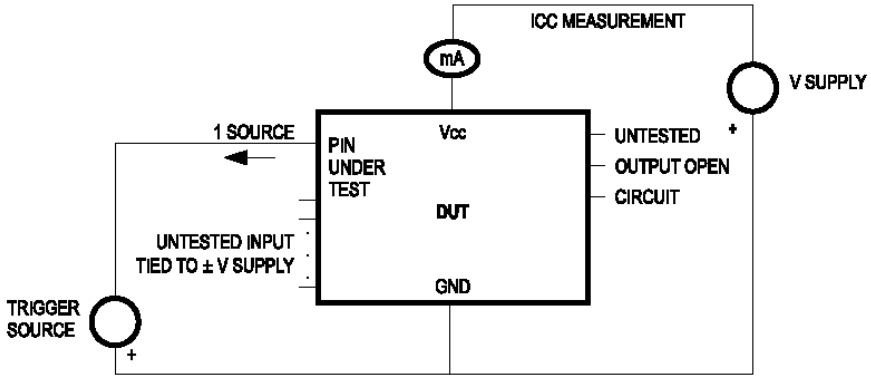
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

Notes:
1. DUT: Device Under Test.
2. PUT: Pin Under Test.

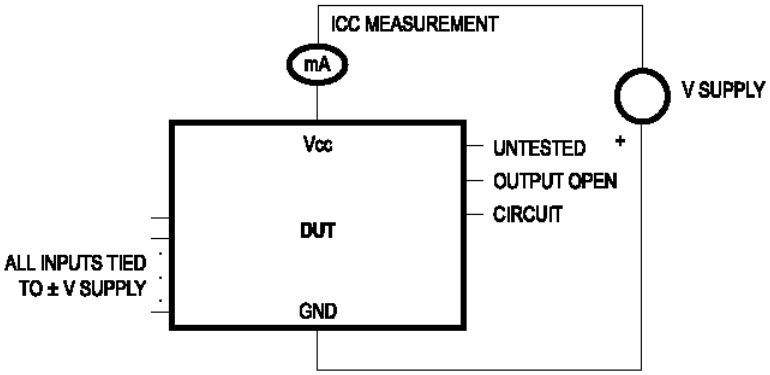
Figure 5.3 Latch-Up Test Results



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



Supply Overvoltage Test

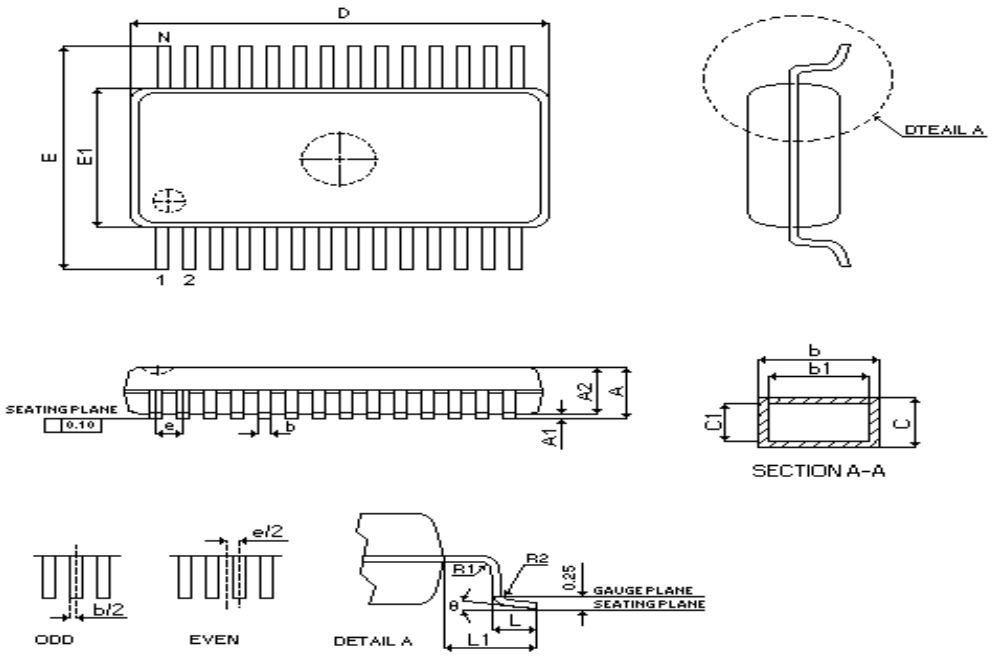
Table 5.10 Latch–Up Data

Mode		Voltage (V)/Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

6.0 Mechanical Information

Following diagrams show the dimensions of the AU9340 28-pin SSOP. Measurements are in inches. Dimensions do not include mold flash and dambar protrusion; allowable mold flash is 0.010 inch.

Figure 6.1 Mechanical Information Diagram



R REV.	DESCRIPTION	BY	DATE
ORIG.	1. REGENERATED FROM PO-P402 VERSION"A" 2. ADD GAUGE PLANE	JIMMY	97.04.21
①	ADD CROSS SECTIONA-A" DRAWING	STEVEN	97.07.31
②	MODIFY 0.020 TO 0.002	IRIS	97.08.21
③	ADD E-PIN CHANGE PIN "I" DOT DIMENSION	IRIS	98.06.10

SYMBOL	COMMON DIMENSION MILLIMETERS			COMMON DIMENSION INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			2			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22		0.38	0.009		0.015
b1	0.22	0.3	0.33	0.009	0.012	0.013
c	0.09		0.25	0.004		0.01
c1	0.09	0.15	0.21	0.004	0.006	0.008
D	9.90	10.20	10.50	0.390	0.402	0.413
E	7.4	7.8	8.2	0.291	0.307	0.323
E1	5	5.3	5.6	0.197	0.209	0.22
e	0.65 BSC			0.0256 BSC		
L	0.55	0.75	0.95	0.021	0.03	0.037
L1	0.25 REF.			0.050 REF.		
R1	0.09			0.004		
R2	0.09			0.004		
θ	0	40	80	0	40	80

N	14	16	18	20	24	28
0 ± 0.30	6.20	6.20	7.20	7.20	8.20	10.20
JEDEC NO.	MO-150 AB	MO-150 AC	MO-150 AD	MO-150 AE	MO-150 AG	MO-150 AH

UNLESS OTHERWISE SPECIFIED	DECMAL X ± xx ±.10 xxx ±.05	ANGULAR ±3°	ORENT SEMCONOUCTOR ELECTRONICS	UNIT	MM	SCALE:10:1
				SHEET:1 OF1		
DRAWN	IRIS 98.06.10		TITLE	FILE:PD-P503C		A3
CHECKED			SSOP 14/16/20/21/28L(209MIL)	DWG. NO.:		
APPROVED			PACKAGE OUTLINE	PD-P503C		

【MEMO】

About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.