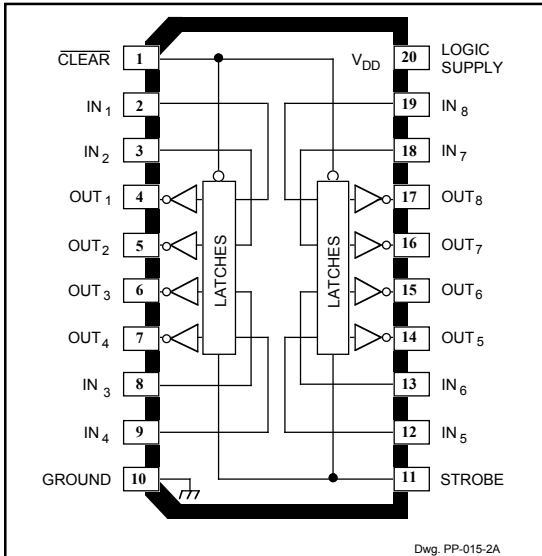


6B273

8-BIT LATCHED DMOS POWER DRIVER



Dwg. PP-015-2A

Note that the A6B273KA (DIP) and the A6B273KLW (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

Output Voltage, V_O	50 V
Output Drain Current, Continuous, I_O	150 mA*
Peak, I_{OM}	500 mA†
Single-Pulse Avalanche Energy, E_{AS}	30 mJ
Logic Supply Voltage, V_{DD}	7.0 V
Input Voltage Range, V_I	-0.3 V to +7.0 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	-40°C to +125°C
Storage Temperature Range, T_S	-55°C to +150°C

* Each output, all outputs on.

† Pulse duration $\leq 100 \mu\text{s}$, duty cycle $\leq 2\%$.

Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6B273KA and A6B273KLW combine eight (positive-edge-triggered D-type) data latches and DMOS outputs for systems requiring relatively high load power. Driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads. The CMOS inputs and latches allow direct interfacing with microprocessor-based systems. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

The DMOS output inverts the DATA input. All of the output drivers are disabled (the DMOS sink drivers turned OFF) with the CLEAR input low. The A6B273KA/KLW DMOS open-drain outputs are capable of sinking up to 500 mA. Similar devices with reduced $r_{DS(on)}$ are available as the A6273KA/KLW.

The A6B273KA is furnished in a 20-pin dual in-line plastic package. The A6B273KLW is furnished in a 20-lead wide-body, small-outline plastic package (SOIC) with gull-wing leads for surface-mount applications. Copper lead frames, reduced supply current requirements, and low on-state resistance allow both devices to sink 150 mA from all outputs continuously, to ambient temperatures over 85°C.

FEATURES

- 50 V Minimum Output Clamp Voltage
- 150 mA Output Current (all outputs simultaneously)
- 5 Ω Typical $r_{DS(on)}$
- Low Power Consumption
- Replacements for TPIC6B273N and TPIC6B273DW

Selection Guide

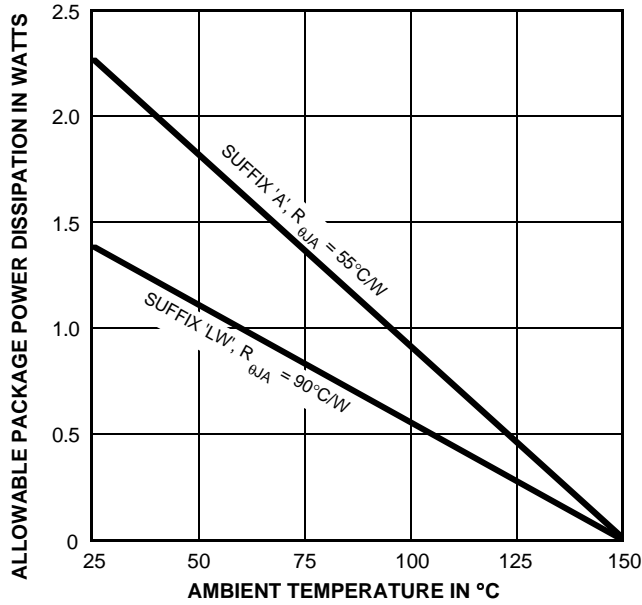
Part Number	Pb-free*	Package	Packing	$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)
A6B273KLW-T	Yes	20-pin SOICW	37 per tube	70	17
A6B273KLWTR-T	Yes	20-pin SOICW	1000 per reel	70	17

*Pb-based variants are being phased out of the product line. Some variants cited in this footnote are in production but have been determined to be LAST TIME BUY or NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The variants should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change for LAST TIME BUY: October 31, 2006. Deadline for receipt of LAST TIME BUY orders: April 27, 2007. These variants include: A6B273KLW and A6B273KLWTR. Status change for NOT FOR NEW DESIGN: May 1, 2006. These variants include: A6B273KA.

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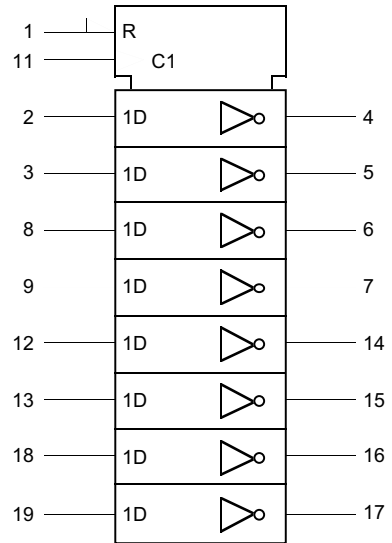
8-BIT LATCHED

DMOS POWER DRIVER

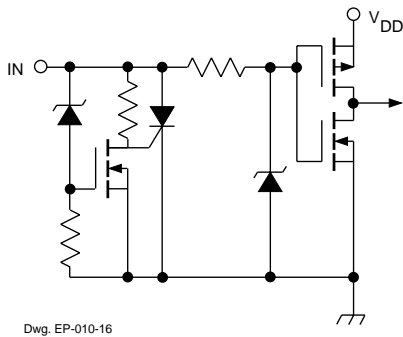


Dwg. GS-004B

LOGIC SYMBOL

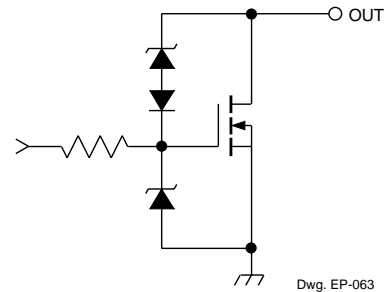


Dwg. FP-046-1A



Dwg. EP-010-16

LOGIC INPUTS



Dwg. EP-063

DMOS POWER DRIVER OUTPUT

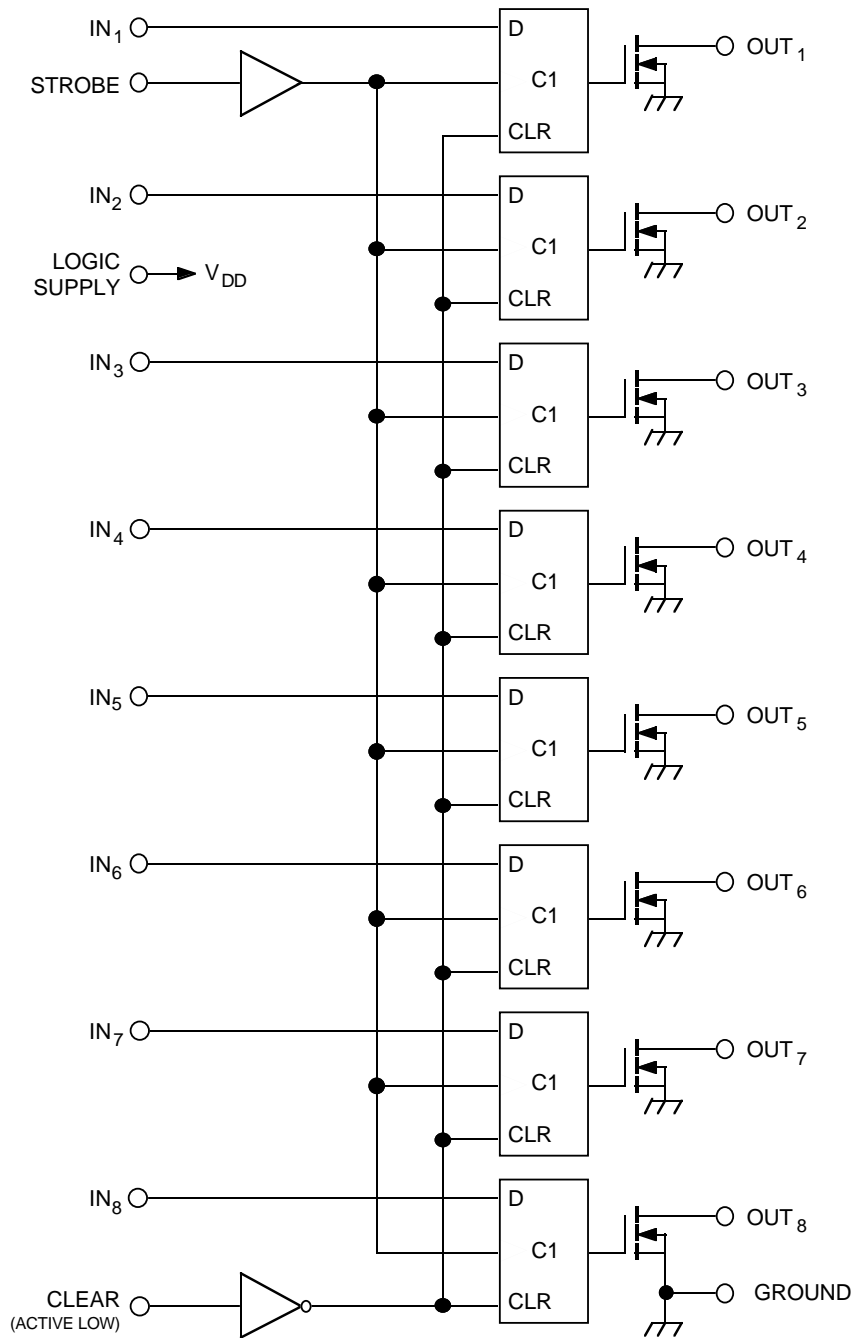
FUNCTION TABLE

$\overline{\text{CLEAR}}$	Inputs		OUT _x
	STROBE	IN _x	
L	X	X	H
H		H	L
H		L	H
H	L	X	R

L = Low Logic Level
H = High Logic Level
X = Irrelevant
R = Previous State

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FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-016-2

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RECOMMENDED OPERATING CONDITIONS

over operating temperature range

Logic Supply Voltage Range, V_{DD} 4.5 V to 5.5 V

High-Level Input Voltage, V_{IH} $\geq 0.85V_{DD}$

Low-level input voltage, V_{IL} $\leq 0.15V_{DD}$

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $t_{ir} = t_{if} \leq 10\text{ ns}$ (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Output Breakdown Voltage	$V_{(BR)DSX}$	$I_O = 1\text{ mA}$	50	—	—	V
Off-State Output Current	I_{DSX}	$V_O = 40\text{ V}$, $V_{DD} = 5.5\text{ V}$	—	0.1	5.0	μA
		$V_O = 40\text{ V}$, $V_{DD} = 5.5\text{ V}$, $T_A = 125^\circ\text{C}$	—	0.15	8.0	μA
Static Drain-Source On-State Resistance	$r_{DS(on)}$	$I_O = 100\text{ mA}$, $V_{DD} = 4.5\text{ V}$	—	4.2	5.7	Ω
		$I_O = 100\text{ mA}$, $V_{DD} = 4.5\text{ V}$, $T_A = 125^\circ\text{C}$	—	6.8	9.5	Ω
		$I_O = 350\text{ mA}$, $V_{DD} = 4.5\text{ V}$ (see note)	—	5.5	8.0	Ω
Nominal Output Current	I_{ON}	$V_{DS(on)} = 0.5\text{ V}$, $T_A = 85^\circ\text{C}$	—	90	—	mA
Logic Input Current	I_{IH}	$V_I = V_{DD} = 5.5\text{ V}$	—	—	1.0	μA
	I_{IL}	$V_I = 0$, $V_{DD} = 5.5\text{ V}$	—	—	-1.0	μA
Prop. Delay Time	t_{PLH}	$I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$	—	150	—	ns
	t_{PHL}	$I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$	—	90	—	ns
Output Rise Time	t_r	$I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$	—	200	—	ns
Output Fall Time	t_f	$I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$	—	200	—	ns
Supply Current	$I_{DD(OFF)}$	$V_{DD} = 5.5\text{ V}$, Outputs off	—	20	100	μA
	$I_{DD(ON)}$	$V_{DD} = 5.5\text{ V}$, Outputs on	—	150	300	μA

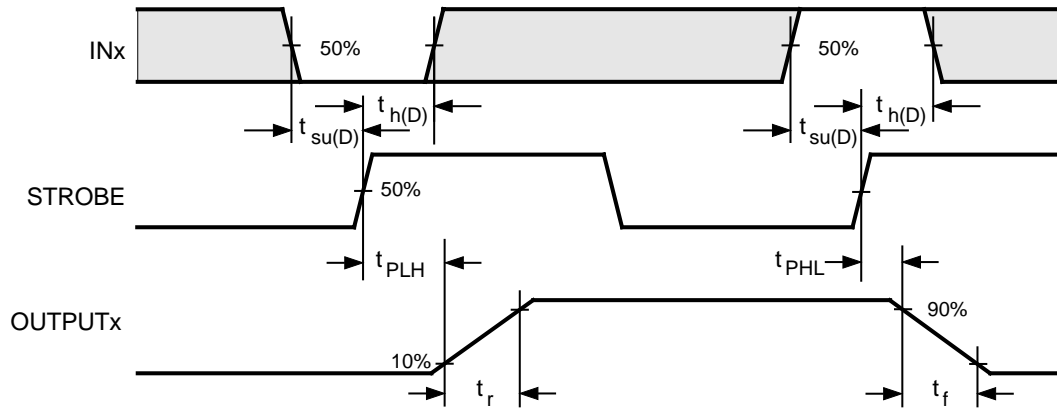
Typical Data is at $V_{DD} = 5\text{ V}$ and is for design information only.

NOTE — Pulse test, duration $\leq 100\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



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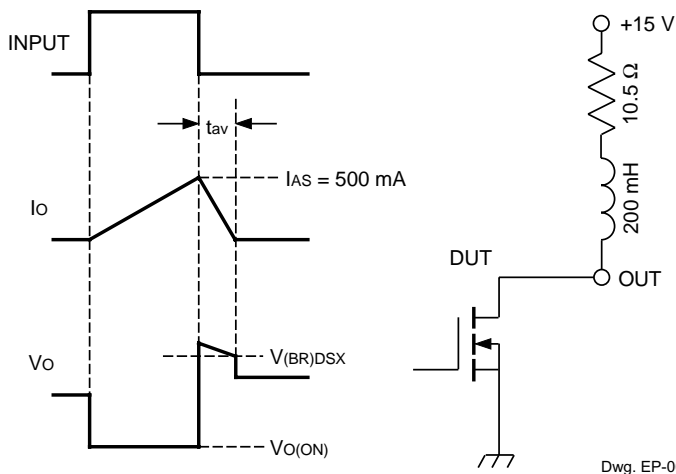
TIMING REQUIREMENTS



Dwg. WP-036-1

Input Active Time Before Strobe (Data Set-Up Time), $t_{su(D)}$	20 ns
Input Active Time After Strobe (Data Hold Time), $t_{h(D)}$	20 ns
Input Pulse Width, $t_{w(D)}$	40 ns
Input Logic High, V_{IH}	$\geq 0.85V_{CC}$
Input Logic Low, V_{IL}	$\leq 0.15V_{CC}$

TEST CIRCUITS



**Single-Pulse Avalanche Energy Test Circuit
and Waveforms**

Dwg. EP-066

$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

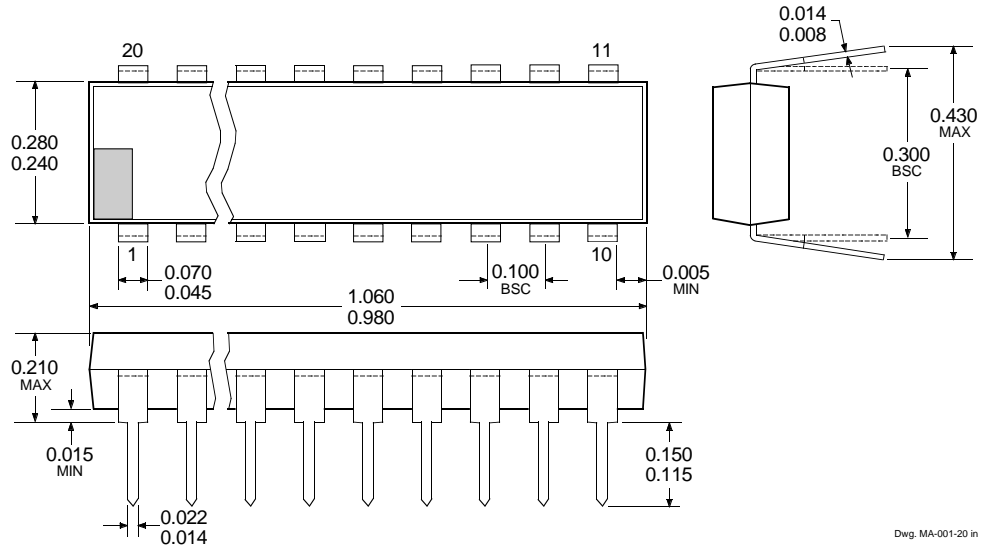
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TERMINAL DESCRIPTIONS

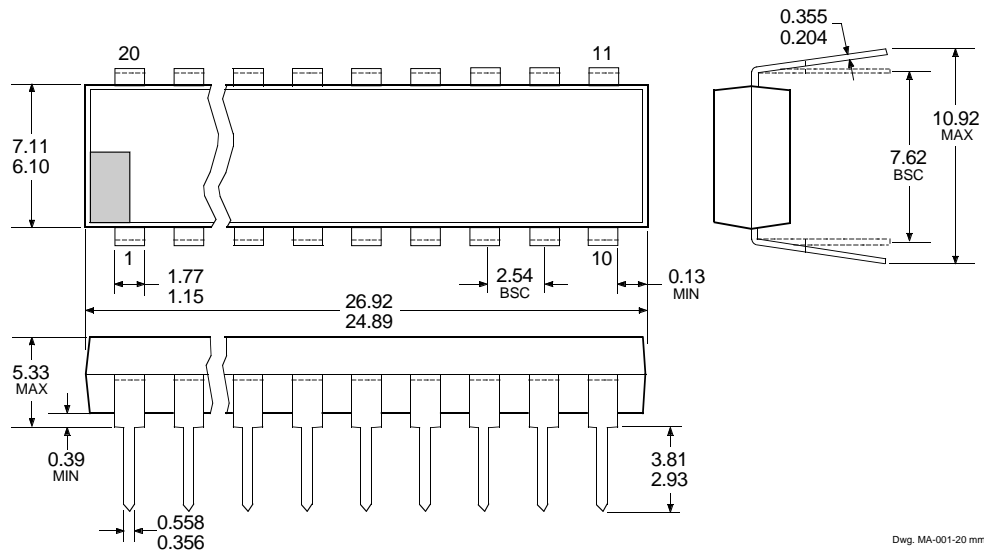
Terminal No.	Terminal Name	Function
1	CLEAR	When (active) LOW, all latches are reset and all outputs go HIGH (turn OFF).
2	IN ₁	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₁ = HIGH, OUT ₁ = LOW).
3	IN ₂	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₂ = HIGH, OUT ₂ = LOW).
4	OUT ₁	Current-sinking, open-drain DMOS output.
5	OUT ₂	Current-sinking, open-drain DMOS output.
6	OUT ₃	Current-sinking, open-drain DMOS output.
7	OUT ₄	Current-sinking, open-drain DMOS output.
8	IN ₃	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₃ = HIGH, OUT ₃ = LOW).
9	IN ₄	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₄ = HIGH, OUT ₄ = LOW).
10	GROUND	Reference terminal for all voltage measurements.
11	STROBE	A CMOS dynamic input to all latches. Data on each IN _x terminal is loaded into its associated latch on a low-to-high STROBE transition.
12	IN ₅	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₅ = HIGH, OUT ₅ = LOW).
13	IN ₆	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₆ = HIGH, OUT ₆ = LOW).
14	OUT ₅	Current-sinking, open-drain DMOS output.
15	OUT ₆	Current-sinking, open-drain DMOS output.
16	OUT ₇	Current-sinking, open-drain DMOS output.
17	OUT ₈	Current-sinking, open-drain DMOS output.
18	IN ₇	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₇ = HIGH, OUT ₇ = LOW).
19	IN ₈	CMOS data input to a latch. When strobed, the output then inverts the data input (IN ₈ = HIGH, OUT ₈ = LOW).
20	LOGIC SUPPLY	(V _{DD}) The logic supply voltage (typically 5 V).

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A6B273KA Dimensions in Inches (controlling dimensions)



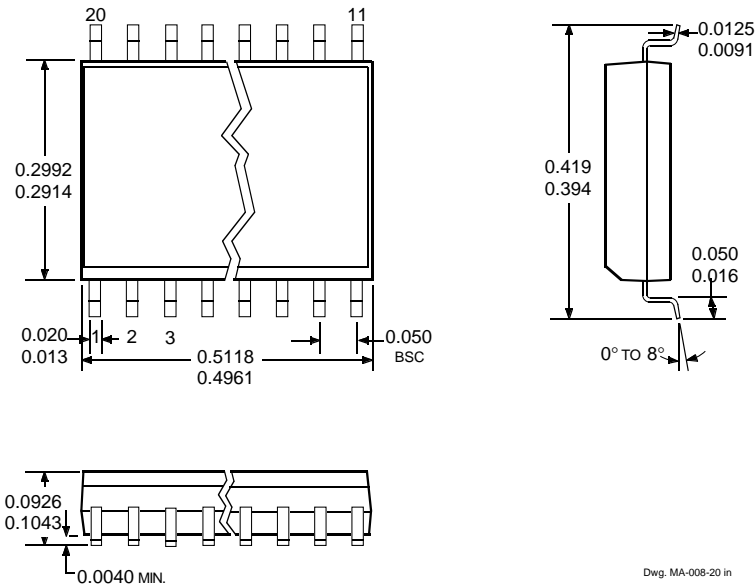
Dimensions in Millimeters (for reference only)



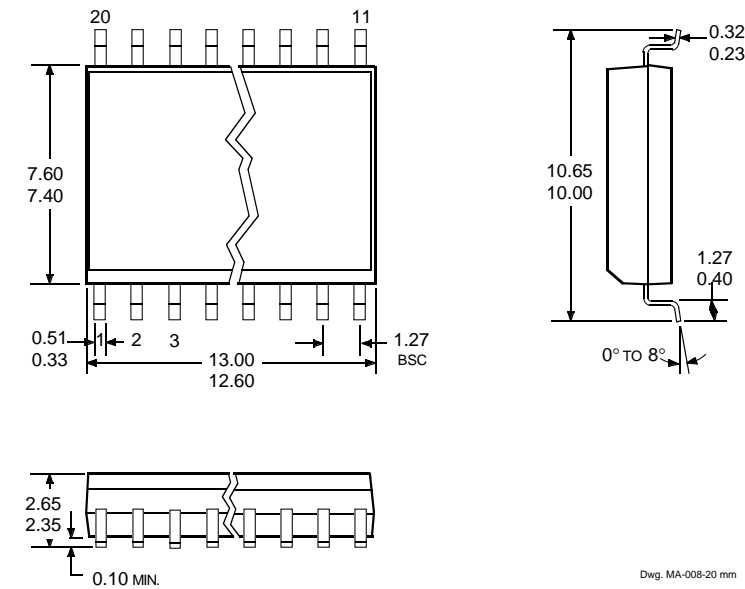
- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative.
 3. Lead thickness is measured at seating plane or below.
 4. Supplied in standard sticks/tubes of 18 devices.

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DMOS POWER DRIVER

A6B273KLW
 Dimensions in Inches
 (for reference only)



Dimensions in Millimeters
 (controlling dimensions)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative.
 3. Supplied in standard sticks/tubes of 37 devices or add 'TR' to part number for tape and reel.

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8-BIT LATCHED
DMOS POWER DRIVER

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8-BIT LATCHED
DMOS POWER DRIVER

POWER
INTERFACE DRIVERS

Function	Output Ratings*		Part Number†
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (constant-current LED driver)	120 mA	24 V	6277
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6810
12-Bit (active pull-downs)	-25 mA	60 V	5811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
SPECIAL-PURPOSE DEVICES			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

