AP3842/3/4/5

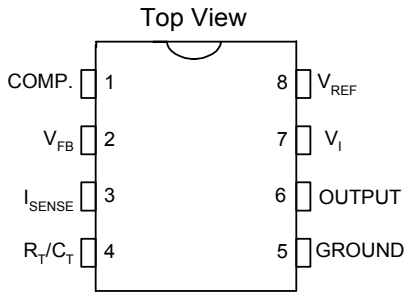
High Performance Current Mode PWM Controller

■ Features

- Optimized for Off-Line and DC to DC Converters
- Low Start-Up Current (≦0.5mA)
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout (UVLO) with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- Current Mode Operation to 500KHZ
- Low Ro Error Amplifier

■ Pin Connections

PDIP-8L, SOP-8L



■ General Description

The AP3842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 0.5 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The AP3842 and AP3844 have UVLO thresholds of 16V(on) and 10V(off), ideally suited for off-line applications. The corresponding thresholds for the AP3843 and AP3845 are 8.5V and 7.6V. The AP3842 and AP3843 can operate to duty cycles approaching 100%. A range of the zero to < 50% is obtained by the AP3844 and AP3845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

■ Ordering Information

AP 384X X X X

Part No.	Package	Lead Free	Packing
2:3842 3:3843 4:3844 5:3845	S8:SOP-8L N8:PDIP-8L	Blank : Normal L : Lead Free Package	Blank: Tube A : Taping

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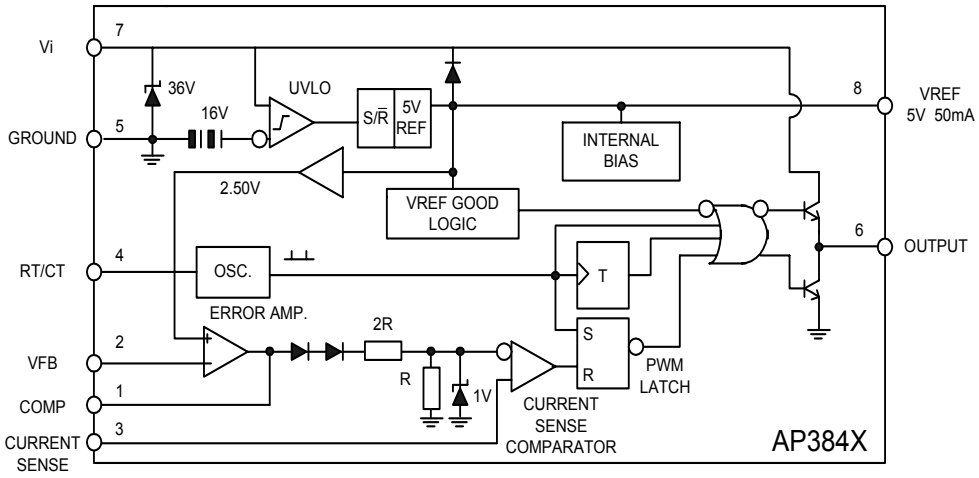
■ Block Diagram (toggle flip flop used only in AP3844 and AP3845)



■ Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	36	V
V_i	Supply Voltage (Ii < 30mA)	Self Limiting	
I_o	Output Current	±0.7	A
E_o	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins2,3)	-0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leqq 50^0C$ (PDIP8)	1.25	W
P_{tot}	Power Dissipation at $T_{amb} \leqq 25^0C$ (SOP8)	800	mW
T_{stg}	Storage Temperature Range	-65 to 150	^0C
T_L	Lead Temperature (soldering 10s)	260	^0C

*Notes: 1. All voltages are with respect to pin 5, all currents are positive into the specified terminal.

■ Electrical Characteristics

(Unless otherwise stated, these specifications apply for $0 \leqq T_{amb} \leqq 70^oC$ for AP384X ; V_i = 15V(note 5); R_T = 10KΩ;C_T = 3.3nF)

Symbol	Parameter	Test Conditions	AP384X			Unit
			Min.	Typ.	Max.	
REFERENCE SECTION						
V_{REF}	Output Voltage	Tj = 25^0C I_0=1mA	4.90	5.00	5.10	V
ΔV_{REF}	Line Regulation	$12V \leqq V_i \leqq 25V$		2	20	mV
ΔV_{REF}	Load Regulation	$1mA \leqq I_o \leqq 20mA$		3	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Notes 2)		0.2	0.4	$mV/^0C$
	Total Output Variation	Line, Load, Temperature (Notes 2)	4.82		5.18	V
e_N	Output Noise Voltage	$10Hz \leqq f \leqq 10KHz$ Tj=25^0C (Notes 2)		50		μV
	Long Term Stability	T_{amb}=125^0C, 1000Hrs (Notes 2)		5	25	mV
I_{SC}	Output Short Circuit current			-85	-120	mA

■ Electrical Characteristics(Continued)

(Unless otherwise stated, these specifications apply for $0 \leqq T_{amb} \leqq 70^{o}C$ for AP384X ; V_i = 15V(note 5); R_T = 10KΩ;C_T = 3.3nF)

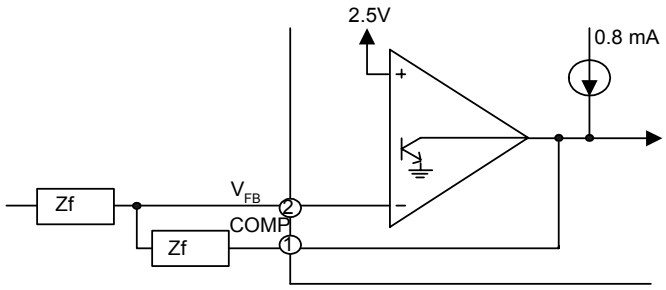
Symbol	Parameter	Test Conditions	AP384X			Unit
			Min.	Typ.	Max.	
OSCILLATOR SECTION						
f_s	Oscillator Frequency	Tj=25°C (Notes 6, 7)	49	52	55	KHz
	Voltage Stability	$12V \leqq V_i \leqq 25V$		0.2	1	%
	Temperature Stability	$T_{MIN} \leqq T_{amb} \leqq T_{MAX}$ (Notes 2)		0.5		%
V_4	Amplitude	V_{PIN4} Peak to Peak		1.6		V
	Discharge Current	Tj=25°C V_{PIN4}=2V	7.8	8.3	8.8	mA
ERROR AMP SECTION						
V_2	Feedback Input Voltage	V_{PIN1}=2.5V	2.42	2.50	2.58	V
I_b	Input Bias Current	V_{FB}=5V		-0.1	-2	μA
	A_{VOL}	$0V \leqq V_0 \leqq 4V$	65	90		dB
B	Unity Gain Bandwidth	Tj=25°C	0.7	1		MHz
SVRR	Supply Voltage Rejection Ratio	$12V \leqq V_i \leqq 25V$	60	70		dB
I_O	Output Sink Current	V_{PIN2}=2.7V V_{PIN1}=1.1V	2	6		mA
I_O	Output Source Current	V_{PIN2}=2.3V V_{PIN1}=5V	-0.5	-0.8		mA
	V_{OUT} High	V_{PIN2}=2.3V; R_L=15KΩ to ground	5	7		V
	V_{OUT} Low	V_{PIN2}=2.7V; R_L=15KΩ to pin 8		0.8	1.1	V
CURRENT SENSE SECTION						
G_v	Gain	(Notes3&Notes4)	2.85	3	3.15	V/V
V_3	Maximum Input Signal	V_{PIN1}=5V (Notes3)	0.9	1	1.1	V
SVRR	Supply Voltage Rejection Ratio	$12 \leqq V_i \leqq 25V$ (Notes3)		70		dB
I_b	Input Bias Current			-2	-10	μA
	Delay to Output			150	300	ns
OUTPUT SECTION						
V_{OL}	Output Low Level	I_{SINK}= 20mA		0.1	0.4	V
		I_{SINK}= 200mA		1.6	2.2	V
V_{OH}	Output High Level	I_{SOURCE}= 20mA	13	13.5		V
		I_{SOURCE}= 200mA	12	13.5		V
T_r	Rise Time	Tj=25°C C_L=1nF (Notes2)		50	150	ns
T_f	Fall Time	Tj=25°C C_L=1nF (Notes2)		50	150	ns
V_{OLS}	UVLO Saturation	Vcc = 6V ; Isink = 1mA		0.1	1.1	V
UNDER-VOLTAGE LOCKOUT SECTION						
	Start Threshold	3842/4	14.5	16	17.5	V
		3843/5	7.8	8.4	9	V
	Min Operating Voltage After Turn-on	3842/4	8.5	10	11.5	V
		3843/5	7.0	7.6	8.2	V
PWM SECTION						
	Maximum Duty Cycle	3842/3	94	96		%
		3844/5	47	48	50	%
	Minimum Duty Cycle				0	%
TOTAL STANDBY CURRENT						
I_{st}	Start-up Current	Vi=14V,3842/4 ; Vi=6.5V 3843/5		0.3	0.5	mA
I_i	Operating Supply Current	V_{PIN2}=V_{PIN3}=0V		12	17	mA
V_{iz}	Zener Voltage	I_i=25mA	30	36		V

Notes：2.These parameters, although guaranteed, are not 100% tested in production.
3.Parameter measured at trip point of latch with V_{PIN2}=0.
4.Gain defined as:

$$A=\frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} \quad ; 0 \leqq V_{PIN3} \leqq 0.8V$$

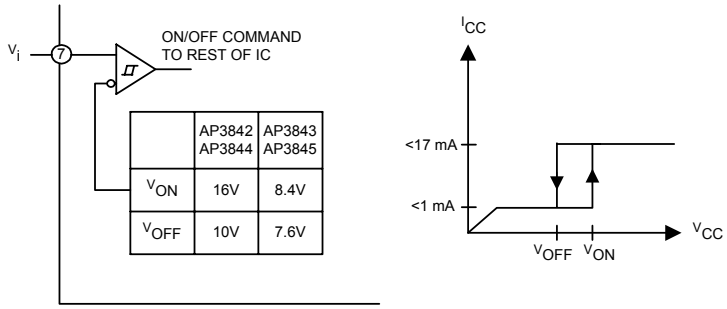
5.Adjust V_i above the start threshold before setting at 15V.
6.Output frequency equals oscillator frequency for the AP3842 and AP3843.
7.Output frequency is one and half oscillator frequency for the AP3844 and AP3845.

Figure 1 : Error Amp Configuration.



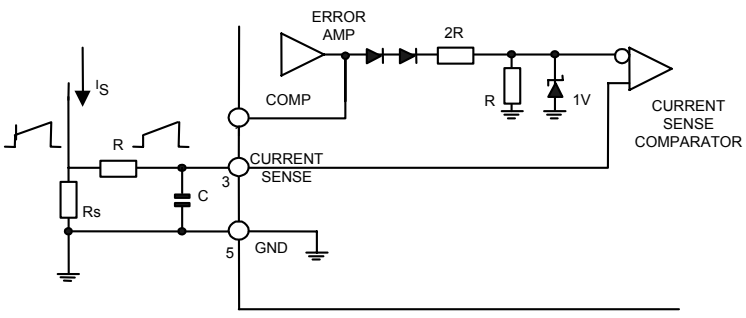
Error amp can source or sink up to 0.5mA

Figure 2 : Under Voltage Lockout.



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Figure 3 : Current Sense Circuit.



Peak current(i_s) is determined by the formula

$$I_S \max \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 4.

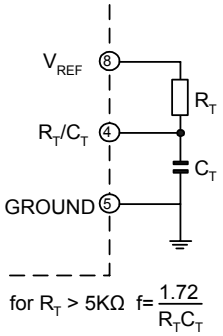
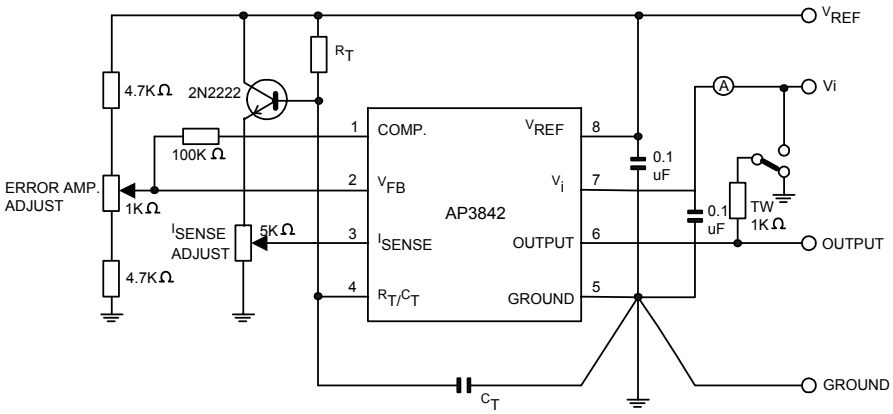
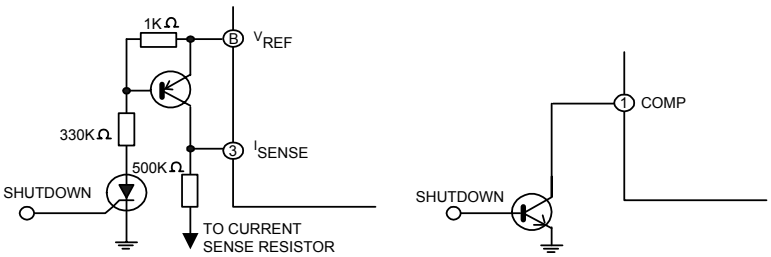


Figure 5 : Open Loop Test Circuit.



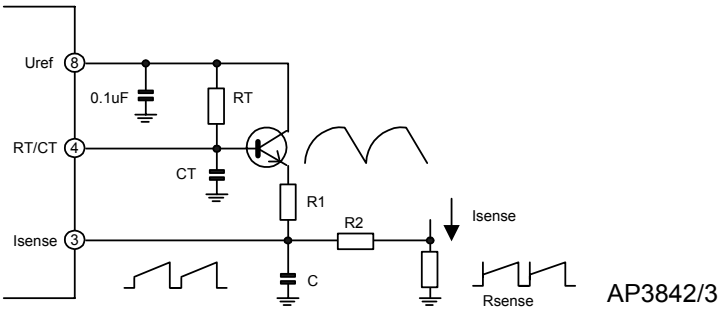
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass apacitors should be connected close to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 6 : Shutdown Techniques.



Shutdown of the AP3842 can be accomplished in two ways; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either one of them causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR that will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

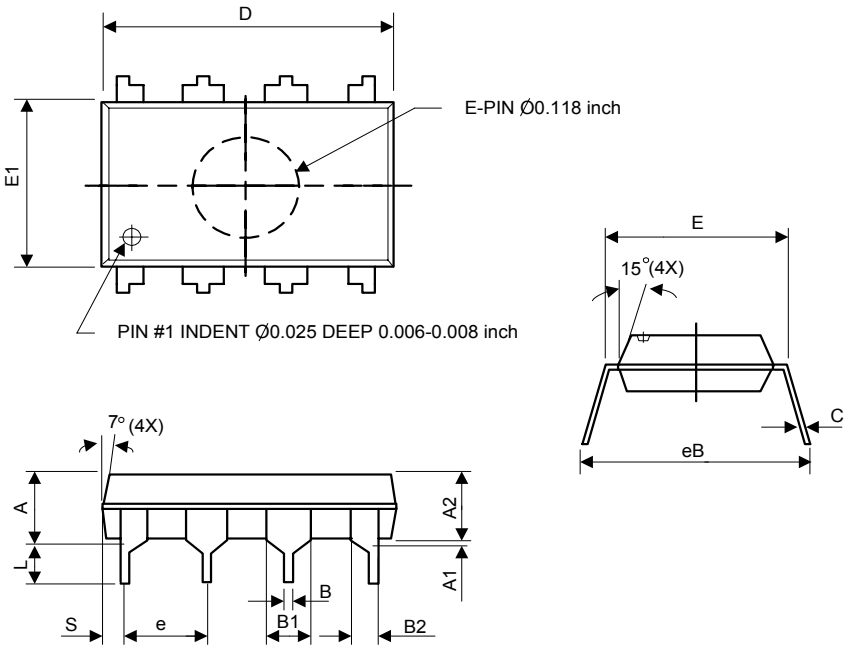
Figure 7 : Slope Compensation.



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor, C, forms a filter with R_2 to suppress the leading edge switch spikes.

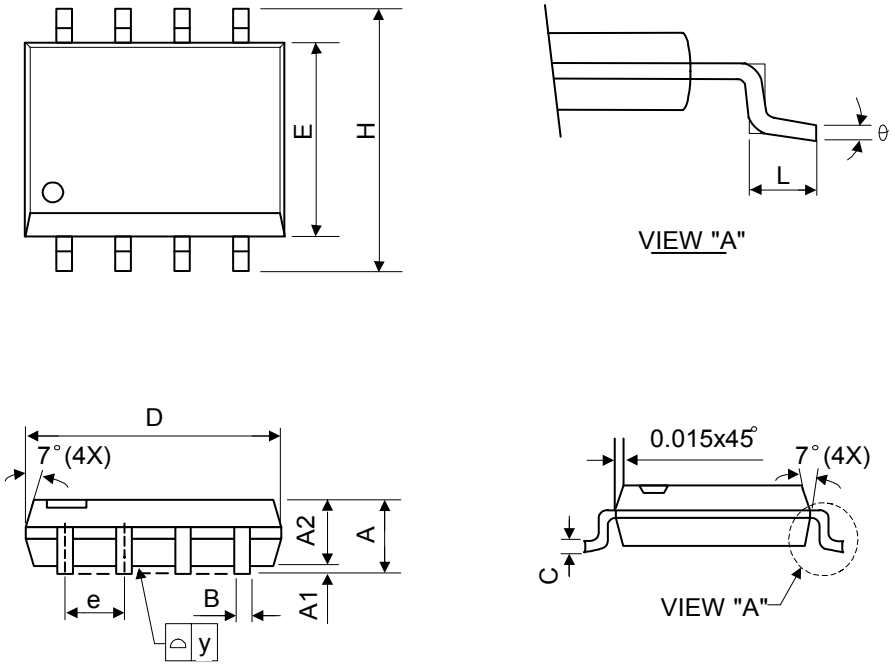
■ Package Diagrams

(1) PDIP-8L (Plastic Dual-in-line Package)



Symbol	Dimensions in millimeters			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.355	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

(2) SOP-8L (JEDEC Small Outline Package)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°

■ Marking Information