G = 0.2, Level Translation, 16-Bit ADC Driver

AD8275

FEATURES

Translates ±10 V to +4 V
Drives 16-bit SAR ADCs
Small MSOP package
Input overvoltage: +40 V to −35 V (V_S = 5 V)
Fast settling time: 450 ns to 0.001%
Rail-to-rail output
Wide supply operation: +3.3 V to +15 V
High CMRR: 80 dB
Low gain drift: 1 ppm/°C
Low offset drift: 2.5 µV/°C

APPLICATIONS

Level translator
ADC driver
Instrumentation amplifier building block
Automated test equipment

PIN CONFIGURATION

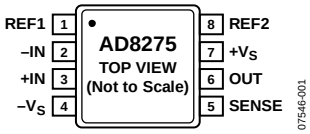

Figure 1.

TYPICAL APPLICATION

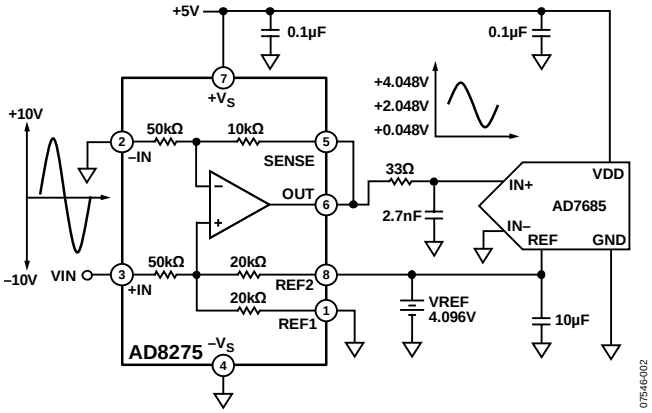

Figure 2. Translating ±10 V to 4.096 V ADC Full Scale

GENERAL DESCRIPTION

The AD8275 is a G = 0.2 difference amplifier that can be used to translate ±10 V signals to a +4 V level. It solves the problem typically encountered in industrial and instrumentation applications where ±10 V signals must be interfaced to a single-supply 4 V or 5 V ADC. The AD8275 interfaces the two signal levels, simplifying design.

The AD8275 has fast settling time of 450 ns and low distortion, making it suitable for driving medium speed successive approximation (SAR) ADCs. Its wide input voltage range and rail-to-rail outputs make it an easy to use building block. Single-supply operation reduces the power consumption of the amplifier and helps to protect the ADC from overdrive conditions.

Internal, matched, precision laser-trimmed resistors ensure low gain error, low gain drift of 1 ppm/°C (maximum), and high common-mode rejection of 80 dB. Low offset and low offset drift, combined with its fast settling time, make the AD8275 suitable for a variety of data acquisition applications where accurate and quick capture is required.

The AD8275 can be used as an analog front end, or it can follow buffers to level translate high voltages to a voltage range accepted by the ADC. In addition, the AD8275 can be configured for differential outputs if used with a differential ADC.

The AD8275 is available in a space-saving, 8-lead MSOP and is specified for performance over the −40°C to +85°C temperature range.

Table 1. Difference Amplifiers by Category

Low Distortion	High Voltage	Single-Supply Current Sense
AD8270	AD628	AD8202
AD8273	AD629	AD8203
AD8274		AD8205
AD8275		AD8206
AMP03		AD8216

Rev. A
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AD8275* Product Page Quick Links

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Comparable Parts

View a parametric search of comparable parts

Documentation

Data Sheet

- AD8275: G = 0.2, Level Translation, 16-Bit ADC Driver Data Sheet

Tools and Simulations

- AD8275 SPICE Macro Model

Reference Designs

- CN0209
- CN0213
- CN0225
- CN0352

Reference Materials

Product Selection Guide

- SAR ADC & Driver Quick-Match Guide

Solutions Bulletins & Brochures

- Test & Instrumentation Solutions Bulletin, Volume 10, Issue 3

Design Resources

- AD8275 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AD8275 EngineerZone Discussions

Sample and Buy

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Technical Support

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REVISION HISTORY

8/10—Rev. 0 to Rev. A

Changes to Figure 40 ... 14

10/08—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, G = 0.2, REF1 connected to GND and REF2 connected to 5 V, R_L = 2 kΩ connected to V_S/2, T_A = 25°C, unless otherwise noted. Specifications referred to output unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
DYNAMIC PERFORMANCE								
Small Signal Bandwidth	−3 dB	10	15		10	15		MHz
Slew Rate	4 V step	20	25		20	25		V/µs
Settling Time to 0.01%	4 V step on output, C_L = 100 pF		350			350	450	ns
Settling Time to 0.001%	4 V step on output, C_L = 100 pF		450			450	550	ns
Overload Recovery Time	50% overdrive		300			300		ns
NOISE/DISTORTION[1]								
THD + N	f = 1 kHz, V_{OUT} = 4 V p-p, 22 kHz band pass filter		106			106		dB
Voltage Noise	f = 0.1 Hz to 10 Hz, referred to output		1	4		1	4	µV p-p
Spectral Noise Density	f = 1 kHz, referred to output		40			40		nV/√Hz
GAIN	V_{REF2} = 4.096 V, REF1 and R_L connected to GND, (V_{IN+}) − (V_{IN-}) = −10 V to +10 V		0.2			0.2		V/V
Gain Error				0.024			0.024	%
Gain Drift	−40°C to +85°C		1	3		0.3	1	ppm/°C
Gain Nonlinearity	V_{OUT} = 4 V p-p, R_L = 600 Ω, 2 kΩ, 10 kΩ		2.5			2.5	3	ppm
OFFSET AND CMRR								
Offset[2]	Referred to output, V_S = ±2.5 V, reference and input pins grounded		300	700		150	500	µV
vs. Temperature	−40°C to +85°C		2.5			2.5	7	µV/°C
vs. Power Supply	V_S = 3.3 V to 5 V	90			100			dB
Reference Divider Accuracy				0.024			0.024	%
Common-Mode Rejection Ratio[3]	V_{CM} = ±10 V, referred to output	80	96		86			dB
INPUT CHARACTERISTICS								
Input Voltage Range[4]		−12.3		+12	−12.3		+12	V
Impedance[5]								
Differential	V_{CM} = V_S/2		108‖2			108‖2		kΩ‖pF
Common Mode			27.5‖2			27.5‖2		kΩ‖pF
OUTPUT CHARACTERISTICS								
Output Swing	V_{REF2} = 4.096 V, REF1 and R_L connected to GND, R_L = 2 kΩ	−V_S + 0.048		+V_S − 0.1	−V_S + 0.048		+V_S − 0.1	V
Capacitive Load[6]			100			100		pF
Short-Circuit Current Limit			30			30		mA
POWER SUPPLY								
Specified Voltage Range			5			5		V
Operating Voltage Range		3.3		15	3.3		15	V
Supply Current	I_O = 0 mA, V_S = ±2.5 V, reference and input pins grounded		1.9	2.3		1.9	2.3	mA
Over Temperature	I_O = 0 mA, V_S = ±2.5 V, reference and input pins grounded, −40°C to +85°C		2.1	2.7		2.1	2.7	mA
TEMPERATURE RANGE								
Specified Performance		−40		+85	−40		+85	°C

[1] Includes amplifier voltage and current noise, as well as noise of internal resistors.
[2] Includes input bias and offset current errors.
[3] See Figure 7 for CMRR vs. temperature.
[4] The input voltage range is a function of the voltage supplies, reference voltage, and ESD diodes. When operating on other supply voltages, see the Absolute Maximum Ratings section, Figure 11, and Table 5 for more information.
[5] Internal resistors are trimmed to be ratio matched but have ±20% absolute accuracy.
[6] See Figure 25 to Figure 28 in the Typical Performance Characteristics section for more information.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	18 V
Output Short-Circuit Current	See derating curve (Figure 3)
Voltage at +IN, –IN Pins	$-V_S + 40$ V, $+V_S - 40$ V
Voltage at REFx, $+V_S$, $-V_S$, SENSE, and OUT Pins	$-V_S - 0.5$ V, $+V_S + 0.5$ V
Current into REFx, +IN, –IN, SENSE, and OUT Pins	3 mA
Storage Temperature Range	–65°C to +130°C
Specified Temperature Range	–40°C to +85°C
Thermal Resistance (θ_{JA})	135°C/W
Package Glass Transition Temperature (T_G)	140°C
ESD Human Body Model	2 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8275 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 140°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8275. Exceeding a junction temperature of 140°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still air thermal properties of the package and PCB (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature is calculated as follows:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some of which is dissipated in the load ($V_{OUT} \times I_{OUT}$).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, the worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a 4-layer JEDEC standard board.

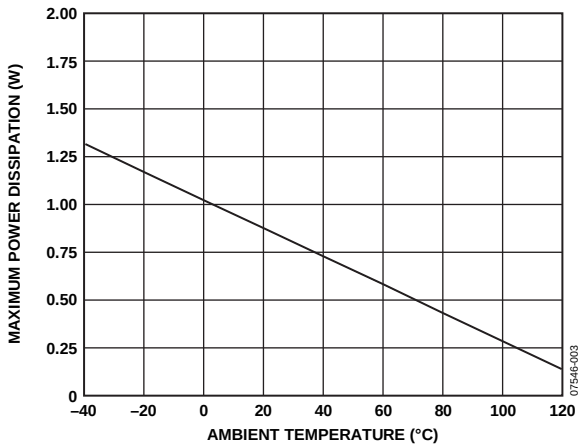

Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

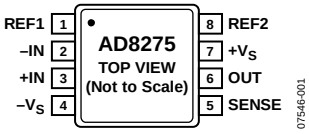

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REF1	Reference Pin. Sets the output voltage level (see the Reference section).
2	–IN	Negative Input Pin.
3	+IN	Positive Input Pin.
4	$-V_S$	Negative Supply Pin.
5	SENSE	Sense Output Pin. Tie this pin to the OUT pin.
6	OUT	Output Pin (Force Output).
7	$+V_S$	Positive Supply Pin.
8	REF2	Reference Pin. Sets the output voltage level (see the Reference section).

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, G = 0.2, REF1 connected to GND and REF2 connected to 5 V, R_L = 2 kΩ connected to V_S/2, T_A = 25°C, unless otherwise noted.

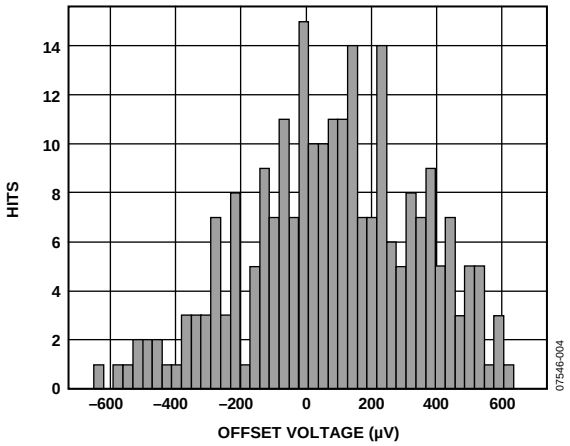

Figure 5. Typical Distribution of System Offset Voltage, Referred to Output

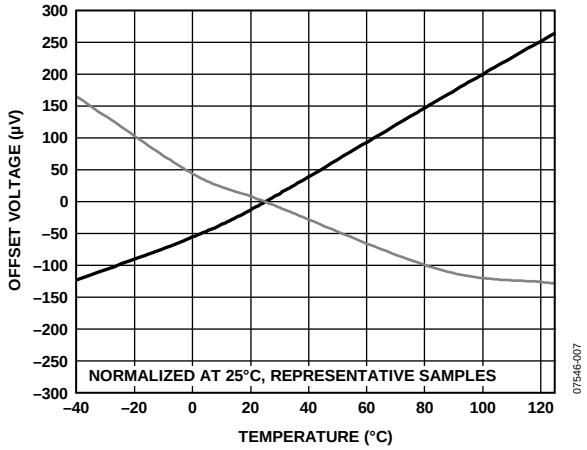

Figure 8. Offset Voltage vs. Temperature, Normalized at 25°C, Referred to Output

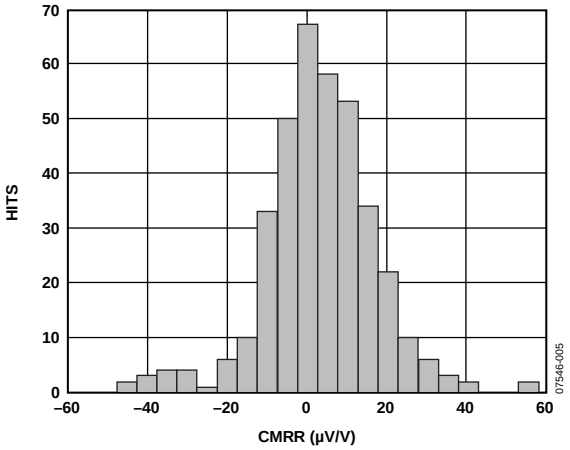

Figure 6. Typical Distribution of CMRR, Referred to Output

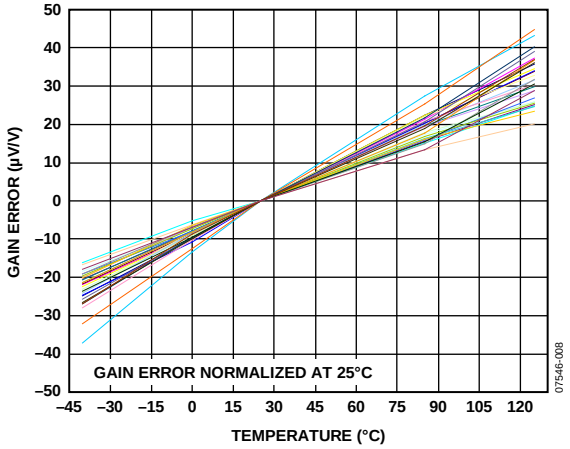

Figure 9. Gain Error vs. Temperature, Normalized at 25°C

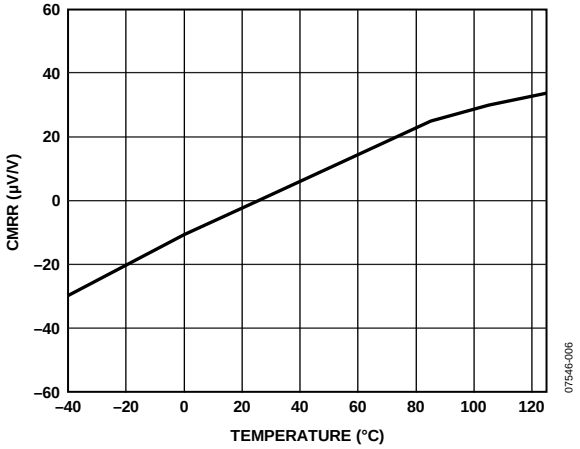

Figure 7. CMRR vs. Temperature, Normalized at 25°C

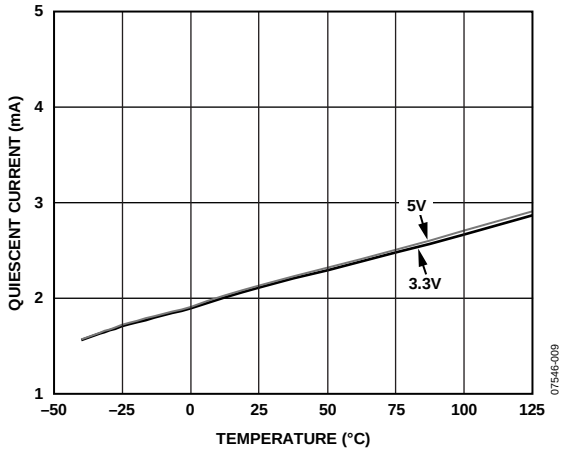

Figure 10. Quiescent Current vs. Temperature

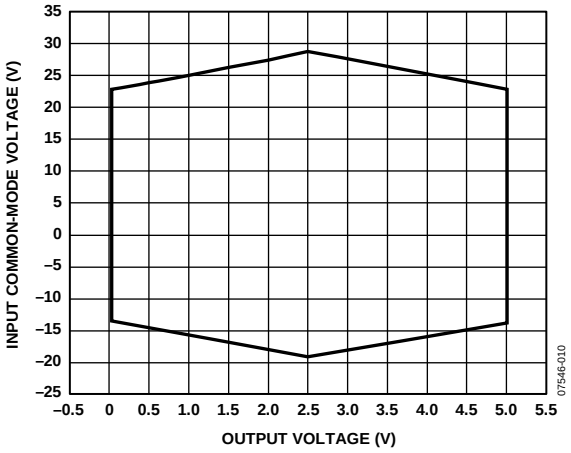

Figure 11. Input Common-Mode Voltage vs. Output Voltage, No Load

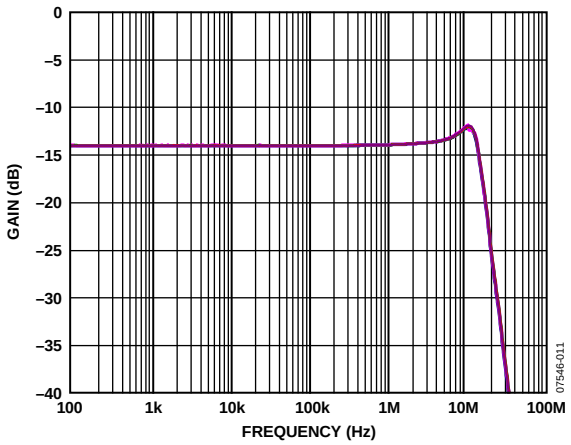

Figure 12. Gain vs. Frequency

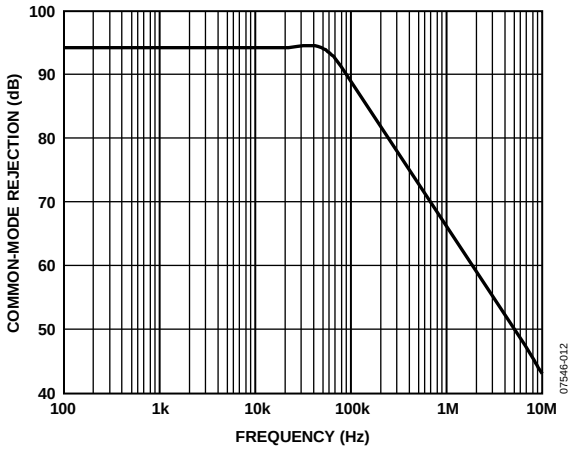

Figure 13. Common-Mode Rejection vs. Frequency, Referred to Input

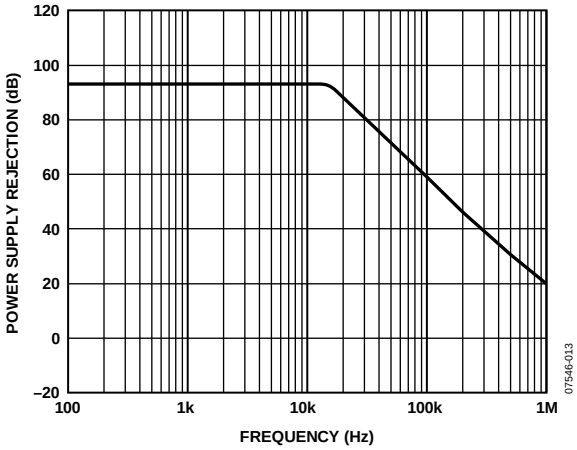

Figure 14. Power Supply Rejection vs. Frequency, Referred to Output

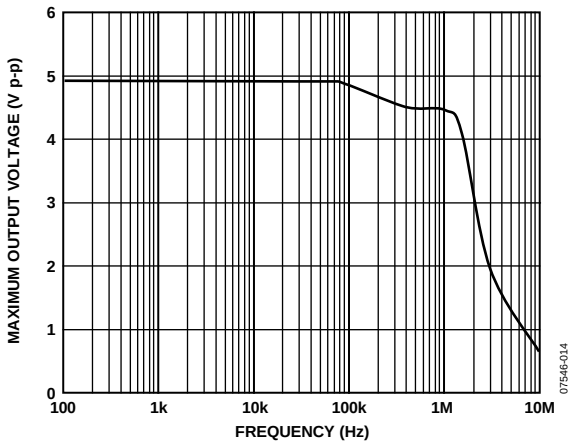

Figure 15. Maximum Output Voltage vs. Frequency

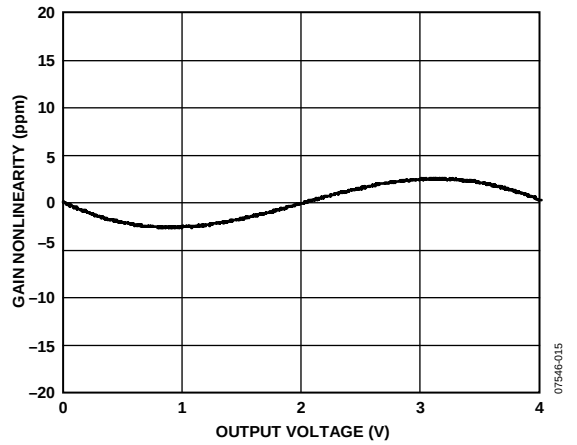

Figure 16. Gain Nonlinearity, R_L = 600 Ω, 2 kΩ, 10 kΩ

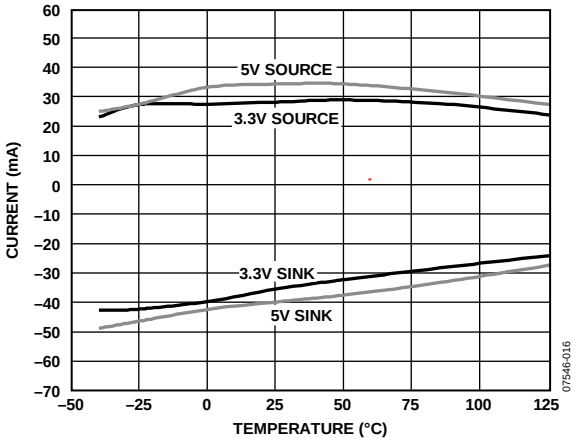

Figure 17. Short-Circuit Current vs. Temperature, V_S = 3.3 V, 5 V

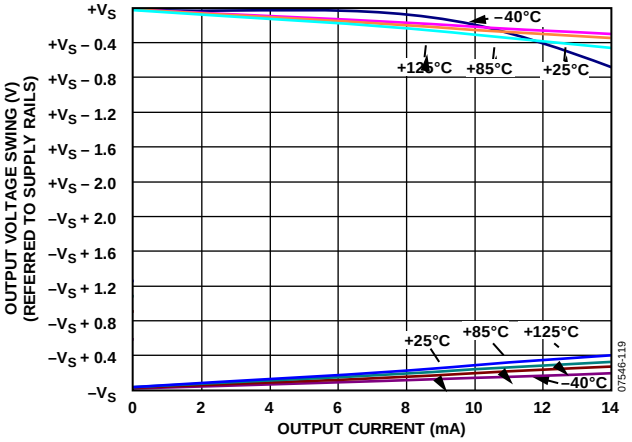

Figure 20. Output Voltage Swing vs. Output Current, V_S = 5 V

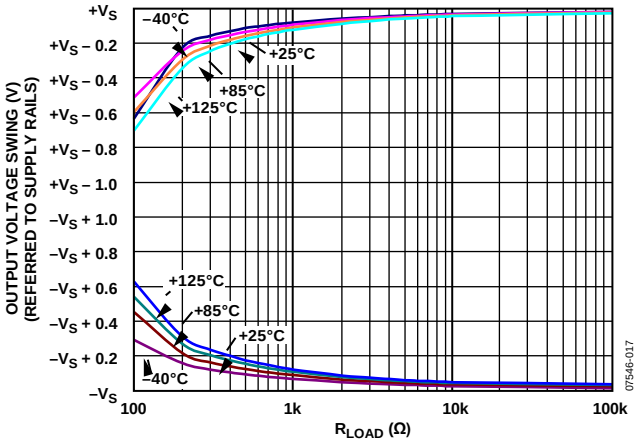

Figure 18. Output Voltage Swing vs. R_{LOAD}, V_S = 5 V

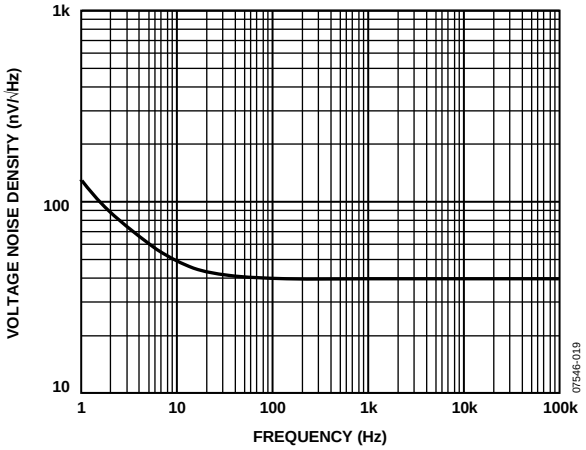

Figure 21. Voltage Noise Density vs. Frequency, Referred to Output

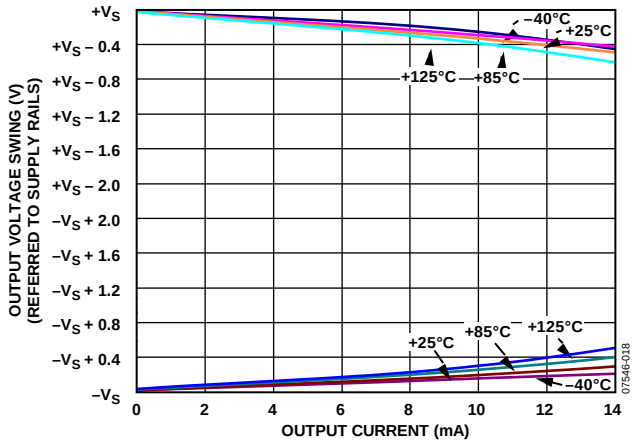

Figure 19. Output Voltage Swing vs. Output Current, V_S = 3.3 V

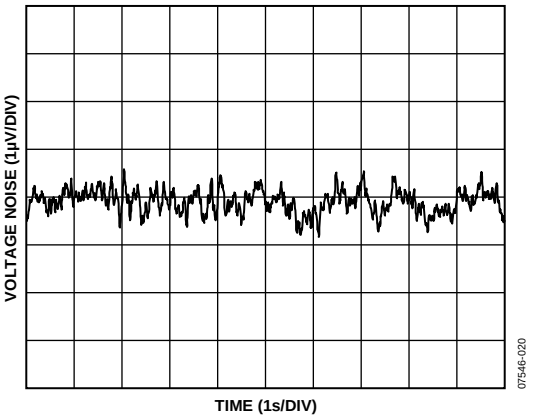

Figure 22. 0.1 Hz to 10 Hz Voltage Noise, Referred to Output

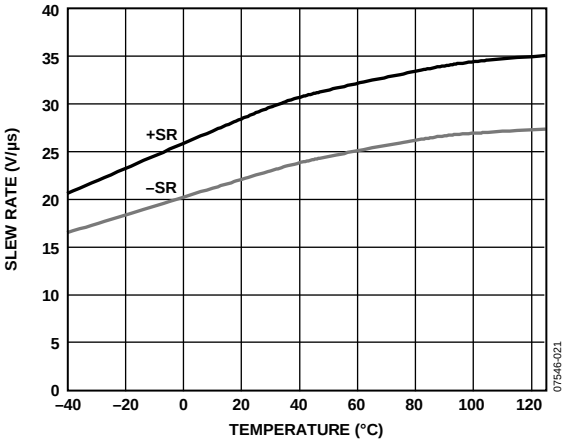

Figure 23. Slew Rate vs. Temperature

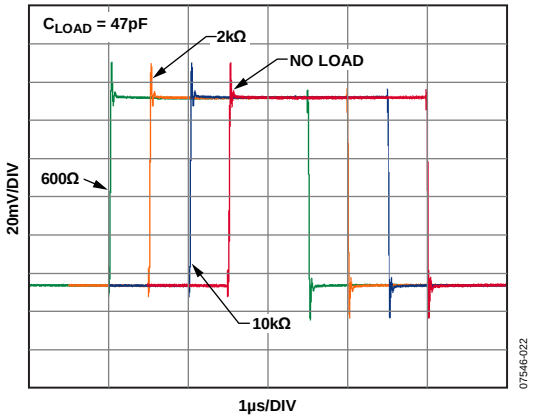

Figure 24. Small Signal Step Response for Various Resistive Loads (Step Responses Staggered for Clarity)

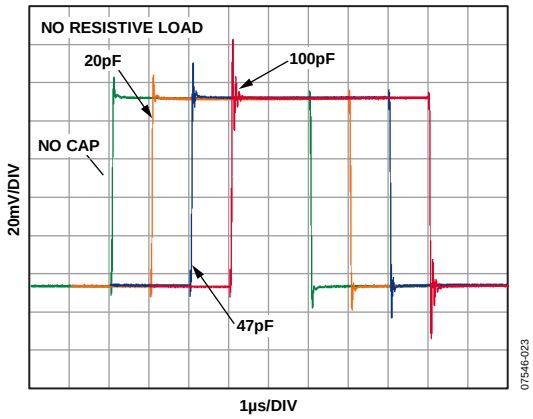

Figure 25. Small Signal Pulse Response for Various Capacitive Loads (Step Responses Staggered for Clarity)

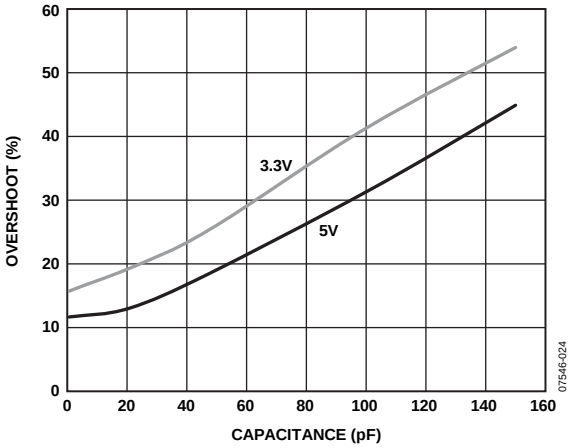

Figure 26. Small Signal Overshoot vs. Capacitive Load, No Resistive Load

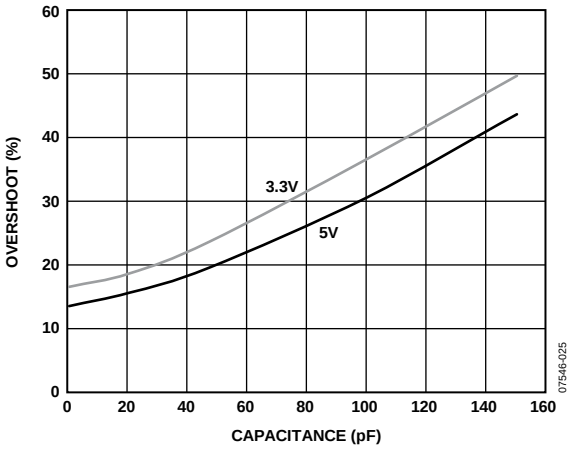

Figure 27. Small Signal Overshoot vs. Capacitive Load, 600 Ω in Parallel with Capacitive Load

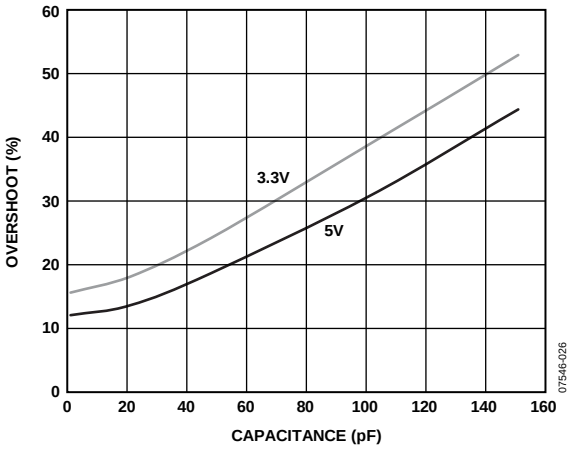

Figure 28. Small Signal Overshoot vs. Capacitive Load, 2 kΩ in Parallel with Capacitive Load

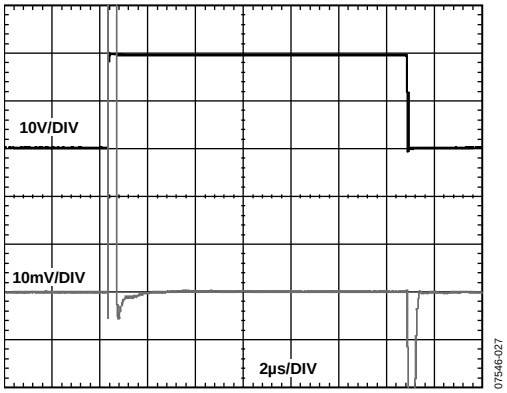

Figure 29. Large Signal Pulse Response and Settling Time, R_L = 2 kΩ

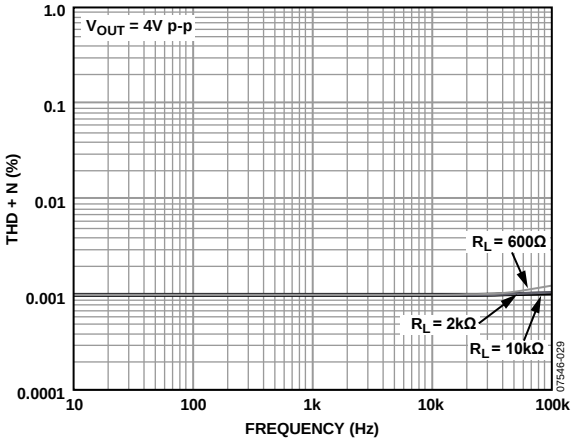

Figure 30. THD + N vs. Frequency, V_{OUT} = 4 V p-p

THEORY OF OPERATION

The AD8275 level translates ±10 V signals at its inputs to 4 V at its output. It does this by attenuating the input signal by 5. A subtractor network performs the attenuation, the level shifting, and the differential-to-single-ended conversion. One benefit of the subtractor topology is that it can accept input signals beyond its supply voltage. The subtractor is composed of tightly matched resistors. By integrating the resistors and trimming the resistor ratios, the AD8275 achieves 80 dB CMRR and 0.024% gain error.

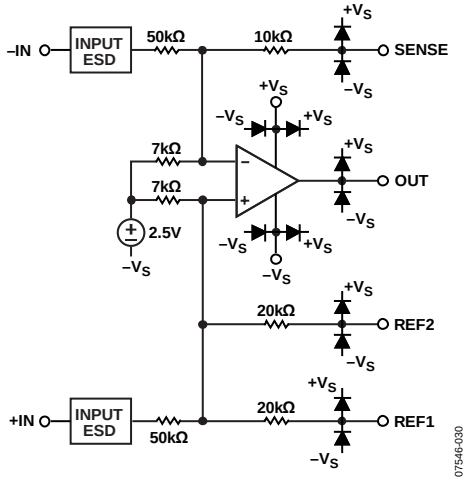

Figure 31. AD8275 Simplified Schematic

To achieve a wider input voltage range, the AD8275 uses an internal 2.5 V voltage bias tied to $-V_S$ and two 7 kΩ resistors, as shown in Figure 31. The resistors help to set the common mode of the internal amplifier. The benefit of this circuit is that it extends the input range without causing crossover distortion typical of amplifiers that have rail-to-rail complementary transistor inputs. The input range of the internal op amp is $+V_S - 0.9$ V to $-V_S + 1.35$ V.

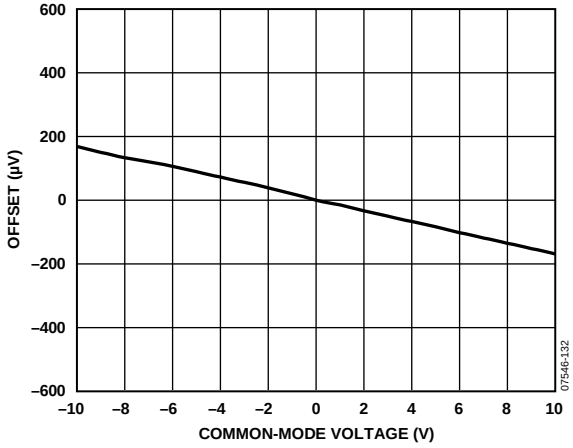

Figure 32. AD8275 Does Not Have Crossover Distortion Typical of Rail-to-Rail Input Amplifiers

The AD8275 employs a balanced, high gain, linear output stage that adaptively generates current as required, eliminating the dynamic errors found in other amplifiers. This is useful when driving SAR ADCs, which can deliver kickback current into the output of the amplifier. The result is a design that achieves low distortion, consistent bandwidth, and high slew rate.

BASIC CONNECTION

The basic configurations for the AD8275 are shown in Figure 33 and Figure 34. In Figure 33, REF1 and REF2 are tied together. A voltage, V_{REF}, applied to the tied REF1 and REF2 pins, sets the output voltage level to V_{REF}. For example, in Figure 33, if $V_{REF} = 2$ V and the inputs are tied to ground, the output remains at 2 V.

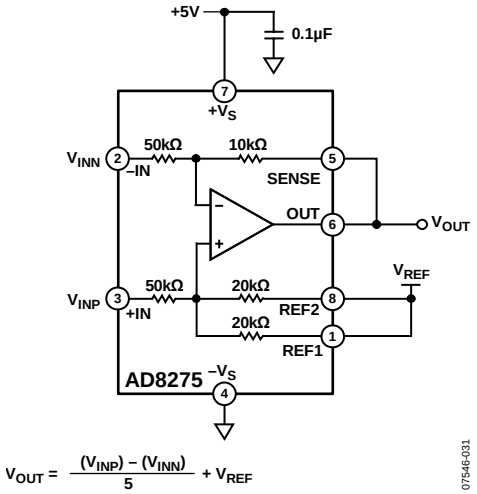

Figure 33. Basic Configuration 1: Shared Reference

In contrast, Figure 34 shows REF1 tied to ground and REF2 tied to V_{REF}. In this example, the two 20 kΩ resistors serve as a resistor divider, and V_{REF} is divided by 2. For example, if both inputs of the AD8275 are grounded and $V_{REF} = 5$ V, the output is 2.5 V.

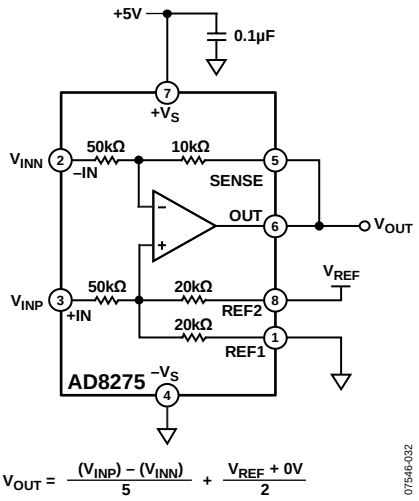

Figure 34. Basic Configuration 2: Split Reference

POWER SUPPLIES

Use a stable dc voltage to power the AD8275. Noise on the supply pins can adversely affect performance. Place a bypass capacitor of 0.1 µF between each supply pin and ground, as close to each pin as possible. A tantalum capacitor of 10 µF should also be used between each supply and ground. It can be farther away from the AD8275 and typically can be shared by other precision integrated circuits.

REFERENCE

The reference terminals are used to provide a bias level for the output. For example, in a single-supply 5 V operation, the reference terminals can be set so that the output is biased at 2.5 V. This ensures that the output can swing positive or negative around a 2.5 V level.

Figure 33 and Figure 34 illustrate two different ways to set the reference voltage. See the Basic Connection section for the differences between the two settings.

The allowable reference voltage range is a function of the common-mode input and supply voltages. The REF1 and REF2 pins should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

The REFx terminals should be driven by low source impedance because parasitic resistance in series with REF1 and REF2 can adversely affect CMRR and gain accuracy.

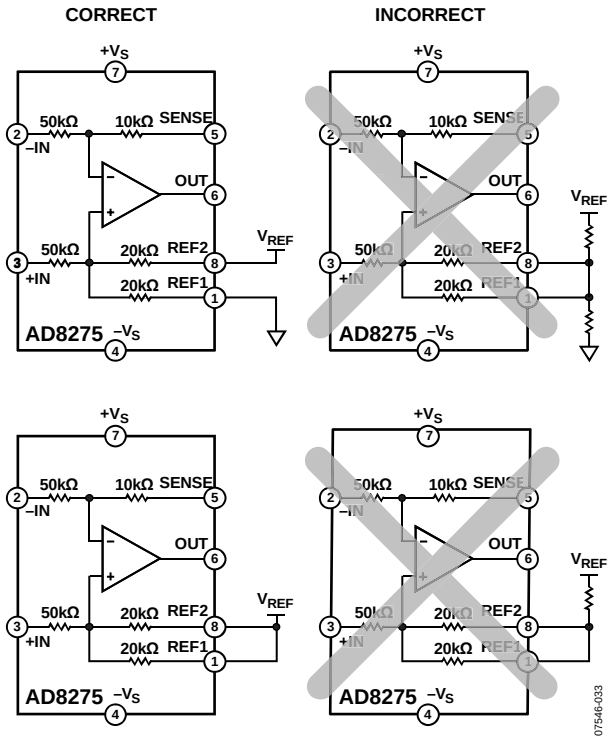

Figure 35. REF1 and REF2 Pin Guidelines

COMMON-MODE INPUT VOLTAGE RANGE

The common-mode voltage range is a function of the input voltage range of the internal op amp, the supply voltage, and the reference voltage.

Equation 1 expresses the maximum positive common-mode voltage range.

$$V_{CM_POS} \leq 13.14(+V_S) - 7.14(-V_S) - 5((REF1 + REF2)/2) - 29.69 \quad (1)$$

Equation 2 expresses the minimum common-mode voltage range.

$$V_{CM_NEG} \geq 6(-V_S) - 5((REF1 + REF2)/2) - 0.11 \quad (2)$$

The voltage range of the internal op amp varies depending on temperature. The equations reflect a typical input voltage range of $+V_S - 0.9$ V and $-V_S + 1.35$ V over temperature. Table 5 lists expected common-mode ranges for typical configurations.

Table 5. Expected Common-Mode Voltage Range for Typical Configurations

$+V_S$ (V)[1]	V_{REF1} (V)	V_{REF2} (V)	$V_{CM}+$ (V)	$V_{CM}-$ (V)
5	5	0	23.5	−12.6
5	2.5	0	29.8	−6.4
5	4.096	0	25.8	−10.4
3.3	3.3	0	5.4	−8.4
3.3	2.5	0	7.4	−6.4
5	5	5	11.0	−25.1
5	4.096	4.096	15.5	−20.6
5	3	3	21.0	−15.1
5	2.5	2.5	23.5	−12.6
5	2.048	2.048	25.8	−10.4
5	1.25	1.25	29.8	−6.4
5	0	0	36.0	−0.1

[1] $-V_S = 0$ V.

INPUT PROTECTION

The inputs of the AD8275, +IN and −IN, are protected by ESD diodes that clamp 40 V above $-V_S$ and 40 V below $+V_S$. When operating on a single +5 V supply, the ESD diode conducts at input voltages less than −35 V and greater than +40 V.

If the input voltage is expected to exceed the maximum ratings of the AD8275, use external transorbs. Adding series resistors to the inputs of the AD8275 is not recommended because the internal resistor ratios are matched to provide optimal CMRR and gain accuracy. Adding external series resistors to the input degrades the performance of the AD8275.

All other pins are protected by ESD diodes that clamp 0.5 V beyond either supply rail. For example, the voltage range of the REF1 and REF2 pins on a 5 V supply is −0.5 V to +5.5 V.

CONFIGURATIONS

Figure 36 and Figure 37, along with Table 6 and Table 7, provide examples of the possible input and output ranges for various supplies and reference voltages.

Note that Table 6 and Table 7 list the typical voltage range of the AD8275; these values do not reflect variation over process or temperature.

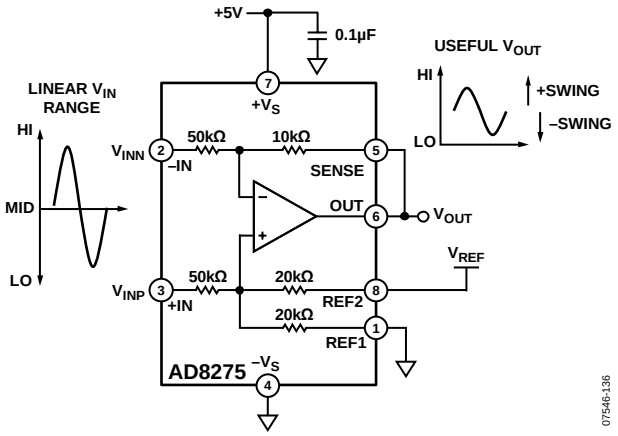

Figure 36. Split Reference

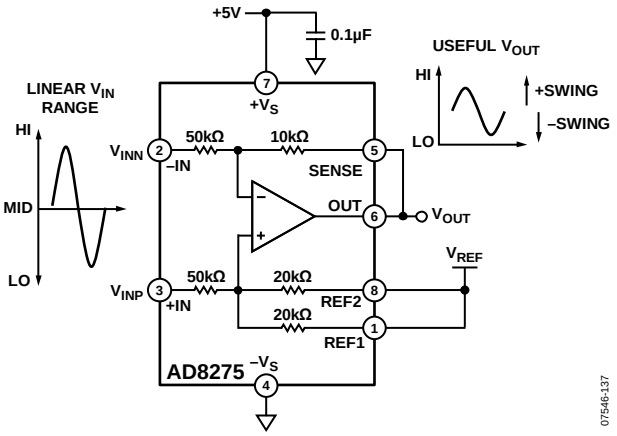

Figure 37. Shared Reference

Table 6. Input and Output Relationships for Split Reference Configuration in Figure 36

$+V_S$[1]	V_{REF}	V_{OUT} for V_{IN} = 0 V	Linear Differential V_{IN} Range	Useful V_{OUT} Ranges
5 V	5 V	2.5 V	High: +12 V Mid: 0 V Low: −12.3 V	High: +4.95 V Swing: +2.45 V, −2.455 V Low: +0.045 V
5 V	2.5 V	1.25 V	High: +18.3 V Mid: 0 V Low: −6 V	High: +4.95 V Swing: +3.7 V, −1.205 V Low: +0.045 V
5 V	4.096 V	2.048 V	High: +14.3 V Mid: 0 V Low: −10 V	High: +4.95 V Swing: +2.902 V, −2.003 V Low: +0.045 V
3.3 V	3.3 V	1.65 V	High: +8 V Mid: 0 V Low: −8 V	High: +3.24 V Swing: +1.59 V, −1.605 V Low: +0.045 V
3.3 V	2.5 V	1.25 V	High: +10 V Mid: 0 V Low: −6 V	High: +3.24 V Swing: +1.99 V, −1.205 V Low: +0.045 V

[1] $-V_S$ = 0 V.

Table 7. Input and Output Relationships for Shared Reference Configuration in Figure 37

$+V_S$[1]	V_{REF}	V_{OUT} for V_{IN} = 0 V	Linear Differential V_{IN} Range	Useful V_{OUT} Ranges
5 V	5 V	5 V	High: −0.1 V Mid: 0 V Low: −24.7 V	High: +4.98 V Swing: −4.94 V Low: +0.06 V
5 V	4.096 V	4.096 V	High: +4.4 V Mid: 0 V Low: −20.2 V	High: +4.98 V Swing: +0.884 V to −4.03 V Low: +0.06 V
5 V	3 V	3 V	High: +9.5 V Mid: 0 V Low: −14.8 V	High: +4.95 V Swing: +1.9 V, −2.955 V Low: +0.045 V
5 V	2.5 V	2.5 V	High: +12 V Mid: 0 V Low: −12.3 V	High: +4.95 V Swing: +2.45 V, −2.455 V Low: +0.045 V
5 V	2.048 V	2.048 V	High: +14.3 V Mid: 0 V Low: −10 V	High: +4.95 V Swing: +2.902 V, −2.003 V Low: +0.045 V
5 V	1.25 V	1.25 V	+18.3 V to −6 V	High: +4.95 V Swing: +3.7 V, −1.205 V Low: +0.045 V
0 V	0 V	0 V	24.5 V to 0.2 V	High: 4.95 V Swing: 4.95 V Low: 0.045 V

[1] $-V_S$ = 0 V.

APPLICATIONS INFORMATION

DRIVING A SINGLE-ENDED ADC

The AD8275 provides the common-mode rejection that SAR ADCs often lack. In addition, it enables designers to use cost-effective, precision, 16-bit ADCs such as the AD7685, yet still condition ±10 V signals.

One important factor in selecting an ADC driver is its ability to settle within the acquisition window of the ADC. The AD8275 is able to drive medium speed SAR ADCs.

In Figure 38, the 2.7 nF capacitor serves to store and deliver necessary charge to the switched capacitor input of the ADC. The 33 Ω series resistor reduces the burden of the 2.7 nF load from the amplifier and isolates it from the kickback current injected from the switched capacitor input of the AD7685. The output impedance of the amplifier can affect the THD of the ADC. In this case, the combined impedance of the 33 Ω resistor and the output impedance of the AD8275 provides extremely low THD of −112 dB. Figure 39 shows the ac response of the AD8275 driving the AD7685.

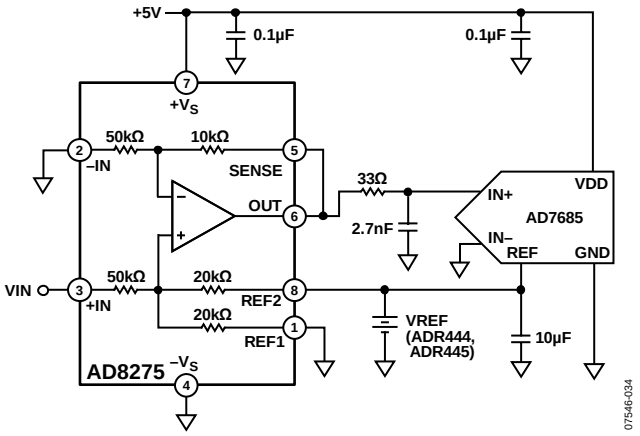

Figure 38. Driving a Single-Ended ADC

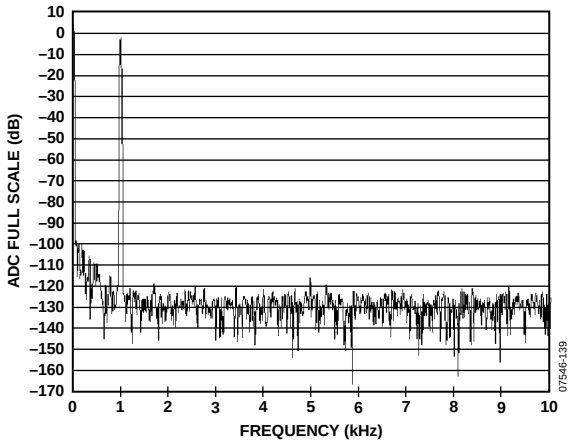

Figure 39. FFT of AD8275 Directly Driving the AD7685 Using the 5 V Reference of the Evaluation Board (Input = 20 V p-p, 1 kHz, THD = −112 dB)

The AD8275 can condition signals for higher resolution ADCs such as 18-bit SAR converters, provided that a narrower bandwidth is sampled to limit noise.

DIFFERENTIAL OUTPUTS

In certain applications, it is necessary to create a differential signal. For example, high resolution ADCs often require a differential input. In other cases, transmission over a long distance can require differential signals for better immunity to interference.

Figure 40 shows how to configure the AD8275 to output a differential signal. The AD8655 op amp is used in an inverting topology to create a differential voltage. VREF sets the output midpoint. Errors from the op amp are common to both outputs and are thus common mode. Likewise, errors from using mismatched resistors cause a common-mode dc offset error. Such errors are rejected in differential signal processing by differential input ADCs or by instrumentation amplifiers.

When using this circuit to drive a differential ADC, V_{REF} can be set using a resistor divider from the ADC reference to make the output ratiometric with the ADC.

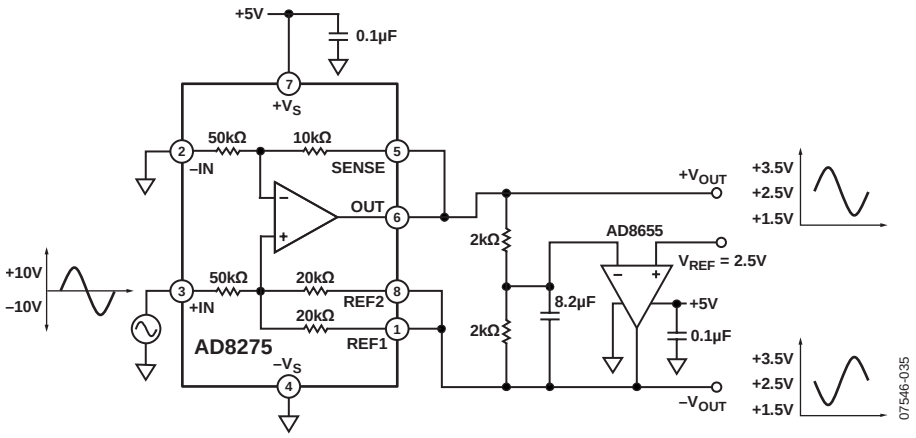

Figure 40. AD8275 Configured for Differential Output (for Driving a Differential ADC)

INCREASING INPUT IMPEDANCE

In applications where a high input impedance is needed, low input bias current op amps can be used to buffer the AD8275. In Figure 41, an AD8620 is used to provide high input impedance. Input bias current is limited to 10 pA.

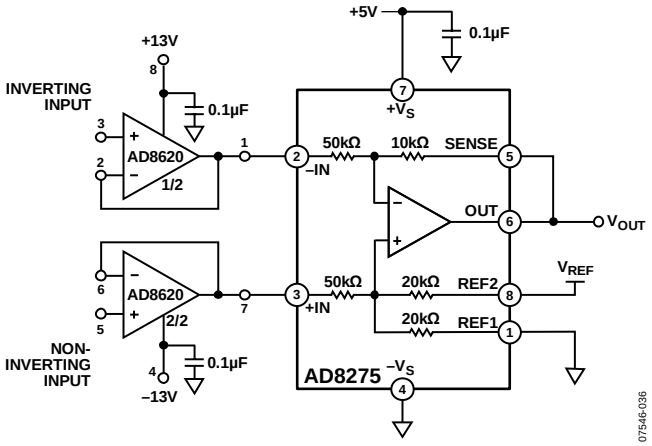

Figure 41. Adding Op Amp Buffers for High Input Impedance

AC COUPLING

An integrator can be tied to the AD8275 in feedback to create a high-pass filter as shown in Figure 42. This circuit can be used to reject dc voltages and offsets. At low frequencies, the impedance of the capacitor, C, is high. Thus, the gain of the integrator is high. DC voltage at the output of the AD8275 is inverted and gained by the integrator. The inverted signal is injected back into the REFx pins, nulling the output. In contrast, at high frequencies, the integrator has low gain because the impedance of C is low. Voltage changes at high frequencies are inverted but at a low gain. The signal is injected into the REFx pins but it is not enough to null the output. High frequency signals are, therefore, allowed to pass.

When a signal exceeds $f_{HIGH\text{-}PASS}$, the AD8275 outputs the conditioned input signal.

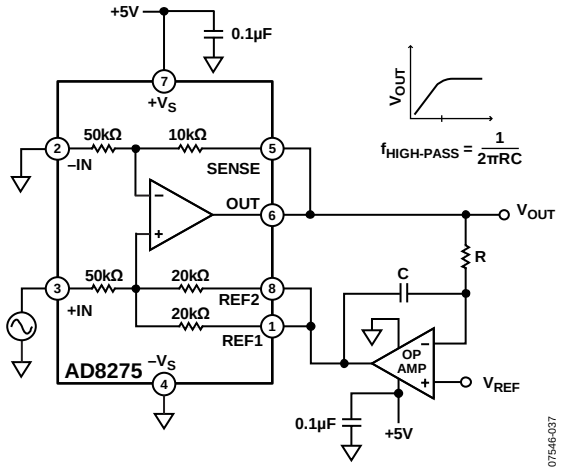

Figure 42. AC-Coupled Level Translator

USING THE AD8275 AS A LEVEL TRANSLATOR IN A DATA ACQUISITION SYSTEM

Signal size varies dramatically in some data acquisition applications. Instrumentation amplifiers, such as the AD8253, AD8228, or AD8221, are often used at the inputs to provide CMRR and high input impedance. However, the instrumentation amplifiers output ±10 V signals and the ADC full scale is 5 V or 4.096 V. In Figure 43, the AD8275 serves as a level translator between the in-amp and the ADC. The AD8275, along with the AD8228 and the AD8253, have very low gain drift because all gain setting resistors are internal and laser-trimmed.

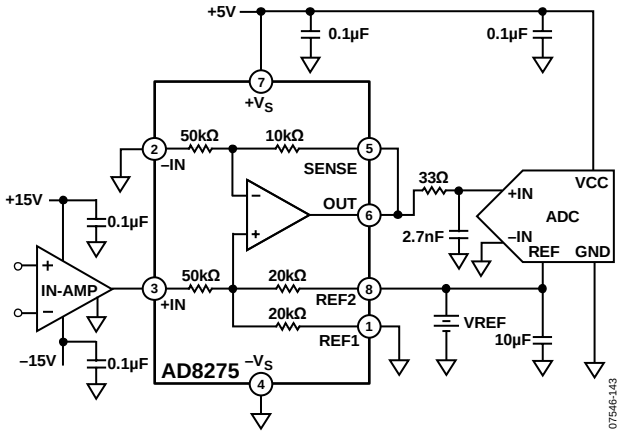

Figure 43. Level Translation in a Data Acquisition System

OUTLINE DIMENSIONS

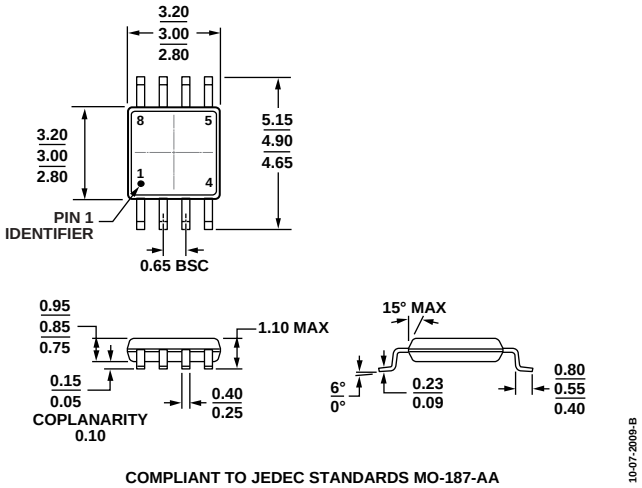

Figure 44. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8275ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	Y13
AD8275ARMZ-R7	−40°C to +85°C	8-Lead MSOP, 7″ Tape and Reel	RM-8	Y13
AD8275ARMZ-RL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y13
AD8275BRMZ	−40°C to +85°C	8-Lead MSOP	RM-8	Y1V
AD8275BRMZ-R7	−40°C to +85°C	8-Lead MSOP, 7″ Tape and Reel	RM-8	Y1V
AD8275BRMZ-RL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y1V

[1] Z = RoHS Compliant Part.

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