128 Channel, 24-bit Current to Digital ADC

Preliminary Technical Data

ADAS1128

FEATURES

128 Channel low level currents- to-digital converter
Up to 24 bit resolution
Up to 20ksps (50µs integration time)
Simultaneous Sampling
Ultra Low noise (down to 0.4fC (2500e$^-$))
User adjustable full-scale range
INL: ±0.025% of Reading ±1ppm of FSR
Very Low Power dissipation: 4.5 mW/channel
LVDS/CMOS self-clocked serial interface
Daisy-chain Configuration registers
On-Board Temperature Sensor and Reference Buffer
Mini-BGA package 10mm × 10mm
Low-cost external components

APPLICATIONS

CT Scanner Data Acquisition
Photodiode Sensors and Power Monitoring
Spectroscopy
High Channel Count Data Acquisition Systems (current or voltage input)

SUPPORT TOOLS

Evaluation Board
Reference Design with reference layout (3 layers)
FPGA Verilog Code

GENERAL DESCRIPTION

The ADAS1128 is a 128-Channel, current to digital analog-to-digital converter ADC. It contains 128 low power, low noise, low input current integrators, simultaneous sample-holds and two high speed, high resolution ADCs with configurable sampling rate and resolution up to 24 bits.

All converted channel results are output on a single LVDS self-clocked serial interface reducing external hardware.

An SPI-compatible serial interface allows configuration of the ADC using the SDI input. The SDO output allows one to daisy chain several ADCs on a single, 3-wire bus. It uses the separate supply VIO to reduce digital noise effect on the conversions.

The ADAS1128 is housed in a mini-BGA package, 10mm by 10mm.

FUNCTIONAL BLOCK DIAGRAM

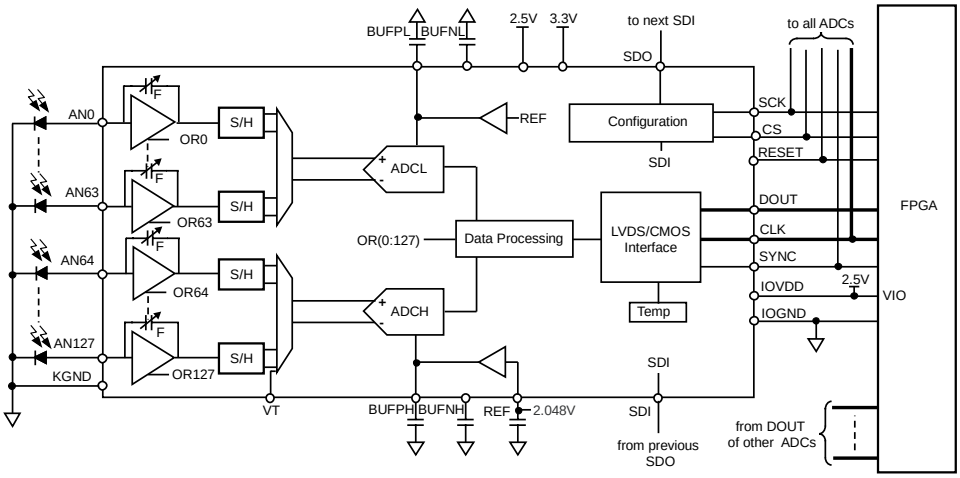

Figure 1. General Block Diagram

For more information about the ADAS1128, contact Analog Devices, Inc., at adas@analog.com

Rev PrE

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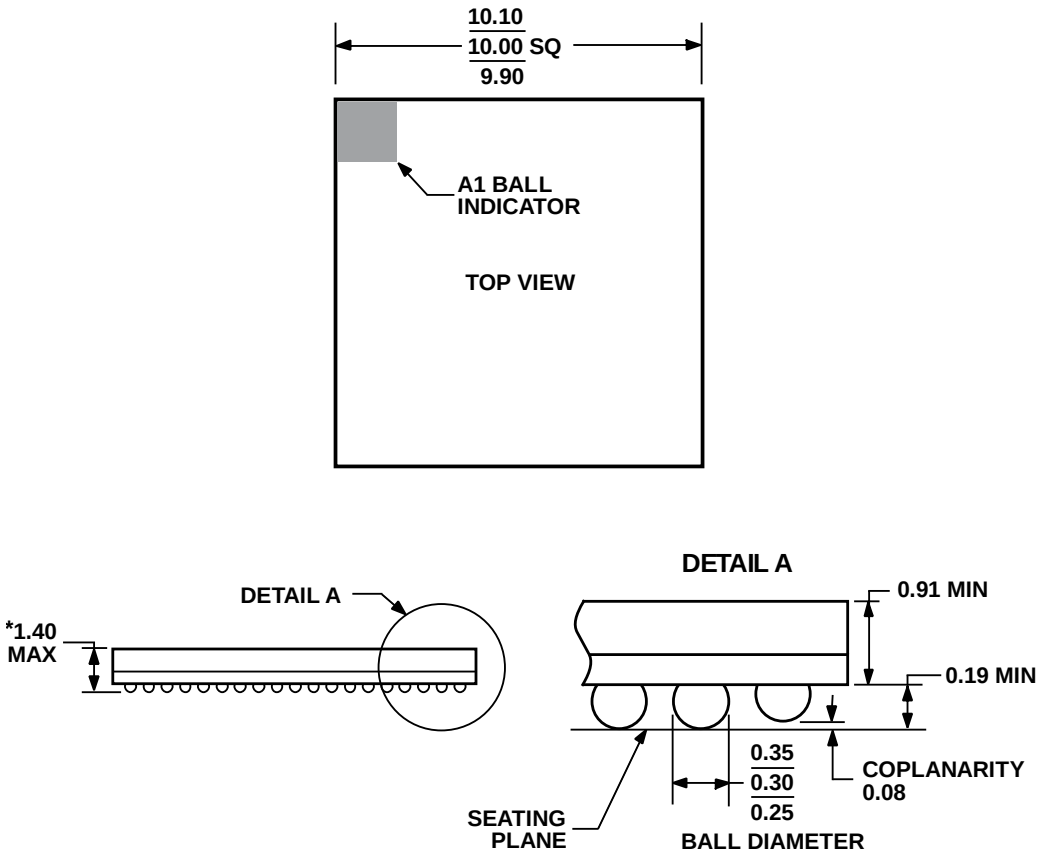
Outline Dimensions



***COMPLIANT TO JEDEC STANDARDS MO-225 WITH EXCEPTION TO PACKAGE HEIGHT.**

Figure 2 242-Ball Chip Scale Package Ball Grid Array [CSP-BGA] (BC-242)
Dimensions shown in millimeters

NOTES