3 V Dual-Loop 50 Mbps to 1.25 Gbps Laser Diode Driver

ADN2848

FEATURES

50 Mbps to 1.25 Gbps Operation
Single 3.3 V Operation
Bias Current Range 2 mA to 100 mA
Modulation Current Range 5 mA to 80 mA
Monitor Photo Diode Current 50 μA to 1200 μA
50 mA Supply Current at 3.3 V
Closed-Loop Control of Power and Extinction Ratio
Full Current Parameter Monitoring
Laser Fail and Laser Degrade Alarms
Automatic Laser Shutdown, ALS
Optional Clocked Data
Supports FEC Rates
32-Lead (5 mm × 5 mm) LFCSP Package

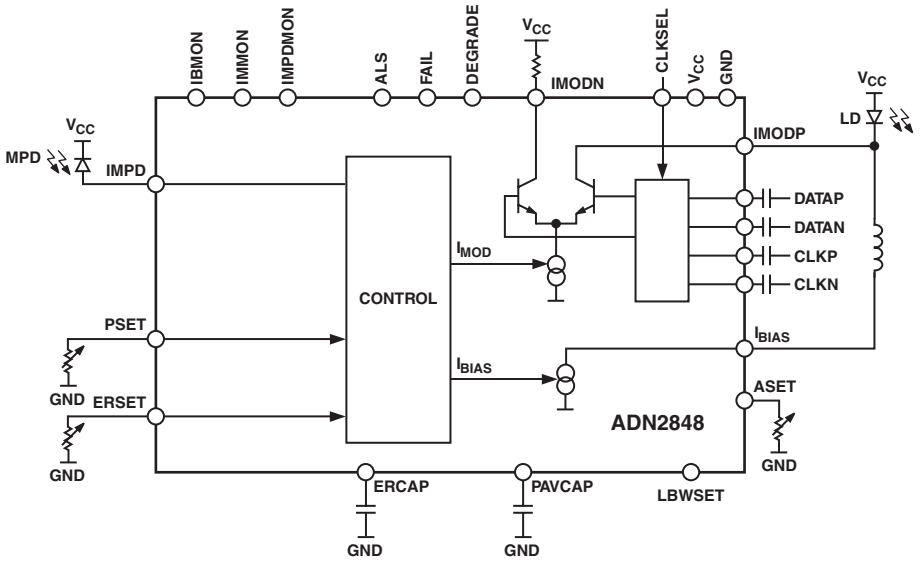
APPLICATIONS

SONET OC-1/3/12
SDH STM-0/1/4
Fibre Channel
Gigabit Ethernet

GENERAL DESCRIPTION

The ADN2848 uses a unique control algorithm to control both the average power and extinction ratio of the laser diode, LD, after initial factory setup. External component count and PCB area are low as both power and extinction ratio control are fully integrated. Programmable alarms are provided for laser fail (end of life) and laser degrade (impending fail).

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADN2848–SPECIFICATIONS (V_{CC} = 3.0 V to 3.6 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1] Typical values as specified at 25°C.)

Parameter	Min	Typ	Max	Unit	Conditions/Comments
LASER BIAS (BIAS)					
Output Current I_{BIAS}	2		100	mA	
Compliance Voltage	1.2		V_{CC}	V	
I_{BIAS} During ALS			0.1	mA	
ALS Response Time			5	μs	I_{BIAS} < 10% of nominal
CCBIAS Compliance Voltage	1.2		V_{CC}	V	
MODULATION CURRENT (IMODP, IMODN)					
Output Current I_{MOD}	5		80	mA	
Compliance Voltage	1.5		V_{CC}	V	
I_{MOD} During ALS			0.1	mA	
Rise Time[2]		80	170	ps	
Fall Time[2]		80	170	ps	
Random Jitter[2]		1	1.5	ps	RMS
Pulsewidth Distortion[2]		15		ps	I_{MOD} = 40 mA
MONITOR PD (MPD)					
Current	50		1200	μA	Average Current
Compliance Voltage			1.65	V	
POWER SET INPUT (PSET)					
Capacitance			80	pF	
Monitor Photodiode Current into RPSET Resistor	50		1200	μA	Average Current
Voltage	1.1	1.2	1.3	V	
EXTINCTION RATIO SET INPUT (ERSET)					
Allowable Resistance Range	1.2		25	kΩ	
Voltage	1.1	1.2	1.3	V	
ALARM SET (ASET)					
Allowable Resistance Range	1.2		25	kΩ	
Voltage	1.1	1.2	1.3	V	
Hysteresis		5		%	
CONTROL LOOP					Low Loop Bandwidth Selection
Time Constant		0.22		s	LBWSET = GND
		2.25		s	LBWSET = V_{CC}
DATA INPUTS (DATAP, DATAN, CLKP, CLKN)[3]					
V p-p (Single-Ended, Peak-to-Peak)	100		500	mV	Data and Clock Inputs Are
Input Impedance (Single-Ended)		50		Ω	AC-Coupled
t_{SETUP}[4] (see Figure 1)	50			ps	
t_{HOLD}[4] (see Figure 1)	100			ps	
LOGIC INPUTS (ALS, LBWSET, CLKSEL)					
V_{IH}	2.4			V	
V_{IL}			0.8	V	
ALARM OUTPUTS (Internal 30 kΩ Pull-Up)					
V_{OH}	2.4			V	
V_{OL}			0.8	V	
IBMON, IMMON, IMPDMON					
IMMON Division Ratio		100		A/A	
IMPDMON		1		A/A	
Compliance Voltage	0		V_{CC} – 1.2	V	
SUPPLY					
I_{CC}[5]		50		mA	I_{BIAS} = I_{MOD} = 0
V_{CC}[6]	3.0	3.3	3.6	V	

NOTES

[1]Temperature range is as follows: –40°C to +85°C.

[2]Measured into a 25 Ω load using a 0-1 pattern at 622 Mbps.

[3]When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows in the IMODP pin.

[4]Guaranteed by design and characterization. Not production tested.

[5]I_{CCMIN} for power calculation on page 6 is the typical I_{CC} given.

[6]All V_{CC} pins should be shorted together.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{CC} to GND . . . . . 4.2 V
Digital Inputs
(ALS, LBWSET, CLKSEL) . . . . . –0.3 V to V_{CC} + 0.3 V
IMODN, IMODP . . . . . V_{CC} + 1.2 V
Operating Temperature Range
Industrial . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J max) . . . . . 150°C
32-Lead LFCSP Package
Power Dissipation[2] . . . . . (T_J max – T_A)/θ_{JA} W
θ_{JA} Thermal Impedance[3] . . . . . 32°C/W
Lead Temperature (Soldering for 10 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Power consumption formulae are provided on Page 6.

[3]θ_{JA} is defined when device is soldered in a 4-layer board.

ORDERING GUIDE

Model	Temperature Range	Package Description
ADN2848ACP-32	–40°C to +85°C	32-Lead LFCSP
ADN2848ACP-32-RL	–40°C to +85°C	32-Lead LFCSP
ADN2848ACP-32-RL7	–40°C to +85°C	32-Lead LFCSP

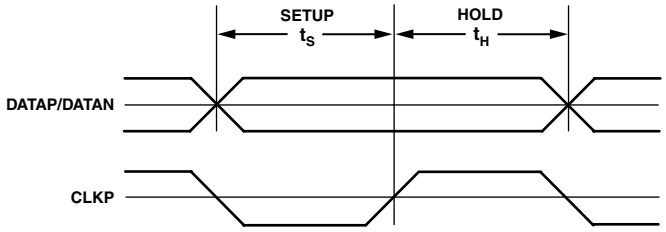
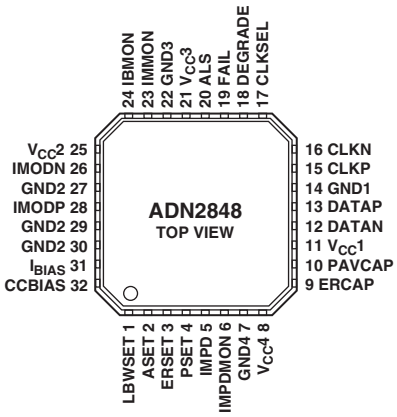


Figure 1. Setup and Hold Time

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2848 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1	LBWSET	Loop Bandwidth Select
2	ASET	Alarm Threshold Set Pin
3	ERSET	Extinction Ratio Set Pin
4	PSET	Average Optical Power Set Pin
5	IMPD	Monitor Photodiode Input
6	IMPDMON	Mirrored Current from Monitor Photodiode—Current Source
7	GND4	Supply Ground
8	$V_{CC}4$	Supply Voltage
9	ERCAP	Extinction Ratio Loop Capacitor
10	PAVCAP	Average Power Loop Capacitor
11	$V_{CC}1$	Supply Voltage
12	DATAN	Data Negative Differential Terminal
13	DATAP	Data Positive Differential Terminal
14	GND1	Supply Ground
15	CLKP	Data Clock Positive Differential Terminal, Used if CLKSEL = V_{CC}
16	CLKN	Data Clock Negative Differential Terminal, Used if CLKSEL = V_{CC}
17	CLKSEL	Clock Select (Active = V_{CC}), Used if Data Is Clocked into Chip
18	DEGRADE	DEGRADE Alarm Output
19	FAIL	FAIL Alarm Output
20	ALS	Automatic Laser Shutdown
21	$V_{CC}3$	Supply Voltage
22	GND3	Supply Ground
23	IMMON	Modulation Current Mirror Output—Current Source
24	IBMON	Bias Current Mirror Output—Current Source
25	$V_{CC}2$	Supply Voltage
26	IMODN	Modulation Current Negative Output, Connect via Matching Resistor to V_{CC}
27	GND2	Supply Ground
28	IMODP	Modulation Current Positive Output, Connect to Laser Diode
29	GND2	Supply Ground
30	GND2	Supply Ground
31	I_{BIAS}	Laser Diode Bias Current Output
32	CCBIAS	Extra Laser Diode Bias When AC-Coupled—Current Sink

GENERAL

Laser diodes have current-in to light-out transfer functions as shown in Figure 2. Two key characteristics of this transfer function are the threshold current, I_{TH}, and slope in the linear region beyond the threshold current, referred to as slope efficiency, LI.

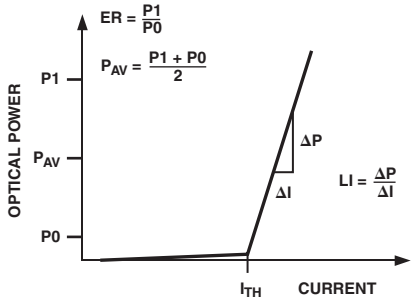


Figure 2. Laser Transfer Function

Control

A monitor photodiode, MPD, is required to control the LD. The MPD current is fed into the ADN2848 to control the power and extinction ratio, continuously adjusting the bias current and modulation current in response to the laser's changing threshold current and light-to-current slope efficiency.

The ADN2848 uses automatic power control, APC, to maintain a constant average power over time and temperature.

The ADN2848 uses closed-loop extinction ratio control to allow optimum setting of extinction ratio for every device. Thus SONET/SDH interface standards can be met over device variation, temperature, and laser aging. Closed-loop modulation control eliminates the need to either overmodulate the LD or include external components for temperature compensation. This reduces research and development time and second sourcing issues caused by characterizing LDs.

Average power and extinction ratio are set using the PSET and ERSET pins, respectively. Potentiometers are connected between these pins and ground. The potentiometer R_{PSET} is used to change the average power. The potentiometer R_{ERSET} is used to adjust the extinction ratio. Both PSET and ERSET are kept 1.2 V above GND.

For an initial setup, R_{PSET} and R_{ERSET} potentiometers may be calculated using the following formulas.

$$R_{PSET} = \frac{1.2\ V}{I_{AV}}\ (\Omega)$$

$$R_{ERSET}\ \frac{1.2V}{\frac{I_{MPD\_CW}}{P_{CW}} \times \frac{ER-1}{ER+1} \times P_{AV}}\ (\Omega)$$

where:
I_{AV} is the average MPD current.
P_{CW} is the dc optical power specified on the laser data sheet.
I_{MPD_CW} is the MPD current at that specified P_{CW}.
P_{AV} is the average power required.
ER is the desired extinction ratio (ER = P1/P0).

Note that I_{ERSET} and I_{PSET} will change from device to device; however, the control loops will determine the actual values. It is not required to know the exact values for LI or MPD optical coupling.

Loop Bandwidth Selection

For continuous operation, the user should hardwire the LBWSET pin high and use 1 µF capacitors to set the actual loop bandwidth. These capacitors are placed between the PAVCAP and ERCAP pins and ground. It is important that these capacitors are low leakage multilayer ceramics with an insulation resistance greater than 100 GΩ or a time constant of 1,000 sec, whichever is less.

Operation Mode	LBWSET	Recommended PAVCAP	Recommended ERCAP
Continuous 50 Mbps to 1.25 Gbps	High	1 µF	1 µF
Optimized for 1.25 Gbps	Low	47 nF	47 nF

Setting LBSET low and using 47 nF capacitors results in a shorter loop time constant (a 10× reduction over using 1 µF capacitors and keeping LBWSET high).

Alarms

The ADN2848 is designed to allow interface compliance to ITU-T-G958 (11/94) section 10.3.1.1.2 (transmitter fail) and section 10.3.1.1.3 (transmitter degrade). The ADN2848 has two active high alarms, DEGRADE and FAIL. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 100:1 to the FAIL alarm threshold. The DEGRADE alarm will be raised at 90% of this level.

Example:

$$I_{FAIL} = 50\ mA\ \ so\ \ I_{DEGRADE} = 45\ mA$$

$$I_{ASET} = \frac{I_{FAIL}}{100} = \frac{50\ mA}{100} = 500\ \mu A$$

$$*R_{ASET} = \frac{1.2V}{I_{ASET}} = \frac{1.2}{500\,\mu A} = 2.4\ k\Omega$$

*The smallest valid value for R_{ASET} is 1.2 kΩ, since this corresponds to the I_{BIAS} maximum of 100 µA.

The laser degrade alarm, DEGRADE, is provided to give a warning of imminent laser failure if the laser diode degrades further or environmental conditions continue to stress the LD, such as increasing temperature.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH compliant. This occurs when one of the following conditions arise:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resulting in the MPD current dropping to zero. This gives closed-loop feedback to the system that ALS has been enabled.

DEGRADE will be raised only when the bias current exceeds 90% of ASET current.

Monitor Currents
IBMON, IMMON, and IMPDMON are current controlled current sources from V_{CC}. They mirror the bias, modulation, and MPD current for increased monitoring functionality. An external resistor to GND gives a voltage proportional to the current monitored.

If the monitoring function IMPDMON is not required, the IMPD pin must be grounded and the monitor photodiode output must be connected directly to the PSET pin.

Data and Clock Inputs
Data and clock inputs are ac-coupled (10 nF capacitors recommended) and terminated via a 100 Ω internal resistor between DATAP and DATAN and also between the CLKP and CLKN pins. There is a high impedance circuit to set the common-mode voltage, which is designed to allow for maximum input voltage headroom over temperature. It is necessary that ac coupling be used to eliminate the need for matching between common-mode voltages.

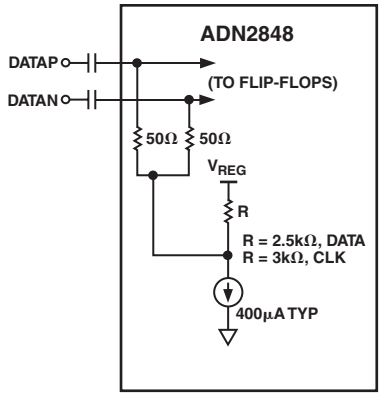


Figure 3. AC Coupling of Data Inputs

For input signals that exceed 500 mV p-p single-ended, it is necessary to insert an attenuation circuit as shown in Figure 4.

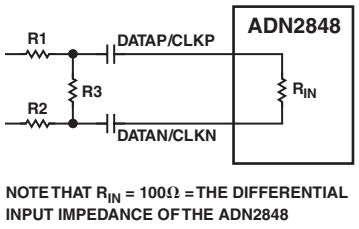


Figure 4. Attenuation Circuit

CCBIAS
When the laser is used in ac-coupled mode, the CCBIAS and the I_{BIAS} pins should be tied together (see Figure 7). In dc-coupled mode, CCBIAS should be tied to V_{CC}.

Automatic Laser Shutdown
The ADN2848 ALS allows compliance to ITU-T-G958 (11/94), section 9.7. When ALS is logic high, both bias and modulation currents are turned off. Correct operation of ALS can be confirmed by the FAIL alarm being raised when ALS is asserted. Note that this is the only time that DEGRADE will be low while FAIL is high.

Alarm Interfaces
The FAIL and DEGRADE outputs have an internal 30 kΩ pull-up resistor that is used to pull the digital high value to V_{CC}. However, the alarm output may be overdriven with an external resistor allowing alarm interfacing to non-V_{CC} levels. **Non-V_{CC} alarm output levels must be below the V_{CC} used for the ADN2848.**

Power Consumption
The ADN2848 die temperature must be kept below 125°C. The LFCSP package has an exposed paddle. The exposed paddle should be connected in such a manner that it is at the same potential as the ADN2848 ground pins. The θ_{JA} for the package is shown under the Absolute Maximum Ratings. Power consumption can be calculated using

$$I_{CC} = I_{CCMIN} + 0.3\ I_{MOD}$$

$$P = V_{CC} \times I_{CC} + (I_{BIAS} \times V_{BIAS\_PIN}) + I_{MOD}\ (V_{MODP\_PIN} + V_{MODN\_PIN})/2$$

$$T_{DIE} = T_{AMBIENT} + \theta_{JA} \times P$$

Thus, the maximum combination of $I_{BIAS} + I_{MOD}$ must be calculated. Where:

I_{CCMIN} = 50 mA, the typical value of I_{CC} provided on Page 2 with $I_{BIAS} = I_{MOD} = 0$

T_{DIE} = die temperature

$T_{AMBIENT}$ = ambient temperature

V_{BIAS_PIN} = voltage at I_{BIAS} pin

V_{MODP_PIN} = average voltage at IMODP pin

V_{MODN_PIN} = average voltage at IMODN pin

Laser Disode Interfacing
Many laser diodes designed for 1.25 Gbps operation are packaged with an internal resistor to bring the effective impedance up to 25 Ω in order to minimize transmission line effects. In high current applications, the voltage drop across this resistor, combined with the laser diode forward voltage, makes direct connection between the laser and the driver impractical in a 3 V system. AC coupling the driver to the laser diode removes this headroom constraint.

Caution must be used when choosing component values for ac coupling to ensure that the time constant (L/R and RC, see Figure 7) are sufficiently long for the data rate and expected number of CIDs (consecutive identical digits). Failure to do this could lead to pattern dependent jitter and vertical eye closure. For designs with low series resistance, or where external components become impractical, the ADN2848 supports direct connection to the laser diode (see Figure 6). In this case, care must be taken to ensure that the voltage drop across the laser diode does not violate the minimum compliance voltage on the IMODP pin.

Optical Supervisor

The PSET and ERSET potentiometers may be replaced with a dual-digital potentiometer, the ADN2850 (see Figure 5). The ADN2850 provides an accurate digital control for the average optical power and extinction ratio and ensures excellent stability over temperature.

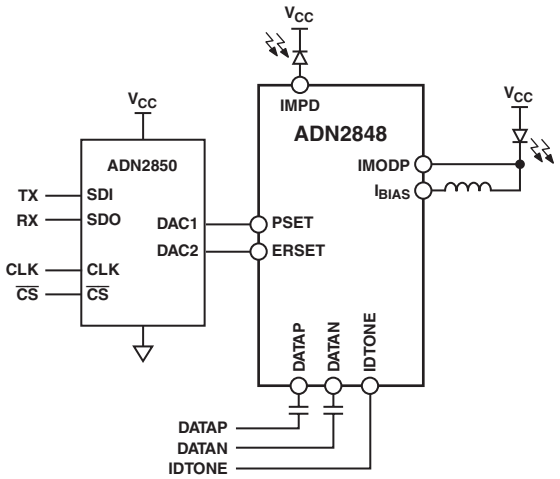


Figure 5. Application Using the ADN2850 Dual 10-Bit Digital Potentiometer with Extremely Low Temperature Coefficient as an Optical Supervisor

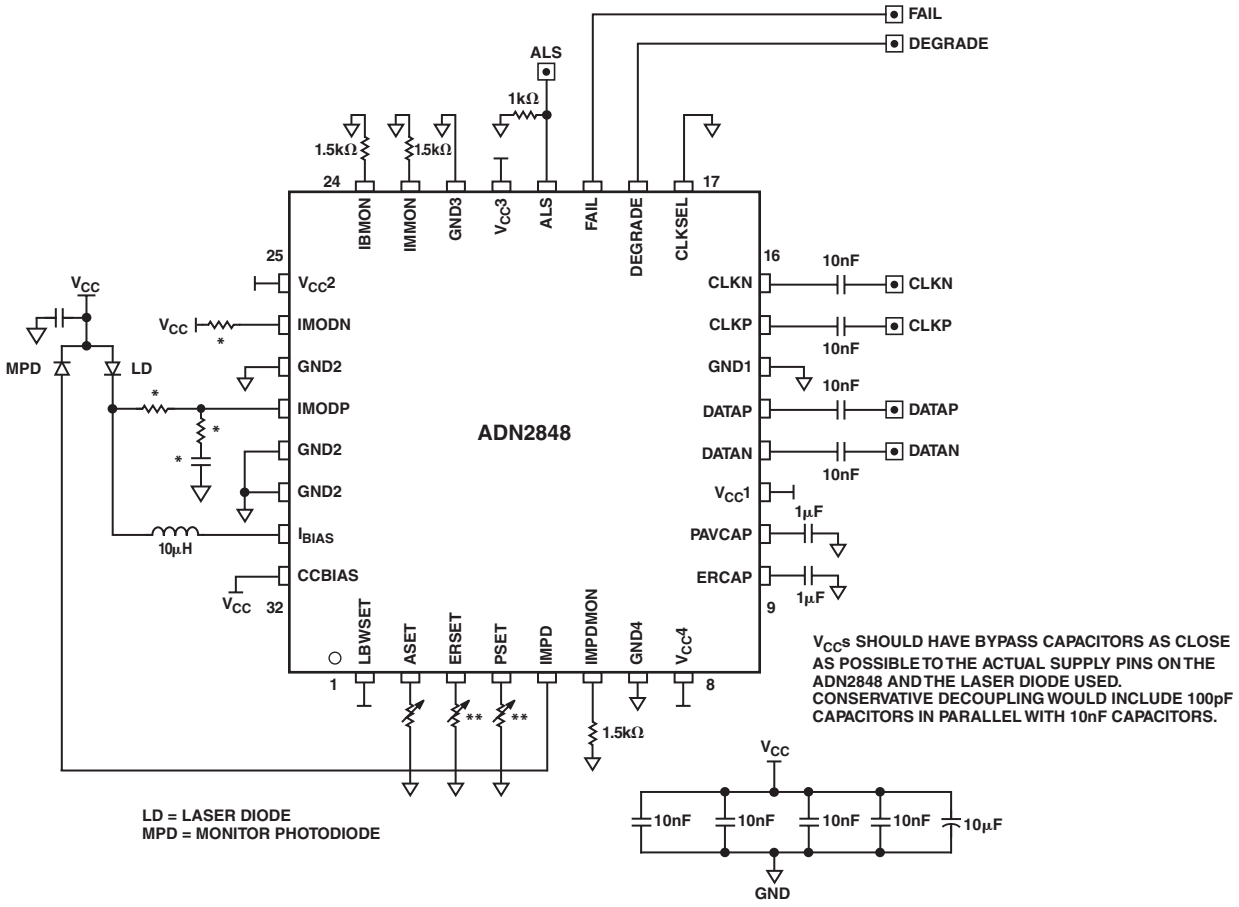


Figure 6. DC-Coupled 50 Mbps to 1.25 Gbps Test Circuit, Data Not Clocked

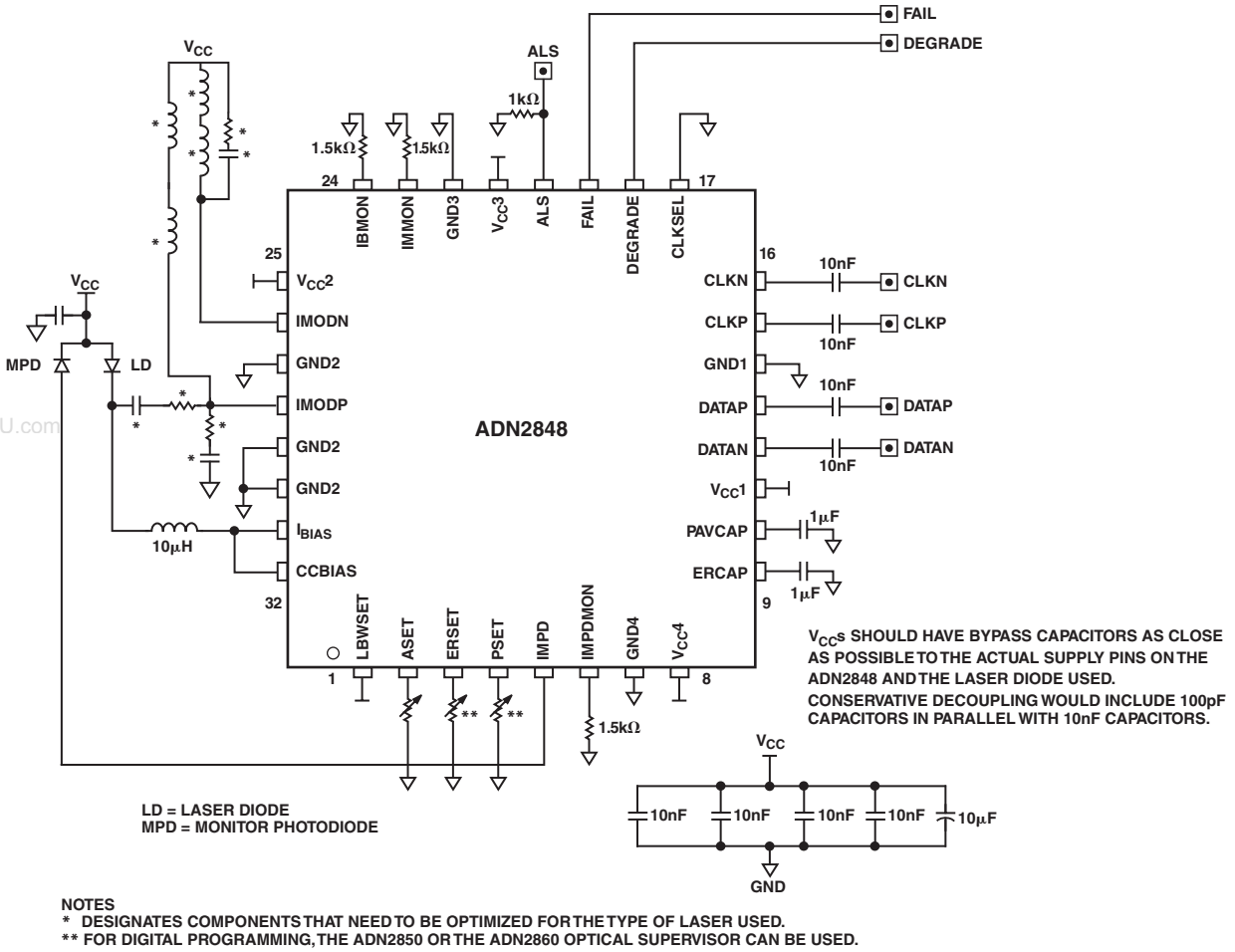


Figure 7. AC-Coupled 50 Mbps to 1.25 Gbps Test Circuit, Data Not Clocked

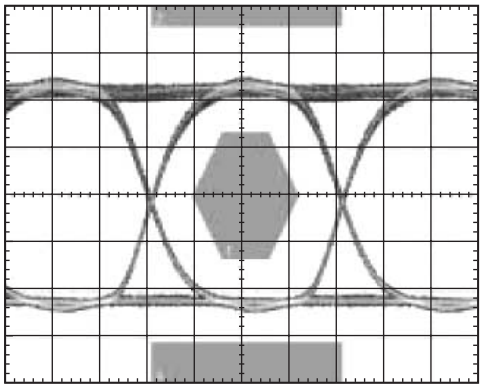


Figure 8. A 1.244 Mbps Optical Eye. Temperature at 25°C. Average Power = 0 dBm, Extinction Ratio = 10 dB, PRBS 31 Pattern, 1 Gb Ethernet Mask. Eye Obtained Using a DFB Laser.

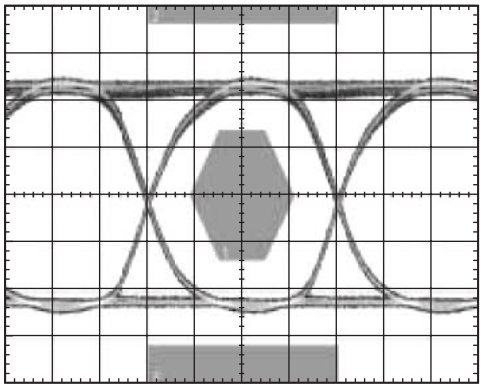
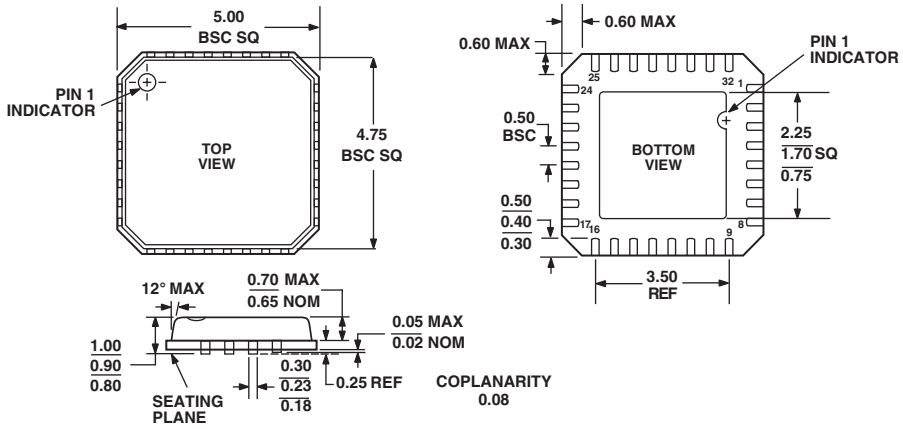


Figure 9. A 1.244 Mbps Optical Eye. Temperature at 85°C. Average Power = 0 dBm, Extinction Ratio = 10 dBm, PRBS 31 Pattern, 1 Gb Ethernet Mask. Eye Obtained Using a DFB Laser.

OUTLINE DIMENSIONS

32-Lead Frame Chip Scale Package [LFCSP]
(CP-32)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

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