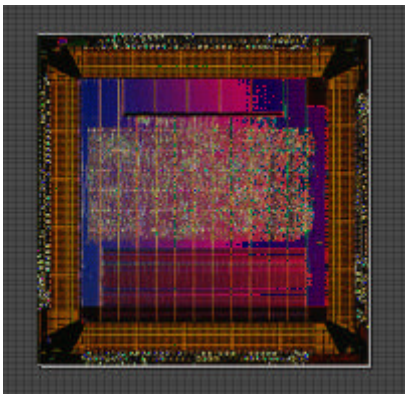
DATASHEET

CX5000
0.18um Structured ASIC



Product Description

The 0.18um CX5000 is an ASIC that utilizes the combination of an advanced metal programmable gate array and optimized EDA system to implement high performance ASIC designs while reducing application tooling costs and design turnaround time. ASIC designers using the CX5000 are able to meet or exceed their design schedules and budgets without compromising technical objectives.

The CX5000 comprises a family of pre-configured platform masterslices that contain varying amounts of general-purpose logic, fast memory, advanced I/Os, clock synthesis and phase management macrocells. When combined with a mix of popular third-party tools and custom designed point EDA solutions, the CX5000 provides not just gate array hardware, but also a complete ASIC Platform from which to develop today's advanced SoC ASICs.

Manufactured in UMC's 0.18um, 6-layer metal CMOS process, the CX5000 combines the reliability and quality of an industry-leading silicon foundry, with the high performance, low power consumption and fast design turnaround time of ChipX Structured ASIC technology. The CX5000 family is very applicable to cost reduction projects, replacing expensive FPGA devices with low-cost metal programmable technology. The CX5000 is the first viable "standard cell alternative" ASIC technology, developed in response to the growing need for cost-effective ASIC implementation capability.

The CX5000 Structured ASIC technology uses just two of the six available metal layers to program the logic, memory, I/O and clocking of an ASIC design and so eliminates the large costs of the remaining "fixed" masks. Wafers are manufactured up to Metal 4, where they are held pending completion of the customer application. Completed chips can be delivered to the customer less than three weeks after sign-off of the finished design.

ChipX Structured ASIC technology is very similar in concept to FPGA, which makes it easy to use and familiar to most ASIC and system designers. Using metal interconnect segments rather than SRAM cells to program the ASIC, CX5000 technology reduces the area of the chip by between 5x and 10x over the equivalent FPGA and brings performance up to 90% of standard cell design speeds.

Key Features and Benefits

- Structured ASIC architecture
- Low NRE and start-up costs
- Fast time to production
- 30K to 1.2M usable ASIC gates
- Up to 2.6M bits of fast block memory
- 2ns access time single-port SRAM, dual-port SRAM and ROM
- Low power consumption (0.06uW/MHz/Gate)
- 200MHz general core logic operation, 650MHz in constrained clock domains

- PCI, PCI-X, SSTL, HSTL, USB1.1, RSDS, LVPECL and LVDS up to 622Mbps
- 1.5V or 1.8V or mixed supply voltage operation
- Up to 1100 total pads
- Low-jitter analog PLL macros with internal loop filter
- Delay Lock Loop (DLL) macros for clock de-skewing
- Wide range of synthesizable IP cores such as CPUs and interface controllers
- Vast packaging library
- Standard ASIC tool flow
- Available front-end and FPGA conversion design services
- BIST and Scan synthesis test options
- Seamless migration to Standard Cell in high volume
- Excellent for SoC designs, new ASICs, and FPGA conversion

The CX5000 Structured ASIC "System Slice"

The CX5000 System Slice product line is designed to incorporate a mix of gates and memory optimized for a wide range of today's advanced SoCs. With a ratio of approximately 160% memory to gates, each slice contains enough memory to support CPU cache, network rate-matching FIFOs, multiple video line buffers and various other single- or dual-port applications.

The CX5000 System-Slice arrays shown in Table 1 have a variety of gate and memory counts. The maximum usable gates in each array is design dependent and refers to the actual size of a customer design prior to test insertion or timing closure.

TABLE 1.
CX5000 SYSTEM SLICE

BASE ARRAY	MAX USABLE ASIC GATES (K)	FAST BLOCK SRAM (K)	LOW JITTER APLL/DLL	BOND PADS
CX50041	30-40	64	4/2	128
CX50101	91-101	160	4/8	256
CX50211	131-144	364	4/8	384
CX50331	207-228	518	4/8	448
CX50561	336-369	880	4/12	640
CX50841	526-578	1264	4/12	768
CX51191	716-787	1774	4/12	896
CX51761	1108-1219	2582	4/12	1152

There are a fixed number of block memories on each masterslice for speed, and for logic and memory efficiency. Each slice has a total available memory count, which can be split into either 18K, 16K or 8K blocks in a variety of widths and depths, or double-pumped to create smaller memories. The memory can be configured as single- or dual-port RAM/ROM, as required.

ChipX uses the latest clock synthesis techniques during layout of the Structured ASIC. We provide the user with four complete analog PLL units for clock phase alignment (when needed), frequency synthesis, or stabilization. These PLL macros have excellent jitter performance and incorporate all of the analog components needed for supply and loop filtering on board the masterslice. A DLL macro generator is available for clock-edge alignment in timing-critical applications.

The CX5000 family has a flexible I/O structure. Each metal-programmable I/O driver cell supports one or two pads, depending on the I/O configuration chosen. The CX5000 product line can be packaged in conventional IC packaging, provided as bare die or processed with an extra layer of metal, bumped and then mounted into a flip-chip package. ChipX has a vast library of standard packages, large pin count FPGA packages, military and hermetic packages. Custom package development services are reasonably priced and include multi-chip modules as well as exotic, ultra-fine pitch and very small outline package types.

CX5000 Architecture: Core, Memory, Corner, I/O Ring

Core

The CX5000 core logic is divided into logic modules each with a closely packed, optimized transistor layout separated by routing channels. The placer software configures the logic modules using pre-defined templates in the top two metal layers to perform the 400 or so library elements supported by the CX5000 technology. Via stacks are used to bring module internal signals up to the programming layers, where they are connected to form the logic function.

The library of logic components described in the CX5000 Data Book uses variously one, two, and sometimes three logic modules. The Synthesis Engine is instructed to use the most complex combinatorial logic components possible to ensure best utilization of each logic module. The router is used to wire up the global routing resources and make short distance connections between the logic modules in the routing channels. The routing channels contain lengthwise and crosswise metal wires of various fetches connected to each other and to the logic modules using the top two metal layers.

The CX5000 core logic operates at clock speeds in excess of 200MHz. The applications targeted for standard cell generally operate at 90% of the standard cell performance and considerably faster than FPGAs. A two input NAND gate in CX5000 technology typically contributes just 180ps of delay to a logic path.

The CX5000 is optimized for low power consumption. Table 2 outlines the power budget of the CX5000 core components.

TABLE 2.
CX5000 CORE COMPONENTS POWER BUDGET

Flip Flop Constant Data (uW/MHz) Typical	0.076
Flip Flop Toggling Data (uW/MHz) Typical	0.49
Logic Cell (uW/MHz) Typical	0.25

Memory

The CX5000 has two memory types. Flexible CX-Memory blocks are arranged at the bottom of the masterslice and extend across the entire width of the chip. Each memory represents 16K bits of available 2ns block SRAM or ROM with two address decoders, two input ports, and two output ports. As shown in Figure 1 (next page), the address decoders can be used to address two separate 8K bit memory instances or one 8K bit dual-port memory instance. Each memory may be as narrow as 2 bits or as wide as 64 bits, with corresponding depth.

In addition, each CX5000 masterslice contains multiple blocks of 18Kbit fast dual port SRAM arranged as 36bits x 512 locations with bitwise-write-enables. This memory is spread around the core logic of the masterslice and is convenient for matching with Xilinx/Altera block SRAM or for combining into larger memories for processor cache or scratchpad memory.

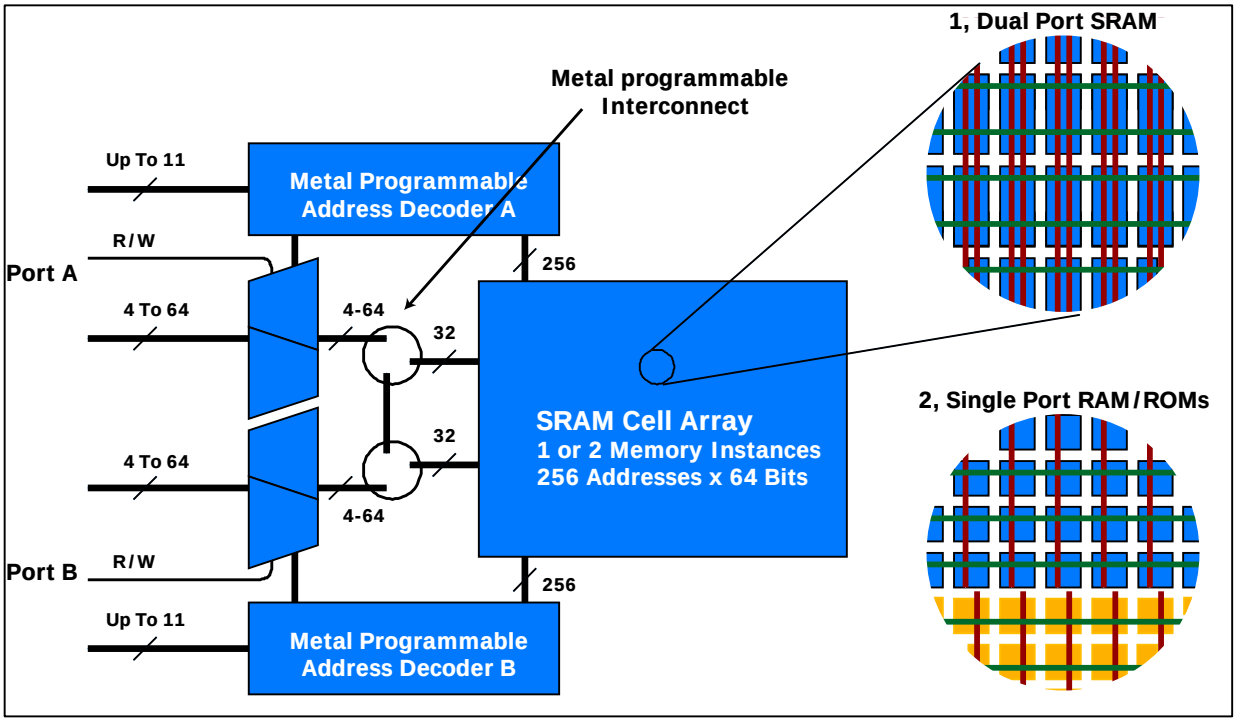


Figure 1. CX5000 CX-Memory Configurations

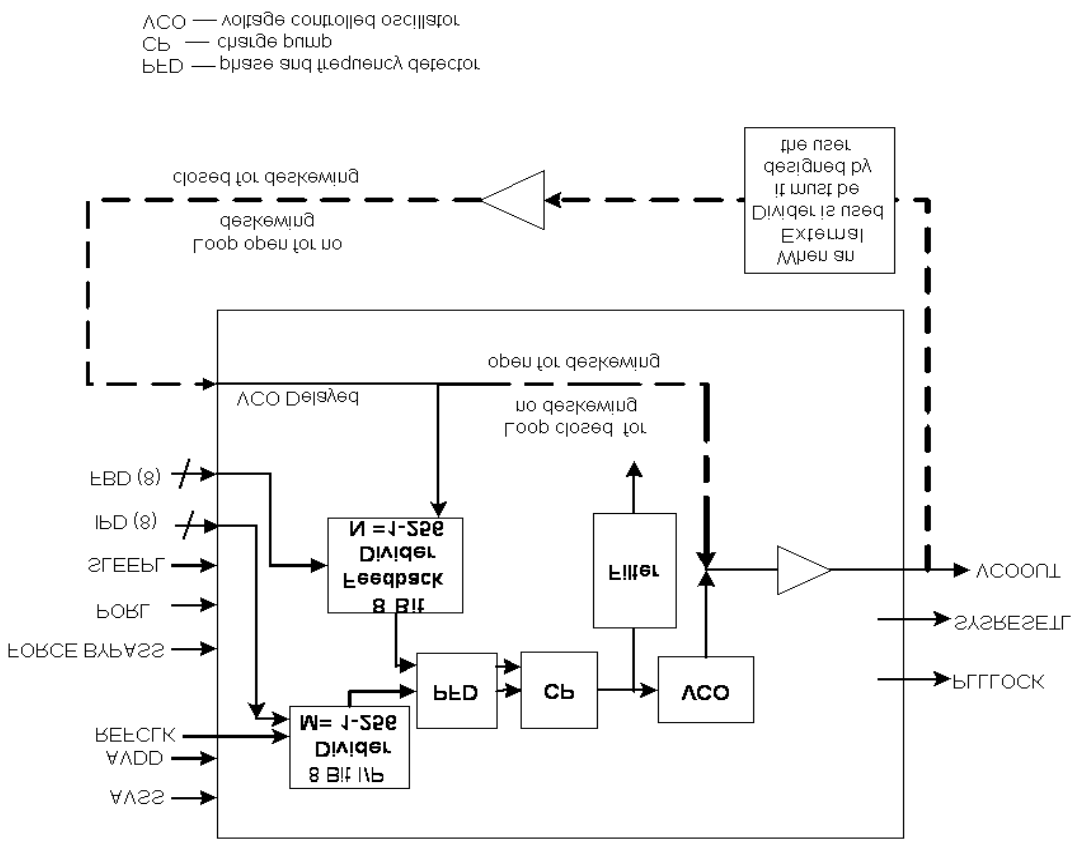
The memories can be surrounded by a BIST shell for convenient and comprehensive production testing. The number of permutations and combinations of memory options prevents easy distribution of pre-defined macros, therefore, ChipX maintains an automatic memory macro generation utility that can email memory models automatically upon request. For instructions on how to use this feature, please check the CX5000 Design Manual.

Corner

Figure 2 (next page) illustrates the CX5000 die corner that contains a number of important analog components. Each corner contains an accurate bandgap device, which is then used to provide reference and bias voltages to other components in the pad ring. Also contained in each corner is a complete, programmable analog PLL.

The PLL may be configured to operate at frequencies between 7.5MHz and 500MHz given certain input clock criterion and loop filter choices. ChipX provides an automatic response server that will reply with simulation and synthesis macros for a specific frequency PLL based on the input frequency, desired output frequency, and phase relationship. The PLL models may be easily disabled and bypassed to reduce simulation time.

ChipX CX5000 logic is fast when compared to standard FPGA logic, so it is possible to create all of the counters, dividers, and clock phase taps from synthesized logic rather than relying on custom macros. The corner also contains an ESD structure that is used in concert with the ESD structures adjacent to the pads to provide 2.5KV of ESD protection to the devices.



I/O Ring

As shown in Figure 3, the CX5000 I/O ring is comprised of blocks of 8 metal programmable I/O drivers, 16 pads and ESD structures.

Each I/O structure may be split into one simple input (CMOS or TTL) and one simple output (CMOS or TTL) to maximize the chip's signal I/O. In cases where the cell is configured as a bi-directional or an advanced single-ended I/O (e.g., PCI), the cell supports one signal only; the other pad can be left unconnected or used for power. Differential I/Os require two I/O structures per channel and use two pads; the remaining two pads are power or no-connect.

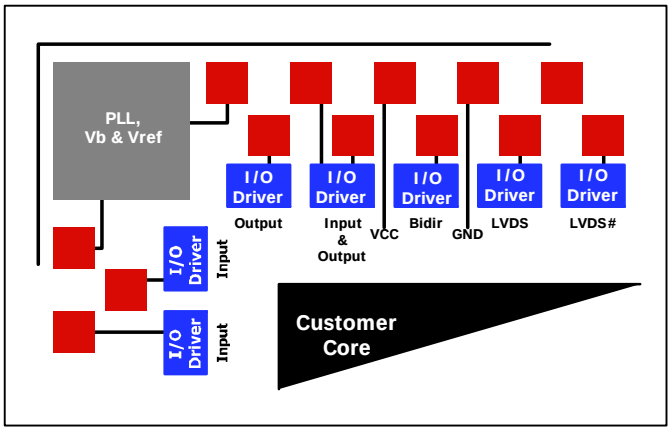


Figure 3. CX5000 I/O Structure

Supported I/O

As shown in Table 4, the CX5000 family supports 676 simple I/O macrocells in addition to a number of advanced I/Os based on popular industry standards.

TABLE 4: CX5000 SUPPORTED I/O		
I/O STANDARD	**VDD**	**NOTES**
LVTTL25/33	2.5V/3.3V	Selectable drive strength, pull-up/down, slew-rate, hysteresis, Bidir
LVCMOS25/33	2.5V/3.3V	Selectable drive strength, pull-up/down, slew-rate, hysteresis, Bidir
PCI	3.3V	PCI Standard 2.2 at up to 66MHz
PCI-X	3.3V	PCI-X standard at up to 133MHz
USB	3.3V	USB Standard 1.1 at 4Mbps and 12Mbps
LVDS	3.3V	IEEE 1596.3-1996, ANSI/TIA/EIA-644-1995
LVPECL	3.3V	
SSTL2/3	2.5V/3.3V	Support for Class I and II
HSTL	1.5V	Support for Class I, II and IV
RSDS		RSDS V1.0

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
VDDCore	Core Supply Voltage	-0.25	2.25	V
VDDI/O	I/O Supply Voltage	-0.25	4.0	V
Vin/Vout	DC Input and Output	-0.25	4.0	V
TJ	Junction Temperature	-55	155	°C

NORMAL OPERATING CONDITIONS				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
VDD1.8v	Core and I/O Supply Voltage	1.5	1.98	V
VDD 2.5v	I/O Supply Voltage	2.25	2.75	V
VDD 3.3v	I/O Supply Voltage	3.0	3.6	V

Design Flow

ChipX spends considerable development effort to ensure that taping out a design to a CX5000 Structured ASIC is a simple, painless, and risk-free endeavor. ChipX provides on-line downloadable libraries for both Synopsys and Synplify ASIC synthesis tools.

RTL or Netlist Handoff

Many customers prefer to handoff their RTL designs early and let ChipX perform the entire timing closure loop, including synthesis and final simulations. ChipX can also convert obsolete design netlists and even well specified concept designs into prototypes rapidly and reliably.

Packaging and Test

ChipX uses world-class external packaging and test facilities in the United States and Taiwan to assemble and complete commercial, industrial, or military testing and qualification of products. A vast standard packaging library that includes the most popular DIP, QFP, BGA, fine-pitch BGA, and PGA package sizes supports the CX5000 product line. The CX5000 is guaranteed to match any standard FPGA device with a pin-for-pin replacement package. For specialist applications, multi-chip modules or hard-to-find hermetic or BGA package sizes, ChipX experienced custom package design staff can create a package or pinout to your specifications. ChipX offers SCAN insertion and ATPG as well as fault grading, at speed test, Mil 883 test flows and a variety of additional test and QA services to match every product requirement.

For more information, please visit our website: www.chipx.com