1 Mbit (128K x 8) nvSRAM With Real-Time Clock

Features

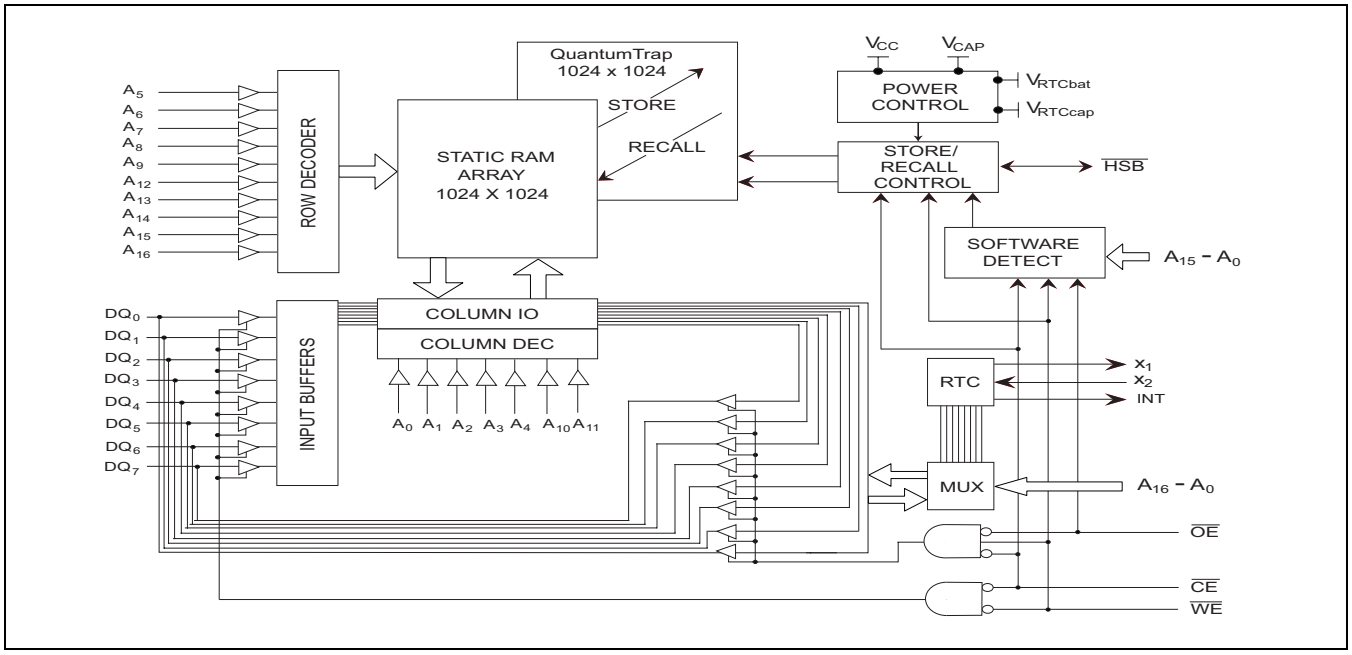
- Data integrity of Cypress nvSRAM combined with full featured Real-Time Clock (RTC)
- Watchdog timer
- Clock alarm with programmable interrupts
- Capacitor or battery backup for RTC
- 25 ns, 35 ns, and 45 ns access times
- "Hands-off" automatic *STORE* on power down with only a small capacitor
- *STORE* to QuantumTrap™ initiated by software, device pin, or on power down
- *RECALL* to SRAM initiated by software or on power up
- Infinite *READ, WRITE,* and *RECALL* cycles
- High reliability
  - Endurance to 200,000 cycles
  - Data retention: 20 years @55°C
- 10 mA typical I_{CC} at 200 ns cycle time
- Single 3V operation +20%, –10%
- Commercial and industrial temperature
- SSOP package (ROHS compliant)

Functional Description

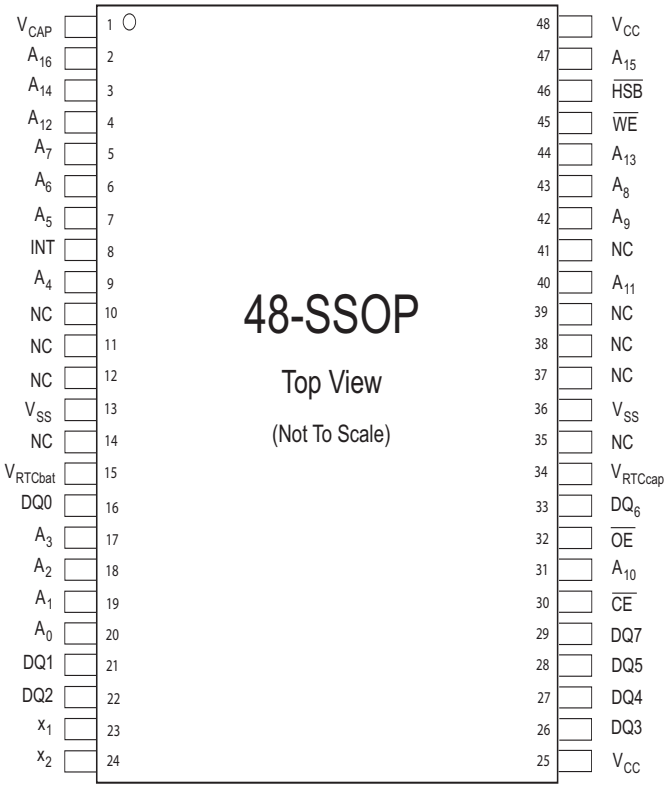
The Cypress CY14B101K combines a 1 Mbit nonvolatile static RAM with a full featured real-time clock in a monolithic integrated circuit. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM can be read and written an infinite number of times, while independent, nonvolatile data resides in the nonvolatile elements.

The Real-Time Clock function provides an accurate clock with leap year tracking and a programmable, high accuracy oscillator. The alarm function is programmable for one time alarm or periodic seconds, minutes, hours, or days. There is also a programmable watchdog timer for process control.

Logic Block Diagram



Pin Configurations



Pin Definitions

Pin Name	IO Type	Description
$A_0 – A_{16}$	Input	**Address inputs used to select one of the 131,072 bytes of the nvSRAM**.
DQ0 – DQ7	Input Output	**Bidirectional data IO lines.** Used as input or output lines depending on operation
NC	No Connect	**No Connects**. This pin is not connected to the die
$\overline{WE}$	Input	**Write Enable Input, active LOW**. When selected LOW, enables data on the IO pins to be written to the address location latched by the falling edge of $\overline{CE}$.
$\overline{CE}$	Input	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, active LOW**. The active low $\overline{OE}$ input enables the data output buffers during READ cycles. Deasserting $\overline{OE}$ high causes the IO pins to tri-state.
X_1	Output	**Crystal connection**, drives crystal on start up.
X_2	Input	**Crystal connection** for 32.768 kHz crystal.
V_{RTCcap}	Power Supply	**Capacitor supplied backup RTC supply voltage**. (Left unconnected if V_{RTCbat} is used)
V_{RTCbat}	Power Supply	**Battery supplied backup RTC supply voltage**. (Left unconnected if V_{RTCcap} is used)
INT	Output	**Interrupt Output**. Program to respond to the clock alarm, the watchdog timer and the power monitor. Programmable to either active HIGH (push/pull) or LOW (open drain).
V_{SS}	Ground	**Ground for the device**. Must be connected to ground of the system.
V_{CC}	Power Supply	**Power Supply inputs to the device**.
$\overline{HSB}$	Input Output	**Hardware Store Busy**. When LOW this output indicates a Hardware Store is in progress. When pulled low external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional).
V_{CAP}	Power Supply	**AutoStore™ Capacitor.** Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

Device Operation

The CY14B101K nvSRAM is made up of two functional components paired in the same physical cell, a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Transfer of the data can be from the SRAM to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The CY14B101K supports infinite reads and writes just like a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200,000 STORE operations.

SRAM READ

The CY14B101K performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are low, while $\overline{WE}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-16} determines which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs will be valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. It remains valid until another address change, or until $\overline{CE}$ or $\overline{OE}$ is brought high, or $\overline{WE}$ or $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are low and $\overline{HSB}$ is high. The address inputs must be stable before entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes high, at the end of the cycle. The data on the common IO pins DQ_{0-7} will be written into the memory if the data is valid t_{SD} before the end of a $\overline{WE}$-controlled WRITE or before the end of an $\overline{CE}$-controlled WRITE. It is recommended that $\overline{OE}$ be kept high during the entire WRITE cycle to avoid data bus contention on common IO lines. If $\overline{OE}$ is left low, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes low.

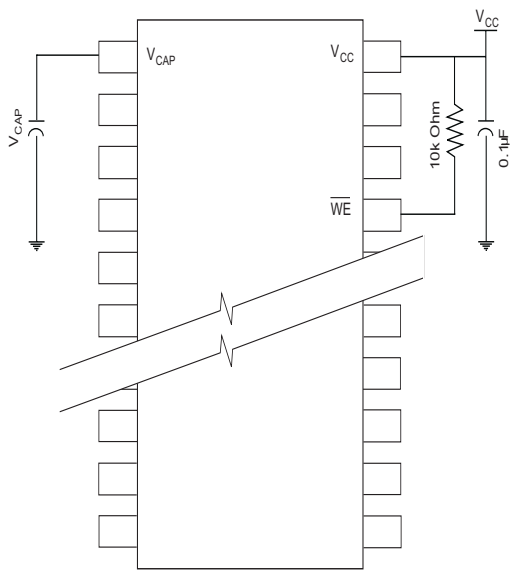
AutoStore Operation

The CY14B101K stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store activated by $\overline{HSB}$, Software Store activated by an address sequence, and AutoStore on device power down. AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101K.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

Figure 1 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the Table , “DC Electrical Characteristics,” on page 14 for the size of V_{CAP}.

Figure 1. AutoStore Mode



The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up must be placed on $\overline{WE}$ to hold it inactive during power up.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. Monitor the $\overline{HSB}$ signal by the system to detect if an AutoStore cycle is in progress.

Hardware STORE ($\overline{HSB}$) Operation

The CY14B101K provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. Use the $\overline{HSB}$ pin to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the CY14B101K conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes low, the CY14B101K continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until $\overline{HSB}$ returns high.

During any STORE operation, regardless of how it was initiated, the CY14B101K continues to drive the $\overline{HSB}$ pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the CY14B101K remains disabled until the $\overline{HSB}$ pin returns high. Leave the $\overline{HSB}$ unconnected if it is not used.

Hardware RECALL (Power Up)

During power up, or after any low power condition (V_{CC} < V_{SWITCH}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will be automatically initiated and takes $t_{HRECALL}$ to complete.

Software STORE

Using a software address sequence, transfer the data from the SRAM to the nonvolatile memory. The CY14B101K software STORE cycle is initiated by executing sequential CE-controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If there are intervening READ OR WRITE accesses, the sequence will be aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with CE-controlled READs or OE-controlled READs. Once the sixth address in the sequence has been entered, the STORE cycle commences and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence. It is not necessary that OE be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

Software RECALL

Transfer the data from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE-controlled READ operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations.The RECALL operation does not alter the data in the nonvolatile elements.

Preventing AutoStore

Disable the AutoStore function by initiating an AutoStore Disable sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore Disable sequence, the following sequence of CE-controlled READ operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8B45 AutoStore Disable

Re-enable the AutoStore by initiating an AutoStore Enable sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore Enable sequence, the following sequence of CE-controlled READ operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled a manual STORE operation (Hardware or Software) needs to be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Data Protection

The CY14B101K protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} < V_{SWITCH}. If the CY14B101K is in a WRITE mode (both CE and WE low) at power up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power up or brownout conditions.

Noise Considerations

The CY14B101K is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground, and signals reduces circuit noise.

Table 1. Mode Selection

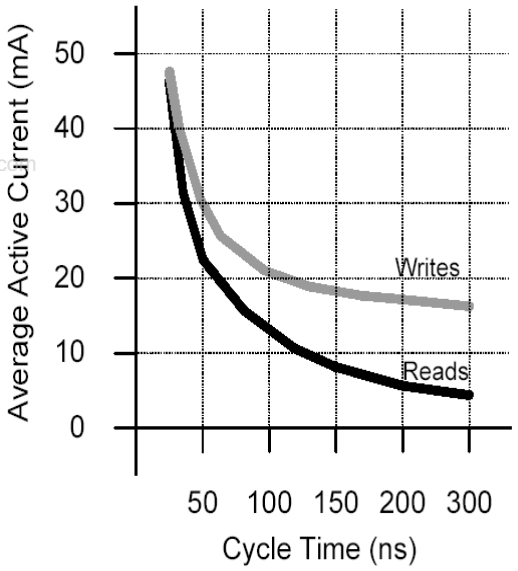
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A15 – A0	Mode	IO	Power
H	X	X	X	Not Selected	Output High-Z	Standby
L	H	L	X	READ SRAM	Output Data	Active
L	L	X	X	WRITE SRAM	Input Data	Active
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	READ SRAM READ SRAM READ SRAM READ SRAM READ SRAM Autostore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 2, 3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	READ SRAM READ SRAM READ SRAM READ SRAM Read SRAM Autostore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 2, 3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High-Z	Active I_{CC2}[1, 2, 3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High-Z	Active[1, 2, 3]

Notes
1. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.
2. While there are 17 address lines on the CY14B101K, only the lower 16 lines are used to control software modes.
3. IO state depends on the state of $\overline{OE}$. The IO table shown is based on $\overline{OE}$ Low.

Low Average Active Power

CMOS technology provides the CY14B101K, the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. *Figure 2* on page 6 shows the relationship

Figure 2. Current vs. Cycle Time



between I_{CC} and READ/WRITE cycle time. Worst case current consumption is sREADhown for commercial temperature range, V_{CC} = 3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled.

The overall average current drawn by the CY14B101K depends on the following items:

1. The duty cycle of chip enable.
2. The overall cycle rate for accesses.
3. The ratio of READs to WRITEs.
4. The operating temperature.
5. The V_{CC} level.
6. IO loading.

Real-Time Clock Operation

nvTIME Operation

The CY14B101K offers internal registers that contain clock, alarm, watchdog, interrupt, and control functions. Internal double buffering of the clock and the clock/timer information registers prevents accessing transitional internal clock data during a READ or WRITE operation. Double buffering also circumvents disrupting normal timing counts or clock accuracy of the internal clock while accessing clock data. Clock and Alarm Registers store data in BCD format.

Clock Operations

The clock registers maintain time up to 9,999 years in one second increments. The user can set the time to any calendar time and the clock automatically keeps track of days of the week, month, leap years, and century transitions. There are eight registers dedicated to the clock functions that are used to set time with a WRITE cycle and to READ time during a READ cycle. These registers contain the Time of Day in BCD format. Bits defined as “0” are currently not used and are reserved for future use by Cypress.

Reading the Clock

While the double-buffered RTC register structure reduces the chance of reading incorrect data from the clock, you have to halt internal updates to the CY14B101K clock registers before reading clock data to prevent the reading of data in transition. Stopping the internal register updates does not affect clock accuracy. The update process is stopped by writing a “1” to the READ bit “R” (in the flags register at 0x1FFF0), and will not restart until a “0” is written to the READ bit. The RTC registers can then be READ while the internal clock continues to run. Within 20 ms after a “0” is written to the READ bit, all CY14B101K registers are simultaneously updated.

Setting the Clock

Setting the WRITE bit “W” (in the flags register at 0x1FFF0) to a “1” halts updates to the CY14B101K registers. The correct day, date, and time can then be written into the registers in 24-hour BCD format. The time written is referred to as the “Base Time.” This value is stored in nonvolatile registers and used in calculation of the current time. Resetting the WRITE bit to “0” transfers those values to the actual clock counters, after which the clock resumes normal operation.

Backup Power

The RTC in the CY14B101K is intended for permanently powered operation. Either the V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When primary power, V_{CC}, fails and drops below V_{SWITCH} the device will switch to the backup power supply.

The clock oscillator uses very little current which maximizes the backup time available from the backup source. Regardless of clock operation with the primary source removed, the data stored in nvSRAM is secure, having been stored in the nonvolatile elements as power was lost.

During backup operation the CY14B101K consumes a maximum of 300 nA at 2 volts. Capacitor or battery values must be chosen according to the application.

Backup time values based on maximum current specs are shown in the following table. Nominal times are approximately three times longer.

Table 2. RTC Backup Time

Capacitor Value	Backup Time
0.1F	72 hours
0.47F	14 days
1.0F	30 days

Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up. If a battery is used, a 3V lithium is recommended and the CY14B101K will only source current from the battery when the primary power is removed. The battery will not however be

recharged at any time by the CY14B101K. The battery capacity should be chosen for total anticipated cumulative downtime required over the life of the system.

Stopping and Starting the Oscillator

The $\overline{\text{OSCEN}}$ bit in the calibration register at 0x1FFF8 controls the starting and stopping of the oscillator. This bit is nonvolatile and shipped to customers in the “enabled” (set to 0) state. To preserve battery life while system is in storage, $\overline{\text{OSCEN}}$ should be set to a 1. This turns off the oscillator circuit extending the battery life. If the $\overline{\text{OSCEN}}$ bit goes from disabled to enabled, it takes approximately 5 seconds (10 seconds max) for the oscillator to start.

The CY14B101K has the ability to detect oscillator failure. This is recorded in the OSCF (Oscillator Failed bit) of the flags register at address 0x1FFF0. When the device is powered on (V_{CC} goes above V_{SWITCH}) the $\overline{\text{OSCEN}}$ bit is checked for “enabled” status. If the $\overline{\text{OSCEN}}$ bit is enabled and the oscillator is not active, the OSCF bit is set. The user should check for this condition and then WRITE a 0 to clear the flag. It should be noted that in addition to setting the OSCF flag bit, the time registers are reset to the “Base Time” (see the section Setting the Clock on page 6), which is the value last written to the timekeeping registers. The Control/Calibration register and the $\overline{\text{OSCEN}}$ bit are not affected by the oscillator failed condition.

If the voltage on the backup supply (either V_{RTCcap} or V_{RTCbat}) falls below their minimum level, the oscillator may fail, leading to the oscillator failed condition, which can be detected when system power is restored.

The value of OSCF should be reset to 0 when the time registers are written for the first time. This initializes the state of this bit which may have become set when the system was first powered on.

Calibrating the Clock

The RTC is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. Clock accuracy depends on the quality of the crystal, usually specified to 35 ppm limits at 25°C. This error could equate to +1.53 minutes in accordance with month. The CY14B101K employs a calibration circuit that can improve the accuracy to +1/–2 ppm at 25°C. The calibration circuit adds or subtracts counts from the oscillator divider circuit.

The number of pulses that are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in calibration register at 0x1FFF8. Adding counts speeds the clock up; subtracting counts slows the clock down. The calibration bits occupy the five lower order bits in the control register 8. Set these bits to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit, where a “1” indicates positive calibration and a “0” indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once in accordance with minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary “1” is loaded into the register, only the first two minutes of the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles. That is 4.068 or –2.034 ppm of adjustment in accordance with calibration step in the calibration register.

In order to determine how to set the calibration one may set the CAL bit in the flags register at 0x1FFF0 to 1, which causes the INT pin to toggle at a nominal 512 Hz. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.010124 Hz would indicate a +20 ppm error, requiring a –10 (001010) to be loaded into the calibration register. Note that setting or changing the calibration register does not affect the frequency test output frequency.

Alarm

The alarm function compares user programmed values to the corresponding time-of-day values. When a match occurs, the alarm event occurs. The alarm drives an internal flag, AF, and may drive the INT pin if desired.

There are four alarm match fields. They are date, hours, minutes, and seconds. Each of these fields also has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to “0” indicates that the corresponding field will be used in the match process.

Depending on the match bits, the alarm can occur as specifically as one particular second on one day of the month, or as frequently as once in accordance with second continuously. The MSB of each alarm register is a match bit. Selecting none of the match bits (all 1s) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to “0” causes the logic to match the seconds alarm value to the current time of day. Since a match occurs for only one value in accordance with minute, the alarm occurs once in accordance with minute. Likewise, setting the seconds and minutes match bits causes an exact match of these values. Thus, an alarm occurs once in accordance with hour. Setting seconds, minutes, and hours causes a match once in accordance with day. Lastly, selecting all match values causes an exact time and date match. Selecting other bit combinations will not produce meaningful results; however the alarm circuit should follow the functions described.

There are two ways a user can detect an alarm event, by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0x1FFF0 will indicate that a date and time match has occurred. The AF bit will be set to 1 when a match occurs. Reading the Flags/Control register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

Watchdog Timer

The watchdog timer is a free running down counter that uses the 32-Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the watchdog timer register.

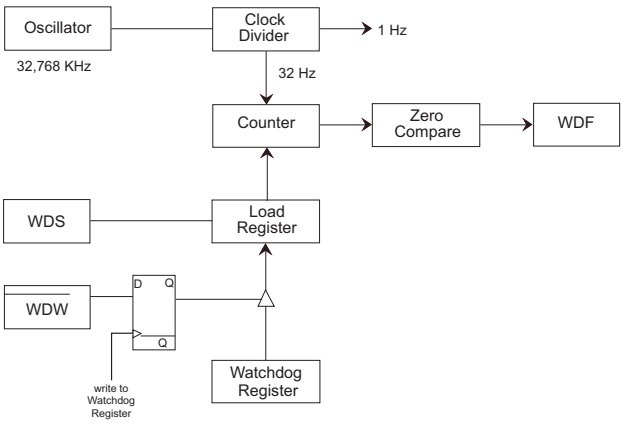
The counter consists of a loadable register and a free-running counter. On power up, the watchdog timeout value in register 0x1FFF7 is loaded into the counter load register. Counting begins on power up and restarts from the loadable value any time the watchdog strobe (WDS) bit is set to 1. The counter is

compared to the terminal value of 0. If the counter reaches this value, it causes an internal flag and an optional interrupt output. You can prevent the timeout interrupt by setting WDS bit to 1 before the counter reaching 0. This causes the counter to be reloaded with the watchdog timeout value and to be restarted. As long as the user sets the WDS bit before the counter reaching the terminal value, the interrupt and flag never occurs.

Write new timeout values by setting the watchdog WRITE bit to 0. When the WDW is 0 (from the previous operation), new writes to the watchdog timeout value bits D5–D0 allow the timeout value to be modified. When WDW is a 1, writes to bits D5 – D0 will be ignored. The WDW function allows a user to set the WDS bit without concern that the watchdog timer value will be modified. A logical diagram of the watchdog timer is shown in *Figure 3*. Note that setting the watchdog timeout value to 0 would be otherwise meaningless and therefore disables the watchdog function.

The output of the watchdog timer is a flag bit WDF that is set if the watchdog is allowed to timeout. The flag is set upon a watchdog timeout and cleared when the Flags/Control register is READREAD by the user. The user can also enable an optional interrupt source to drive the INT pin if the watchdog timeout occurs.

Figure 3. Watchdog Timer Block Diagram



Power Monitor

The CY14B101K provides a power management scheme with power fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low V_{CC} access. The power monitor is based on an internal band gap reference circuit that compares the V_{CC} voltage to various thresholds.

As described in the AutoStore section previously, when V_{SWITCH} is reached as V_{CC} decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source no data may be read or written and the clock functions are not available to the user. The clock continues to operate in the background. Updated clock data is available to the user after VCC has been restored to the device and tHRECALL delay (see AutoStore/Power Up RECALL on page 16) .

Interrupts

The CY14B101K provides three potential interrupt sources. They include the watchdog timer, the power monitor, and the clock/calendar alarm. Individually enable each and assign to drive the INT pin. In addition, each has an associated flag bit that the host processor can use to determine the cause of the interrupt. Some of the sources have additional control bits that determine functional behavior. In addition, the pin driver has three bits that specify its behavior when an interrupt occurs.

The three interrupts each have a source and an enable. Both the source and the enable must be active (true high) in order to generate an interrupt output. Only one source is necessary to drive the pin. The user can identify the source by reading the Flags/Control register, which contains the flags associated with each source. All flags are cleared to 0 when the register is READ. The flags will be cleared only after a complete read cycle (WE high); The power monitor has two programmable settings that are explained in the power monitor section.

Once an interrupt source is active, the pin driver determines the behavior of the output. It has two programmable settings as shown in the following section. Pin driver control bits are located in the Interrupts register.

According to the programming selections, the pin can be driven in the backup mode for an alarm interrupt. In addition, the pin can be an active LOW (open drain) or an active HIGH (push pull) driver. If programmed for operation during backup mode, it can only be active LOW. Lastly, the pin can provide a one shot function so that the active condition is a pulse or a level condition. In one shot mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In level mode, the pin goes to its active polarity until the Flags/Control register is read by the user. This mode is intended to be used as an interrupt to a host microcontroller. The Interrupt register is initialized to 00h. The control bits are summarized as follows:

Watchdog Interrupt Enable – WIE. When set to 1, the watchdog timer drives the INT pin as well as an internal flag when a watchdog timeout occurs. When WIE is set to 0, the watchdog timer affects only the internal flag.

Alarm Interrupt Enable – AIE. When set to 1, the alarm match drives the INT pin as well as an internal flag. When set to 0, the alarm match only affects to internal flag.

Power Fail Interrupt Enable – PFE. When set to 1, the power fail monitor drives the pin as well as an internal flag. When set to 0, the power fail monitor affects only the internal flag.

High/Low – H/L. When set to a 1, the INT pin is active high and the driver mode is push-pull. The INT pin can drive high only when $V_{CC} > V_{SWITCH}$. When set to a 0, the INT pin is active LOW and the drive mode is open drain. Active LOW (open drain) is operational even in battery backup mode.

Pulse/Level – P/L. When set to a 1 and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a 0, the INT pin is driven high or low (determined by H/L) until the Flags/Control register is READd.

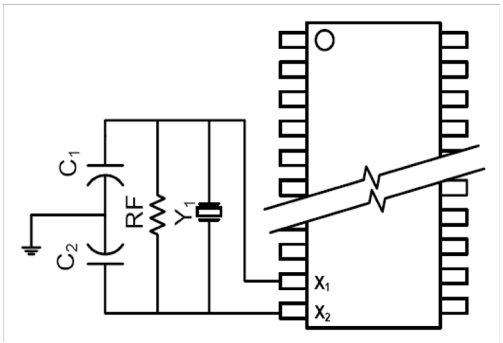
When an enabled interrupt source activates the INT pin, an external host can READ the Flags/Control register to determine the cause. Remember that all flags will be cleared

when the register is READ. If the INT pin is programmed for level mode, then the condition clears and the INT pin returns to its inactive state. If the pin is programmed for pulse mode, then reading the flag also clears the flag and the pin. The pulse will not complete its specified duration if the Flags/Control register is READ. If the INT pin is used as a host reset, then the Flags/Control register should not be READ during a reset.

During a power on reset with no battery, the interrupt register is automatically loaded with the value 24h. This causes power fail interrupt to be enabled with an active LOW pulse.

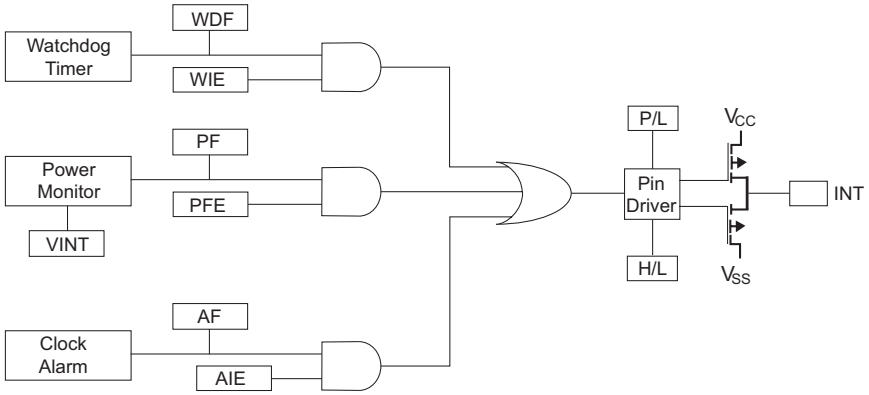
Flags Register – The Flags register has three flag bits: WDF, AF, and PF. These flag bits are initialized to 00h. These flags are set by the watchdog timeout, alarm match, or power fail monitor respectively. The processor can either poll this register or enable interrupts to be informed when a flag is set. The flags are automatically reset once the register is READ.

RTC Recommended Component Configuration



Recommended Values
Y1 = 32.768 KHz
RF = 10 MΩ
C_1 = 0
C_2 = 56 pF

Figure 4. Interrupt Block Diagram



WDF - Watchdog Timer Flag
WIE - Watchdog Interrupt Enable
PF - Power F ail Flag
PFE - Power Fail Enable
AF - Alarm Flag
AIE - Alarm Interrupt Enable
P/L - Pulse Level
H/L - High/Low

Table 3. RTC Register Map

Register	BCD Format Data								Function/Range
	D7	D6	D5	D4	D3	D2	D1	D0	
0x1FFFF	10s Years				Years				Years: 00 – 99
0x1FFFE	0	0	0	10s Months	Months				Months: 01 – 12
0x1FFFD	0	0	10s Day of Month		Day Of Month				Day of Month: 01 – 31
0x1FFFC	0	0	0	0	0	Day of week			Day of week: 01 – 07
0x1FFFB	0	0	10s Hours		Hours				Hours: 00 – 23
0x1FFFA	0	10s Minutes			Minutes				Minutes: 00 – 59
0x1FFF9		10s Seconds			Seconds				Seconds: 00 – 59
0x1FFF8	$\overline{\text{OSCEN}}$	0	Cal Sign		Calibration				Calibration Values [4]
0x1FFF7	WDS	$\overline{\text{WDW}}$	WDT						Watchdog [4]
0x1FFF6	WIE	AIE	PFE	0	$\overline{\text{H/L}}$	$\overline{\text{P/L}}$	0	0	Interrupts [4]
0x1FFF5	$\overline{\text{M}}$	0	10s Alarm Date		Alarm Day				Alarm, Day of Month: 01 – 31
0x1FFF4	$\overline{\text{M}}$	0	10s Alarm Hours		Alarm Hours				Alarm, Hours: 00 – 23
0x1FFF3	$\overline{\text{M}}$	10 Alarm Minutes			Alarm Minutes				Alarm, Minutes: 00 – 59
0x1FFF2	$\overline{\text{M}}$	10 Alarm Minutes			Alarm, Seconds				Alarm, Seconds: 00 – 59
0x1FFF1	10s Centuries				Centuries				Centuries: 00 – 99
0x1FFF0	WDF	AF	PF	OSCF	0	CAL	W	R	Flags [4]

Table 4. Register Map Detail

0x1FFFF	**Time Keeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10s Years				Years			
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0 – 99.							
0x1FFFE	**Time Keeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10s Month	Months			
	Contains the BCD digits of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1 – 12.							
0x1FFFD	**Time Keeping – Date**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s Day of Month		Day of Month			
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1 – 31. Leap years are automatically adjusted for.							
0x1FFFC	**Time Keeping – Day**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day of Week		
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date.							

Note
4. This register contains a binary, not BCD, value. .

Table 4. Register Map Detail (continued)

0x1FFFB	**Time Keeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	12/24	0	10s Hours		Hours			
	Contains the BCD value of hours in 24 hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0 – 23.							
0x1FFFA	**Time Keeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s Minutes			Minutes			
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0 – 59.							
0x1FFF9	**Time Keeping – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s Seconds			Seconds			
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0 – 59.							
0X1FFF8	**Calibration/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{\text{OSCEN}}$	0	Calibration Sign	Calibration				
OSCEN	Oscillator Enable. When set to 1, the oscillator is halted. When set to 0, the oscillator runs. Disabling the oscillator saves battery/capacitor power during storage. On a no battery power up, this bit is set to 0.							
Calibration Sign	Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time base.							
Calibration	These five bits control the calibration of the clock.							
0x1FFF7	**WatchDog Timer**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDS	$\overline{\text{WDW}}$	WDT					
WDS	Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no affect. The bit is cleared automatically once the watchdog timer is reset. The WDS bit is WRITE only. Reading it always returns a 0.							
WDW	Watchdog Write Enable. Setting this bit to 1 masks the watchdog timeout value (WDT5–WDT0) so it cannot be written. This allows the user to strobe the watchdog without disturbing the timeout value. Setting this bit to 0 allows bits 5 – 0 to be written on the next WRITE to the watchdog register. The new value will be loaded on the next internal watchdog clock after the WRITE cycle is complete. This function is explained in more detail in the watchdog timer section.							
WDT	Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The minimum range or timeout value is 31.25 ms (a setting of 1) and the maximum timeout is 2 seconds (setting of 3 Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the WDW bit was cleared to 0 on a previous cycle.							

Table 4. Register Map Detail (continued)

0x1FFF6	**Interrupt Status/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WIE	AIE	PFIE	0	$\overline{H/L}$	$\overline{P/L}$	0	0
WIE	Watchdog Interrupt Enable. When set to 1 and a watchdog timeout occurs, the watchdog timer drives the INT pin as well as the WDF flag. When set to 0, the watchdog timeout affects only the WDF flag.							
AIE	Alarm Interrupt Enable. When set to 1, the alarm match drives the INT pin as well as the AF flag. When set to 0, the alarm match only affects the AF flag.							
PFIE	Power Fail Enable. When set to 1, the alarm match drives the INT pin as well as the AF flag. When set to 0, the power fail monitor affects only the PF flag.							
0	Reserved For Future Use.							
H/L	High/Low. When set to a 1, the INT pin is driven active high. When set to 0, the INT pin is open drain, active LOW.							
P/L	Pulse/Level. When set to a 1, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to a 0, the INT pin is driven to an active level (as set by H/L) until the Flags/Control register is READ.							
0x1FFF5	**Alarm – Day**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10s Alarm Date		Alarm Date			
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
$\overline{M}$	Match. Setting this bit to 0 causes the date value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.							
0x1FFF4	**Alarm – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10s Alarm Hours		Alarm Hours			
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
$\overline{M}$	Match. Setting this bit to 0 causes the hours value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hour value.							
0x1FFF3	**Alarm – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10s Alarm Minutes		Alarm Minutes			
	Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.							
$\overline{M}$	Match. Setting this bit to 0 causes the minutes value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the minute value.							
0x1FFF2	**Alarm – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10s Alarm Seconds		Alarm Seconds			
	Contains the alarm value for the seconds and the mask bit to select or deselect the second value.							
$\overline{M}$	Match. Setting this bit to 0 causes the second value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the second value.							
0x1FFF1	**Time Keeping – Centuries**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s Centuries		Centuries			

Table 4. Register Map Detail (continued)

0x1FFF0	Flags							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDF	AF	PF	OSCF	0	CAL	W	R
WDF	Watchdog Timer Flag. This READ only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags/Control register is READ.							
AF	Alarm Flag. This READ only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags/Control register is READ.							
PF	Power Fail Flag. This READ only bit is set to 1 when power falls below the power fail threshold V_{SWITCH}. It is cleared to 0 when the Flags/Control register is READ.							
OSCF	Oscillator Fail Flag. Set to 1 on power up only if the oscillator is not running in the first 5 ms of power on operation. This indicates that time counts are no longer valid. The user must reset this bit to 0 to clear this condition. The chip will not clear this flag. This bit survives power cycles.							
CAL	Calibration Mode. When set to 1, a 512 Hz square wave is output on the INT pin. When set to 0, the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power up.							
W	Write Time. Setting the W bit to 1 freeze updates of the timekeeping registers. The user can then WRITE them with updated values. Setting the W bit to 0 causes the contents of the time registers to be transferred to the timekeeping counters. The W-bit enables writes to RTC, Alarm, Calibration, Interrupt, and Flag registers.							
R	READ Time. Setting the R bit to 1 copies a static image of the timekeeping registers and places them in a holding register. The user can then READ them without concerns over changing values causing system errors. The R bit going from 0 to 1 causes the timekeeping capture, so the bit must be returned to 0 before reading again.							

Maximum Ratings

Exceeding maximum ratings may impair the useful life of device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ..... –0.5V to 4.1V

Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V

Input Voltage ..... –0.5V to Vcc + 0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Pb Soldering Temperature (3 Seconds) ..... +260°C

Output Short Circuit Current [5] ..... 15 mA

Static Discharge Voltage ..... > 2001V (in accordance with MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	–40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics

Over the Operating Range (VCC = 2.7V to 3.6V) [6, 7, 8]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		65 55 50	mA mA mA
			Industrial		55 (t_{RC} = 45 ns)	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			6	mA
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200 ns, 3V, 25°C typical	$\overline{WE}$ > (V_{CC} – 0.2). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{SB}	V_{CC} Standby Current	$\overline{WE}$ > (V_{CC} – 0.2). All others V_{IN} < 0.2V or > (V_{CC}–0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz			3	mA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$		–1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$, $\overline{CE}$ or $\overline{OE}$ > V_{IH}		–1	+1	µA
V_{IH}	Input HIGH Voltage[9]			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and V_{SS}, 5V rated		17	120	µF

Notes

5. Outputs shorted for no more than one second. No more than one output shorted at a time.
6. Typical conditions for the active current shown at the beginning of the data sheet are average values at 25°C (room temperature), and V_{CC} = 3V. Not 100% tested.
7. The HSB pin has I_{OUT} = –10 µA for V_{OH} of 2.4 V, this parameter is characterized but not tested.
8. The INT pin is open drain and does not source or sink current when interrupt register bit D3 is low.
9. V_{IH} changes by 100 mV when V_{CC} > 3.5V.

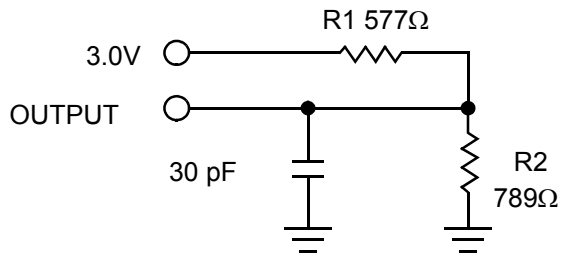
Capacitance [10]

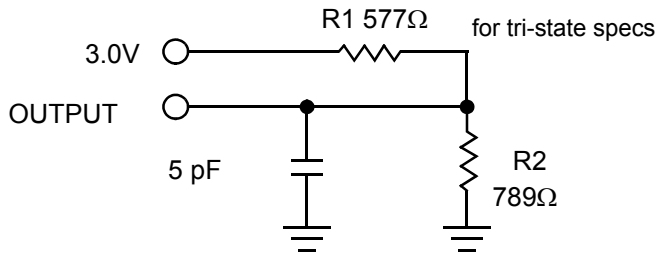
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0 V	7	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance [10]

Parameter	Description	Test Conditions	48-SSOP	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	TBD	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		TBD	°C/W

AC Test Loads





AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% - 90%) ..... ≤5 ns
Input and Output Timing Reference Levels ..... 1.5 V

Note
10. These parameters are guaranteed but not tested.

AC Switching Characteristics

Parameter		Description	25 ns part		35 ns part		45 ns part		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	Min	Max	
SRAM READ Cycle									
t_{ACE}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
t_{RC} [11]	t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA} [12]	t_{AA}	Address Access Time		25		35		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		12		15		20	ns
t_{OHA} [12]	t_{OH}	Output Hold After Address Change	3		3		3		ns
t_{LZCE} [13]	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
t_{HZCE} [13]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
t_{LZOE} [13]	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
t_{HZOE} [13]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
t_{PU} [10]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
t_{PD} [10]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns
SRAM WRITE Cycle									
t_{WC}	t_{WC}	Write Cycle Time	25		35		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	20		25		30		ns
t_{SCE}	t_{CW}	Chip Enable To End of Write	20		25		30		ns
t_{SD}	t_{DW}	Data Setup to End of Write	10		12		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AW}	Address Setup to End of Write	20		25		30		ns
t_{SA}	t_{AS}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		0		ns
t_{HZWE} [13, 14]	t_{WZ}	Write Enable to Output Disable		10		13		15	ns
t_{LZWE} [13]	t_{OW}	Output Active after End of Write	3		3		3		ns

AutoStore/Power Up RECALL

Parameter	Description	CY14B101K		Unit
		Min	Max	
$t_{HRECALL}$ [15]	Power Up RECALL Duration		20	ms
t_{STORE} [16, 17]	STORE Cycle Duration		12.5	ms
V_{SWITCH}	Low Voltage Trigger Level		2.65	V
$t_{VCCRISE}$	VCC Rise Time	150		µs

Notes
11. $\overline{WE}$ must be HIGH during SRAM READ cycles.
12. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both low.
13. Measured ±200 mV from steady state output voltage.
14. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.
15. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
16. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE takes place.
17. Industrial grade devices require 15 ms max.

Software Controlled STORE/RECALL Cycle [18, 19, 20]

Parameter	Description	25 ns part		35 ns part		45 ns part		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{CW}	Clock Pulse Width	20		25		30		ns
t_{GHAX}	Address Hold Time	1		1		1		ns
t_{RECALL}	RECALL Duration		100		100		100	µs
t_{SS} [21, 22]	Soft Sequence Processing Time		70		70		70	µs

Hardware STORE Cycle

Parameter	Description	CY14B101K		Unit
		Min	Max	
t_{DELAY} [23]	Time allowed to complete SRAM Cycle	1	70	µs
t_{HLHX}	Hardware STORE Pulse Width	15		ns

RTC Characteristics

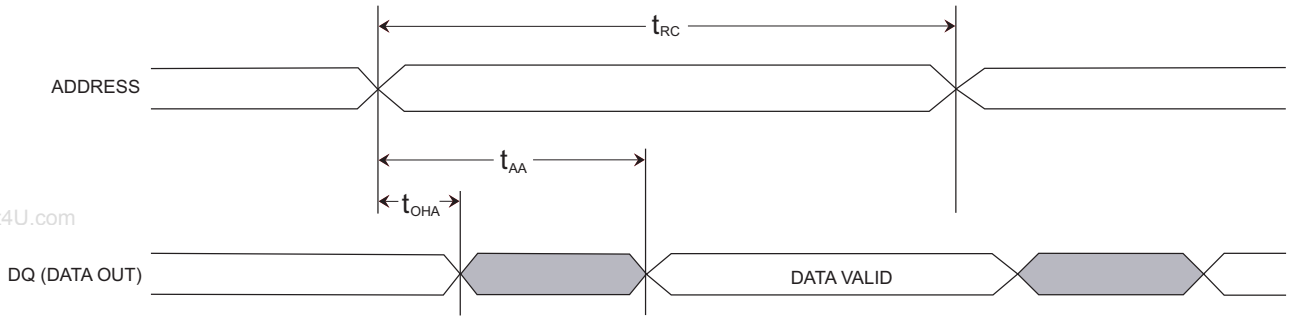
Parameters	Description	Test Conditions		Min	Max	Units
I_{BAK} [24]	RTC Backup Current		Commercial		300	nA
			Industrial		350	nA
V_{RTCbat} [25]	RTC Battery Pin Voltage		Commercial	1.8	3.3	V
			Industrial	1.8	3.3	V
V_{RTCcap} [26]	RTC Capacitor Pin Voltage		Commercial	1.2	2.7	V
			Industrial	1.2	2.7	V
tOCS	RTC Oscillator Time to Start	@Min Temperature from Power up or Enable	Commercial		10	sec
		@25°C Temperature from Power up or Enable	Commercial		5	sec
		@Min Temperature from Power up or Enable	Industrial		10	sec
		@25°C Temperature from Power up or Enable	Industrial		5	sec

Notes

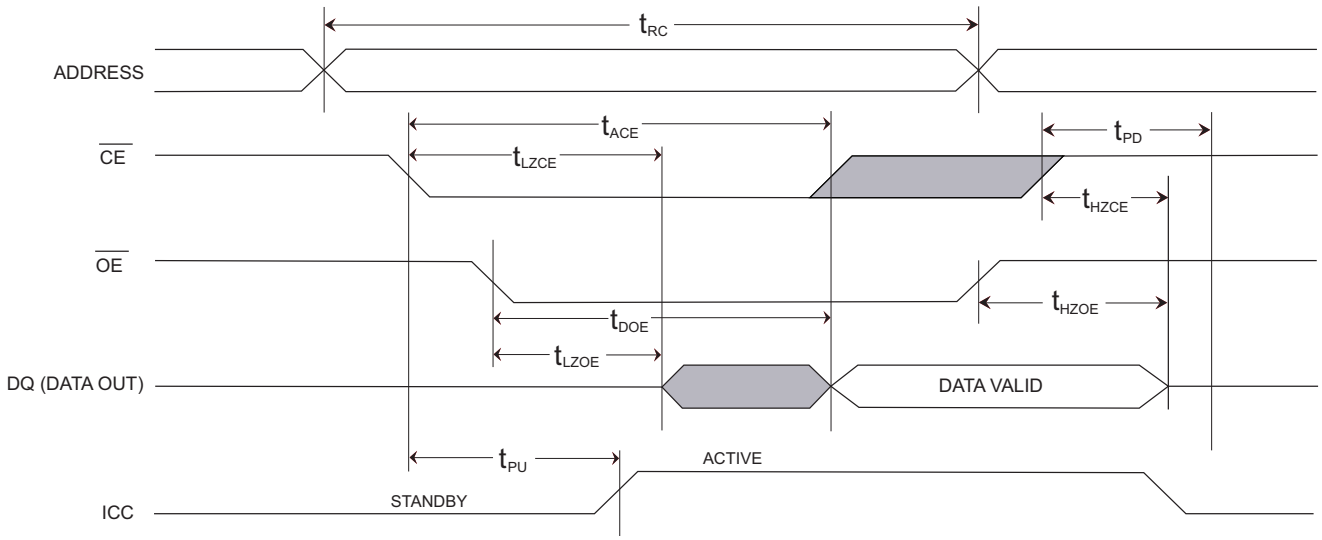
18. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled READs.
19. The six consecutive addresses must be READ in the order listed in the mode selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.
20. A 600Ω resistor must be connected to $\overline{HSB}$ to use the software command.
21. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register the command.
22. Commands like STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.
23. READ and WRITE cycles in progress before $\overline{HSB}$ are given this amount of time to complete.
24. From either V_{RTCcap} or $V_{RTCbat.}$
25. Typical = 3.0V during normal operation.
26. Typical = 2.4V during normal operation.

Switching Waveforms

SRAM Read Cycle 1 (address controlled) [11, 12, 27]



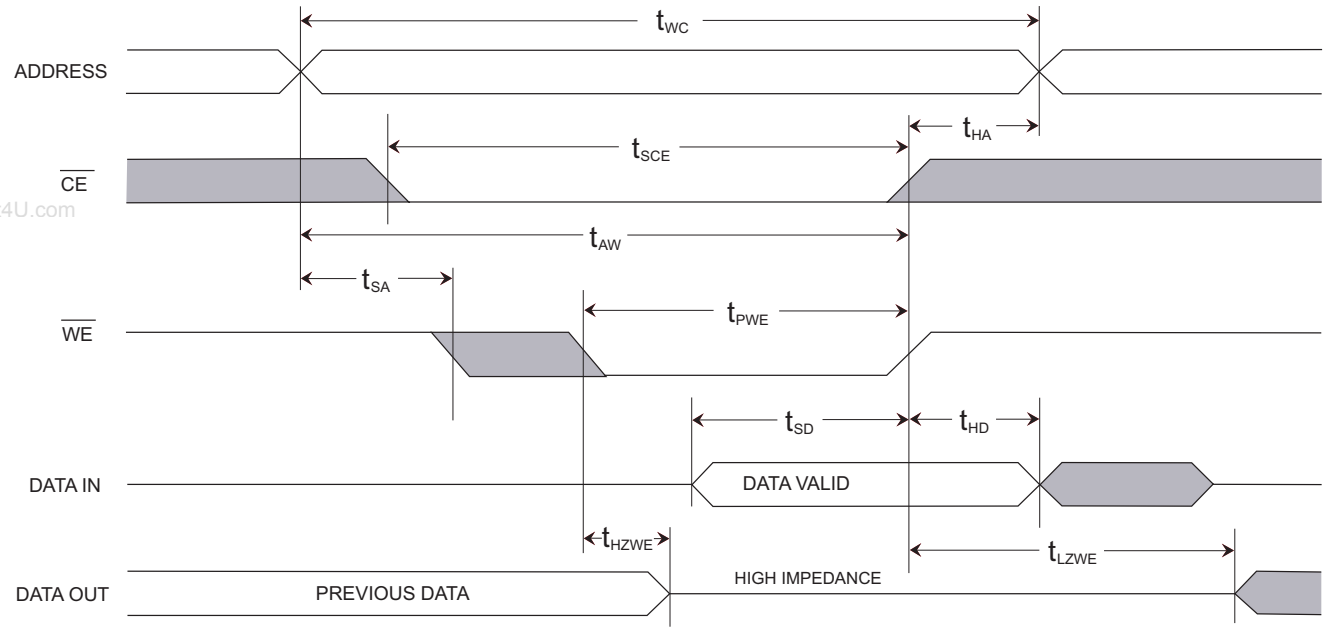
SRAM Read Cycle 2 ($\overline{CE}$ and $\overline{OE}$ controlled) [11, 27]



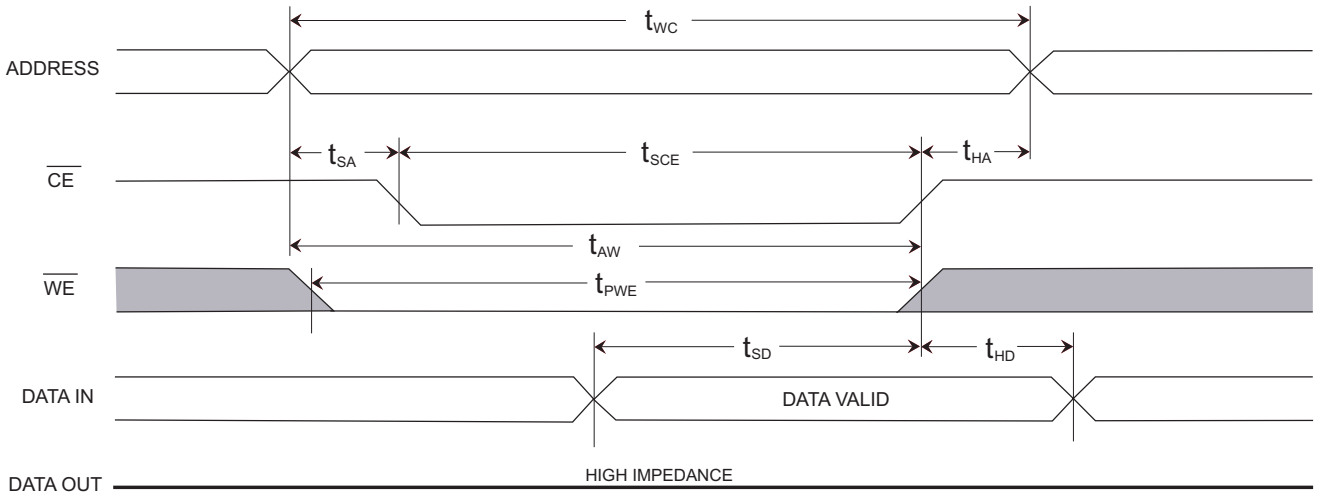
Note
27. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

SRAM WRITE Cycle 1 ($\overline{WE}$ controlled) [27, 28]



SRAM WRITE Cycle 2 ($\overline{CE}$ controlled)



Note
28. $\overline{CE}$ or $\overline{WE}$ must be > V_{IH} during address transitions.

Switching Waveforms (continued)

Figure 5. AutoStore/Power Up RECALL

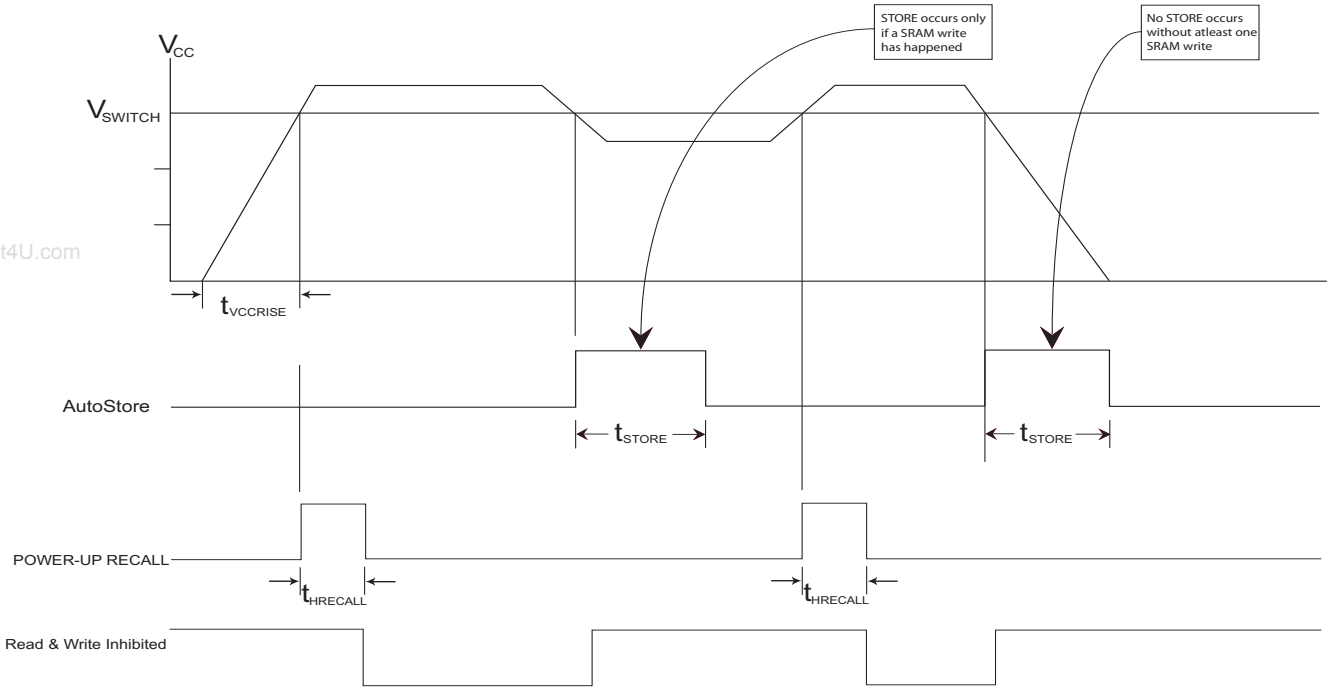
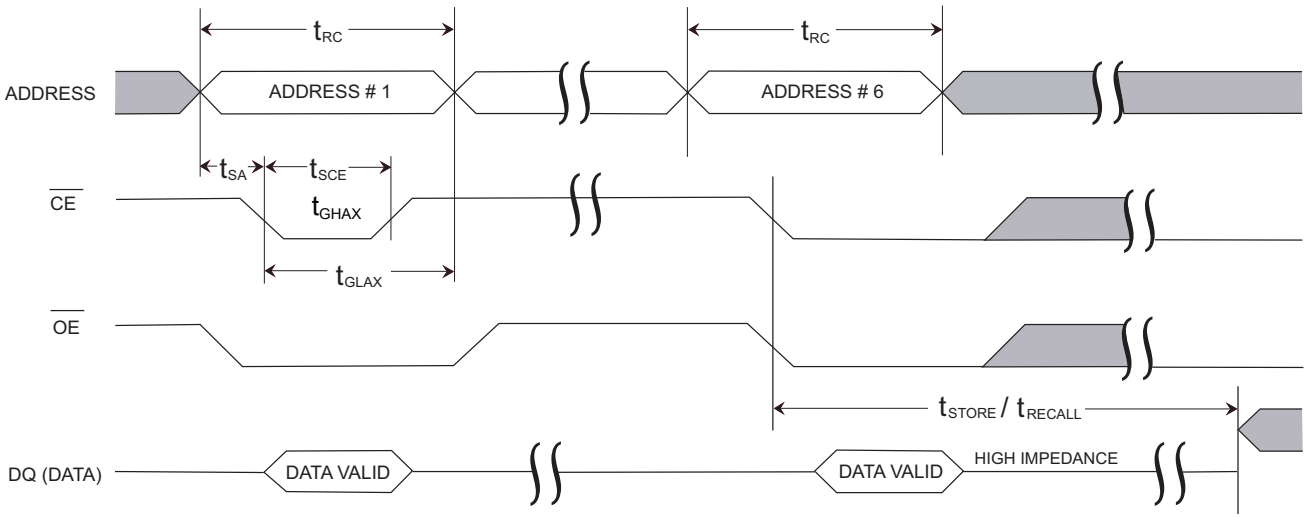


Figure 6. $\overline{CE}$-Controlled Software STORE/RECALL Cycle [19]



Switching Waveforms (continued)

Figure 7. $\overline{OE}$-Controlled Software STORE/RECALL Cycle [19]

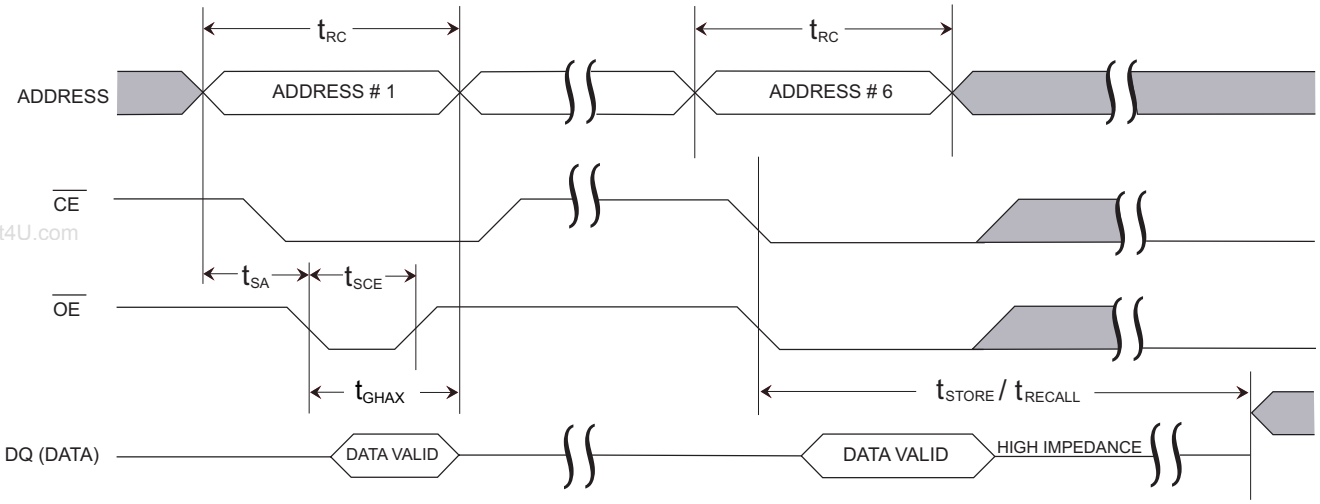


Figure 8. Hardware STORE Cycle

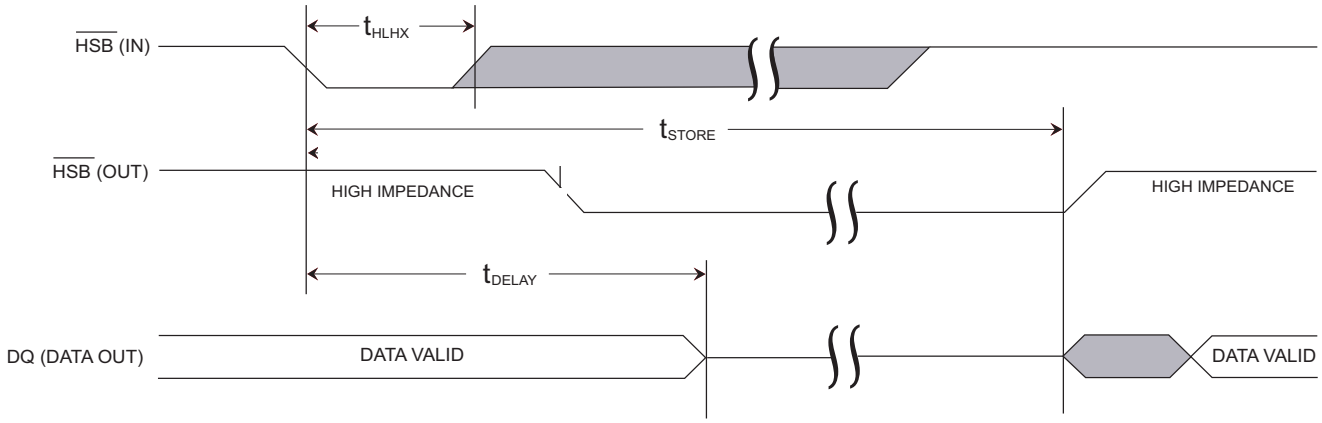
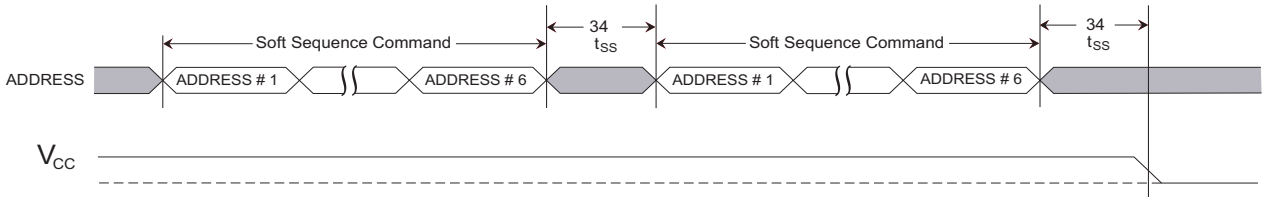
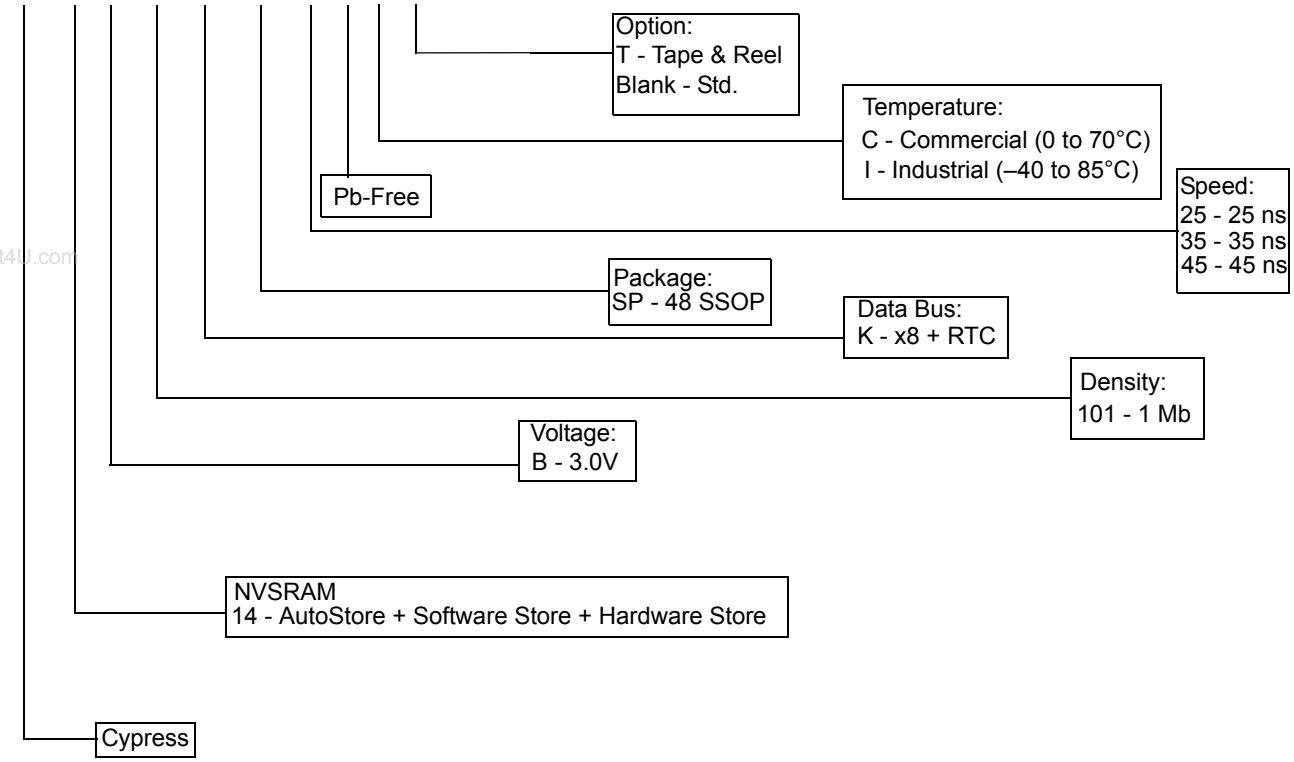


Figure 9. Soft Sequence Processing [21, 22]



PART NUMBERING NOMENCLATURE

CY 14 B 101 K - SP 25 X C T



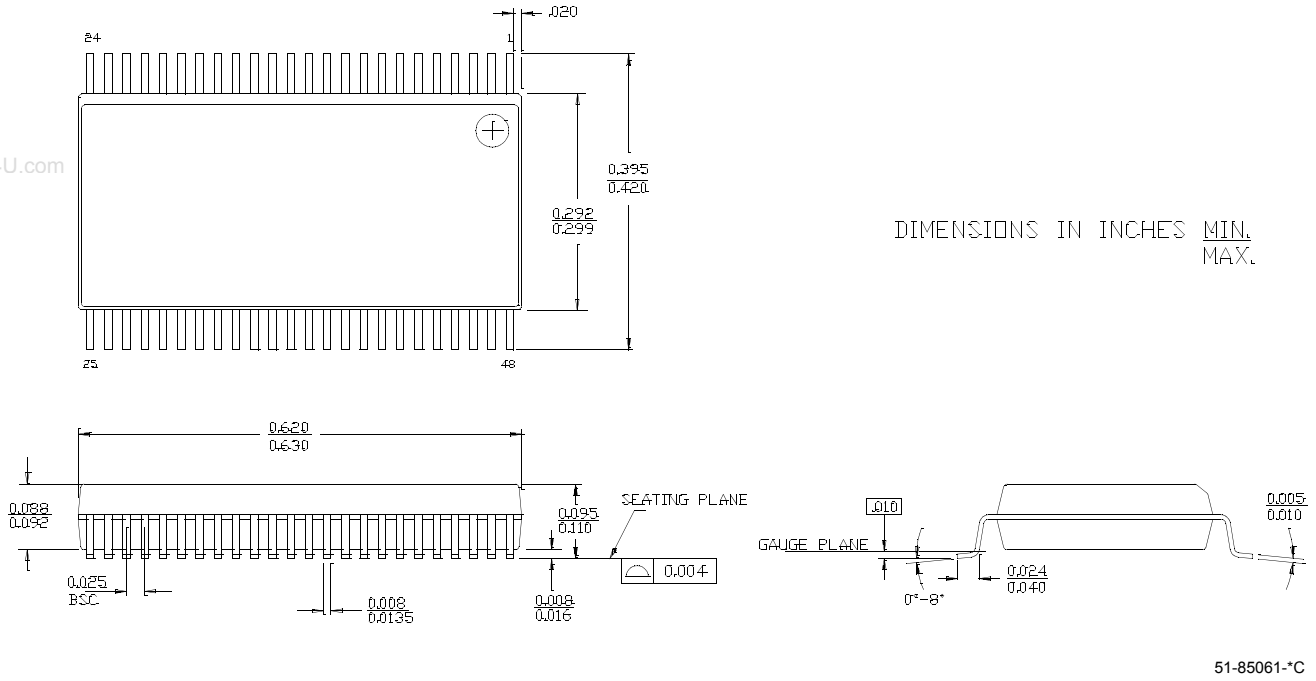
Ordering Information

All of the above mentioned parts are of “Pb-free” type. Shaded areas contain advance information. Contact your local Cypress sales representative for availability of these parts.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B101K-SP25XCT	51-85061	48-pin SSOP	Commercial
35	CY14B101K-SP35XCT	51-85061	48-pin SSOP	Commercial
45	CY14B101K-SP45XCT	51-85061	48-pin SSOP	Commercial
45	CY14B101K-SP45XIT	51-85061	48-pin SSOP	Industrial
	CY14B101K-SP45XI	51-85061	48-pin SSOP	

Package Diagram

Figure 10. 48-Pin Shrunk Small Outline Package, 51-85061



Document History Page

Document Title: CY14B101K 1 Mbit (128K x 8) nvSRAM With Real-Time Clock Document Number: 001-06401				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	425138	See ECN	TUP	New Data Sheet
*A	437321	See ECN	TUP	Show Data Sheet on External Web
*B	471966	See ECN	TUP	Changed I_{CC3} from 5 mA to 10 mA Changed ISB from 2 mA to 3 mA Changed $V_{IH(min)}$ from 2.2V to 2.0V Changed t_{RECALL} from 40 µs to 100 µs Changed Endurance from 1Million Cycles to 500K Cycles Changed Data Retention from 100 Years to 20 Years Added Soft Sequence Processing Time Waveform Updated Part Numbering Nomenclature and Ordering Information Added RTC Characteristics Table Added RTC Recommended Component Configuration
*C	503272	See ECN	PCI	Changed from Advance to Preliminary Changed the term “Unlimited” to “Infinite” Changed Endurance from 500K Cycles to 200K Cycles Added temperature spec. to Data Retention - 20 years at 55°C Removed Icc_1 values from the DC table for 25 ns and 35 ns Industrial Grade Changed Icc_2 value from 3 mA to 6 mA in the DC Table Added a footnote on V_{IH} Added footnote 18 related to using the software command Changed $V_{SWITCH(min)}$ from 2.55V to 2.45V Updated Part Nomenclature Table and Ordering Information Table
*D	597002	See ECN	TUP	Removed $V_{SWITCH(min)}$ spec from the AutoStore/Power Up RECALL Table Changed t_{GLAX} spec from 20 ns to 1 ns Added $t_{DELAY(max)}$ spec of 70 µs in the Hardware STORE Cycle Table Removed t_{HLBL} specification Changed t_{SS} specification form 70 µs (min) to 70 µs (max) Changed $V_{CAP(max)}$ from 57 µF to 120 µF
*E	688776	See ECN	VKN	Added footnote 7 related to $\overline{HSB}$ Added footnote 8 related to INT pin Changed t_{GLAX} to t_{GHAX} Removed ABE bit from interrupt register