

# 16-Mbit (1 M × 16) Static RAM

## Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V to 2.25 V
- Ultra low standby power
  - Typical standby current: 1.5  $\mu$ A
  - Maximum standby current: 12  $\mu$ A
- Ultra low active power
  - Typical active current: 2.2 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball very fine ball grid array (VFBGA) packages

## Functional Description

The CY62167EV18 is a high performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an

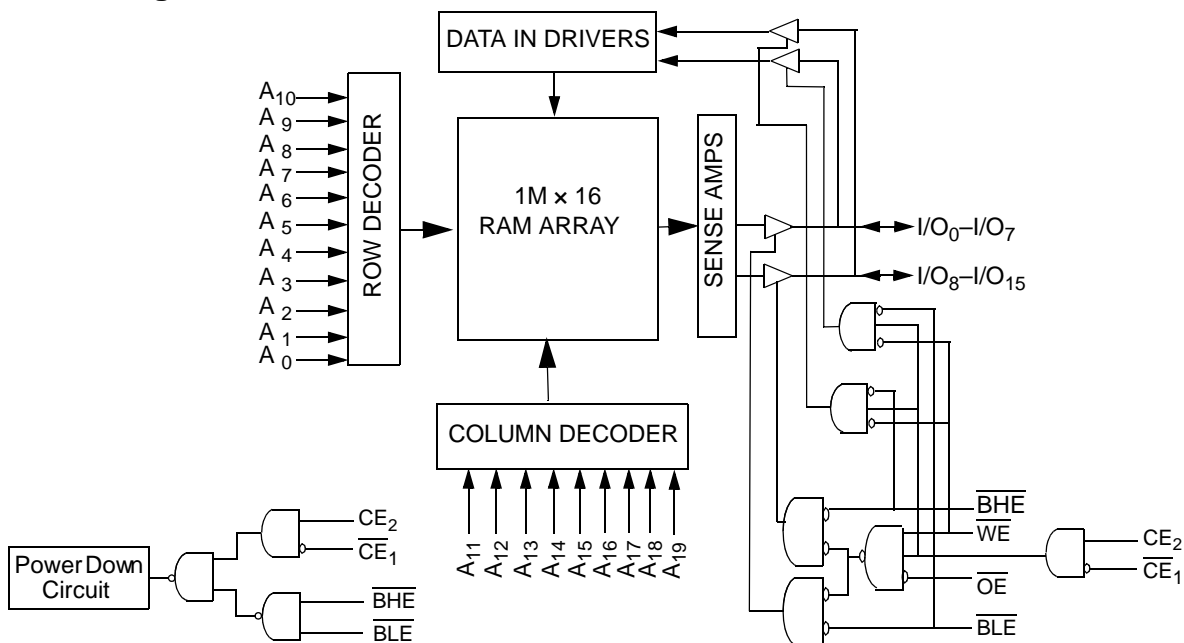
automatic power down feature that reduces power consumption by 99 percent when addresses are not toggling. Place the device into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when: the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW); outputs are disabled ( $\overline{OE}$  HIGH); both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH); and a write operation is in progress ( $CE_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW).

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

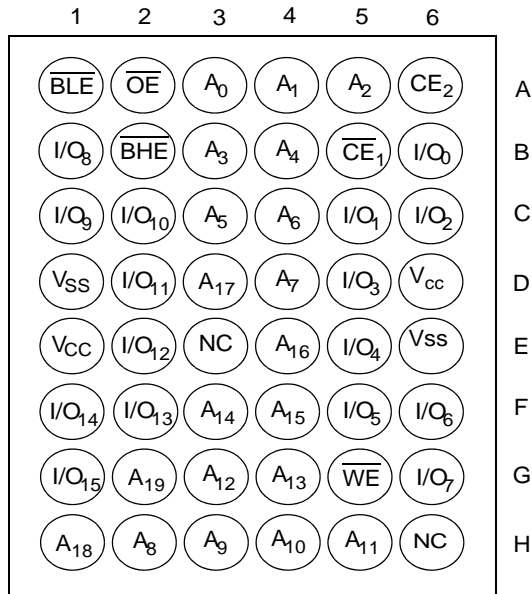


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## Pin Configurations

Figure 1. 48-Ball VFBGA pinout (Top View) <sup>[1, 2]</sup>



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1 MHz		f = f <sub>max</sub>			
Min	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max		
CY62167EV18LL	1.65	1.8	2.25	55	2.2	4.0	25	30	1.5	12
CY62167EV30LL <sup>[4]</sup>										

### Notes

1. NC pins are not connected on the die.
2. Ball H6 for the VFBGA package can be used to upgrade to a 32 M density.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
4. This part can be operated in the V<sub>CC</sub> range of 1.65 V–2.25 V at 55ns speed. It can also be operated in the V<sub>CC</sub> range of 2.2 V–3.6 V at 45ns speed.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature with power applied ..... -55 °C to + 125 °C

Supply voltage to ground potential ..... -0.2 V to 2.45 V ( $V_{CC(max)}$  + 0.2 V)

DC voltage applied to outputs in High Z state <sup>[5, 6]</sup> ..... -0.2 V to 2.45 V ( $V_{CC(max)}$  + 0.2 V)

DC input voltage<sup>[5, 6]</sup> ..... -0.2 V to 2.45 V ( $V_{CC(max)}$  + 0.2 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch up current ..... >200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[7]</sup>
CY62167EV18LL	Industrial	-40 °C to +85 °C	1.65 V to 2.25 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ <sup>[8]</sup>	Max	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -0.1$ mA	1.4	–	–	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 0.1$ mA	–	–	0.2	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 1.65$ V to 2.25 V	1.4	–	$V_{CC} + 0.2$ V	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 1.65$ V to 2.25 V	-0.2	–	0.4	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	–	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1	–	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$	–	25	30	mA
		$f = 1$ MHz		2.2	4.0	
$I_{SB1}$ <sup>[9]</sup>	Automatic power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or (BHE and BLE) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V), $f = f_{max}$ (address and data only), $f = 0$ (OE, and WE), $V_{CC} = V_{CC(max)}$	–	1.5	12	μA
$I_{SB2}$ <sup>[9]</sup>	Automatic power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, or (BHE and BLE) $\geq V_{CC} - 0.2$ V, $f = 0$ , $V_{CC} = V_{CC(max)}$	–	1.5	12	μA

### Notes

5.  $V_{IL}(min) = -2.0$  V for pulse durations less than 20 ns.

6.  $V_{IH}(max) = V_{CC} + 0.75$  V for pulse durations less than 20 ns.

7. Full Device AC operation is based on a 100 μs ramp time from 0 to  $V_{CC}(min)$  and 200 μs wait time after  $V_{CC}$  stabilization.

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}(typ)$ ,  $T_A = 25$  °C.

9. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ), and byte enables (BHE and BLE) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.

### Capacitance

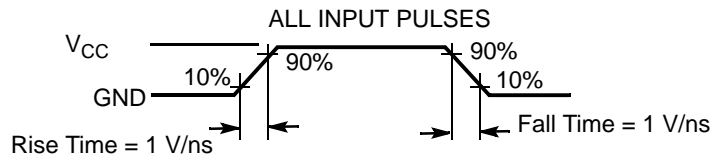
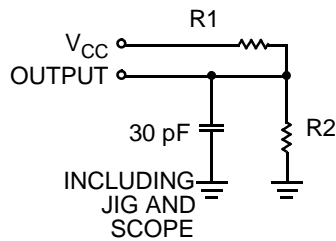
Parameter <sup>[10]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

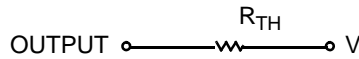
Parameter <sup>[10]</sup>	Description	Test Conditions	VFBGA	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		16	°C/W

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8 V	Unit
R1	13500	Ω
R2	10800	Ω
R <sub>TH</sub>	6000	Ω
V <sub>TH</sub>	0.80	V

**Note**

10. Tested initially and after any design or process changes that may affect these parameters.

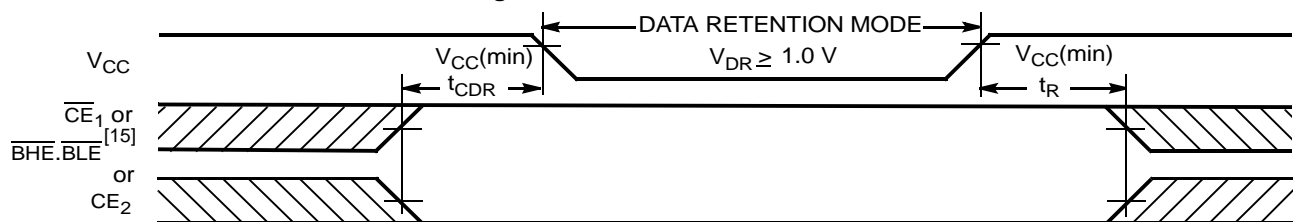
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[11]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	–	V
$I_{CCDR}$ <sup>[12]</sup>	Data retention current	$V_{CC} = 1.0\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or ( $\overline{BHE}$ and $\overline{BLE}$ ) $\geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	10	$\mu\text{A}$
$t_{CDR}$ <sup>[13]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[14]</sup>	Operation recovery time		55	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}(\text{typ})$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
12. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ), and byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$ .
15.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Parameter <sup>[16, 17]</sup>	Description	55 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
t <sub>RC</sub>	Read cycle time	55	–	ns
t <sub>AA</sub>	Address to data valid	–	55	ns
t <sub>OHA</sub>	Data hold from address change	10	–	ns
t <sub>ACE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to data valid	–	55	ns
t <sub>DOE</sub>	OE LOW to data valid	–	25	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[18]</sup>	5	–	ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[18, 19]</sup>	–	18	ns
t <sub>LZCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Low Z <sup>[18]</sup>	10	–	ns
t <sub>HZCE</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to High Z <sup>[18, 19]</sup>	–	18	ns
t <sub>PU</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to power-up	0	–	ns
t <sub>PD</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to Power-down	–	55	ns
t <sub>DBE</sub>	BLE/BHE LOW to data valid	–	55	ns
t <sub>LZBE</sub>	BLE/BHE LOW to Low Z <sup>[18]</sup>	10	–	ns
t <sub>HZBE</sub>	BLE/BHE HIGH to High Z <sup>[18, 19]</sup>	–	18	ns
<b>Write Cycle<sup>[20, 21]</sup></b>				
t <sub>WC</sub>	Write cycle time	55	–	ns
t <sub>SCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to write end	40	–	ns
t <sub>AW</sub>	Address setup to write end	40	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	WE pulse Width	40	–	ns
t <sub>BW</sub>	BLE/BHE LOW to write end	40	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[18, 19]</sup>	–	20	ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[18]</sup>	10	–	ns

### Notes

16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
17. Test conditions for all parameters other than tri-state parameters are based on signal transition time of 1 V/ns, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0 to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in Figure 2 on page 5.
18. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
19. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the output enters a high impedance state.
20. The internal memory write time is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width for Write Cycle No. 3 (WE controlled, OE LOW) should be equal to the sum of t<sub>SD</sub> and t<sub>HZWE</sub>.

### Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled).<sup>[22, 23]</sup>

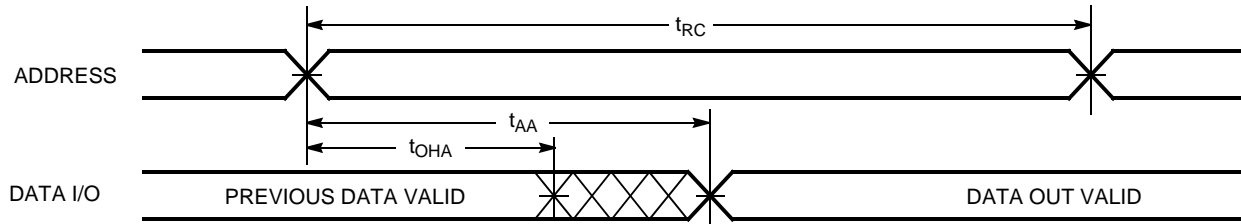
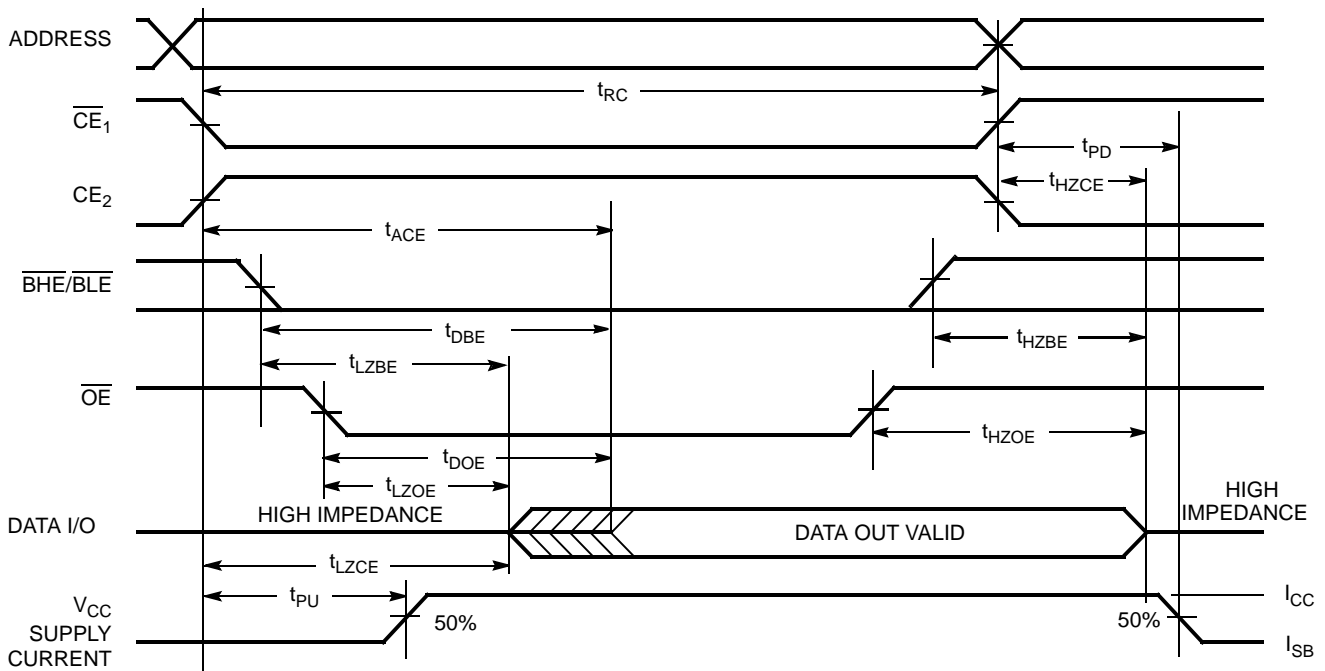


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[23, 24]</sup>



**Notes**

- 22. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .
- 23.  $\overline{WE}$  is HIGH for read cycle.
- 24. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.



Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) [25, 26, 27]

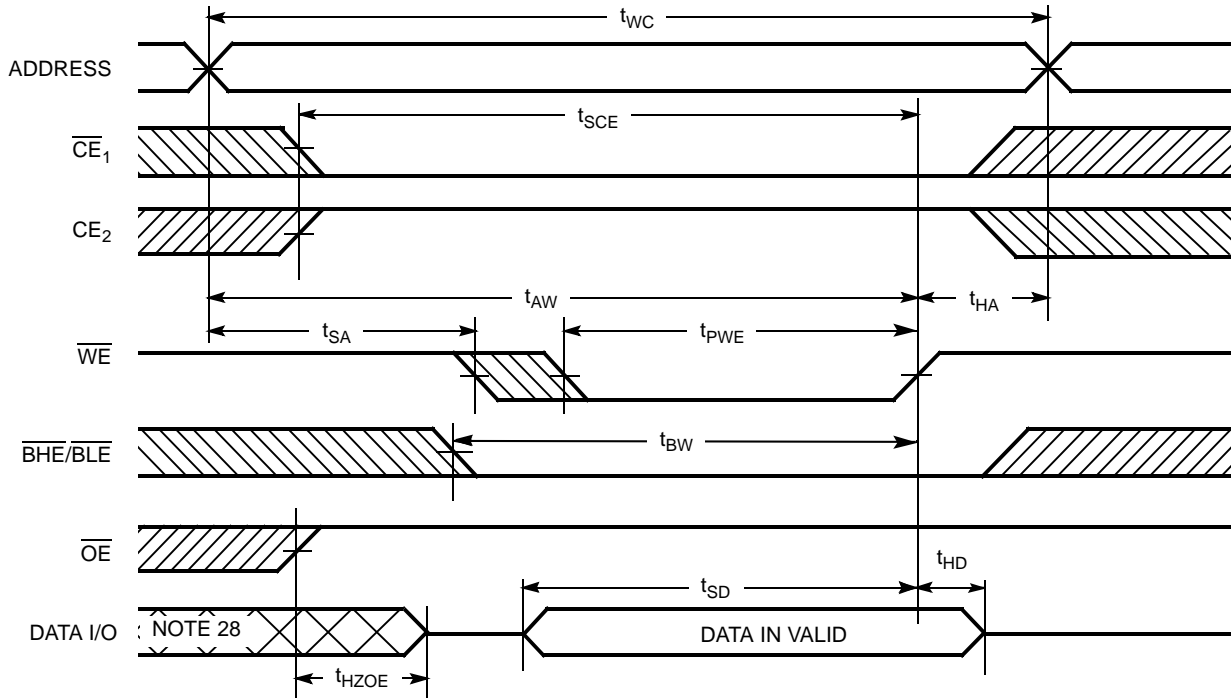
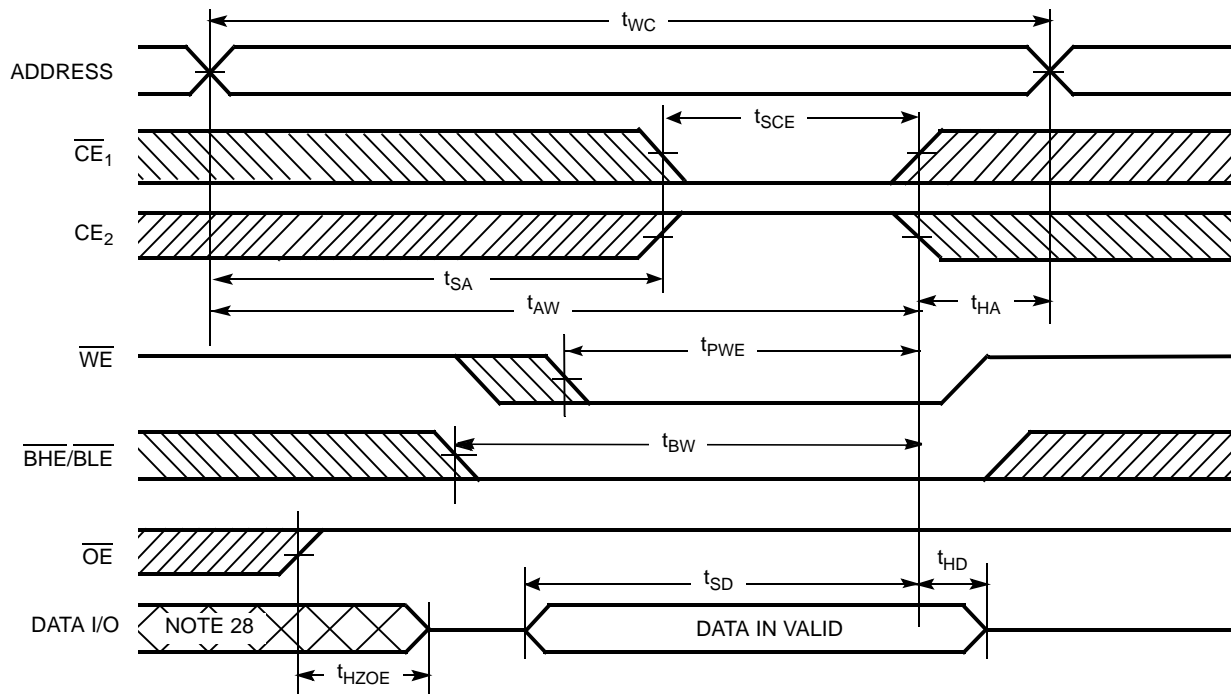


Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}_1$  or  $\overline{\text{CE}}_2$  Controlled) [25, 26, 27]



Notes

- 25. The internal memory write time is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}_1 = V_{IL}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IL}$ , and  $\text{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if  $\text{OE} = V_{IH}$ .
- 27. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = V_{IH}$ , the output remains in a high impedance state.
- 28. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) [29, 31]

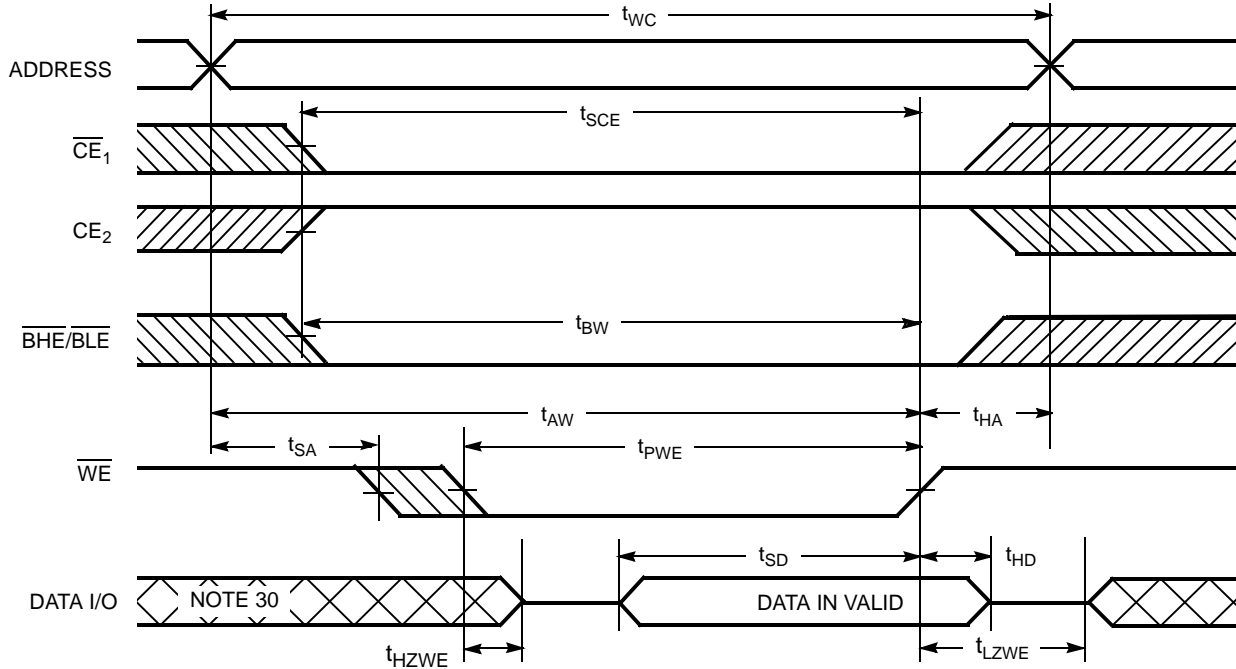
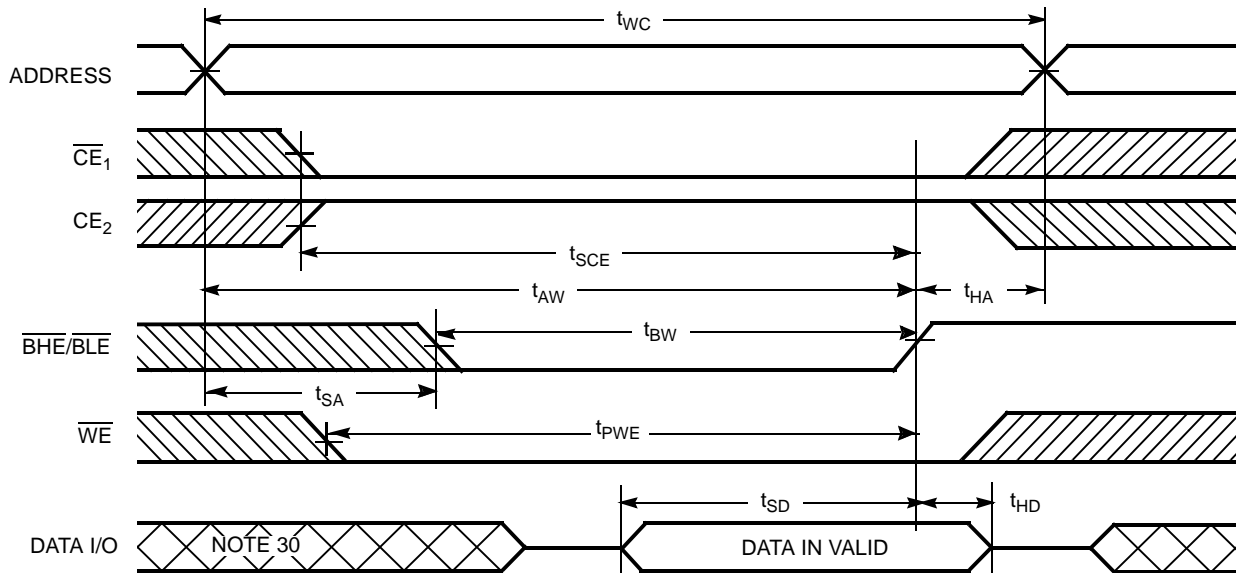


Figure 9. Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled) [29]



Notes

29. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

30. During this period the I/Os are in output state. Do not apply input signals.

31. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X <sup>[32]</sup>	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	L	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	X <sup>[32]</sup>	X	X	H	H	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data Out ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data In ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )

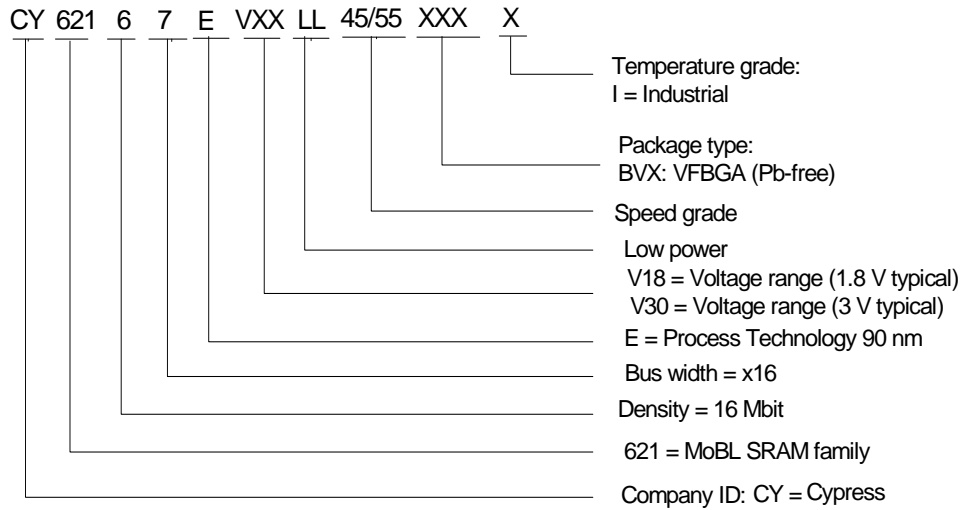
**Note**

32. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167EV18LL-55BVI	51-85150	48-ball VFBGA (6 × 8 × 1 mm)	Industrial
	CY62167EV18LL-55BVXI		48-ball VFBGA (6 × 8 × 1 mm) (Pb-free)	
	CY62167EV30LL-45BVI <sup>[33]</sup>		48-ball VFBGA (6 × 8 × 1 mm)	

### Ordering Code Definitions

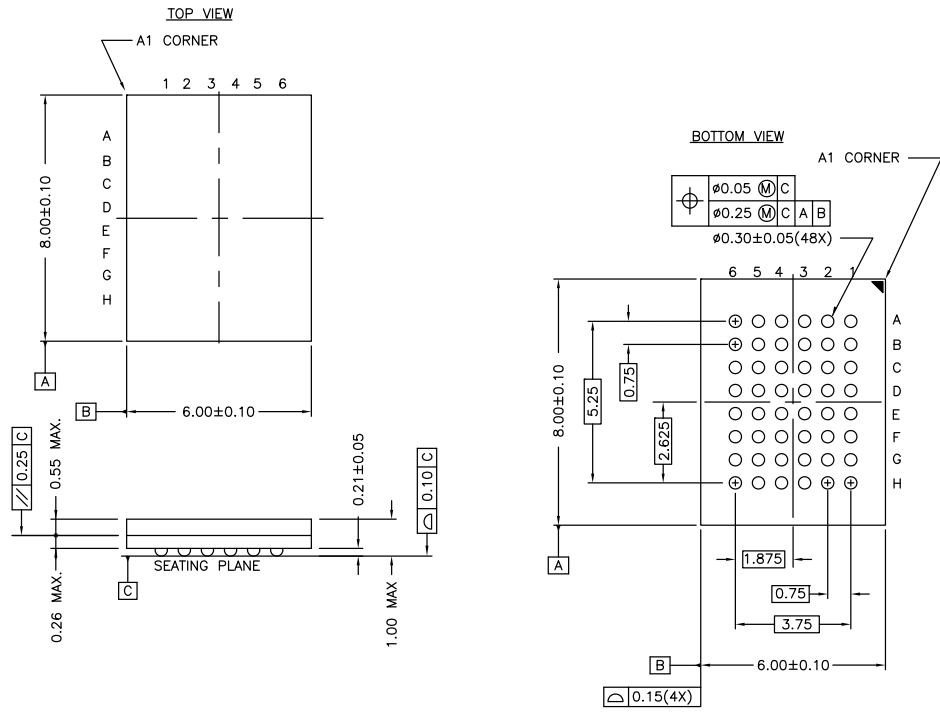


**Note**

33. This part can be operated in the V<sub>CC</sub> range of 1.65 V to 2.25 V at 55 ns speed. It can also be operated in the V<sub>CC</sub> range of 2.2 V–3.6 V at 45ns speed.

Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
 posted on the Cypress web.

51-85150 \*H

## Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY62167EV18 MoBL <sup>®</sup> , 16-Mbit (1 M × 16) Static RAM Document Number: 38-05447				
Rev.	ECN No.	Orig. of Change	Submission date	Description of Change
**	202600	AJU	01/23/2004	New data sheet.
*A	463674	NXR	See ECN	Converted from Advance Information to Preliminary Changed $V_{CC(max)}$ from 2.20 V to 2.25 V Removed 'L' bin and 35 ns speed bin from product offering Changed ball E3 from DNU to NC Removed redundant foot note on DNU Changed the $I_{SB2(typ)}$ value from 1.3 $\mu$ A to 1.5 $\mu$ A Changed the $I_{CC(max)}$ value from 40 mA to 25 mA Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics ( $t_R$ ) from 100 $\mu$ s to $t_{RC}$ ns Changed the $I_{CCDR}$ Value from 8 $\mu$ A to 5 $\mu$ A Changed $t_{OHA}$ , $t_{LZCE}$ , $t_{LZBE}$ , and $t_{LZWE}$ from 6 ns to 10 ns Changed $t_{LZOE}$ from 3 ns to 5 ns Changed $t_{HZOE}$ , $t_{HZCE}$ , $t_{HZBE}$ , and $t_{HZWE}$ from 15 ns to 18 ns Changed $t_{SCE}$ , $t_{AW}$ , and $t_{BW}$ from 40 ns to 35 ns Changed $t_{PE}$ from 30 ns to 35 ns Changed $t_{SD}$ from 20 ns to 25 ns Updated 48 ball FBGA Package Information Updated the Ordering Information table
*B	469182	NSI	See ECN	Minor Change: Moved to external web
*C	619122	NXR	See ECN	Replaced 45 ns speed bin with 55 ns speed bin
*D	1130323	VKN	See ECN	Converted from preliminary to final Added footnote# 8 related $I_{SB2}$ and $I_{CCDR}$ Changed $I_{SB1}$ and $I_{SB2}$ spec from 10 $\mu$ A to 12 $\mu$ A Changed $I_{CCDR}$ spec from 8 $\mu$ A to 10 $\mu$ A Added footnote# 13 related AC timing parameters Changed $t_{WC}$ spec from 45 ns to 55 ns Changed $t_{SCE}$ , $t_{AW}$ , $t_{PWE}$ , $t_{BW}$ spec from 35 ns to 40 ns Changed $t_{HZWE}$ spec from 18 ns to 20 ns
*E	1388287	VKN	See ECN	Added 48-Ball VFBGA (6 x 7 x 1mm) package Added footnote# 1 related to FBGA package Updated Ordering Information table
*F	1664843	VKN / AESA	See ECN	Added CY62167EV30LL-45BVI part in the Ordering Information table Added footnote# 5 related to CY62167EV30LL-45BVI part
*G	2675375	VKN / PYRS	03/17/2009	Added CY62167EV18LL-55BVI part in the Ordering Information table
*H	2904565	AJU	04/05/2010	Removed inactive part from the ordering information table. Updated package diagrams.
*I	2934396	VKN	06/03/10	Added footnote #24 related to chip enable Updated template
*J	3006301	RAME	08/12/2010	Included BHE and BLE in $I_{SB1}$ , $I_{SB2}$ , and $I_{CCDR}$ test conditions to reflect Byte power down feature. Removed 48-Ball VFBGA (6 x 7 x 1 mm) package related information. Added Acronyms and Ordering code definition. Format updates to match template.
*K	3113908	PRAS	12/17/2010	Updated Figure 1 and Package Diagram.

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Rev.	ECN No.	Orig. of Change	Submission date	Description of Change
*L	3295175	RAME	06/29/2011	Updated <a href="#">Package Diagrams</a> . Added <a href="#">Document Conventions</a> . Removed reference to AN1064 SRAM system guidelines. Added I <sub>SB1</sub> to footnotes 9 and 13. Modified <a href="#">Ordering Code Definitions</a> . Updated Table of Contents.
*M	3421697	TAVA	10/25/2011	Removed Figure caption for AC Test Loads and Waveforms Updated <a href="#">Figure 4</a> , <a href="#">Figure 5</a> , <a href="#">Figure 6</a> , <a href="#">Figure 7</a> , <a href="#">Figure 8</a> , and <a href="#">Figure 9</a> Updated <a href="#">Package Diagrams</a>
*N	4100342	VINI	08/21/2013	Updated <a href="#">Switching Characteristics</a> : Added Note 16 and referred the same note in "Parameter" column. Updated <a href="#">Package Diagrams</a> : spec 51-85150 – Changed revision from *G to *H. Removed spec 51-85183 (48-pin TSOP I Package). Updated in new template. Completing Sunset Review.
*O	4576406	VINI	01/16/2015	Added related documentation hyperlink in page 1. Added Note 21 in <a href="#">Switching Characteristics</a> . Added note reference 21 in the <a href="#">Switching Characteristics</a> table. Added Note 31 in <a href="#">Switching Waveforms</a> . Added note reference 31 in <a href="#">Figure 8</a> . Updated the Write Cycle number to 4 in <a href="#">Figure 9</a> title.



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