DS07-16907-2E

32-bit Microcontrollers

CMOS

FR80 MB91610 Series

MB91F610A/613

■ DESCRIPTION

The MB91610 series is a line of Fujitsu Microelectronics microcontrollers based on a 32-bit RISC CPU core that feature a variety of peripheral functions for embedded applications that demand high-performance and high-speed CPU processing.
This series is based on the FR80* family CPU and is implemented as a single chip.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURES

- FR80 CPU
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - General-purpose registers : 32-bit × 16
  - 16-bit fixed-length instructions (basic instructions) : 1 instruction per cycle
  - Instructions suitable for embedded applications
    - Memory-to-memory transfer, bit processing, barrel shift instructions, etc.
    - Instruction support for high level languages
      Function entry and exit instructions, instructions for register multi-load and multi-store
    - Bit search instruction
      "1" detection, "0" detection, transition point detection
    - Branch instructions with delay slots
      Reduced overhead when processing branches
    - Register interlock functions
      Facilitate coding in assembly language

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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- Built-in multiplier/instruction-level support
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupts (save PC and PS) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch function has been added with 4 word instruction queue of CPU

- Instruction compatible with FR family CPU
  - Additional bit search instructions
  - No resource instructions and coprocessor instructions

- Maximum operating frequency
  - CPU : 33 MHz
  - Resources : 33 MHz

- DMA controller (DMAC)
  - 8 channels
  - Address space : 32 bits (4 Gbytes)
  - Transfer modes : Block transfer/burst transfer/demand transfer
  - Address update : Increment/decrement/fixed (increment/decrement step size of 1, 2, or 4)
  - Transfer data length : Selectable from 8-bit, 16-bit, 32-bit
  - Block size : 1 to 16
  - Number of transfers : 1 to 65535
  - Transfer requests
    - Requests from software
    - Interrupt requests from peripheral resources (interrupt requests are shared, including external interrupts)
  - Reload functions : Reload can be specified on all channels
  - Priority order : Fixed (ch.0 > ch.1 > ch.2 > ch.3 > ...) or round-robin
  - Interrupt requests : Interrupts can be generated for transfer complete, transfer error, and transfer interrupted.

- Multifunction serial interface

  - 4 channels with 16-byte FIFO, 4 channels without FIFO
  - Operation mode is selectable from UART/CSIO/I^{2}C for each channel (For ch.0, I^{2}C is not available.)
    - UART
      - Full-duplex double buffer
      - Selectable parity on/off
      - Built-in dedicated baud rate generator
      - External clock can be used as a serial clock
      - Error detection function for parity, frame and overrun errors
    - CSIO
      - Full-duplex double buffer
      - Built-in dedicated baud rate generator
      - Overrun error detection function
    - I^{2}C
      - Supports both standard mode (Max 100 kbps) and Fast mode (Max 400 kbps)
      - Some channels are 5 V tolerant

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- Interrupts
  - Total of 16 external interrupts (some pins are 5 V tolerant)
  - Interrupts from peripheral resources
  - Programmable interrupt levels (16 levels)
  - Can be used to return from stop mode, sleep mode

- A/D converter
  - 8 channels, 1 unit
  - 10-bit resolution
  - Conversion time : approx. 1.2 μs (PCLK = 33 MHz)
  - Priority conversion (2 levels)
  - Conversion modes : Single-shot conversion mode, scan conversion mode
  - Activation sources : Software, external trigger, base timer
  - Built-in FIFO for storing conversion data (for scan conversion:16, for priority conversion:4)

- Base timer
  - 8 channels
  - Operation mode is selectable from the followings for each channel
    - 16/32-bit reload timer
    - 16-bit PWM timer
    - 16/32-bit PWC timer
    - 16-bit PPG timer
  - Cascading connection between 2 channels allows them to be used as one 32-bit timer
  - Multiple channels can be started simultaneously
  - Input/output select function

- 16-bit reload timer
  - 3 channels (including 1 channel for REALOS)
  - Interval timer function
  - Count clock select function (peripheral clock (PCLK) divided by 2 to 64)

- Compare timer
  - 32-bit input capture : 4 channels
  - 32-bit output compare : 4 channels
  - 32-bit free-run timer : 1 channel

- Other interval timers
  - Watch counter : 1 channel
  - Watchdog timer : 2 channels
    - Watchdog timer 0
      - After resetting this device, the watchdog timer becomes active when an arbitrary value is written to the WDTCPR0 register.
      - The cycle of the watchdog timer 0 can be selected from the peripheral clock (PCLK) $\times$ (2^9 to 2^{24}).
    - Watchdog timer 1
      - After releasing the reset of this device, it counts with the CPU clock (CCLK).
      - Disable/ enable of the counter operation can be controlled by HWDE pin.
      - The cycle of the watchdog timer 1 is CCLK $\times$ 2^{23} cycle fixed.

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- USB function / HOST
  - 1 channel
  - Supports Full-Speed only
  - The USB function and USB HOST are the switch types (USB I/O multiplexed)
  - Support of DMA transfer
  - USB Function
    - Support of up to six endpoints
      - Endpoint 0 is provided for the fixed use of control transfers
      - Bulk or interrupt transfer can be selected for endpoint 1 to 5
    - Double buffer structure for endpoint 1 to 5
  - USB HOST
    - Support control transfer, bulk transfer, interrupt transfer, and isochronous transfer
    - Automatic detection of connection/disconnection of USB devices
    - Automatic processing of a handshake packet for IN/OUT token processing
    - Support of a maximum packet length of up to 256 bytes
    - Support for a wakeup function

- HDMI-CEC/Remote Control Reception
  - 1 channel
  - HDMI-CEC reception function (with automatic ACK response function)
  - Remote control reception function (built-in 4-byte receive buffer)

- OSDC function
  - 16 bits RGB (256 colors available among 65536 colors)
  - Analog RGB output : Max 50 MHz
    Digital RGB output : Max 75 MHz
  - A font in 32 × 32 dots can be displayed up to 60 × 32
  - Two-layered display of MAIN/SUB
  - 16384 characters at the maximum
  - Equipped with one PLL for dot clock generation

- Main timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the main clock (MCLK)
  - Counts the oscillation stabilization wait time of the PLL clock (PLLCLK)
  - Can be used as an interval timer while the main clock (MCLK) oscillations is stable

- Sub timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the sub clock (SBCLK)
  - Can be used as an interval timer while the sub clock (SBCLK) oscillations is stable

- Clock generation
  - Main clock (MCLK) oscillator
  - Sub clock (SBCLK) oscillator
  - PLL clock (PLLCLK) oscillator

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- Low-power dissipation mode
  - Stop mode
  - Watch mode
  - Sleep mode
  - Doze mode
  - Clock division function

- Other features
  - I/O port
  - $\overline{\text{INIT}}$ pin is provided as a reset pin
  - Watchdog timer reset, software reset
  - Delay interrupt
  - Power supply
    - Single power supply (3.0 V to 3.6 V)

■ PRODUCT LINEUP

Items \ Product Name	MB91F610A	MB91613
Product type	Flash memory product	MASK ROM product
Built-in program memory capacity	512 Kbytes (Flash)	512 Kbytes (ROM)
Built-in RAM capacity	32 Kbytes	
DMA controller (DMAC)	8 channels	
Base timer	8 channels	
Multifunction serial interface	Without FIFO : 4 channels (ch.0 to ch.3) With FIFO : 4 channels (ch.8 to ch.11)	
External interrupt	16 channels	
10-bit A/D converter	8 channels (1 unit)	
16-bit reload timer	3 channels	
Compare timer	32-bit input capture : 4 channels 32-bit output compare : 4 channels 32-bit free-run timer : 1 channel	
Watch counter	1 channel	
I/O port	50 (Max)	
USB function / HOST	1 channel	
HDMI-CEC/Remote control reception	1 channel	
OSDC	Font FLASH : 16384 characters	Font ROM : 7168 characters
Main timer	1 channel	
Sub timer	1 channel	
Wild register	16 channels	
Debug function	DSU4	—

■ PACKAGES

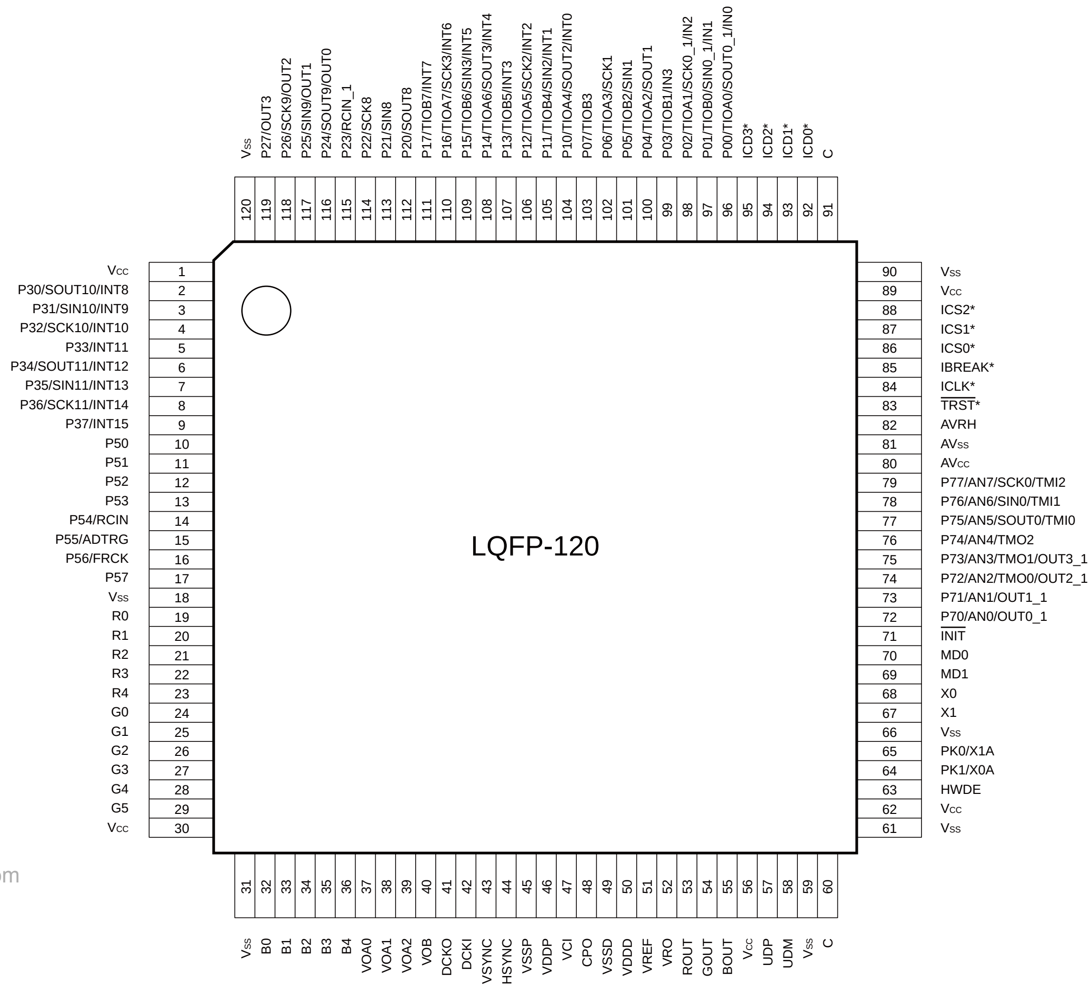
Package \ Product name	MB91F610A	MB91613
FPT-120P-M21	○	○

○ : Supported

Note: Refer to "■ PACKAGE DIMENSIONS" for detailed information on each package.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-120P-M21)

* : N.C. pin for MB91613.

Note : The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ PIN DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the port number.
For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin no.	Pin name	I/O circuit type*	Function
1	V_{CC}	—	3.3 V power supply
2	P30	C	General-purpose I/O port
	SOUT10		Multifunction serial ch.10 output [operation modes 0 to 2]
	(SDA10)		I^2C ch.10 serial data line [operation mode 4]
	INT8		External interrupt 8 input
3	P31	C	General-purpose I/O port
	SIN10		Multifunction serial ch.10 input
	INT9		External interrupt 9 input
4	P32	C	General-purpose I/O port
	SCK10		Multifunction serial ch.10 clock [operation modes 0 to 2]
	(SCL10)		I^2C ch.10 serial clock line [operation mode 4]
	INT10		External interrupt 10 input
5	P33	C	General-purpose I/O port
	INT11		External interrupt 11 input
6	P34	C	General-purpose I/O port
	SOUT11		Multifunction serial ch.11 output [operation modes 0 to 2]
	(SDA11)		I^2C ch.11 serial data line [operation mode 4]
	INT12		External interrupt 12 input
7	P35	C	General-purpose I/O port
	SIN11		Multifunction serial ch.11 input
	INT13		External interrupt 13 input
8	P36	C	General-purpose I/O port
	SCK11		Multifunction serial ch.11 clock [operation modes 0 to 2]
	(SCL11)		I^2C ch.11 serial clock line [operation mode 4]
	INT14		External interrupt 14 input
9	P37	C	General-purpose I/O port
	INT15		External interrupt 15 input
10	P50	B	General-purpose I/O port
11	P51	B	General-purpose I/O port

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
12	P52	B	General-purpose I/O port
13	P53	B	General-purpose I/O port
14	P54	B	General-purpose I/O port
	RCIN		Remote control I/O
15	P55	B	General-purpose I/O port
	ADTRG		A/D converter external trigger input
16	P56	B	General-purpose I/O port
	FRCK		Free-run timer clock input
17	P57	B	General-purpose I/O port
18	V_{SS}	—	GND
19	R0	H	RGB digital output
20	R1	H	RGB digital output
21	R2	H	RGB digital output
22	R3	H	RGB digital output
23	R4	H	RGB digital output
24	G0	H	RGB digital output
25	G1	H	RGB digital output
26	G2	H	RGB digital output
27	G3	H	RGB digital output
28	G4	H	RGB digital output
29	G5	H	RGB digital output
30	V_{CC}	—	3.3V power supply
31	V_{SS}	—	GND
32	B0	H	RGB digital output
33	B1	H	RGB digital output
34	B2	H	RGB digital output
35	B3	H	RGB digital output
36	B4	H	RGB digital output
37	VOA0	H	Alpha blend output
38	VOA1	H	Alpha blend output
39	VOA2	H	Alpha blend output

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
40	VOB	H	OSD display period output
41	DCKO	H	Dot clock output
42	DCKI	F	Dot clock input
43	VSYNC	F	Vertical synchronous input
44	HSYNC	F	Horizontal synchronous input
45	VSSP	—	Dot clock PLL ground
46	VDDP	—	Dot clock PLL power supply
47	VCI	—	VCO control voltage input
48	CPO	M	Charge pump output
49	VSSD	—	RGB analog output GND
50	VDDD	—	RGB analog output power supply
51	VREF	M	RGB analog output reference power supply
52	VRO	M	RGB analog output resistance connected pin
53	ROUT	M	R output (analog)
54	GOUT	M	G output (analog)
55	BOUT	M	B output (analog)
56	V_{CC}	—	3.3 V power supply
57	UDP	USB	USB pin
58	UDM	USB	USB pin
59	V_{SS}	—	GND
60	C	—	C pin for a regulator
61	V_{SS}	—	GND
62	V_{CC}	—	3.3 V power supply
63	HWDE	F	Hardware watchdog enable input
64	PK1	G	General-purpose I/O port
	X0A		32kHz oscillation pin
65	PK0	G	General-purpose I/O port
	X1A		32 kHz oscillation pin
66	V_{SS}	—	GND
67	X1	A	Main oscillation pin
68	X0	A	Main oscillation pin

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Pin no.	Pin name	I/O circuit type*	Function
69	MD1	F, L	Mode pin
70	MD0	F, L	Mode pin
71	$\overline{\text{INIT}}$	F, L	Initial (reset) pin
72	P70	D	General-purpose I/O port
	AN0		A/D converter ch.0 analog input
	OUT0_1		Output compare ch.0 output (Port 1)
73	P71	D	General-purpose I/O port
	AN1		A/D converter ch.1 analog input
	OUT1_1		Output compare ch.1 output (Port 1)
74	P72	D	General-purpose I/O port
	AN2		A/D converter ch.2 analog input
	TMO0		Reload timer ch.0 output
	OUT2_1		Output compare ch.2 output (Port 1)
75	P73	D	General-purpose I/O port
	AN3		A/D converter ch.3 analog input
	TMO1		Reload timer ch.1 output
	OUT3_1		Output compare ch.3 output (Port 1)
76	P74	D	General-purpose I/O port
	AN4		A/D converter ch.4 analog input
	TMO2		Reload timer ch.2 output
77	P75	D	General-purpose I/O port
	AN5		A/D converter ch.5 analog input
	SOUT0		Multifunction serial ch.0 output [operation modes 0 to 2]
	TMI0		Reload timer ch.0 input
78	P76	D	General-purpose I/O port
	AN6		A/D converter ch.6 analog input
	SIN0		Multifunction serial ch.0 input
	TMI1		Reload timer ch.1 input

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
79	P77	D	General-purpose I/O port
	AN7		A/D converter ch.7 analog input
	SCK0		Multifunction serial ch.0 clock [operation modes 0 to 2]
	TMI2		Reload timer ch.2 input
80	AV_{CC}	—	A/D converter analog power supply
81	AV_{SS}	—	A/D converter GND
82	AVRH	—	A/D converter analog reference power supply
83	$\overline{TRST}$	E	Tool reset input for DSU4 N.C. pin for MASK products.
84	ICLK	K	Clock pin for DSU4 N.C. pin for MASK products.
85	IBREAK	I	Break pin for DSU4 N.C. pin for MASK products.
86	ICS0	H	DSU4 status N.C. pin for MASK products.
87	ICS1	H	DSU4 status N.C. pin for MASK products.
88	ICS2	H	DSU4 status N.C. pin for MASK products.
89	V_{CC}	—	3.3 V power supply
90	V_{SS}	—	GND
91	C	—	C pin for a regulator
92	ICD0	J	DSU4 data N.C. pin for MASK products.
93	ICD1	J	DSU4 data N.C. pin for MASK products.
94	ICD2	J	DSU4 data N.C. pin for MASK products.
95	ICD3	J	DSU4 data N.C. pin for MASK products.
96	P00	B	General-purpose I/O port
	TIOA0		Base timer ch.0 TIOA
	SOUT0_1		Multifunction serial ch.0 output (Port 1) [operation modes 0 to 2]
	IN0		Input capture ch.0 input

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Pin no.	Pin name	I/O circuit type*	Function
97	P01	B	General-purpose I/O port
	TIOB0		Base timer ch.0 TIOB
	SIN0_1		Multifunction serial ch.0 input (Port 1)
	IN1		Input capture ch.1 input
98	P02	B	General-purpose I/O port
	TIOA1		Base timer ch.1 TIOA
	SCK0_1		Multifunction serial ch.0 clock (Port 1) [operation modes 0 to 2]
	IN2		Input capture ch.2 input
99	P03	B	General-purpose I/O port
	TIOB1		Base timer ch.1 TIOB
	IN3		Input capture ch.3 input
100	P04	B	General-purpose I/O port
	TIOA2		Base timer ch.2 TIOA
	SOUT1		Multifunction serial ch.1 output [operation modes 0 to 2]
	(SDA1)		I²C ch.1 serial data line [operation mode 4]
101	P05	B	General-purpose I/O port
	TIOB2		Base timer ch.2 TIOB
	SIN1		Multifunction serial ch.1 input
102	P06	B	General-purpose I/O port
	TIOA3		Base timer ch.3 TIOA
	SCK1		Multifunction serial ch.1 clock [operation modes 0 to 2]
	(SCL1)		I²C ch.1 serial clock line [operation mode 4]
103	P07	B	General-purpose I/O port
	TIOB3		Base timer ch.3 TIOB
104	P10	B	General-purpose I/O port
	TIOA4		Base timer ch.4 TIOA
	SOUT2		Multifunction serial ch.2 output [operation modes 0 to 2]
	(SDA2)		I²C ch.2 serial data line [operation mode 4]
	INT0		External interrupt 0 input

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
105	P11	B	General-purpose I/O port
	TIOB4		Base timer ch.4 TIOB
	SIN2		Multifunction serial ch.2 input
	INT1		External interrupt 1 input
106	P12	B	General-purpose I/O port
	TIOA5		Base timer ch.5 TIOA
	SCK2		Multifunction serial ch.2 clock [operation modes 0 to 2]
	(SCL2)		I^2C ch.2 serial clock line [operation mode 4]
	INT2		External interrupt 2 input
107	P13	B	General-purpose I/O port
	TIOB5		Base timer ch.5 TIOB
	INT3		External interrupt 3 input
108	P14	B	General-purpose I/O port
	TIOA6		Base timer ch.6 TIOA
	SOUT3		Multifunction serial ch.3 output [operation modes 0 to 2]
	(SDA3)		I^2C ch.3 serial data line [operation mode 4]
	INT4		External interrupt 4 input
109	P15	B	General-purpose I/O port
	TIOB6		Base timer ch.6 TIOB
	SIN3		Multifunction serial ch.3 input
	INT5		External interrupt 5 input
110	P16	B	General-purpose I/O port
	TIOA7		Base timer ch.7 TIOA
	SCK3		Multifunction serial ch.3 clock [operation modes 0 to 2]
	(SCL3)		I^2C ch.3 serial clock line [operation mode 4]
	INT6		External interrupt 6 input
111	P17	B	General-purpose I/O port
	TIOB7		Base timer ch.7 TIOB
	INT7		External interrupt 7 input
112	P20	C	General-purpose I/O port
	SOUT8		Multifunction serial ch.8 output [operation modes 0 to 2]
	(SDA8)		I^2C ch.8 serial data line [operation mode 4]

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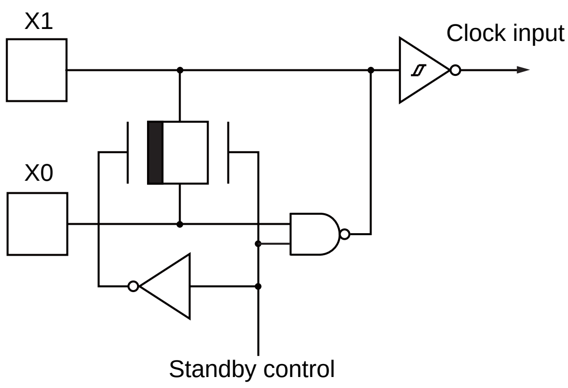
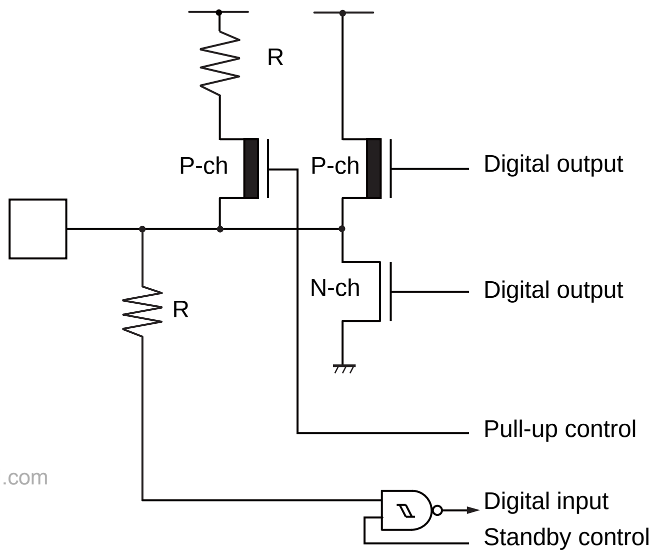
Pin no.	Pin name	I/O circuit type*	Function
113	P21	C	General-purpose I/O port
	SIN8		Multifunction serial ch.8 input
114	P22	C	General-purpose I/O port
	SCK8		Multifunction serial ch.8 clock [operation modes 0 to 2]
	(SCL8)		I^2C ch.8 serial clock line [operation mode 4]
115	P23	C	General-purpose I/O port
	RCIN_1		Remote control I/O (1)
116	P24	C	General-purpose I/O port
	SOUT9		Multifunction serial ch.9 output [operation modes 0 to 2]
	(SDA9)		I^2C ch.9 serial data line [operation mode 4]
	OUT0		Output compare ch.0 output
117	P25	C	General-purpose I/O port
	SIN9		Multifunction serial ch.9 input
	OUT1		Output compare ch.1 output
118	P26	C	General-purpose I/O port
	SCK9		Multifunction serial ch.9 clock [operation modes 0 to 2]
	(SCL9)		I^2C ch.9 serial clock line [operation mode 4]
	OUT2		Output compare ch.2 output
119	P27	C	General-purpose I/O port
	OUT3		Output compare ch.3 output
120	V_{SS}	—	GND

* : Refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.

■ I/O CIRCUIT TYPE

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>A</td><td>
</td><td>

- Oscillation feedback resistance approx.1 MΩ
- With standby control

</td></tr>
<tr><td>B</td><td>
</td><td>

- CMOS level output
- CMOS level hysteresis input
- With pull-up control
- With standby control

Note: When this pin is used as an I²C pin, the digital output P-ch transistor is always off.</td></tr>
</table>

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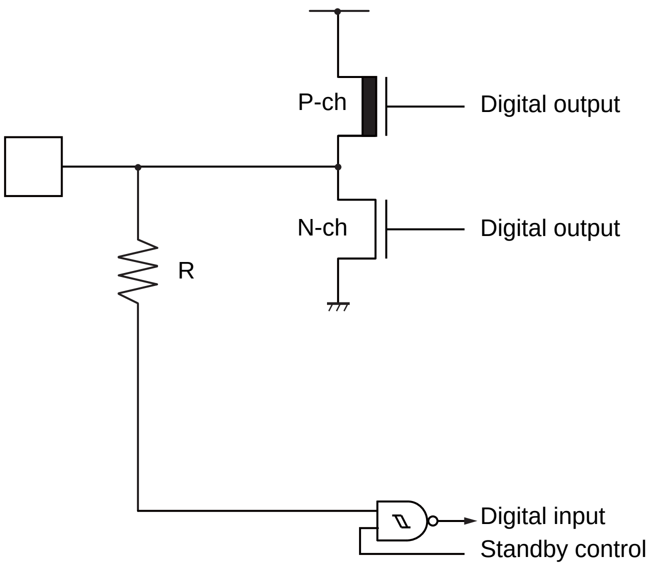
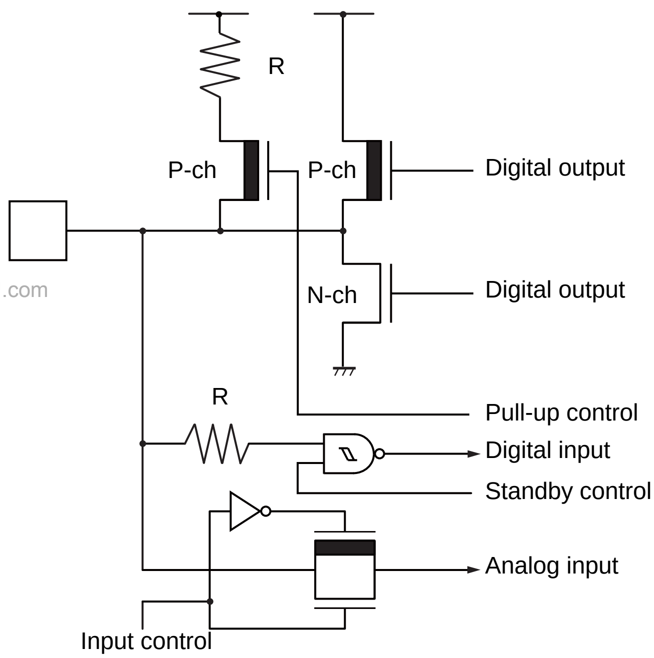
Type	Circuit	Remarks
C		• CMOS level output • CMOS level hysteresis input • 5 V tolerant input • With standby control Note: When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
D		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up control • With standby control Note: When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

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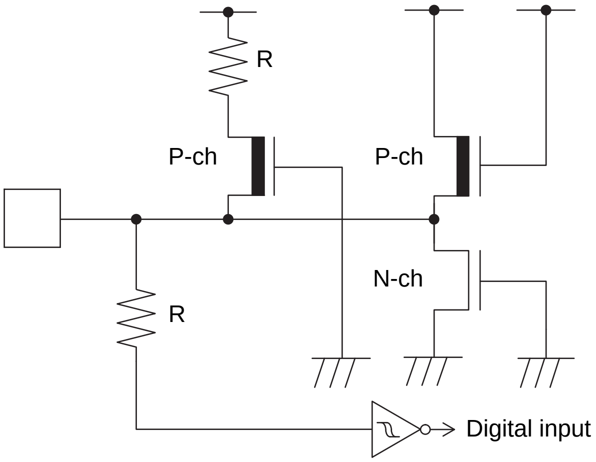
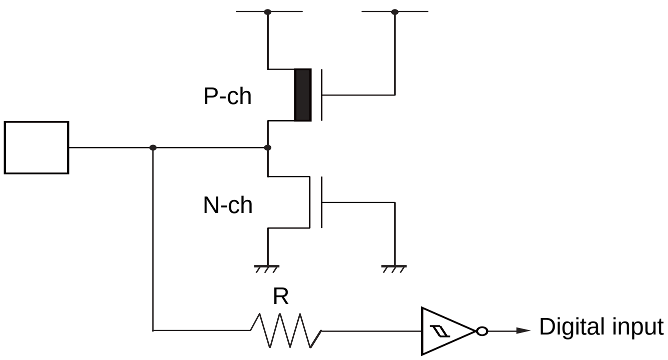
Type	Circuit	Remarks
E		• CMOS level hysteresis input • With pull-up
F		CMOS level hysteresis input

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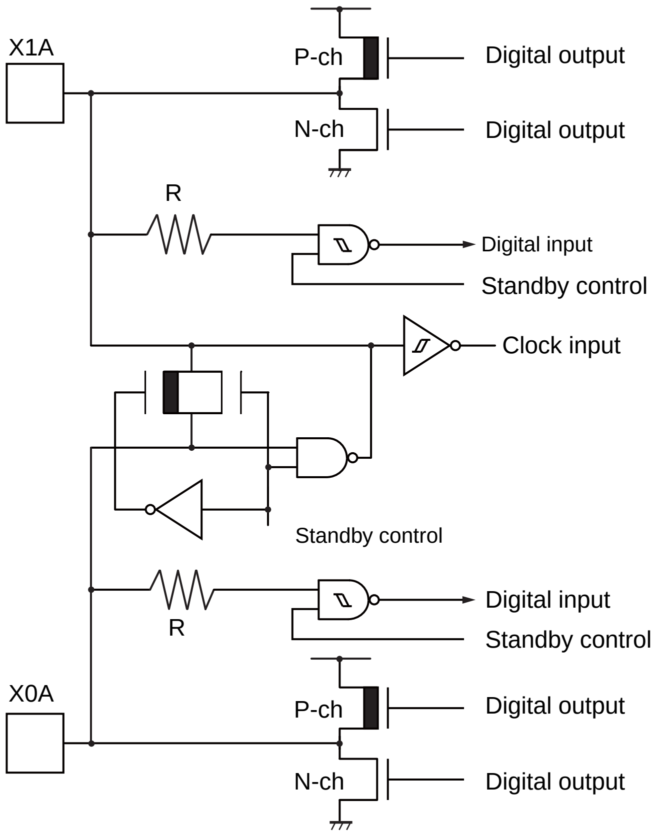
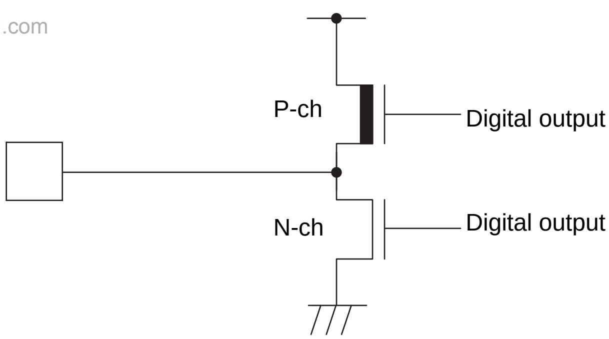
Type	Circuit	Remarks
G		• Oscillation feedback resistance approx.10MΩ • CMOS level output • CMOS level hysteresis input • With standby control
H		CMOS level output

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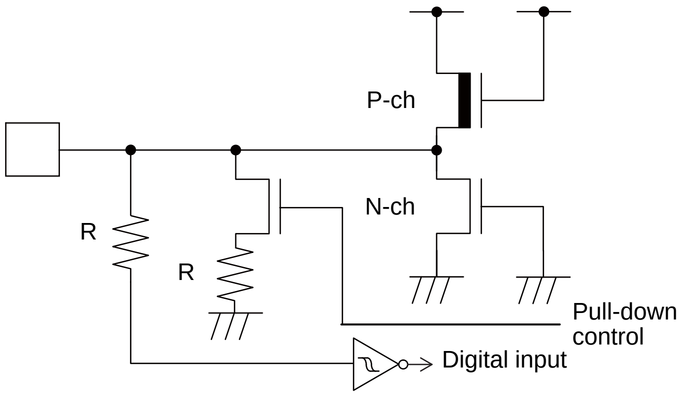
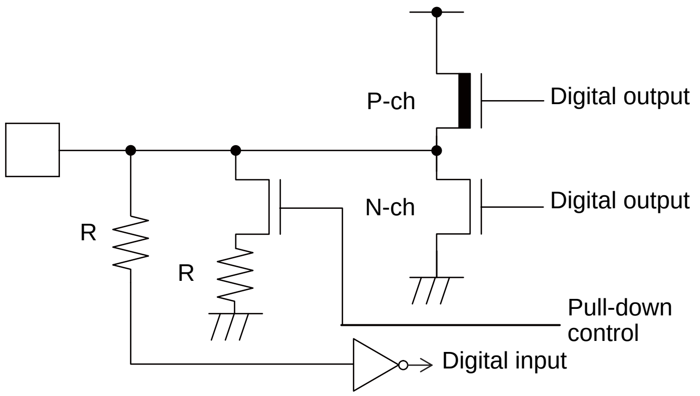
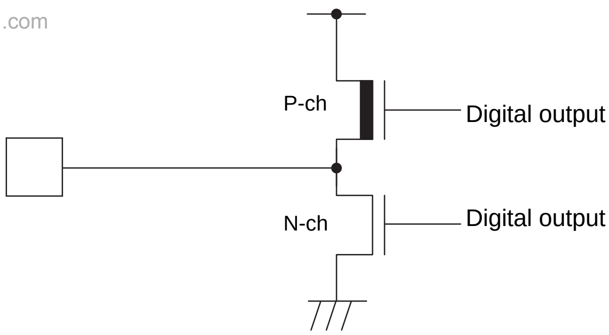
Type	Circuit	Remarks
I		• CMOS level hysteresis input • With Pull-down control
J		• CMOS level output • CMOS level input • With Pull-down control
K		CMOS level output (8 mA)

(Continued)

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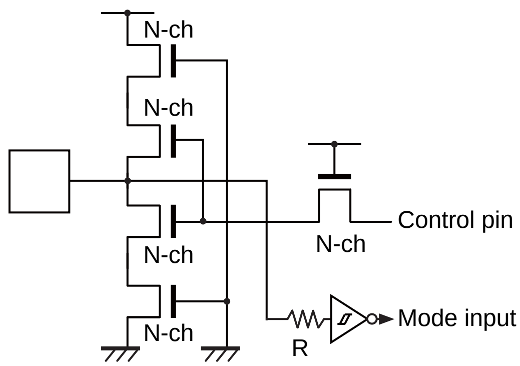
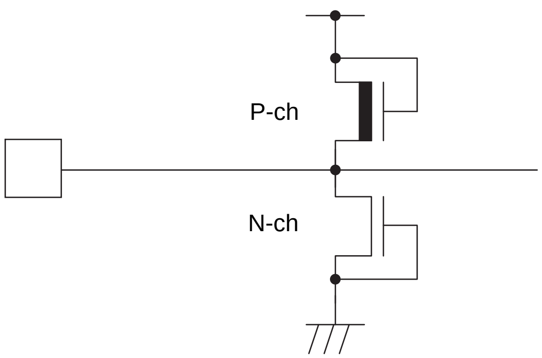
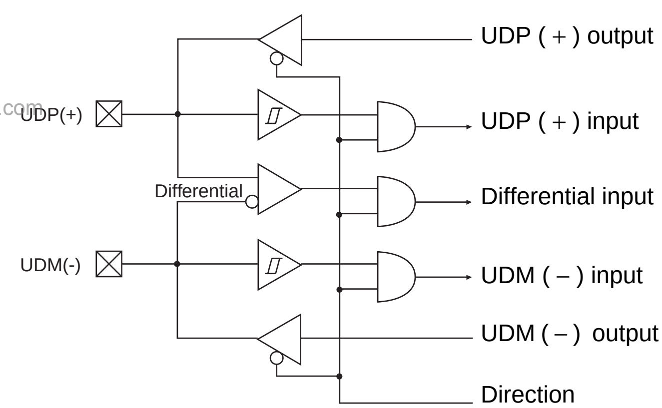
Type	Circuit	Remarks
L		• Flash memory product only • CMOS level hysteresis input • High voltage control for testing Flash memory
M		Analog pin
USB		USB I/O pin

■ PRECAUTIONS FOR HANDLING THE DEVICES

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU MICROELECTRONICS semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

• Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

• Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

• Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- PLL pin for OSD (recommended pin handling when PLL for OSD is not in use)

Pin no.	Pin name	Recommended handling of unused pin
45	VSSP	V_{SS} (PLL macro GND)
46	VDDP	V_{SS} (PLL macro power supply)
47	VCI	V_{SS}
48	CPO	V_{SS}

- Analog OSD (recommended pin handling when analog OSD is not in use)

Pin no.	Pin name	Recommended handling of unused pin
49	VSSD	V_{SS} (DAC macro GND)

50	VDDD	V_{SS} (DAC macro power supply)
51	VREF	V_{SS}
52	VRO	V_{SS}
53	ROUT	V_{SS}
54	GOUT	V_{SS}
55	BOUT	V_{SS}

- Digital OSD (recommended pin handling when digital OSD is not in use)

Pin no.	Pin name	Recommended handling of unused pin
19	R0	OPEN
20	R1	OPEN
21	R2	OPEN
22	R3	OPEN
23	R4	OPEN
24	G0	OPEN
25	G1	OPEN
26	G2	OPEN
27	G3	OPEN
28	G4	OPEN
29	G5	OPEN
32	B0	OPEN
33	B1	OPEN
34	B2	OPEN
35	B3	OPEN
36	B4	OPEN

- Other OSD pins

Pin no.	Pin name	Recommended handling of unused pin
37	VOA0	OPEN
38	VOA1	OPEN
39	VOA2	OPEN
40	VOB	OPEN
41	DCKO	OPEN
42	DCKI	pull-down
43	VSYNC	pull-down
44	HSYNC	pull-down

- USB (example of pin handling when USB is not in use)

Pin no.	Pin name	Recommended handling of unused pin
57	UDP	pull-down
58	UDM	pull-down

- DSU pin

Pin no.	Pin name	Recommended handling of unused pin
83	$\overline{\text{TRST}}$	Reset signal input from user board
84	ICLK	OPEN
85	IBREAK	OPEN
86	ICS0	OPEN
87	ICS1	OPEN
88	ICS2	OPEN
92	ICD0	OPEN
93	ICD1	OPEN
94	ICD2	OPEN
95	ICD3	OPEN

- Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

Note: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:
(a) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
(b) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

FUJITSU MICROELECTRONICS semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU MICROELECTRONICS sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU MICROELECTRONICS's recommended conditions. For detailed information about mount conditions, contact your sales representative.

• Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder.

In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

• Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU MICROELECTRONICS recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU MICROELECTRONICS ranking of recommended conditions.

• Lead-Free Packaging

Note: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

• Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(a) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(b) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(c) When necessary, FUJITSU MICROELECTRONICS packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(d) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU MICROELECTRONICS recommended conditions for baking.

Condition: + 125 °C/24 h

- Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(a) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(b) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(c) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(d) Ground all fixtures and instruments, or protect with anti-static measures.

(e) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

- Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

Note : Plastic molded devices are flammable, and therefore should not be used near combustible substances.

If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU MICROELECTRONICS products in other special environmental conditions should consult with sales representatives.

■ HANDLING DEVICES

• Power supply pins

In products with multiple Vcc and Vss pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the Vcc and Vss pins of this device at low impedance.
It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between Vcc and Vss near this device.

• Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.
It is strongly recommended that the PC board artwork be designed such that the X0 and X1 pins are surrounded by ground plane as this is expected to produce stable operation.

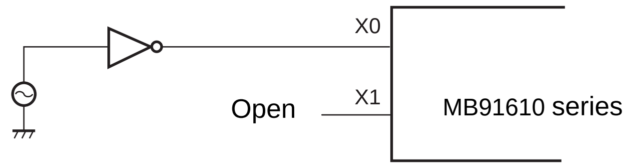
• OSDC output pin

The OSDC output pins (R0 to R4, G0 to G5, B0 to B4, VOA0 to VOA2, VOB, DCKO) are high-speed corresponded output pin.
Adjust the signal waveform such as by inserting damping resistor on the board as needed.

• Using an external clock

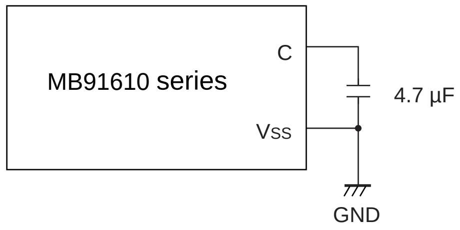
When using an external clock, the clock signal should be input to the X0 pin only and the X1 pin should be kept open.

• Example of Using an External Clock



• C Pin

As MB91610 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 µF to the C pin for use by the regulator.



- Mode pins (MD0, MD1)

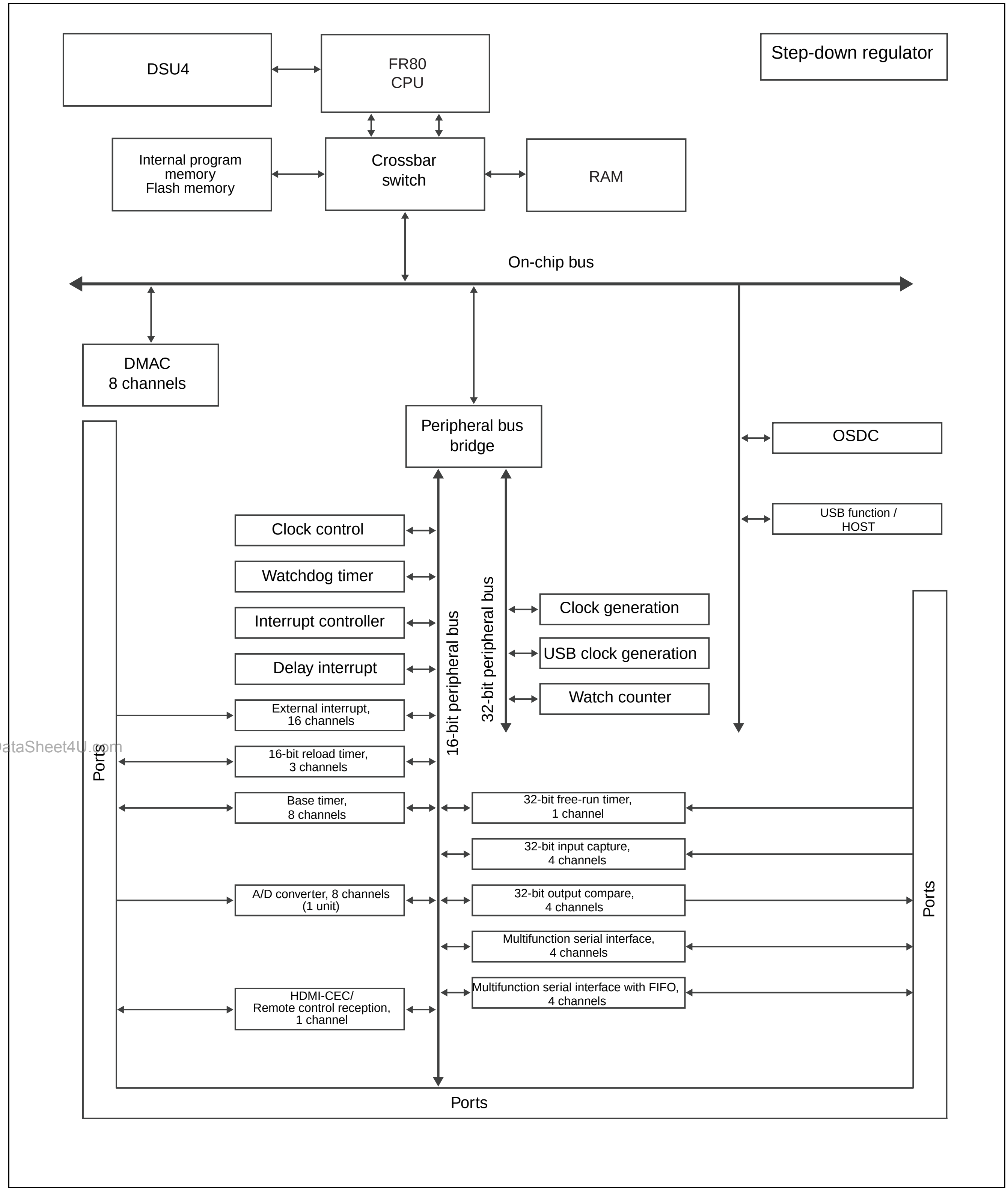
  Connect the MD pin (MD0, MD1) directly to V_{CC} or V_{SS} pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and V_{CC} pins or V_{SS} pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on
  - To ensure that the internal regulator and the oscillator have stabilized immediately after the power is turned on, keep an "L" level input connected to the $\overline{\text{INIT}}$ pin for the duration of the regulator voltage stabilization wait time + the oscillator start time of the oscillator + the main oscillator stabilization wait time.
  - Turn power on/off in the following order
    Turning on : $V_{CC} \rightarrow AV_{CC} \rightarrow$ AVRH
    Turning off : AVRH $\rightarrow AV_{CC} \rightarrow V_{CC}$
  - Release the reset ($\overline{\text{INIT}}$ pin "L" level to "H" level) after the power supply has stabilized.

- Caution on operations during PLL clock mode

  On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency.
  However, Fujitsu Microelectronics will not guarantee results of operations if such failure occurs.

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory Space

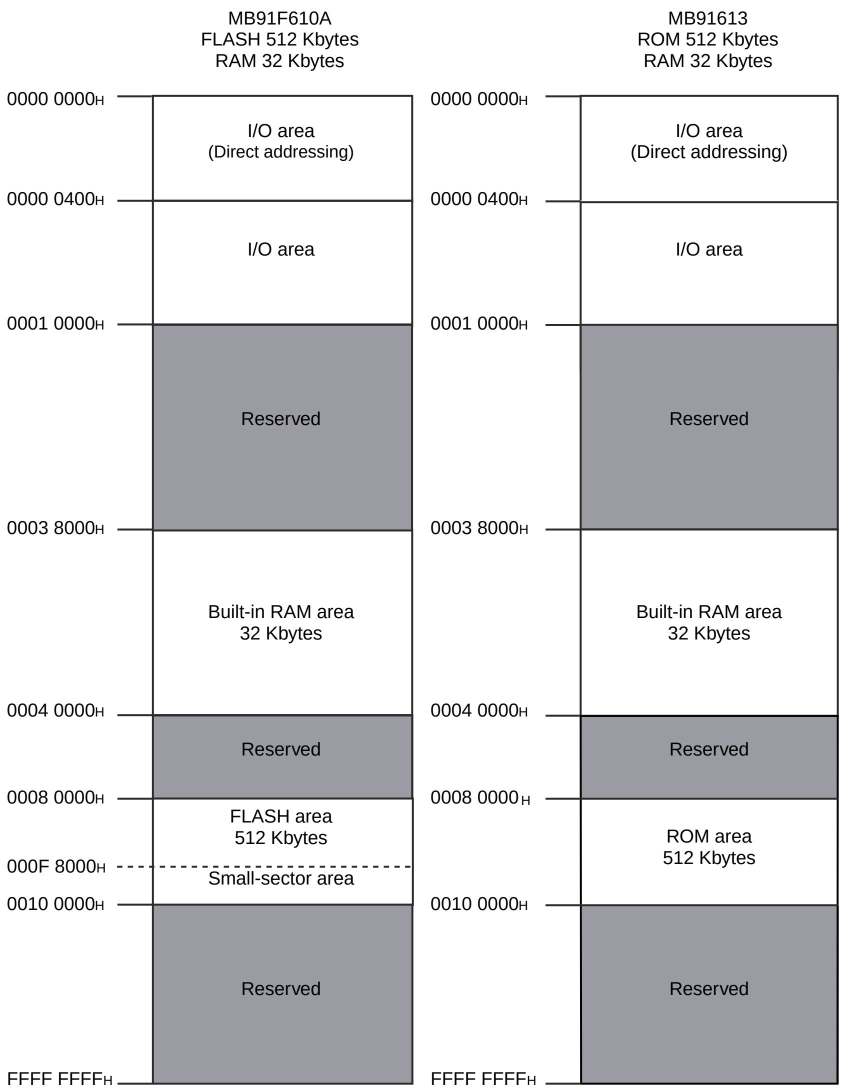
The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

• Direct Addressing Areas

The following areas in the address space are used as I/O areas.
These areas are called direct addressing areas, and the address of an operand in these areas can be specified directly within an instruction. The size of the directly addressable area depends on the length of the data being accessed as follows.

- Byte data access : 0000 0000_H to 0000 $00FF_H$
- Half word data access : 0000 0000_H to 0000 $01FF_H$
- Word data access : 0000 0000_H to 0000 $03FF_H$

2. Memory Map



Notes:
- Small sector area is related to flash products only. Please refer to the Flash Memory section of the Hardware Manual for more details.
- Do not access the reserved areas.

■ I/O MAP

[How to read the table]

Address	Register				Block
	+ **0**	+ **1**	+ **2**	+ **3**	
0000 0000H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port data register
0000 003CH	WDTCR0 [R/W] B, H -0--0000	WDTCPR0 [R/W] B, H 00000000	—		Watchdog timer
0000 0040H	EIRR0 [R/W] B, H, W 000 0000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt 0 to 7

Initial value after reset
"1" : Initial value"1"
"0" : Initial value"0"
"X" : Initial value undefined
" - " : Reserved bit or undefined bit

— : Reserved area

Access unit
(B : byte, H : half word, W : word)

Read/write attribute
"R" : Indicates that there is a read only bit.
"R/W" : Indicates that there is a read/write bit.
"W" : Indicates that there is a write only bit.

Register name (column 1 of the register is at address 4n, column 2 is at address 4 n + 2...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

Notes : • When performing a data access, the addresses should be as below.
- Word access : Address should be multiples of 4 (least significant 2 bits should be "00B")
- Half word access : Address should be multiples of 2 (least significant bit should be "0B")
- Byte access : —

• Do not access the reserved areas.

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 0000H	PDR0 [R/W] B,H XXXXXXXX	PDR1 [R/W] B,H XXXXXXXX	PDR2 [R/W] B,H XXXXXXXX	PDR3 [R/W] B,H XXXXXXXX	Port data register
0000 0004H	—	PDR5 [R/W] B,H XXXXXXXX	—	PDR7[R/W] B,H XXXXXXXX	
0000 0008H to 0000 0010H	—				
0000 0014H	PDRK [R/W] B ------XX	—			
0000 0018H to 0000 001CH	—				
0000 0020H	RCCR [R/W] B 0---0000	RCST [R/W] B 00000000	RCSHW [R/W] B 00000000	RCDAHW [R/W] B 00000000	HDMI-CEC/ Remote controller
0000 0024H	RCDBHW [R/W] B 00000000	—	RCADR1 [R/W] B ---00000	RCADR2 [R/W] B ---00000	
0000 0028H	RCDTHH [R] B,H,W 00000000	RCDTHL [R] B,H,W 00000000	RCDTLH [R] B,H,W 00000000	RCDTLL [R] B,H,W 00000000	
0000 002CH	RCCKD [R/W] H ---00000 00000000		—		
0000 0030H to 0000 0038H	—				Reserved
0000 003CH	WDTCR0[R/W] B,H 00000000	WDTCPR0[R/W] B,H 00000000	WDTCR1[R] B,H XXXX0000	WDTCPR1[R/W] B,H 00000000	Watchdog timer
0000 0040H	EIRR0[R/W] B,H,W 00000000	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt 0 to 7
0000 0044H	DICR [R/W] B -------0	—			Delay interrupt
0000 0048H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.0
0000 004CH	—		TMCSR0 [R/W] H --000000 --000000		
0000 0050H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.1
0000 0054H	—		TMCSR1 [R/W] H --000000 --000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000 0058$_H$	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.2
0000 005C$_H$	—		TMCSR2 [R/W] H --000000 --000000		
0000 0060$_H$	SCR0 [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R,R/W] B,H,W 0-000011	ESCR0 [R/W] B,H,W -0000000	Multi-function serial interface ch.0
0000 0064$_H$	RDR0[R]/TDR0[W] B,H,W*1 -------0 00000000		BGR10[R/W]H,W 00000000	BGR00[R/W] H,W 00000000	
0000 0068$_H$	SCR1[R/W] IBCR1[R,R/W] B,H,W*2 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R,R/W] B,H,W 0-000011	ESCR1[R/W] IBSR1[R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.1
0000 006C$_H$	RDR1[R]/TDR1[W] B,H,W*1 -------0 00000000		BGR11[R/W] H,W 00000000	BGR01[R/W] H,W 00000000	
0000 0070$_H$	ISMK1 [R/W] B,H*2 --------	ISBA1 [R/W] B,H*2 --------	—		
0000 0074$_H$	SCR2[R/W] IBCR2[R,R/W] B,H,W*2 0--00000	SMR2 [R/W] B,H,W 000-0000	SSR2 [R,R/W] B,H,W 0-000011	ESCR2[R/W] IBSR2 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.2
0000 0078$_H$	RDR2[R]/TDR2[W] B,H,W*1 -------0 00000000		BGR12[R/W] H,W 00000000	BGR02[R/W] H,W 00000000	
0000 007C$_H$	ISMK2 [R/W] B,H*2 --------	ISBA2 [R/W] B,H*2 --------	—		
0000 0080$_H$	SCR3[R/W] IBCR3[R,R/W] B,H,W*2 0--00000	SMR3 [R/W] B,H,W 000-0000	SSR3 [R,R/W] B,H,W 0-000011	ESCR3[R/W] IBSR3[R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.3
0000 0084$_H$	RDR3[R]/TDR3[W] B,H,W*1 -------0 00000000		BGR13[R/W] H,W 00000000	BGR03[R/W] H,W 00000000	
0000 0088$_H$	ISMK3 [R/W] B,H*2 --------	ISBA3 [R/W] B,H*2 --------	—		
0000 008C$_H$ to 0000 00BC$_H$	—				Reserved

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 00C0$_H$	RDRM0 [R]/ TDRM0[W] B,H,W 00000000	RDRM1 [R]/ TDRM1[W] B,H,W 00000000	RDRM2 [R]/ TDRM2[W] B,H,W 00000000	RDRM3 [R]/ TDRM3[W] B,H,W 00000000	Multi-function serial interface data register (mirror)
0000 00C4$_H$	—				
0000 00C8$_H$	SSEL0123 [R/W] B ------00	—			Multi-function serial interface serial clock selection
0000 00CC$_H$	—				Reserved
0000 00D0$_H$	SCR8 [R/W] IBCR8 [R,R/W] B,H,W*2 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R,R/W] B,H,W 0-000011	ESCR8 [R/W] IBSR8 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch. 8 (FIFO)
0000 00D4$_H$	RDR8[R]/TDR8[W] B,H,W*1 -------0 00000000		BGR18 [R/W] H,W 00000000	BGR08 [R,R/W] H,W 00000000	
0000 00D8$_H$	ISMK8 [R/W] B,H*2 --------	ISBA8 [R/W] B,H*2 --------	—		
0000 00DC$_H$	FCR18 [R/W] B,H,W ---00100	FCR08 [R,R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	
0000 00E0$_H$	SCR9 [R/W] IBCR9 [R,R/W] B,H,W*2 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R,R/W] B,H,W 0-000011	ESCR9 [R/W] IBSR9[R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch. 9 (FIFO)
0000 00E4$_H$	RDR9[R]/TDR9[W] B,H,W*1 -------0 00000000		BGR19 [R/W] H,W 00000000	BGR09 [R/W] H,W 00000000	
0000 00E8$_H$	ISMK9 [R/W] B,H*2 --------	ISBA9 [R/W] B,H*2 --------	—		
0000 00EC$_H$	FCR19 [R/W] B,H,W ---00100	FCR09 [R,R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 00F0H	SCR10 [R/W] IBCR10 [R,R/W] B,H,W*2 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R,R/W] B,H,W 0-000011	ESCR10 [R/W] IBSR10 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.10 (FIFO)
0000 00F4H	RDR10[R]/TDR10[W] B,H,W*1 -------0 00000000		BGR110 [R/W] H,W 00000000	BGR010 [R/W] H,W 00000000	
0000 00F8H	ISMK10 [R/W] B,H*2 --------	ISBA10 [R/W] B,H*2 --------	—		
0000 00FCH	FCR110 [R/W] B,H,W ---00100	FCR010 [R,R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	
0000 0100H	SCR11 [R/W] IBCR11 [R,R/W] B,H,W*2 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R,R/W] B,H,W 0-000011	ESCR11 [R/W] IBSR11 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.11 (FIFO)
0000 0104H	RDR11[R]/TDR11[W] B,H,W*1 -------0 00000000		BGR111 [R/W] H,W 00000000	BGR011 [R/W] H,W 00000000	
0000 0108H	ISMK11 [R/W] B,H*2 --------	ISBA11 [R/W] B,H*2 --------	—		
0000 010CH	FCR111 [R/W] B,H,W ---00100	FCR011 [R,R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	
0000 0110H	EIRR1[R/W] B,H,W 00000000	ENIR1[R/W] B,H,W 00000000	ELVR1[R/W] B,H,W 00000000 00000000		External interrupt 8 to 15
0000 0114H to 0000 011CH	—				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000 0120H	ADCR0[R/W] B,H 000-0000	ADSR0[R,R/W] B,H 00---000	—		A/D converter
0000 0124H	SCCR0[R,R/W] B,H 1000-000	SFNS0[R/W] B,H ----0000	SCFD0[R] B,H XXXXXXXX XX-XXXXX		
0000 0128H	—			SCIS00[R/W] B 00000000	
0000 012CH	PCCR0[R,R/W] B,H 1000-000	PFNS0[R/W] B,H ------00	PCFD0[R] B,H XXXXXXXX XXXXXXXX		
0000 0130H	PCIS0[R/W] B 00000000	—	CMPD0[R/W] B,H 00000000	CMPCR0[R/W] B,H 00000000	
0000 0134H	—			ADSS00[R/W] B 00000000	
0000 0138H	ADST00[R/W] B,H 00100000	ADST10[R/W] B,H 00100000	ADCT0[R/W] B -----111	—	
0000 013CH	—				Reserved
0000 0140H	BT0TMR[R]H 00000000 00000000		BT0TMCR[R/W] B,H -0000000 00000000		Base timer ch.0
0000 0144H	—	BT0STC[R/W]B 0000-000	—		
0000 0148H	BT0PCSR/BT0PRLL[R/W]H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 014CH	—				
0000 0150H	BT1TMR[R]H 00000000 00000000		BT1TMCR[R/W] B,H -0000000 00000000		Base timer ch.1
0000 0154H	—	BT1STC[R/W]B 0000-000	—		
0000 0158H	BT1PCSR/BT1PRLL[R/W]H XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 015CH	—				

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 0160H	BT2TMR[R]H 00000000 00000000		BT2TMCR [R/W] B,H -0000000 00000000		Base timer ch.2
0000 0164H	—	BT2STC[R/W]B 0000-000	—		
0000 0168H	BT2PCSR/BT2PRLL[R/W]H XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH/BT2DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 016CH	—				
0000 0170H	BT3TMR[R]H 00000000 00000000		BT3TMCR[R/W] B,H -0000000 00000000		Base timer ch.3
0000 0174H	—	BT3STC[R/W]B 0000-000	—		
0000 0178H	BT3PCSR/BT3PRLL[R/W]H XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH/BT3DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 017CH	BTSEL0123 [R/W] B 00000000	—			
0000 0180H to 0000 01A8H	—				Reserved
0000 01ACH	ADCHE [R/W] B,H,W -------- -------- -------- 11111111				A/D channel enable
0000 01B0H	IRPR0H [R] B 000-----	—	IRPR1H [R] B,H 000-000-	IRPR1L [R] B,H 000-000-	Interrupt request batch read function
0000 01B4H	—	IRPR2L [R] B,H,W 000-----	IRPR3H [R] B,H,W 0000----	—	
0000 01B8H	IRPR4H [R] B,H,W 0000----	—	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 0000----	
0000 01BCH	—			IRPR7L [R] B,H,W 0000----	
0000 01C0H to 0000 01FCH	—				Reserved
0000 0200H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.0
0000 0204H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
0000 0208H	TCCSH0 [R/W] B,H 0-----00	TCCSL0 [R/W] B,H -1-00000	—		

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 020CH	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.0 to ch.3
0000 0210H	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0214H	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0218H	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 021CH	—	ICS01 [R/W] B 00000000	—	ICS23 [R/W] B 00000000	
0000 0220H to 0000 0230H	—				Reserved
0000 0234H	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.0 to ch.3
0000 0238H	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0000 023CH	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				
0000 0240H	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0000 0244H	OCSH1 [R/W] B,H,W ---0--00	OCSL0 [R/W] B,H,W 0000--00	OCSH3 [R/W] B,H,W ---0--00	OCSL2 [R/W] B,H,W 0000--00	
0000 0248H to 0000 031CH	—				Reserved
0000 0320H	FCTLR[R/W] H -0--1011 --------		—	FSTR[R] B -------1	Flash memory control
0000 0324H to 0000 0334H	—				Reserved
0000 0338H	—		WREN[R/W] B,H 00000000 00000000		Wild register
0000 033CH	—				
0000 0340H to 0000 037CH	—				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000 0380H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register
0000 0384H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0388H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 038CH	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0390H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 0394H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0398H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 039CH	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A0H	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03A4H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A8H	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03ACH	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B0H	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03B4H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B8H	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03BCH	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C0H	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03C4H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C8H	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03CCH	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 03D0H	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register
0000 03D4H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D8H	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03DCH	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E0H	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03E4H	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E8H	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03ECH	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F0H	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03F4H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F8H	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0000 03FCH	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0400H	DDR0 [R/W] B,H 00000000	DDR1 [R/W] B,H 00000000	DDR2 [R/W] B,H 00000000	DDR3 [R/W] B,H 00000000	Data direction register
0000 0404H	—	DDR5 [R/W] B,H 00000000	—	DDR7[R/W] B,H 00000000	
0000 0408H to 0000 0410H	—				
0000 0414H	DDRK [R/W] B ------00	—			
0000 0418H to 0000 041CH	—				
0000 0420H	PCR0 [R/W] B,H 00000000	PCR1 [R/W] B,H 00000000	—		Pull-up control register
0000 0424H	—	PCR5 [R/W] B 00000000	—	PCR7[R/W] B,H 00000000	
0000 0428H to 0000 043CH	—				

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 0440H	ICR00 [R,R/W] B,H,W ---11111	ICR01 [R,R/W] B,H,W ---11111	ICR02 [R,R/W] B,H,W ---11111	ICR03 [R,R/W] B,H,W ---11111	Interrupt control
0000 0444H	ICR04 [R,R/W] B,H,W ---11111	ICR05 [R,R/W] B,H,W ---11111	ICR06 [R,R/W] B,H,W ---11111	ICR07 [R,R/W] B,H,W ---11111	
0000 0448H	ICR08 [R,R/W] B,H,W ---11111	ICR09 [R,R/W] B,H,W ---11111	ICR10 [R,R/W] B,H,W ---11111	ICR11 [R,R/W] B,H,W ---11111	
0000 044CH	ICR12 [R,R/W] B,H,W ---11111	ICR13 [R,R/W] B,H,W ---11111	ICR14 [R,R/W] B,H,W ---11111	ICR15 [R,R/W] B,H,W ---11111	
0000 0450H	ICR16 [R,R/W] B,H,W ---11111	ICR17 [R,R/W] B,H,W ---11111	ICR18 [R,R/W] B,H,W ---11111	ICR19 [R,R/W] B,H,W ---11111	
0000 0454H	ICR20 [R,R/W] B,H,W ---11111	ICR21 [R,R/W] B,H,W ---11111	ICR22 [R,R/W] B,H,W ---11111	ICR23 [R,R/W] B,H,W ---11111	
0000 0458H	ICR24 [R,R/W] B,H,W ---11111	ICR25 [R,R/W] B,H,W ---11111	ICR26 [R,R/W] B,H,W ---11111	ICR27 [R,R/W] B,H,W ---11111	
0000 045CH	ICR28 [R,R/W] B,H,W ---11111	ICR29 [R,R/W] B,H,W ---11111	ICR30 [R,R/W] B,H,W ---11111	ICR31 [R,R/W] B,H,W ---11111	
0000 0460H	ICR32 [R,R/W] B,H,W ---11111	ICR33 [R,R/W] B,H,W ---11111	ICR34 [R,R/W] B,H,W ---11111	ICR35 [R,R/W] B,H,W ---11111	
0000 0464H	ICR36 [R,R/W] B,H,W ---11111	ICR37 [R,R/W] B,H,W ---11111	ICR38 [R,R/W] B,H,W ---11111	ICR39 [R,R/W] B,H,W ---11111	
0000 0468H	ICR40 [R,R/W] B,H,W ---11111	ICR41 [R,R/W] B,H,W ---11111	ICR42 [R,R/W] B,H,W ---11111	ICR43 [R,R/W] B,H,W ---11111	
0000 046CH	ICR44 [R,R/W] B,H,W ---11111	ICR45 [R,R/W] B,H,W ---11111	ICR46 [R,R/W] B,H,W ---11111	ICR47 [R,R/W] B,H,W ---11111	
0000 0470H to 0000 047CH	—				Reserved
0000 0480H	RSTRR [R] B,H,W 11XX---X*3	RSTCR [R/W] B,H,W 000----0	STBCR [R/W] B,H,W 0000--11	SLPRR [R/W] B,H,W 00000000	Reset control/ Power consumption control
0000 0484H	—				

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 0488H	DIVR0 [R/W] B,H 000--011	—	DIVR2 [R/W] B 0011----	—	Clock division control
0000 048CH	—				
0000 0490H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	Peripheral DMA transmission request control
0000 0494H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
0000 0498H to 0000 049CH	—				Reserved
0000 04A0H	PFR0 [R/W] B,H 00000000	PFR1 [R/W] B,H 00000000	PFR2 [R/W] B,H 00000000	PFR3 [R/W] B,H 00000000	Port function register
0000 04A4H	—	PFR5 [R/W] B,H 00000000	—	PFR7[R/W] B,H 00000000	
0000 04A8H to 0000 04B0H	—				
0000 04B4H	PFRK [R/W] B,H ----0000	—			
0000 04B8H	EPFR0 [R/W] B,H ---00-00	EPFR1 [R/W] B,H ---00-00	—		Extended port function register
0000 04BCH	—		EPFR6 [R/W] B,H -00-00-0	EPFR7 [R/W] B,H ----0-0-	
0000 04C0H	EPFR8 [R/W] B,H ----0-0-	EPFR9 [R/W] B,H ----00-0	EPFR10 [R/W] B,H ----0---	—	
0000 04C4H	—		EPFR14 [R/W] B,H ----0-0-	EPFR15 [R/W] B,H ----0-0-	
0000 04C8H	EPFR16 [R/W] B,H ----0-0-	EPFR17 [R/W] B,H ----0-0-	—	EPFR19 [R/W] B,H -------1	
0000 04CCH	EPFR20 [R/W] B,H ---0--0-	EPFR21 [R/W] B,H ---0--0-	EPFR22 [R/W] B,H ---0--0-	EPFR23 [R/W] B,H ---0--0-	
0000 04D0H, 0000 04D4H	—				
0000 04D8H	—	EPFR33 [R/W] B,H ---0--0-	EPFR34 [R/W] B,H --0-----	—	
0000 04DCH	—				

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
0000 04E0H to 0000 04ECH	—				Reserved
0000 04F0H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -----000	—		DMA start request clear select function
0000 04F4H	ICSEL4[R/W] B,H,W ------00	—	ICSEL6[R/W] B,H,W ------00	ICSEL7[R/W] B,H,W -------0	
0000 04F8H	ICSEL8[R/W] B,H,W ------00	—	ICSEL10[R/W] B,H,W ----0000	ICSEL11[R/W] B,H,W ----0000	
0000 04FCH	—				
0000 0500H to 0000 050CH	—				Reserved
0000 0510H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock generation/ Main timer/ Sub timer
0000 0514H	PLLCR [R/W] B,H --000000 11110000		CSTBR [R/W] B -0000000	—	
0000 0518H	WCRD [R] B,H --000000	WCRL [R/W] B,H --000000	WCCR [R,R/W] B 00--0000	—	Clock counter
0000 051CH	UCCR [R/W] B -----001	—			USB clock generation
0000 0520H to 0000 0BFCH	—				Reserved
0000 0C00H	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMAC
0000 0C04H	DCSR0 [R,R/W] H 0------- -----000		DTCR0 [R/W] H 00000000 00000000		
0000 0C08H	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C0CH	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C10H	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C14H	DCSR1 [R,R/W] H 0------- -----000		DTCR1 [R/W] H 00000000 00000000		
0000 0C18H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C1CH	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register +0	Register +1	Register +2	Register +3	Block
0000 0C20H	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				DMAC
0000 0C24H	DCSR2 [R,R/W] H 0------- -----000		DTCR2 [R/W] H 00000000 00000000		
0000 0C28H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C2CH	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C30H	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C34H	DCSR3 [R,R/W] H 0------- -----000		DTCR3 [R/W] H 00000000 00000000		
0000 0C38H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C3CH	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C40H	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C44H	DCSR4 [R,R/W] H 0------- -----000		DTCR4 [R/W] H 00000000 00000000		
0000 0C48H	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C4CH	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C50H	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C54H	DCSR5 [R,R/W] H 0------- -----000		DTCR5 [R/W] H 00000000 00000000		
0000 0C58H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C5CH	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C60H	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C64H	DCSR6 [R,R/W] H 0------- -----000		DTCR6 [R/W] H 00000000 00000000		
0000 0C68H	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C6CH	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C70H	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C74H	DCSR7 [R,R/W] H 0------- -----000		DTCR7 [R/W] H 00000000 00000000		

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Address	Register +0	Register +1	Register +2	Register +3	Block
0000 0C78H	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
0000 0C7CH	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C80H to 0000 0DF0H	—				
0000 0DF4H	—			DILVR [R,R/W] B ---11111	
0000 0DF8H	DMACR [R/W] W 0------- -------- 0------- --------				
0000 0DFCH to 0000 0F3CH	—				Reserved
0000 0F40H	BT4TMR[R]H 00000000 00000000		BT4TMCR[R/W] B,H -0000000 00000000		Base timer ch.4
0000 0F44H	—	BT4STC[R/W]B 0000-000	—		
0000 0F48H	BT4PCSR/BT4PRLL[R/W]H XXXXXXXX XXXXXXXX		BT4PDUT/BT4PRLH/BT4DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F4CH	—				
0000 0F50H	BT5TMR[R]H 00000000 00000000		BT5TMCR[R/W] B,H -0000000 00000000		Base timer ch.5
0000 0F54H	—	BT5STC[R/W]B 0000-000	—		
0000 0F58H	BT5PCSR/BT5PRLL[R/W]H XXXXXXXX XXXXXXXX		BT5PDUT/BT5PRLH/BT5DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F5CH	—				
0000 0F60H	BT6TMR[R]H 00000000 00000000		BT6TMCR[R/W] B,H -0000000 00000000		Base timer ch.6
0000 0F64H	—	BT6STC[R/W]B 0000-000	—		
0000 0F68H	BT6PCSR/BT6PRLL[R/W]H XXXXXXXX XXXXXXXX		BT6PDUT/BT6PRLH/BT6DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F6CH	—				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0F70H	BT7TMR[R]H 00000000 00000000		BT7TMCR[R/W] B,H -0000000 00000000		Base timer ch.7
0000 0F74H	—	BT7STC[R/W]B 0000-000	—		
0000 0F78H	BT7PCSR/BT7PRLL[R/W]H XXXXXXXX XXXXXXXX		BT7PDUT/BT7PRLH/BT7DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F7CH	BTSEL4567 [R/W] B 00000000	—			
0000 0F80H to 0000 0FF8H	—				Reserved
0000 0FFCH	—		BTSSSR[W] H XXXXXXXX XXXXXXXX		Base Timer I/O Select Function
0000 1000H to 0000 20FCH	—				Reserved
0000 2100H	HCNT1[R/W] B,H -----001	HCNT0[R/W] B,H 00000000	—		USB function / HOST
0000 2104H	HERR[R/W] B,H 00000011	HIRQ[R/W] B,H 0-000000	—		
0000 2108H	HFCOMP[R/W] B,H 00000000	HSTATE[R,R/W] B,H ---10010	—		
0000 210CH	HRTIMER1[R/W] B,H 00000000	HRTIMER0[R/W] B,H 00000000	—		
0000 2110H	HADR[R/W] B,H -0000000	HRTIMER2[R/W] B,H ------00	—		
0000 2114H	HEOF1[R/W] B,H --000000	HEOF0[R/W] B,H 00000000	—		
0000 2118H	HFRAME1[R/W] B,H -----000	HFRAME0[R/W] B,H 00000000	—		
0000 211CH	—	HTOKEN[R/W] B 00000000	—		
0000 2120H	—	UDCC[R/W] B 1010--00	—		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 2124H	EP0C[R/W] H ------0- -1000000		—		USB function / HOST
0000 2128H	EP1C[R/W] H 01100001 00000000		—		
0000 212CH	EP2C[R/W] H 0110000- -1000000		—		
0000 2130H	EP3C[R/W] H 0110000- -1000000		—		
0000 2134H	EP4C[R/W] H 0110000- -1000000		—		
0000 2138H	EP5C[R/W] H 0110000- -1000000		—		
0000 213CH	TMSP[R] H -----000 00000000		—		
0000 2140H	UDCIE[R,R/W] B,H --000000	UDCS[R/W] B,H --000000	—		
0000 2144H	EP0IS[R/W] H 10---1-- --------		—		
0000 2148H	EP00S[R,R/W] H 100--00- -XXXXXXX		—		
0000 214CH	EP1S[R,R/W] H 100-000X XXXXXXXX		—		
0000 2150H	EP2S[R,R/W] H 100-000- -XXXXXXX		—		
0000 2154H	EP3S[R,R/W] H 100-000- -XXXXXXX		—		
0000 2158H	EP4S[R,R/W] H 100-000- -XXXXXXX		—		
0000 215CH	EP5S[R,R/W] H 100-000- -XXXXXXX		—		
0000 2160H	EP0DTH [R/W] B,H XXXXXXXX	EP0DTL [R/W] B,H XXXXXXXX	—		
0000 2164H	EP1DTH [R/W] B,H XXXXXXXX	EP1DTL [R/W] B,H XXXXXXXX	—		
0000 2168H	EP2DTH [R/W] B,H XXXXXXXX	EP2DTL [R/W] B,H XXXXXXXX	—		
0000 216CH	EP3DTH [R/W] B,H XXXXXXXX	EP3DTL [R/W] B,H XXXXXXXX	—		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000 2170H	EP4DTH [R/W] B,H XXXXXXXX	EP4DTL [R/W] B,H XXXXXXXX	—		USB function / HOST
0000 2174H	EP5DTH [R/W] B,H XXXXXXXX	EP5DTL [R/W] B,H XXXXXXXX	—		
0000 2178H to 0000 217CH	—				
0000 2180H to 0000 21A0H	—				Reserved
0000 21A4H	DREQSEL [R/W] B,H 00111011	USBSEL [R/W] B,H -------0	USBEN [R/W] B -------0	—	DMA transfer request selector/ USB enable
0000 21A8H to 0000 3FFCH	—				Reserved
0000 4000H	MOSD_VADR [W] W -------- -------0 ---00000 --000000				OSDC (MAIN)
0000 4004H	MOSD_CDS1 [W] W 00000000 ---00000 00000000 00000000				
0000 4008H	MOSD_CDS2 [W] W -------- 0000-000 --000000 00000000				
0000 400CH	MOSD_LDS1 [W] W 0000-000 00000000 ----0000 00000000				
0000 4010H	MOSD_LDS2 [W] W -------- ---00000 --000000 00000000				
0000 4014H	MOSD_SCOC [W] W ------00 0000---- ---0---0 XXXX----				
0000 4018H	MOSD_HVDP [W] W -----000 00000000 -----000 00000000				
0000 401CH	MOSD_TSBC [W] W -------- -------- -------0 00000000				
0000 4020H	MOSD_GRCC [W] W -------0 00000000 -------0 00000000				
0000 4024H	MOSD_SBCC [W] W -----000 ------00 --000000 00000000				
0000 4028H	MOSD_SCBC [W] W -------- --00--00 ---0-000 00000000				
0000 402CH	MOSD_WPC1 [W] W -----000 00000000 -----000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 4030H	MOSD_WPC2 [W] W ----0000 00000000 ----0000 00000000				OSDC (MAIN)
0000 4034H	MOSD_SPC1 [W] W ---0-000 ------00 --000000 00000000				
0000 4038H	MOSD_SPC2 [W] W ----0000 00000000 -----000 00000000				
0000 403CH	MOSD_SYNC [W] W -------- --000000 -------- -0-0----				
0000 4040H	MOSD_CBC0 [W] W --000000 00000000 --000000 00000000				
0000 4044H	MOSD_CBC1 [W] W --000000 00000000 --000000 00000000				
0000 4048H	MOSD_CBC2 [W] W --000000 00000000 --000000 00000000				
0000 404CH	MOSD_CBC3 [W] W --000000 00000000 --000000 00000000				
0000 4050H	MOSD_CBC4 [W] W --000000 00000000 --000000 00000000				
0000 4054H	MOSD_CBC5 [W] W --000000 00000000 --000000 00000000				
0000 4058H	MOSD_CBC6 [W] W --000000 00000000 --000000 00000000				
0000 405CH	MOSD_CBC7 [W] W --000000 00000000 --000000 00000000				
0000 4060H	MOSD_IOTC [W] W -------0 0----00- -------- -----XXX				
0000 4064H	MOSD_CDP1 [W] W -----000 00000000 -----000 00000000				
0000 4068H	MOSD_CDP2 [W] W ----0000 00000000 ----0000 00000000				
0000 406CH	MOSD_INTC [R/W] W -------- -------- -----XXX -----XXX				
0000 4070H	MOSD_SBC0 [W] W 00000000 00000000 00000000 00000000				
0000 4074H	MOSD_SBC1 [W] W 00000000 00000000 00000000 00000000				
0000 4078H	MOSD_SBC2 [W] W 00000000 00000000 00000000 00000000				
0000 407CH	MOSD_SBC3 [W] W 00000000 00000000 00000000 00000000				

(Continued)

Address	Register (+0 / +1 / +2 / +3)	Block
0000 4080H to 0000 40FCH	—	Reserved
0000 4100H	SOSD_VADR [W] W -------- -------0 ---00000 --000000	OSDC (SUB)
0000 4104H	SOSD_CDS1 [W] W 00000000 ---00000 00000000 00000000	
0000 4108H	SOSD_CDS2 [W] W -------- 0000-000 --000000 00000000	
0000 410CH	SOSD_LDS1 [W] W 0000-000 00000000 ----0000 00000000	
0000 4110H	SOSD_LDS2 [W] W -------- ---00000 --000000 00000000	
0000 4114H	SOSD_SCOC [W] W ------00 0000---- ---0---0 XX-X---X	
0000 4118H	SOSD_HVDP [W] W -----000 00000000 -----000 00000000	
0000 411CH	SOSD_TSBC [W] W -------- -------- -------0 00000000	
0000 4120H	SOSD_GRCC [W] W -------0 00000000 -------0 00000000	
0000 4124H	—	
0000 4128H	SOSD_SCBC [W] W -------- --00--00 ---0-000 00000000	
0000 412CH	SOSD_WPC1 [W] W -----000 00000000 -----000 00000000	
0000 4130H	SOSD_WPC2 [W] W ----0000 00000000 ----0000 00000000	
0000 4134H	SOSD_SPC1 [W] W ---0-000 ------00 --000000 00000000	
0000 4138H	SOSD_SPC2 [W] W ----0000 00000000 -----000 00000000	
0000 413CH to 0000 4168H	—	
0000 416CH	SOSD_INTC [R/W] W -------- -------- -----XXX -----XXX	
0000 4170H	SOSD_SBC0 [W] W 00000000 00000000 00000000 00000000	
0000 4174H	SOSD_SBC1 [W] W 00000000 00000000 00000000 00000000	
0000 4178H	SOSD_SBC2 [W] W 00000000 00000000 00000000 00000000	
0000 417CH	SOSD_SBC3 [W] W 00000000 00000000 00000000 00000000	

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 4180H to 0000 41FCH	—				Reserved
0000 4200H to 0000 43FCH	MOSD_PLn [W] W *n: 0 to 127 00000000 00000000 00000000 00000000				OSDC (MAIN)
0000 4400H	MOSD_OSDC [W] W -------- --XX--XX ------XX ---X---X				
0000 4404H	MOSD_PLLC [W] W --000000 00000000 00000000 ---00000				
0000 4408H to 0000 FFFCH	—				Reserved

*1 : Byte access is available only when accessing the lower 8 bits within 9 bits.

*2 : The register of I²C can not be read immediate after reset.

*3 : Value just after reset by $\overline{\text{INIT}}$ pin.
Do not access the reserved areas.

■ VECTOR TABLE

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Deci-mal	Hexa-deci-mal			
Reset	0	00	—	$3FC_H$	$000F\ FFFC_H$
System reserved	1	01	—	$3F8_H$	$000F\ FFF8_H$
System reserved	2	02	—	$3F4_H$	$000F\ FFF4_H$
System reserved	3	03	—	$3F0_H$	$000F\ FFF0_H$
System reserved	4	04	—	$3EC_H$	$000F\ FFEC_H$
System reserved	5	05	—	$3E8_H$	$000F\ FFE8_H$
System reserved	6	06	—	$3E4_H$	$000F\ FFE4_H$
System reserved	7	07	—	$3E0_H$	$000F\ FFE0_H$
System reserved	8	08	—	$3DC_H$	$000F\ FFDC_H$
INTE instruction	9	09	—	$3D8_H$	$000F\ FFD8_H$
Instruction break exception	10	0A	—	$3D4_H$	$000F\ FFD4_H$
Operand break	11	0B	—	$3D0_H$	$000F\ FFD0_H$
Step trace trap	12	0C	—	$3CC_H$	$000F\ FFCC_H$
System reserved	13	0D	—	$3C8_H$	$000F\ FFC8_H$
Undefined instruction exception	14	0E	—	$3C4_H$	$000F\ FFC4_H$
—	15	0F	15 (F_H) fixed	$3C0_H$	$000F\ FFC0_H$
External interrupt request ch.0 to ch.7	16	10	ICR00	$3BC_H$	$000F\ FFBC_H$
External interrupt request ch.8 to ch.15	17	11	ICR01	$3B8_H$	$000F\ FFB8_H$
Reserved	18	12	ICR02	$3B4_H$	$000F\ FFB4_H$
Reserved	19	13	ICR03	$3B0_H$	$000F\ FFB0_H$
16-bit reload timer ch.0 to ch.2	20	14	ICR04	$3AC_H$	$000F\ FFAC_H$
Reception interrupt request of UART/CSIO ch.0	21	15	ICR05	$3A8_H$	$000F\ FFA8_H$
Transmission interrupt request of UART/CSIO ch.0 Transmission bus idle interrupt request of UART/CSIO ch.0	22	16	ICR06	$3A4_H$	$000F\ FFA4_H$
Reception interrupt request of UART/CSIO/ I^2C ch.1	23	17	ICR07	$3A0_H$	$000F\ FFA0_H$
Transmission interrupt request of UART/ CSIO/ I^2C ch.1 Transmission bus idle interrupt request of UART/CSIO ch.1	24	18	ICR08	$39C_H$	$000F\ FF9C_H$
Status interrupt request of I^2C ch.1	25	19	ICR09	398_H	$000F\ FF98_H$

(Continued)

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Deci-mal	Hexa-deci-mal			
Reception interrupt request of UART/CSIO/I²C ch.2	26	1A	ICR10	394_H	$000F\ FF94_H$
Transmission interrupt request of UART/CSIO/I²C ch.2 Transmission bus idle interrupt request of UART/CSIO ch.2	27	1B	ICR11	390_H	$000F\ FF90_H$
Status interrupt request of I²C ch.2	28	1C	ICR12	$38C_H$	$000F\ FF8C_H$
Reception interrupt request of UART/CSIO/I²C ch.3	29	1D	ICR13	388_H	$000F\ FF88_H$
Transmission interrupt request of UART/CSIO/I²C ch.3 Transmission bus idle interrupt request of UART/CSIO ch.3 Status interrupt request of I²C ch.3	30	1E	ICR14	384_H	$000F\ FF84_H$
Reserved	31	1F	ICR15	380_H	$000F\ FF80_H$
Reserved	32	20	ICR16	$37C_H$	$000F\ FF7C_H$
Reserved	33	21	ICR17	378_H	$000F\ FF78_H$
Reserved	34	22	ICR18	374_H	$000F\ FF74_H$
Reserved	35	23	ICR19	370_H	$000F\ FF70_H$
Reserved	36	24	ICR20	$36C_H$	$000F\ FF6C_H$
Reserved	37	25	ICR21	368_H	$000F\ FF68_H$
Reserved	38	26	ICR22	364_H	$000F\ FF64_H$
Reception interrupt request of UART/CSIO/I²C ch.8 to ch.11 Transmission interrupt request of UART/CSIO/I²C ch.8 to ch.11 Transmission bus idle interrupt request of UART/CSIO ch.8 to ch.11 Transmission FIFO interrupt request UART/CSIO/I²C ch.8 to ch.11 Status interrupt request of I²C ch.8 to ch.11	39	27	ICR23	360_H	$000F\ FF60_H$
HDMI-CEC/Remote control reception	40	28	ICR24	$35C_H$	$000F\ FF5C_H$
Main timer/Sub timer/Watch counter	41	29	ICR25	358_H	$000F\ FF58_H$
10-bit A/D converter • Scan conversion interrupt request • Priority conversion interrupt request • FIFO overrun interrupt request • Conversion result compare interrupt request	42	2A	ICR26	354_H	$000F\ FF54_H$

(Continued)

(Continued)

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Deci-mal	Hexa-deci-mal			
32-bit free run timer ch.0	43	2B	ICR27	350_H	$000F\ FF50_H$
32-bit input capture ch.0 to ch.3	44	2C	ICR28	$34C_H$	$000F\ FF4C_H$
32-bit output compare ch.0 to ch.3	45	2D	ICR29	348_H	$000F\ FF48_H$
Base timer ch.0	46	2E	ICR30	344_H	$000F\ FF44_H$
Base timer ch.1	47	2F	ICR31	340_H	$000F\ FF40_H$
Base timer ch.2	48	30	ICR32	$33C_H$	$000F\ FF3C_H$
Base timer ch.3	49	31	ICR33	338_H	$000F\ FF38_H$
Base timer ch.4, ch.5	50	32	ICR34	334_H	$000F\ FF34_H$
Base timer ch.6, ch.7	51	33	ICR35	330_H	$000F\ FF30_H$
Reserved	52	34	ICR36	$32C_H$	$000F\ FF2C_H$
OSDC (MAIN)	53	35	ICR37	328_H	$000F\ FF28_H$
USB function (DRQ of End Point 1 to 5)	54	36	ICR38	324_H	$000F\ FF24_H$
USB function (DRQI of End Point 0, DRQO and each status/ USB HOST (each status)	55	37	ICR39	320_H	$000F\ FF20_H$
OSDC (SUB)	56	38	ICR40	$31C_H$	$000F\ FF1C_H$
DMA controller (DMAC) ch.0	57	39	ICR41	318_H	$000F\ FF18_H$
DMA controller (DMAC) ch.1	58	3A	ICR42	314_H	$000F\ FF14_H$
DMA controller (DMAC) ch.2	59	3B	ICR43	310_H	$000F\ FF10_H$
DMA controller (DMAC) ch.3	60	3C	ICR44	$30C_H$	$000F\ FF0C_H$
DMA controller (DMAC) ch.4 to ch.7	61	3D	ICR45	308_H	$000F\ FF08_H$
System reserved	62	3E	ICR46	304_H	$000F\ FF04_H$
Delay interrupt	63	3F	ICR47	300_H	$000F\ FF00_H$
System reserved (Used by REALOS)	64	40	—	$2FC_H$	$000F\ FEFC_H$
System reserved (Used by REALOS)	65	41	—	$2F8_H$	$000F\ FEF8_H$
Used by INT instruction	66 to 255	42 to FF	—	$2F4_H$ to 000_H	$000F\ FEF4_H$ to $000F\ FC00_H$

* : USB interrupt source

Number		USB interrupt source	Details
Decimal	Hexadecimal		
54	36	USB function (DRQ of End Point 1 to 5)	DRQ (End Point1 to 5)
55	37	USB function (DRQI, DRQO of End Point 0 and each status)	DRQI, DRQO, SPK, SUSP, SOF, BRST, CONF, WKUP
		USB HOST (Each status)	DIRQ, URIRQ, RWKIRQ, CNNIRQ, SOFIRQ, CMPIRQ

■ PIN STATUS IN EACH CPU STATE

- When $\overline{\text{INIT}}$ = "L"

This is the period when the $\overline{\text{INIT}}$ pin is the "L" level.

- When $\overline{\text{INIT}}$ = "H"

The status immediately after the $\overline{\text{INIT}}$ pin changes from the "L" level to the "H" level.

- SLVL1

This bit is a standby level setting bit in the standby mode control register (STBCR) .

- Input enabled

Indicates that the input function can be used.

- Input disabled

Indicates that the input function cannot be used.

- Output Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

- Maintain previous state

Maintains the state that was being output immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

- Internal input fixed at "0"

The input gate connected to the pin is disconnected from the external input and internally connected to "0".

- Input enabled when interrupt function selected and enabled

Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

• List of pin status

<table>
<tr><th rowspan="2">Pin name</th><th rowspan="2">Function</th><th colspan="2">During initialization</th><th rowspan="2">Sleep Mode</th><th colspan="2">Standby Mode</th></tr>
<tr><th>$\overline{\text{INIT}}$ = “L”</th><th>$\overline{\text{INIT}}$ = “H”</th><th>SLVL1 = 0</th><th>SLVL1 = 1</th></tr>
<tr><td>$\overline{\text{INIT}}$</td><td>$\overline{\text{INIT}}$</td><td>—</td><td>—</td><td rowspan="7">Input enabled</td><td>Input enabled</td><td>Input enabled</td></tr>
<tr><td>X0</td><td>X0</td><td>Input enabled</td><td>Input enabled</td><td>Hi-Z/ Input enabled</td><td>Hi-Z/ Input enabled</td></tr>
<tr><td>X1</td><td>X1</td><td>Input enabled</td><td>Input enabled</td><td>"H" output/ Input enabled</td><td>"H" output/ Input enabled</td></tr>
<tr><td>X0A</td><td>X0A
(When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)</td><td>Input disabled</td><td>Input disabled</td><td>Hi-Z/ Input enabled</td><td>Hi-Z/ Input enabled</td></tr>
<tr><td>X1A</td><td>X1A
(When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)</td><td>Input disabled</td><td>Input disabled</td><td>"H" output/ Input enabled</td><td>"H" output/ Input enabled</td></tr>
<tr><td>MD0</td><td>MD0</td><td>Input enabled</td><td>Input enabled</td><td rowspan="2">Input enabled</td><td rowspan="2">Input enabled</td></tr>
<tr><td>MD1</td><td>MD1</td><td>Input enabled</td><td>Input enabled</td></tr>
<tr><td>P00</td><td>P00/TIOA0/SOUT0_1/IN0</td><td rowspan="8">Output Hi-Z</td><td rowspan="8">Output Hi-Z Input enabled</td><td rowspan="8">Maintain previous state</td><td rowspan="8">Maintain previous state</td><td rowspan="8">Output Hi-Z/ Internal in-put fixed at "0"</td></tr>
<tr><td>P01</td><td>P01/TIOB0/SIN0_1/IN1</td></tr>
<tr><td>P02</td><td>P02/TIOA1/SCK0_1/IN2</td></tr>
<tr><td>P03</td><td>P03/TIOB1/IN3</td></tr>
<tr><td>P04</td><td>P04/TIOA2/SOUT1</td></tr>
<tr><td>P05</td><td>P05/TIOB2/SIN1</td></tr>
<tr><td>P06</td><td>P06/TIOA3/SCK1</td></tr>
<tr><td>P07</td><td>P07/TIOB3</td></tr>
<tr><td>P10</td><td>P10/TIOA4/SOUT2/INT0</td><td rowspan="8">Output Hi-Z</td><td rowspan="8">Output Hi-Z Input enabled</td><td rowspan="8">Maintain previous state</td><td rowspan="8">Maintain previous state</td><td rowspan="8">Output Hi-Z/ Internal input fixed at "0"

Input enabled when interrupt function selected and enabled</td></tr>
<tr><td>P11</td><td>P11/TIOB4/SIN2/INT1</td></tr>
<tr><td>P12</td><td>P12/TIOA5/SCK2/INT2</td></tr>
<tr><td>P13</td><td>P13/TIOB5/INT3</td></tr>
<tr><td>P14</td><td>P14/TIOA6/SOUT3/INT4</td></tr>
<tr><td>P15</td><td>P15/TIOB6/SIN3/INT5</td></tr>
<tr><td>P16</td><td>P16/TIOA7/SCK3/INT6</td></tr>
<tr><td>P17</td><td>P17/TIOB7/INT7</td></tr>
</table>

(Continued)

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		SLVL1 = 0	SLVL1 = 1
P20	P20/SOUT8	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P21	P21/SIN8					
P22	P22/SCK8					
P23	P23/RCIN_1					
P24	P24/SOUT9/OUT0					
P25	P25/SIN9/OUT1					
P26	P26/SCK9/OUT2					
P27	P27/OUT3					
P30	P30/SOUT10/INT8	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P31	P31/SIN10/INT9					
P32	P32/SCK10/INT10					
P33	P33/INT11					
P34	P34/SOUT11/INT12					
P35	P35/SIN11/INT13					
P36	P36/SCK11/INT14					
P37	P37/INT15					
P50	P50	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P51	P51					
P52	P52					
P53	P53					
P54	P54/RCIN					
P55	P55/ADTRG					
P56	P56/FRCK					
P57	P57					
P70	P70/AN0/OUT0_1	Output Hi-Z	Output Hi-Z Input enabled*	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P71	P71/AN1/OUT1_1					
P72	P72/AN2/TMO0/OUT2_1					
P73	P73/AN3/TMO1/OUT3_1					
P74	P74/AN4/TMO2					
P75	P75/AN5/SOUT0/TMI0					
P76	P76/AN6/SIN0/TMI1					
P77	P77/AN7/SCK0/TMI2					
PK0	PK0	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PK1	PK1					

* : Analog input has a priority (digital input is disconnected)

(Continued)

(Continued)

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}}$ = "L"	**$\overline{\text{INIT}}$ = "H"**		**SLVL1 = 0**	**SLVL1 = 1**
UDP	UDP(USB)	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state/ Input enabled	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
UDM	UDM(USB)					
DCKI	DCKI	Input state	Input enabled	Input enabled	Input state	Input state
DCKO	DCKO	L output	L output/ DCK output	L output/ DCK output	L output (OSDC stop)	L output (OSDC stop)
VSYNC	VSYNC	Input state	Input enabled	Input enabled	Input state	Input state
HSYNC	HSYNC					
R4 to R0	R4 to R0	L output	L output/ R output	L output/ R output	L output (OSDC stop)	L output (OSDC stop)
G5 to G0	G5 to G0		L output/ G output	L output/ G output		
B4 to B0	B4 to B0		L output/ B output	L output/ B output		
VOA2 to VOA0	VOA2 to VOA0		L output/ VOA output	L output/ VOA output		
VOB	VOB		L output/ VOB output	L output/ VOB output		
ROUT	ROUT		L output/ ROUT output	L output/ ROUT output		
GOUT	GOUT		L output/ GOUT output	L output/ GOUT output		
BOUT	BOUT		L output/ BOUT output	L output/ BOUT output		
HWDE	HWDE	Input state	Input enabled	Input enabled	Input state	Input state

• List of pin status (serial write mode)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"	
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	—
X0	X0	Input enabled	Input enabled	Input enabled
X1	X1	Input enabled	Input enabled	Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
MD0	MD0	Input enabled	Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled	Input enabled
P00	P00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P01	P01/TIOB0/SIN0_1/IN1			
P02	P02/TIOA1/SCK0_1/IN2			
P03	P03/TIOB1/IN3			
P04	P04/TIOA2/SOUT1			
P05	P05/TIOB2/SIN1			
P06	P06/TIOA3/SCK1			
P07	P07/TIOB3			
P10	P10/TIOA4/SOUT2/INT0	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P11	P11/TIOB4/SIN2/INT1			
P12	P12/TIOA5/SCK2/INT2			
P13	P13/TIOB5/INT3			
P14	P14/TIOA6/SOUT3/INT4			
P15	P15/TIOB6/SIN3/INT5			
P16	P16/TIOA7/SCK3/INT6			
P17	P17/TIOB7/INT7			
P20	P20/SOUT8	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P21	P21/SIN8			
P22	P22/SCK8			
P23	P23/RCIN_1			
P24	P24/SOUT9/OUT0			
P25	P25/SIN9/OUT1			
P26	P26/SCK9/OUT2			
P27	P27/OUT3			

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"	
P30	P30/SOUT10/INT8	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P31	P31/SIN10/INT9	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P32	P32/SCK10/INT10	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P33	P33/INT11	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P34	P34/SOUT11/INT12	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P35	P35/SIN11/INT13	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P36	P36/SCK11/INT14	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P37	P37/INT15	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P50	P50	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P51	P51	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P52	P52	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P53	P53	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P54	P54/RCIN	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P55	P55/ADTRG	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P56	P56/FRCK	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P57	P57	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P70	P70/AN0/OUT0_1	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P71	P71/AN1/OUT1_1	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P72	P72/AN2/TMO0/OUT2_1	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P73	P73/AN3/TMO1/OUT3_1	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P74	P74/AN4/TMO2	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P75	P75/AN5/SOUT0/TMI0	Output Hi-Z	Output	Output
P76	P76/AN6/SIN0/TMI1	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P77	P77/AN7/SCK0/TMI2	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
PK0	PK0	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
PK1	PK1	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
UDP	UDP (USB)	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
UDM	UDM (USB)	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
DCKI	DCKI	Input state	Input enabled	Input enabled
DCKO	DCKO	L output	L output	L output
VSYNC	VSYNC	Input state	Input enabled	Input enabled
HSYNC	HSYNC	Input state	Input enabled	Input enabled

(Continued)

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"	
R4 to R0	R4 to R0	L output	L output	L output
G5 to G0	G5 to G0			
B4 to B0	B4 to B0			
VOA2 to VOA0	VOA2 to VOA0			
VOB	VOB			
ROUT	ROUT	L output	L output	L output
GOUT	GOUT			
BOUT	BOUT			
HWDE	HWDE	Input state	Input enabled	Input enabled

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	Vss – 0.3	Vss + 4.0	V	
Analog power supply voltage*1, *3	AV_{CC}	Vss – 0.3	Vss + 4.0	V	
Analog reference voltage*1, *3	AVRH	Vss – 0.3	Vss + 4.0	V	
Input voltage*1	V_I	Vss – 0.3	Vcc + 0.3 (≤ 4.0)	V	*7
		Vss – 0.3	Vss + 6.0	V	5 V tolerant
		Vss – 0.5	Vss + 4.5	V	USB I/O
Analog pin input voltage*1	V_{IA}	Vss – 0.3	Vss + 4.0	V	
Output voltage*1	V_O	Vss – 0.3	Vcc + 0.3	V	
		Vss – 0.5	Vss + 4.5	V	USB I/O
Maximum clamp current	I_{CLAMP}	– 4	+ 4	mA	*8
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	—	40	mA	*8
“L” level maximum output current*4	I_{OL}	—	10	mA	
		—	43	mA	USB I/O
“L” level average output current*5	I_{OLAV}	—	4	mA	
		—	15	mA	USB I/O
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*6	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*4	I_{OH}	—	– 10	mA	
		—	– 43	mA	USB I/O
“H” level average output current*5	I_{OHAV}	—	– 4	mA	
		—	– 15	mA	USB I/O
“H” level total maximum output current*6	ΣI_{OH}	—	– 100	mA	
“H” level total average output current	ΣI_{OHAV}	—	– 50	mA	
Power consumption (Flash product)	P_D	—	850	mW	
Power consumption (MASK product)		—	600	mW	
Operating temperature	Ta	– 40	+ 85	°C	
Storage temperature	T_{STG}	– 55	+ 125	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : V_{CC} must not drop below V_{SS} – 0.3 V.

*3 : Be careful not to exceed V_{CC} + 0.3 V, for example, when the power is turned on.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output is the average current for a single pin over a period of 100 ms.

(Continued)

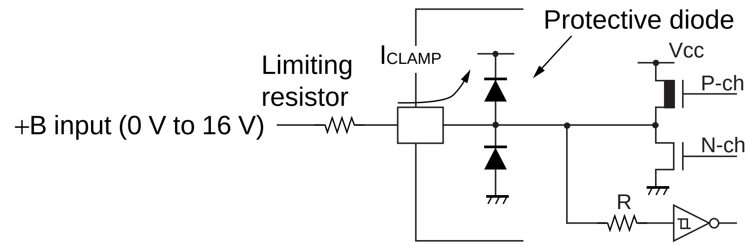
(Continued)

*6 : The total average output current is the average current for all pins over a period of 100 ms.

*7 : If the input current or the maximum input current are limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*8 : • Corresponding pins:P14 to P17,P20 to P27,P30 to P37,P50 to P57
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Do not leave +B input pins open.
- Sample recommended circuit

•Input/output equivalent circuit



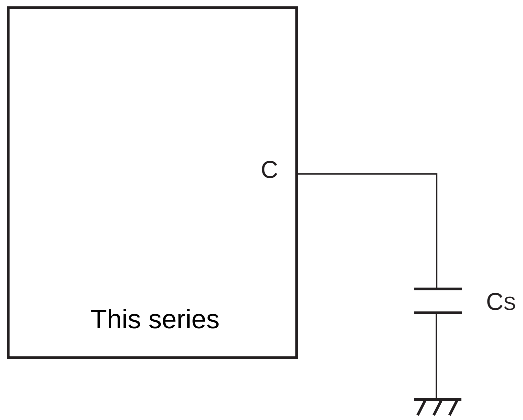
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	—	3.6	V	
Analog power supply voltage	AV_{CC}	3.0	—	3.6	V	$AV_{CC} \leq V_{CC}$
Analog reference voltage	AVRH	AV_{SS}	—	AV_{CC}	V	
Smoothing capacitor	Cs	—	4.7	—	µF	
Operating temperature	Ta	– 40	—	+ 85	°C	

• C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(1) DC Characteristics

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current (Flash product)	I_{CC}	V_{CC}	Normal operation	—	45	60	mA	OSDC stopped Not using USB CPU : 33 MHz, Peripheral : 33 MHz
				—	55	75	mA	OSDC stopped Using USB CPU : 32 MHz, Peripheral : 32 MHz
	I_{CCO}			—	100	130	mA	Dot clock 50 MHz (PLL) Dot clock PLL is used Analog RGB DAC is used Digital RGB is not used CPU : 33 MHz, Peripheral : 33 MHz
				—	105	150	mA	Dot clock 75 MHz (PLL) Dot clock PLL is used Analog RGB DAC is not used Digital RGB is used CPU : 33 MHz, Peripheral:33 MHz
	I_{CCS}		SLEEP mode	—	15	25	mA	OSDC stopped Not using USB Peripheral : 33 MHz
				—	25	40	mA	OSDC stopped Using USB Peripheral : 32 MHz
	I_{CCL}		Sub operation*	—	150	550	µA	CPU : 32 kHz Peripheral : 32 kHz
	I_{CCT}		Watch mode*	—	120	450	µA	
	I_{CCH}		STOP mode*	—	65	320	µA	

* : Ta = + 25 °C and V_{CC} = 3.3 V

(Continued)

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current (MASK product)	I_{CC}	V_{CC}	Normal operation	—	35	45	mA	OSDC stopped Not using USB CPU : 33 MHz, Peripheral : 33 MHz
				—	50	60	mA	OSDC stopped Us-ing USB CPU : 32 MHz, Peripheral : 32 MHz
	I_{CCO}			—	80	100	mA	Dot clock 50 MHz (PLL) Dot clock PLL is used Analog RGB DAC is used Digital RGB is not used CPU : 33 MHz, Peripheral : 33 MHz
				—	80	110	mA	Dot clock 75 MHz (PLL) Dot clock PLL is used Analog RGB DAC is not used Digital RGB is used CPU : 33 MHz, Peripheral:33 MHz
	I_{CCS}		SLEEP mode	—	15	25	mA	OSDC stopped Not using USB Peripheral : 33 MHz
				—	25	40	mA	OSDC stopped Us-ing USB Peripheral : 32 MHz
	I_{CCL}		Sub operation*	—	150	550	µA	CPU : 32 kHz Peripheral : 32 kHz
	I_{CCT}		Watch mode*	—	120	450	µA	
	I_{CCH}		STOP mode*	—	65	320	µA	

* : Ta = + 25 °C and V_{CC} = 3.3 V

(Continued)

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	P00 to P07, P10 to P17, P50 to P57, P70 to P77, PK0, PK1, DCKI, VSYNC, HSYNC, $\overline{\text{INIT}}$, MD0, MD1	—	V_{CC} × 0.8	—	V_{CC} + 0.3	V	
		P20 to P27, P30 to P37	—	V_{CC} × 0.8	—	V_{SS} + 5.5	V	5 V tolerant
"L"level input voltage (hysteresis input)	V_{ILS}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, PK0, PK1, DCKI, VSYNC, HSYNC, $\overline{\text{INIT}}$, MD0, MD1	—	Vss − 0.3	—	V_{CC} × 0.2	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, PK0, PK1, R0 to R4, G0 to G5, B0 to B4, VOA0 to VOA2, VOB, DCKO	V_{CC} = 3.0 V, I_{OH} = − 4 mA	V_{CC} − 0.5	—	V_{CC}	V	
"L" level output voltage	V_{OL}		V_{CC} = 3.0 V, I_{OL} = 4 mA	V_{SS}	—	0.4	V	
Input leak current	I_{IL}	—	—	− 5	—	+ 5	µA	Digital pin
				− 10	—	+ 10	µA	Analog pin
Pull-up resistance value	R_{PU}	Pull-up pin	—	16.6	33	66	kΩ	
Pull-down resistance value	R_{PD}	IBREAK ICD0 to ICD3	—	16.6	33	66	kΩ	MB91F610A only
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, AVRH	—	—	10	15	pF	

(Continued)

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(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB reference voltage	V_{REF}	VREF	—	1.05	1.10	1.15	V	
Analog RGB reference resistance	R_{REF}	VRO-VSSD	—	2.4	2.7	—	kΩ	
Analog RGB external load resistance	R_L	ROUT, GOUT, BOUT	—	—	150	160	Ω	

4. AC Characteristics

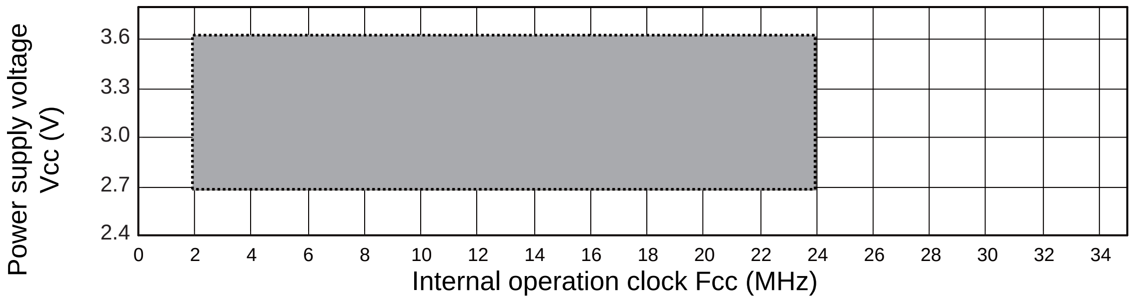
(1) Main Clock (MCLK) Input Standard

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

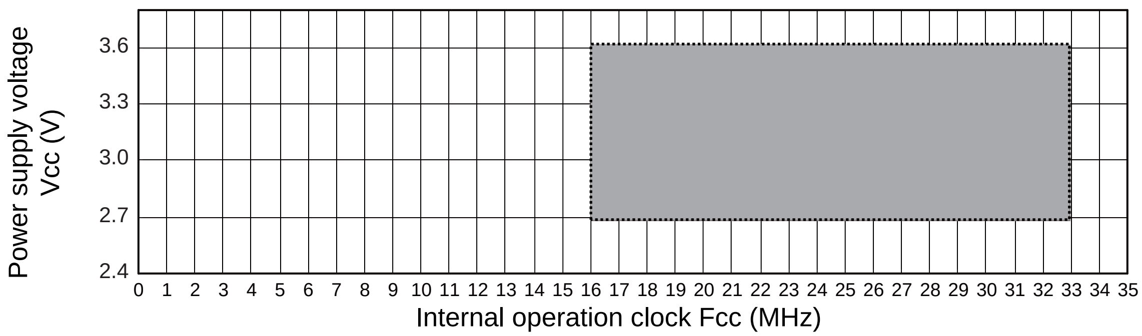
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	—	4	48	MHz	When crystal oscillator is connected
			—	4	48	MHz	When using external clock
Input clock cycle	t_{CYLH}		—	20.83	250	ns	When using external clock
Input clock pulse width	—		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF} t_{CR}		—	—	5	ns	When using external clock
Internal operating clock frequency	F_{CS}	—	—	—	33	MHz	Source clock
	F_{CC}	—	—	—	33	MHz	CPU clock
	F_{CP}	—	—	—	33	MHz	Peripheral bus clock
Internal operating clock cycle time	t_{CYCS}	—	—	30	—	ns	Source clock
	t_{CYCC}	—	—	30	—	ns	CPU clock
	t_{CYCP}	—	—	30	—	ns	Peripheral bus clock

• Operating guaranteed range (Not using USB)

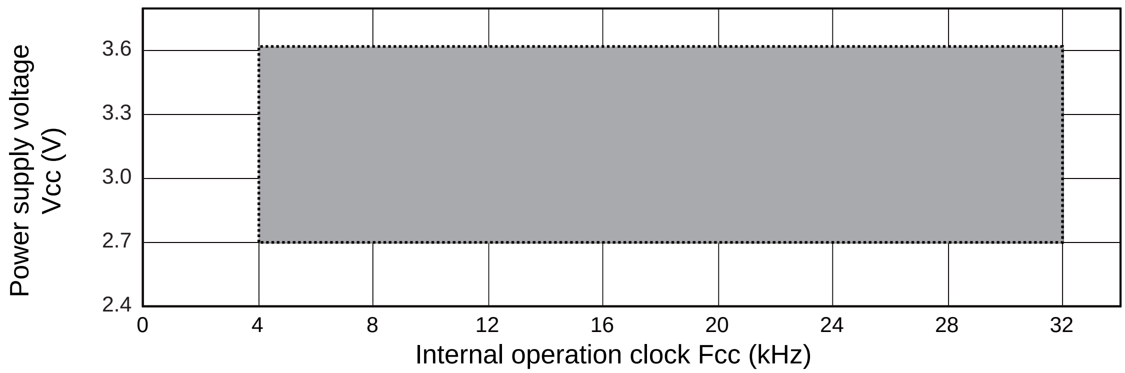
• When the main clock is selected (DIVB=000)



• When the PLL clock is selected (DIVB=000)

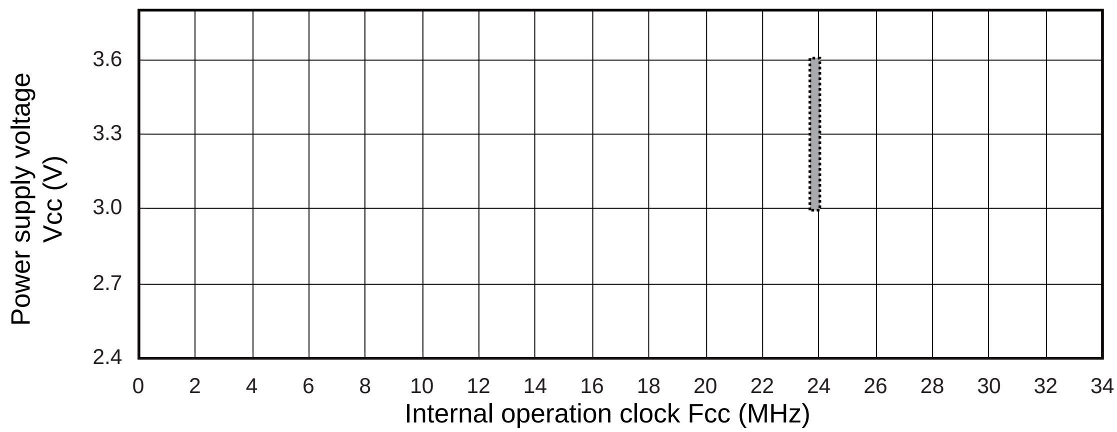


• When the sub clock is selected

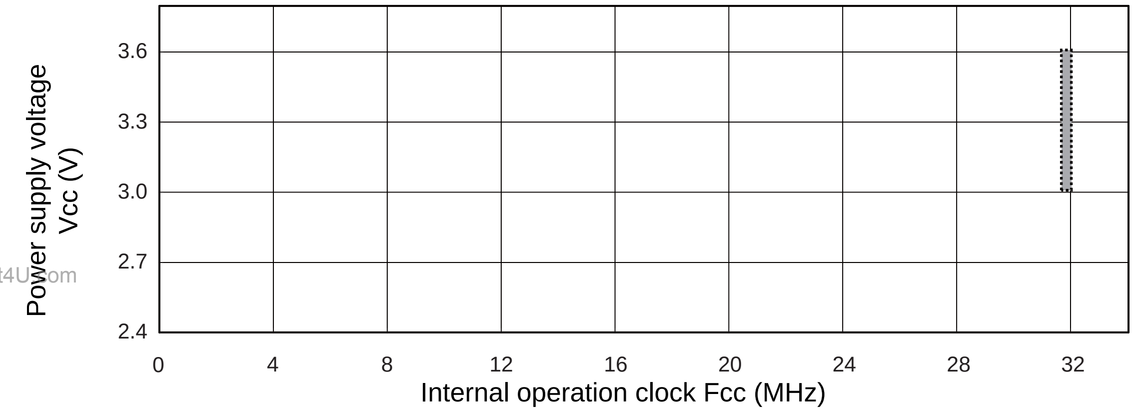


• Operating guaranteed range (at using USB)

• When the main clock is selected (DIVB=000*1)



• When the PLL clock is selected (DIVB=000*1, ODS=10*3, PMS=0111*4, PDS=0000*2, X0=4 MHz or DIVB=000*1, ODS=10*3, PMS=0001*4, PDS=0010*2, X0=48 MHz)



*1 : The values other than DIVB = 000 are omitted.

*2 : The values other than PDS = 0000, 0001,0010 are omitted.

*3 : The values other than ODS = 10 are omitted.

*4 : The values other than PMS = 0001,0111 are omitted.

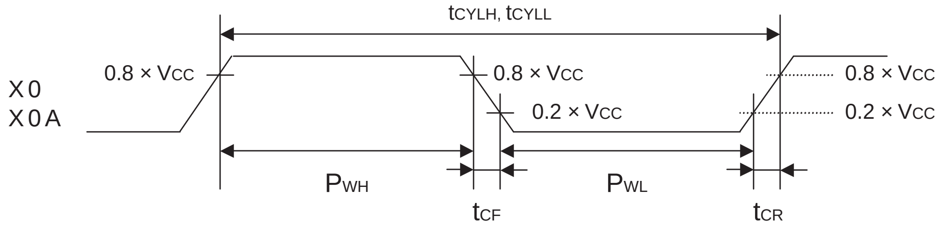
Note: DIVB : Base clock division configuration bit
ODS : PLL macro oscillation clock division rate select bit
PDS : PLL input clock division select bit
PMS : PLL clock multiple rate select bit

(2) Sub Clock (SBCLK) Input Standard

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When crystal oscillator is connected
			—	—	32.768	—	kHz	When using external clock
Input clock cycle	t_{CYLL}		—	—	30.518	—	µs	When using external clock
Input clock pulse width	—		P_{WH} / t_{CYLL} P_{WL} / t_{CYLL}	45	—	55	%	When using external clock
Input clock rise time and fall time	t_{CF} t_{CR}		—	—	—	200	ns	When using external clock

<When external clock input>



(3) Conditions of PLL

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = −40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	600	—	—	µs	Time from when the PLL starts operating until the oscillation stabilizes
PLL oscillation stabilization wait time for OSDC (LOCK UP time)	t_L	10	—	—	ms	
PLL input clock frequency	f_{PLLI}	4	—	24	MHz	
PLL multiple rate	—	4	—	24	multiplied by	ODS × PMS
PLL macro oscillation clock frequency	f_{PLLO}	96	—	100	MHz	

(4) Regulator Voltage Stabilization Wait Time

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = −40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Regulator voltage stabilization wait time	t_{REG}	50	—	µs	Time taken for the regulator voltage to stabilize

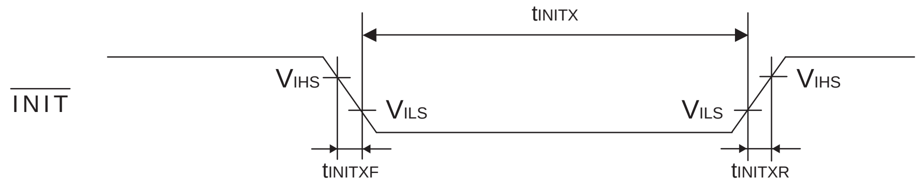
Note : This is the time from when the external power supply stabilizes (after reaching 3.0 V).

(5) Reset Input Standards

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time (At power-on, main oscillation stop mode)	t_{INITX}	$\overline{INIT}$	—	Oscillation time of oscillator + 10 t_{CYLH}	—	ns	*
Reset input time (At other times)	t_{INITX}	$\overline{INIT}$	—	10 t_{CYLH}	—	ns	
Reset input rise time and fall time	t_{INITXF}, t_{INITXR}	$\overline{INIT}$	—	—	10	ms	

* : After the supply voltage has stabilized, it takes a further 50 µs until the internal supply stabilizes. Hold the input to the $\overline{INIT}$ pin during that period.
- At power-on
- When in stop mode
- When in sub mode and sub watch mode when the main oscillation is stopped.

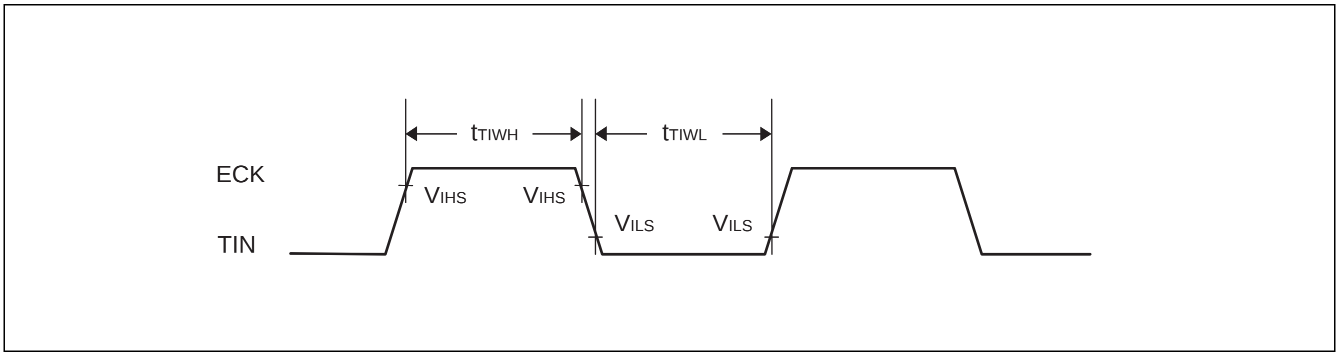


(6) Base Timer Input Timing

• Timer input timing

($V_{CC} = AV_{CC} = 3.0$ V to 3.6 V, $V_{SS} = AV_{SS} = 0$ V, Ta = – 40 °C to + 85 °C)

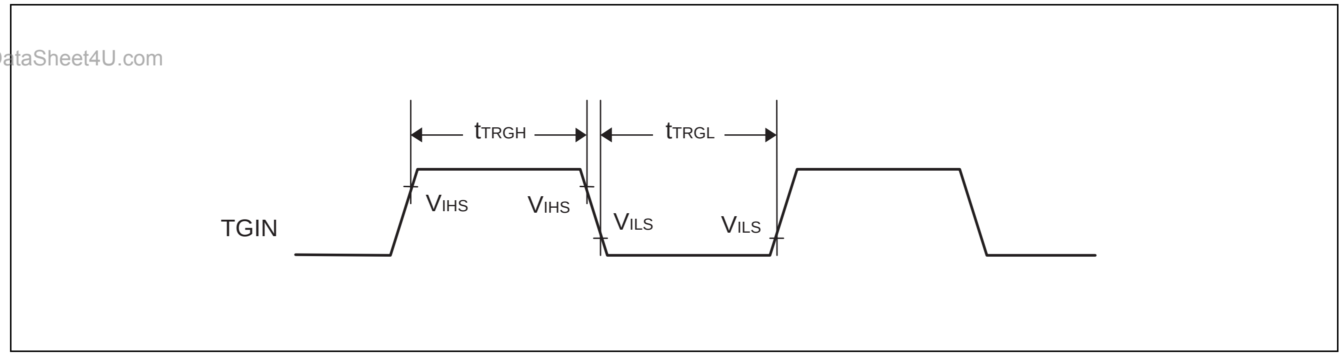
Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (When used as ECK, TIN)	—	2 t_{CYCP}	—	ns



• Trigger Input Timing

($V_{CC} = AV_{CC} = 3.0$ V to 3.6 V, $V_{SS} = AV_{SS} = 0$ V, Ta = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	TIOAn/TIOBn (When used as TGIN)	—	2 t_{CYCP}	—	ns



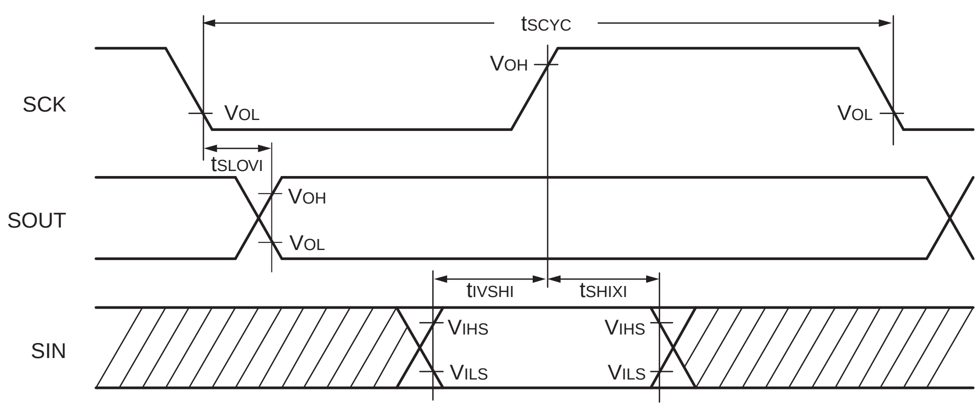
(7) Synchronous serial (CSIO) timing

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

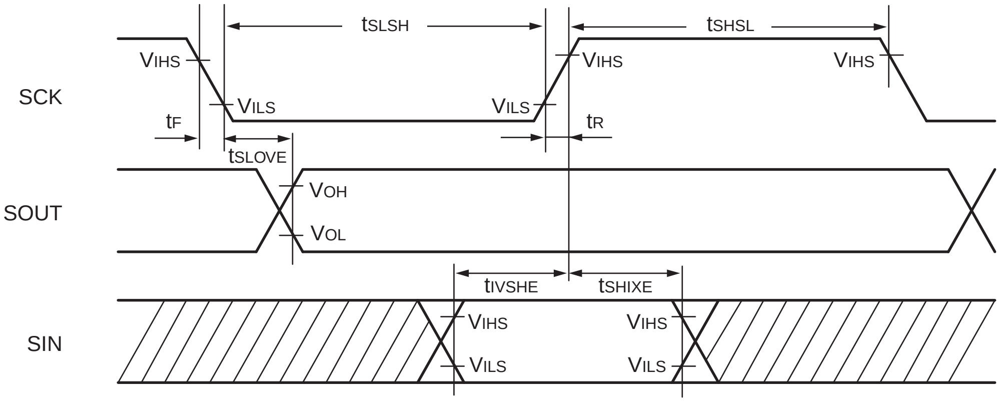
• Synchronous serial (SPI = 0, SCINV = 0)

Parameter	Symbol	Pin name	Conditions	Value Min	Value Max	Unit
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn, SOUTn	Internal shift clock operation	− 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn	Internal shift clock operation	57	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn	Internal shift clock operation	0	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ − 10	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn	External shift clock operation	t_{CYCP} + 10	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn, SOUTn	External shift clock operation	—	48	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn	External shift clock operation	25	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn	External shift clock operation	20	—	ns
SCK fall time	t_F	SCKn	External shift clock operation	—	5	ns
SCK rise time	t_R	SCKn	External shift clock operation	—	5	ns

Notes: • The above standards apply to CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.
• When the external load capacitance C = 50 pF.



MS bit = 0

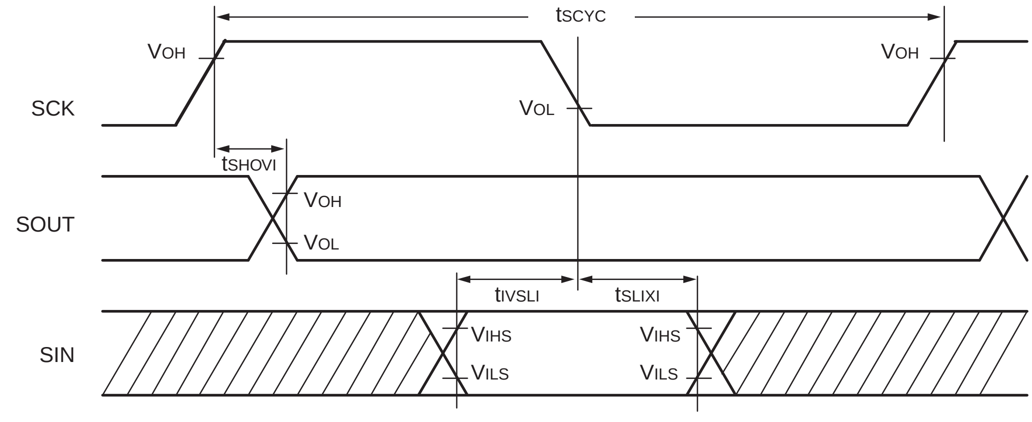


MS bit = 1

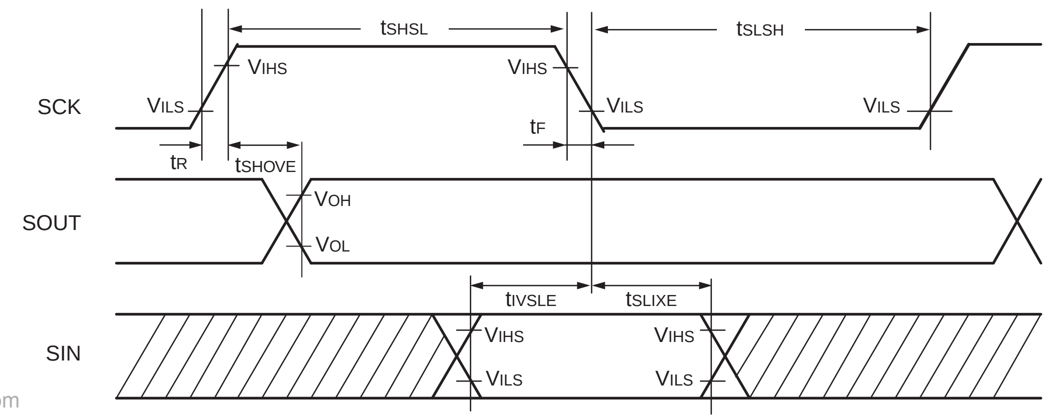
• Synchronous serial (SPI = 0, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value Min	Value Max	Unit
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↑→ SOUT delay time	t_{SHOVI}	SCKn SOUTn		– 30	+ 30	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKn SINn		57	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKn SINn		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		$t_{CYCP} + 10$	—	ns
SCK ↑ → SOUT delay time	t_{SHOVE}	SCKn SOUTn		—	48	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKn SINn		25	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes:
- The above standards apply to CLK synchronous mode.
- t_{CYCP} indicates the peripheral clock cycle time.
- When the external load capacitance C = 50 pF.



MS bit = 0

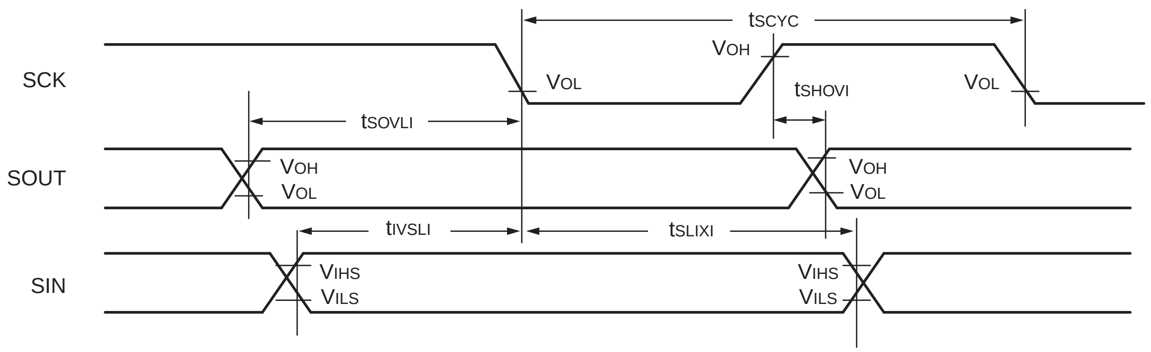


MS bit = 1

• Synchronous serial (SPI = 1,SCINV = 0)

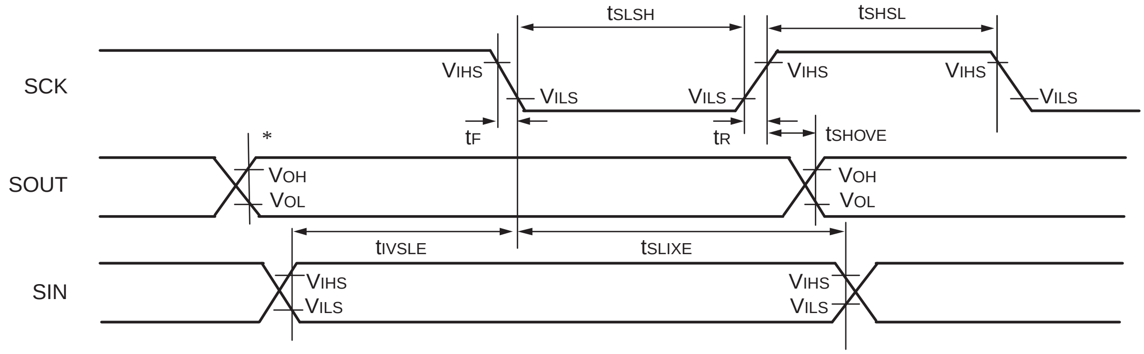
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↑→ SOUT delay time	t_{SHOVI}	SCKn SOUTn		– 30	+ 30	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKn SINn		57	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKn SINn		0	—	ns
SOUT → SCK ↓ delay time	t_{SOVLI}	SCKn SOUTn		$2t_{CYCP}$ – 30	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ – 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↑ → SOUT delay time	t_{SHOVE}	SCKn SOUTn		—	48	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKn SINn		25	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.
• When the external load capacitance C = 50 pF.



MS bit = 0

FUJITSU



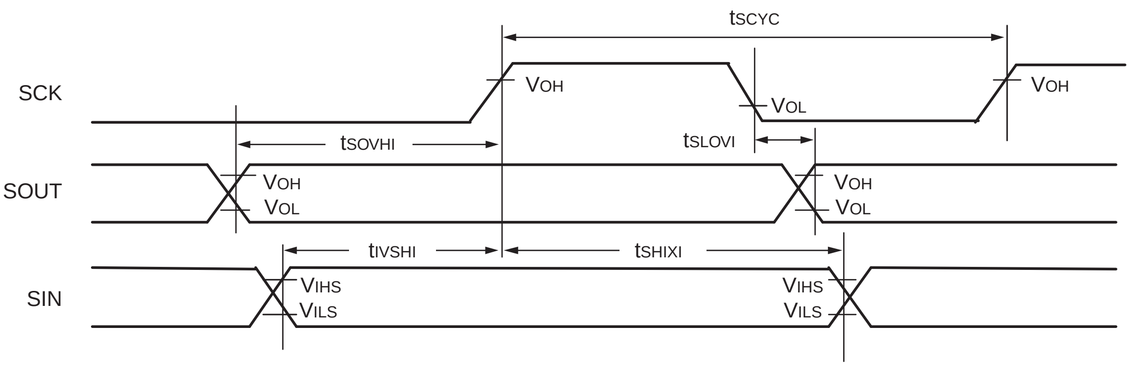
MS bit = 1

* : Changes when writing to TDR register

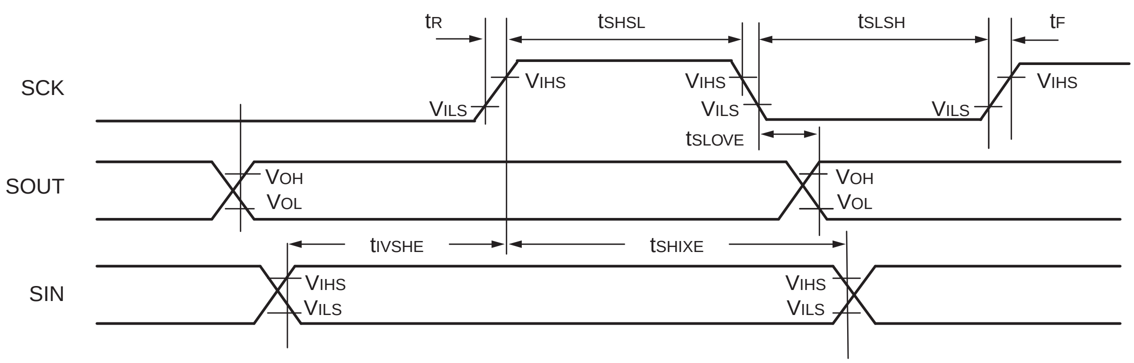
• Synchronous serial (SPI = 1, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value Min	Value Max	Unit
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn SOUTn		– 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		57	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn SINn		0	—	ns
SOUT → SCK ↑ delay time	t_{SOVHI}	SCKn SOUTn		$2t_{CYCP} - 30$	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		$t_{CYCP} + 10$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn SOUTn		—	48	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		25	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.
• When the external load capacitance C = 50 pF.



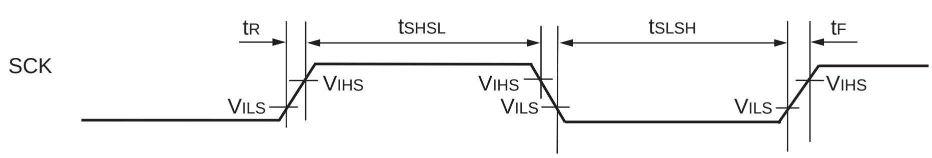
MS bit = 0



MS bit = 1

- External clock (EXT = 1) : asynchronous only

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock “L” pulse width	t_{SLSH}	C_L = 50 pF	t_{CYCP} + 10	—	ns
Serial clock “H” pulse width	t_{SHSL}		t_{CYCP} + 10	—	ns
SCK fall time	t_F		—	5	ns
SCK rise time	t_R		—	5	ns



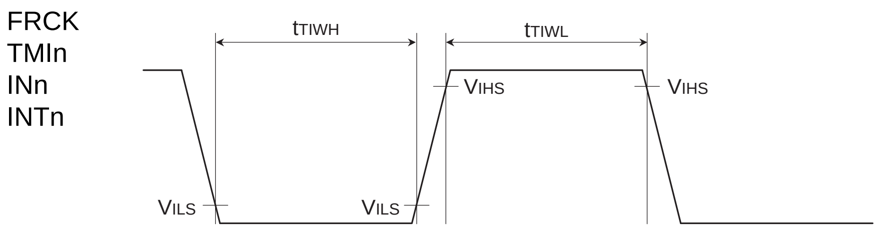
(8) Free-run Timer Clock, Reload Timer Event Input,Input Capture Input, Interrupt Input Timing

($V_{CC} = AV_{CC} = 3.0$ V to 3.6 V, $V_{SS} = AV_{SS} = 0$ V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	FRCK TMIn INn	—	2 t_{CYCP}	—	ns	*1
		INTn	—	3 t_{CYCP}	—	ns	*1
			—	1.0	—	µs	*2

*1 : t_{CYCP} indicates peripheral clock cycle time, except when in stop mode, in main timer mode and in watch mode.

*2 : When in stop mode, in main timer mode, or in watch mode.

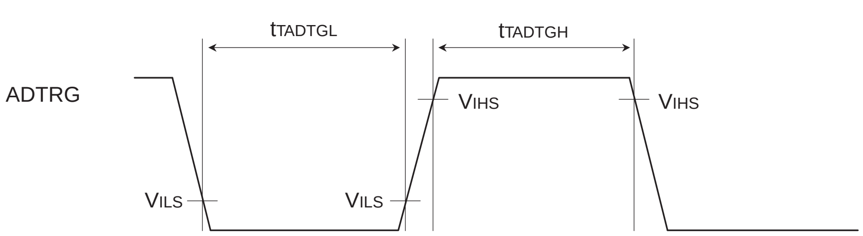


(9) A/D Converter Trigger Input Timing

($V_{CC} = AV_{CC} = 3.0$ V to 3.6 V, $V_{SS} = AV_{SS} = 0$ V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
A/D converter trigger input	t_{TADTGL} t_{TADTGH}	ADTRG	—	2 t_{CYCP}	—	ns	*

* : t_{CYCP} indicates peripheral clock cycle time.



(10) I²C Timing

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

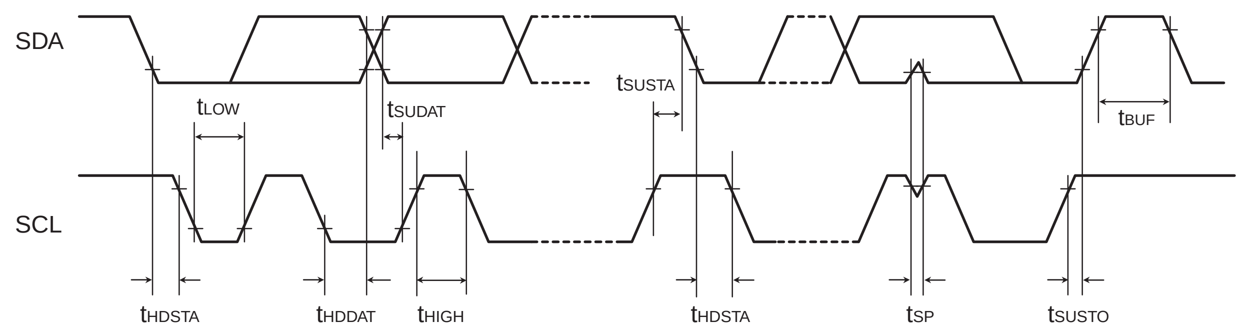
Parameter	Symbol	Pin name	Conditions	Typical mode		High-speed mode*3		Unit
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCKn (SCLn)	C_L = 50 pF, R = (V_p/I_{OL}) *1	0	100	0	400	kHz
"(Repeated) START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOUTn (SDAn) SCKn (SCLn)		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCKn (SCLn)		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCKn (SCLn)		4.0	—	0.6	—	µs
"Repeated START condition" setup time SCL ↑→ SDA ↓	t_{SUSTA}	SCKn (SCLn)		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOUTn (SDAn) SCKn (SCLn)		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑→ SCL↑	t_{SUDAT}	SOUTn (SDAn) SCKn (SCLn)		250	—	100	—	ns
"STOP condition" setup time SCL↑→ SDA↑	t_{SUSTO}	SOUTn (SDAn) SCKn (SCLn)		4.0	—	0.6	—	µs
Bus free time between "STOP condition" and "START condition"	t_{BUF}	—		4.7	—	1.3	—	µs
Noise filter	t_{SP}	—	—	2 t_{CYCP} *4	—	2 t_{CYCP} *4	—	ns

*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4 : t_{CYCP} is the peripheral clock cycle time. To use I²C, set the peripheral bus clock at 8 MHz or more.



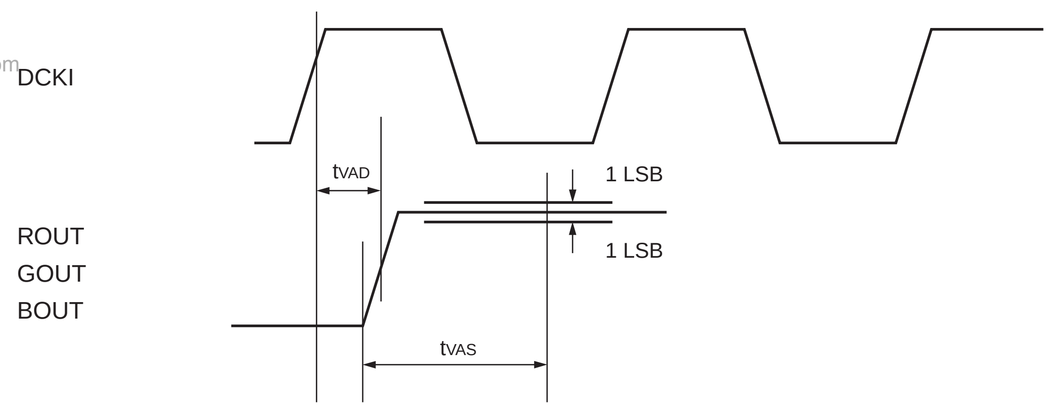
(11) Analog RGB

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB output delay	t_{VAD}	ROUT, GOUT, BOUT	VREF = 1.1 V, VDDD = 3.3 V, VRO* = 2.7 kΩ	—	12	—	ns	50 MHz (Max)
Analog RGB output settling time	t_{VAS}			—	—	20	ns	

* : VRO is an external resistance for DAC.

- Display signal output timing



(12) Digital RGB

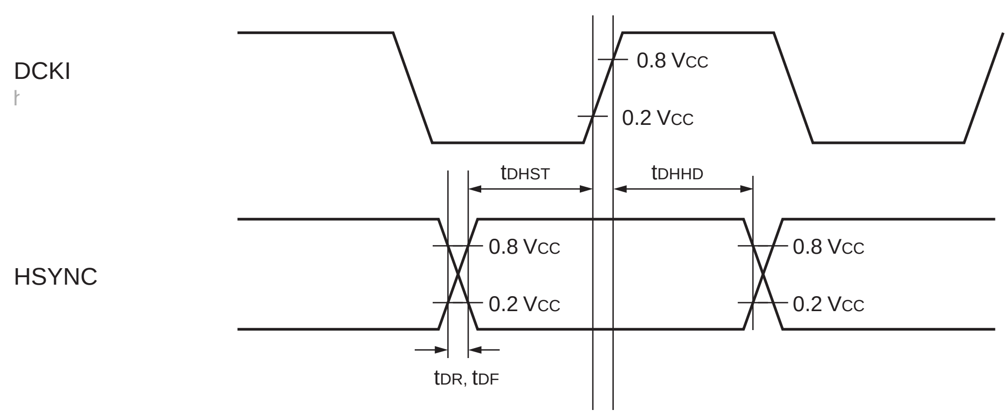
Vertical synchronous/ horizontal synchronous/ display output control signal input timing

($V_{CC} = AV_{CC} = 3.0$ V to 3.6 V, $V_{SS} = AV_{SS} = 0$ V, Ta = − 40 °C to + 85 °C)

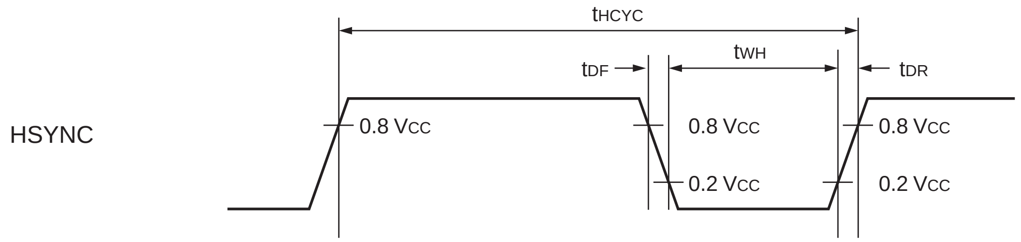
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Horizontal synchronous signal cycle time	t_{HCYC}	HSYNC	100 + t_{WH}	—	Dot clock	
Horizontal synchronous signal pulse width	t_{WH}	HSYNC	20	—	Dot clock	
			—	6	µs	
Horizontal synchronous signal setup time	t_{DHST}	HSYNC	4	—	ns	
Horizontal synchronous signal hold time	t_{DHHD}		0	—	ns	
Vertical synchronous signal setup time	t_{HVST}	VSYNC	5	—	Dot clock	
Vertical synchronous signal hold time	t_{HVHD}		1H – 5	—	Dot clock	*
Input synchronous signal rising/ falling time	t_{DR} t_{DF}	HSYNC, VSYNC	—	2	ns	

* : H stands for the horizontal synchronous signal. 1 synchronous is 1 unit.

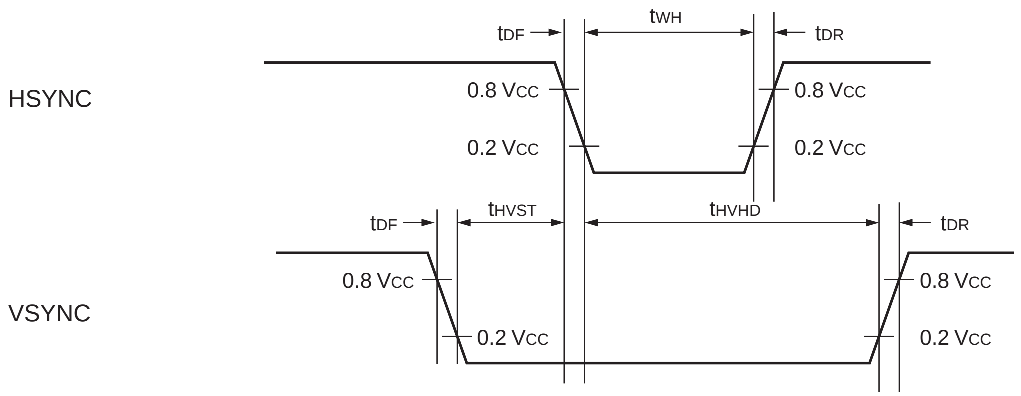
• Horizontal synchronous signal and display output control signal input timing



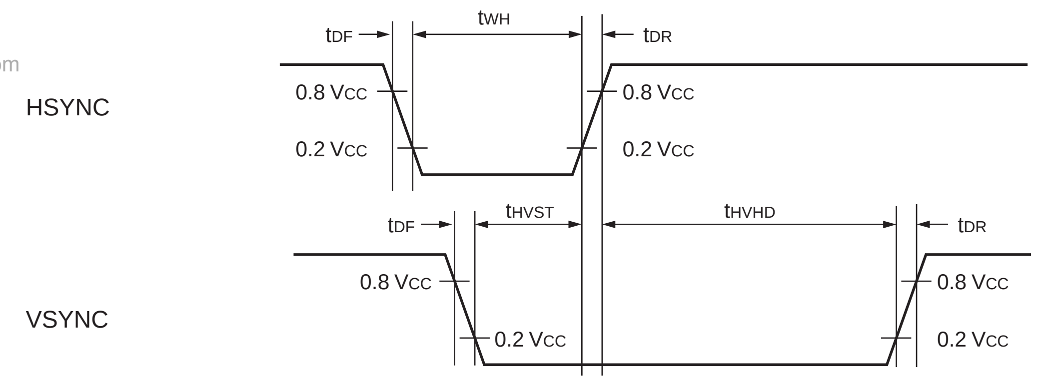
- Horizontal synchronous signal input



- Vertical synchronous signal input timing
    - Detect VSYNC at HSYNC leading edge



- Detect VSYNC at HSYNC trailing edge



(13) Display signal timing

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

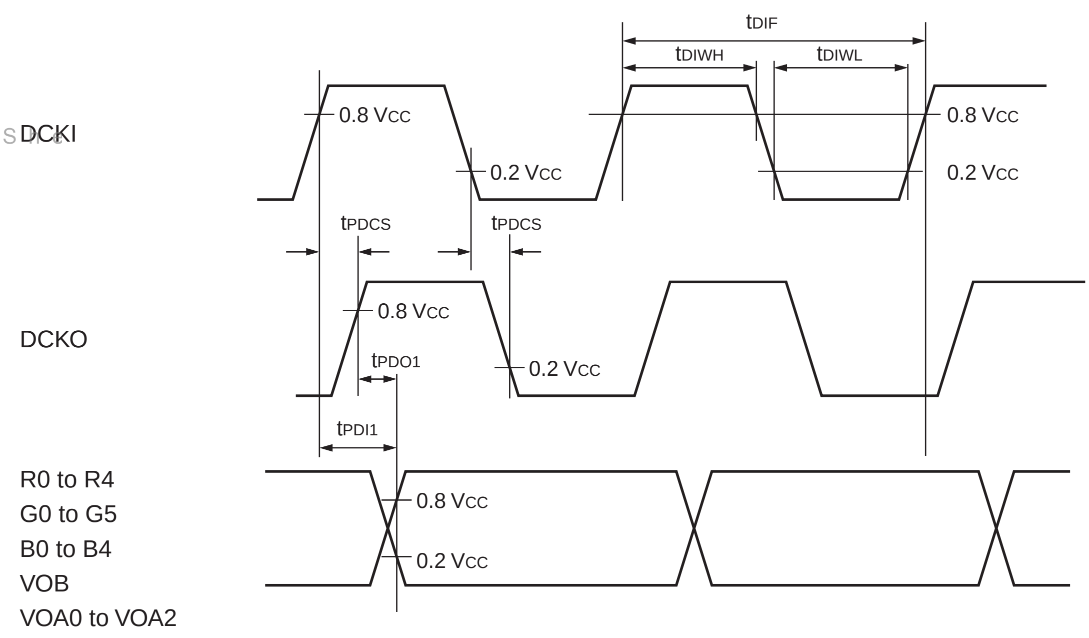
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Dot clock input cycle time	t_{DIF}	DCKI	8	75	MHz	*1
Dot clock input pulse width	t_{DIWH}	DCKI	5	—	ns	*1
	t_{DIWL}		5	—	ns	
Dot clock output delay time1	t_{PDCS}	DCKO	2.2	8	ns	*2
Display signal output delay time I1	t_{PDI1}	R0 to R4, G0 to G5, B0 to B4, VOB, VOA0 to VOA2	2	8.3	ns	*2
Display signal output delay time O1	t_{PDO1}		–4	+5	ns	*2

*1 : Input continuous signal to the dot clock.

*2 : Output load 16 pF

Note: Actual display output varies depending on what is controlled, such as display output control and display location control in each display layer.

• Display signal output timing



5. Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error	—	− 5	—	+ 5	LSB	AV_{CC} = 3.3 V, AVRH = 3.3 V
Linearity error	—	− 3.5	—	+ 3.5	LSB	
Differential linearity error	—	− 3	—	+ 3	LSB	
Zero transition voltage	AN0 to AN7	− 1.5	+ 0.5	+ 4	LSB	
Full transition voltage	AN0 to AN7	AVRH − 4	AVRH − 1.5	AVRH + 0.5	LSB	
Compare time	—	0.72*3	—	—	µs	PCLK = 33 MHz
Conversion time	—	1.2*1	—	—	µs	PCLK = 33 MHz
Power supply current (analog + digital)	AV_{CC}	—	—	3.5	mA	D/A stopped
		—	—	11	µA	At power-down*2
Reference power supply current (between AVRH and AV_{SS})	AVRH	—	—	0.6	mA	AVRH = 3.0 V
		—	—	5	µA	At power-down*2
Analog input capacity	—	—	—	8.5	pF	
Interchannel disparity	—	—	—	4	LSB	
Analog port input current	AN0 to AN7	—	—	10	µA	
Analog input voltage	AN0 to AN7	AV_{SS}	—	AVRH	V	
Standard voltage	AVRH	AV_{SS}	—	AV_{CC}	V	

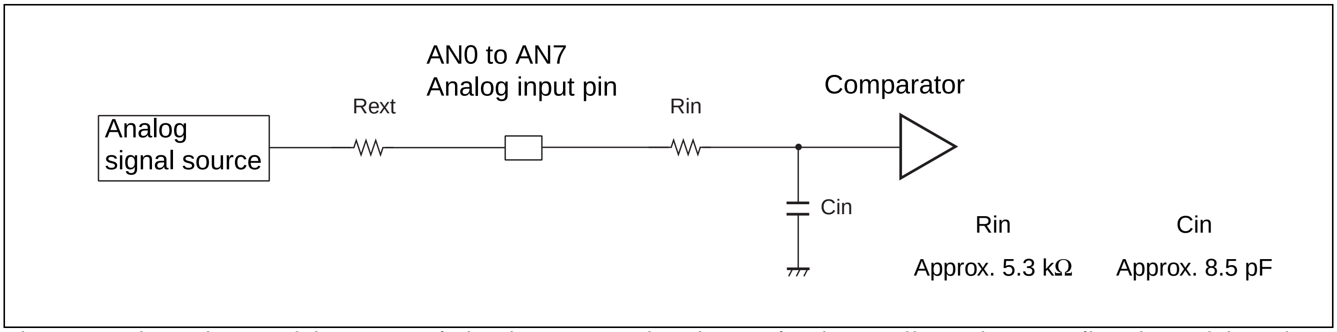
*1 : Depending on the clock cycle supplied to peripheral resources.
Ensure that it satisfies the value; PCLK cycle × more than 4 + the value calculated from (Equation 1).
The condition of the minimum conversion time is when PCLK = 33 MHz, the value of sampling time: 0.424 µs, external impedance: 1.4 kΩ or less and compare time: 0.72 µs.

(Continued)

(Continued)

*2 : The current when the CPU is in stop mode and the A/D converter is not operating.

*3 : Compare time = {(CT + 1) × 10 + 4} × peripheral clock (PCLK) period. (CT indicates compare time setting bits.)
The condition of the minimum compare time is when CT = 1 and PCLK = 33 MHz.



The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of Ts calculated from the following equation.

(Equation 1) Ts = (Rin + Rext) × Cin × 8

Ts : Sampling time
Rin : Input resistance of A/D = 5.3 kΩ
Cin : Input capacitance of A/D = 8.5 pF
Rext : Output impedance of external circuit

If the sampling time is set as 600 ns,

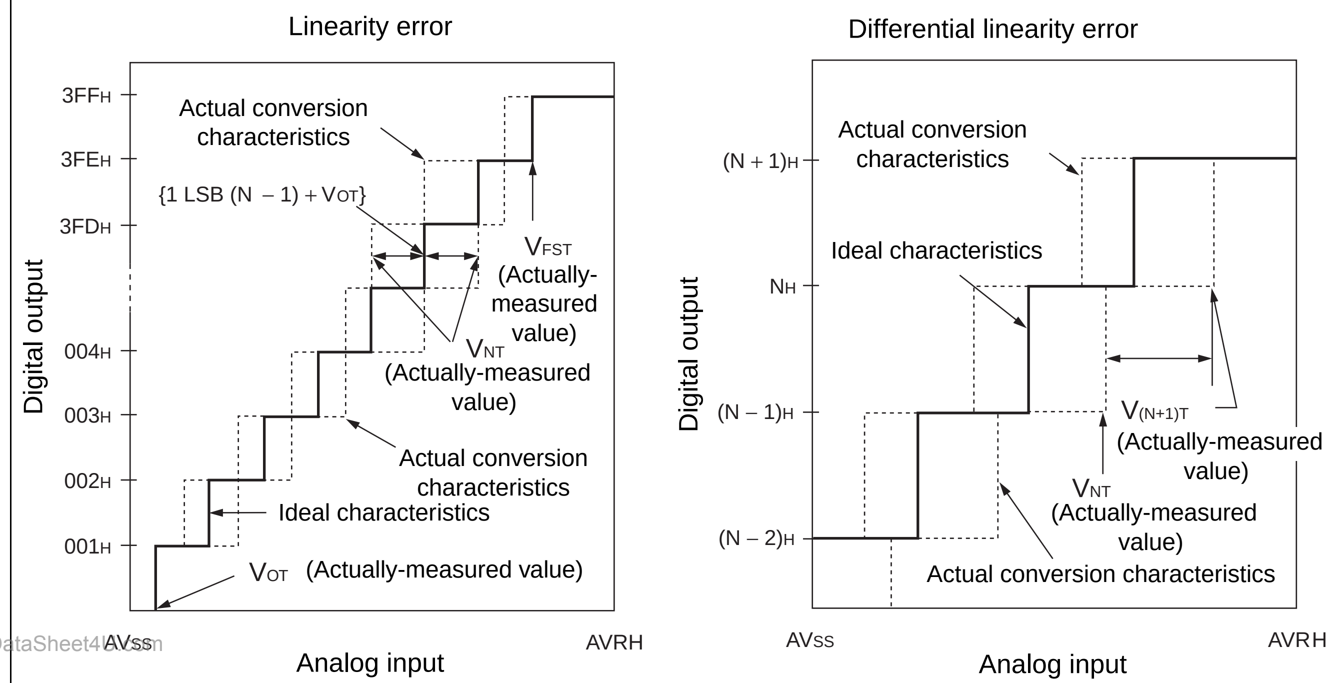
$600\ \text{ns} \geq (5.3\ \text{k}\Omega + \text{Rext}) \times 8.5\ \text{pF} \times 8$

$\therefore \text{Rext} \leq 3.5\ \text{k}\Omega$

And the impedance of the external circuit therefore needs to be 3.5 kΩ or less.

- Definition of 10-bit A/D Converter Terms

  - Resolution : Analog variation that is recognized by an A/D converter.
  - Linearity error : Deviation of the line between the zero-transition point (0000000000←→0000000001) and the full-scale transition point (1111111110←→1111111111) from the actual conversion characteristics.
  - Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
  - Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}'}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.
V_{NT} : Voltage at which the digital output changes from $(N - 1)_H$ to N_H.

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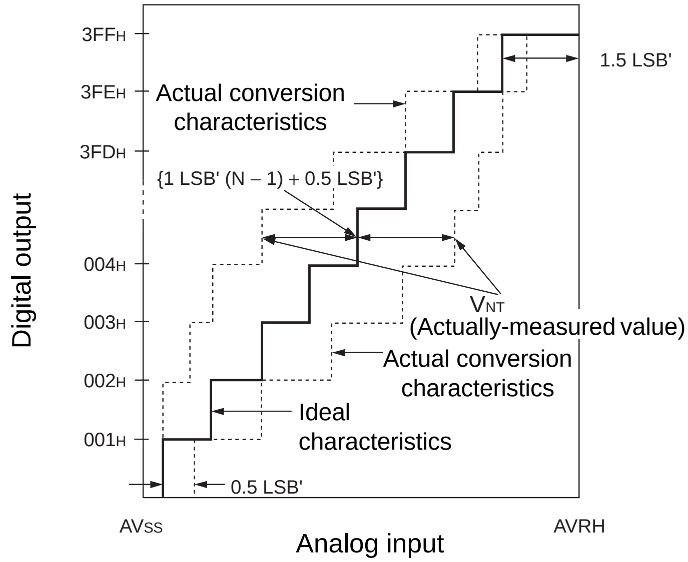
Total error



$$1\text{ LSB' (Ideal value)} = \frac{AVRH - AV_{SS}}{1024}\ [V]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\text{ LSB'} \times (N-1) + 0.5\text{ LSB'}\}}{1\text{ LSB'}}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H.
V_{OT}' (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST}' (Ideal value) = AVRH – 1.5 LSB [V]

6. Electrical Characteristics for the Analog RGB D/A Converter

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = – 40 °C to + 85 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	5	bit	ROUT, BOUT
	—	—	6	bit	GOUT
Linearity error	– 2.0	—	+ 2.0	LSB	When the output is unloaded
Differential linearity error	– 1.0	—	+ 1.0	LSB	When the output is unloaded
Analog output impedance	—	250	—	kΩ	Analog output < 1.0 V
Analog current (R/B/GOUT)	4.5	5.2	5.8	mA	Full-scale
	0	2	20	µA	Zero-scale
Power supply current (VDDD)	—	25	27	mA	VREF = 1.1 V

7. USB Characteristics

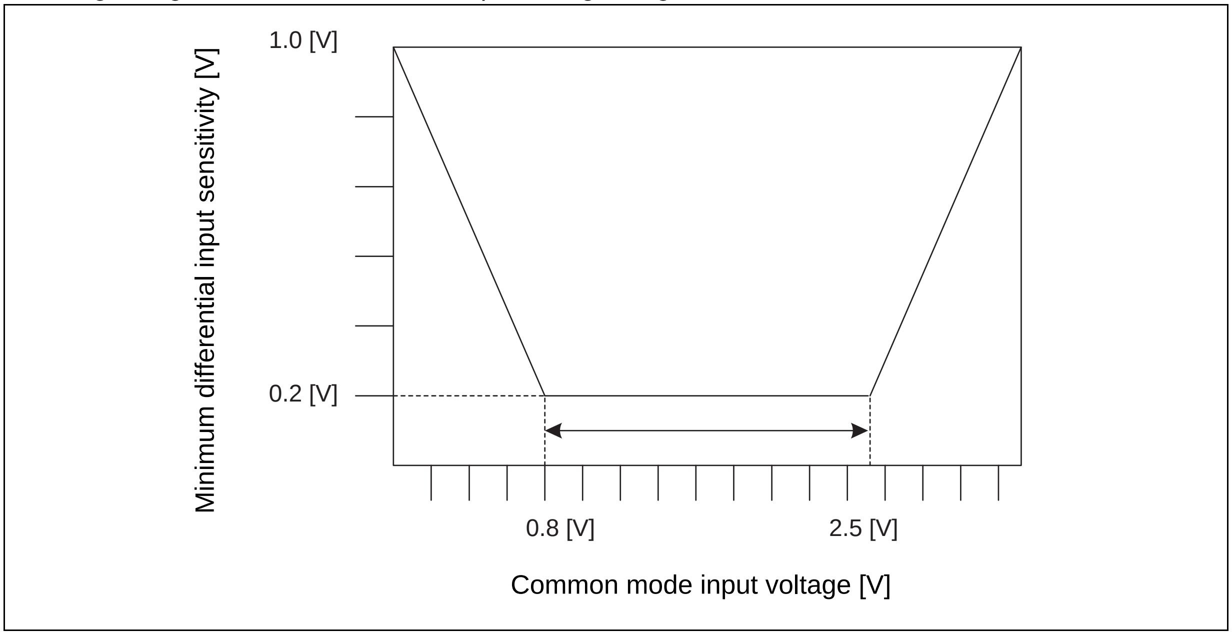
(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter		Symbol	Pin name	Conditions	Value Min	Value Max	Unit	Remarks
Input characteristics	Input High level voltage	V_{IH}	UDP, UDM	—	2.0	V_{CC} + 0.3	V	*1
	Input Low level voltage	V_{IL}		—	V_{SS} − 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		—	0.2	—	V	*2
	Differential common mode input voltage	V_{CM}		—	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output Low level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		—	1.3	2.0	V	*4
	Rise time	t_{FR}		—	4	20	nS	*5
	Fall time	t_{FF}		—	4	20	nS	*5
	Rise/fall time matching	t_{RFM}		—	90	111.11	%	*5
	Output impedance	Z_{DRV}		—	28	44	Ω	Including Rs = 27 Ω
Input capacitance	Transceiver edge rate control capacitance	C_{EDGE}		—	—	75	pF	*6
Series resistance		R_S		—	25	30	Ω	Recommended value:27 Ω

*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 [V], V_{IH} (Min) = 2.0 [V] (TTL input standard).
There are some hystereses to lower noise sensitivity.

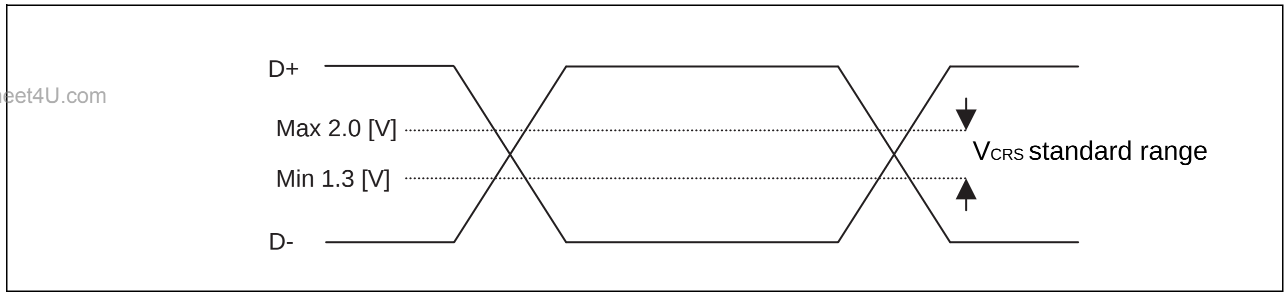
(Continued)

*2 : Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 [mV] of differential input sensitivity when the differential data input is within 0.8 [V] to 2.5 [V] to the local ground reference level.
Above voltage range is the common mode input voltage range.

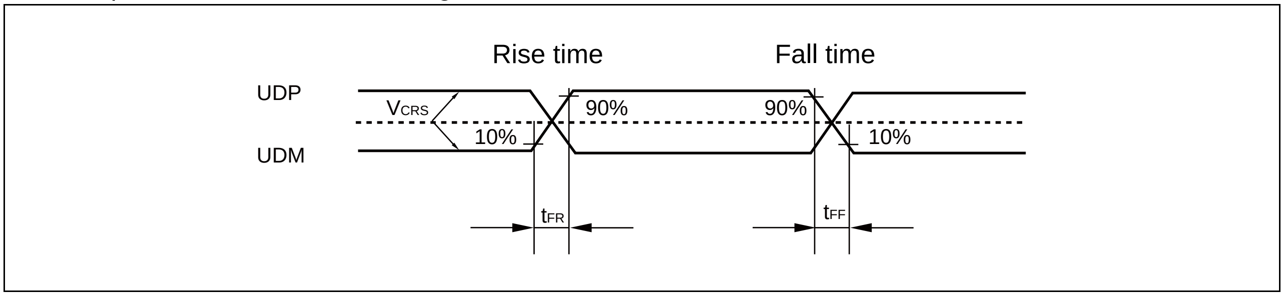


*3 : The output drive capability of the driver is below 0.3 [V] at Low-State (V_{OL}) (to 3.6 [V] and 1.5 kΩ load), and 2.8 [V] or above (to the V_{SS} and 1.5 kΩ load) at High-State (V_{OH}).

*4 : The cross voltage of the external differential output signal (D + /D –) of USB I/O buffer is within 1.3 [V] to 2.0 [V].



*5 : Regarding t_{FR} ,t_{FF}, t_{RFM}
They indicate rise time (Trise) and fall time (Tfall) of the differential data signal.
They are defined by the time between 10% to 90% of the output signal voltage.
For full-speed buffer, t_{FR}/t_{FF} ratio is regulated as within ±10% to minimize RFI emission.



(Continued)

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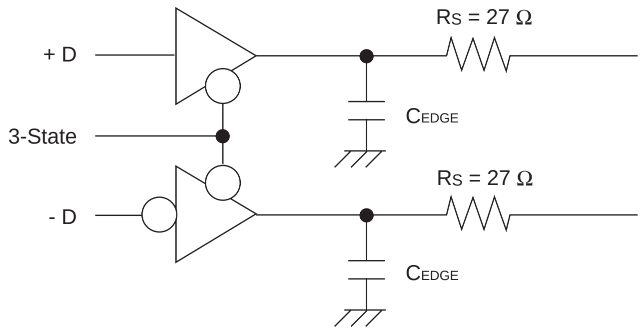
*6 : The place to connect transceiver edge rate control capacitance C_{EDGE}
For this USB I/O, it is recommended to use C_{EDGE} control capacitor.
For USB Max standard as 75 pF, please control the edge characteristic of output waveform by connecting 30 [pF] to 50 [pF] (recommended value : 47 [pF] ≒ 50[pF]) to D + and D – lines when implementing on the board.



Driver output impedance 3 Ω to 19 Ω
Rs serial resistance value 25 Ω to 30 Ω
Please apply 27 Ω of serial resistance value as a recommended value.

8. Flash Memory Write/Erase Characteristics

(V_{CC} = 3.3 V, Ta = + 25 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.9	3.6	s	Excludes write time prior to internal erase
Half word (16bits) write time	—	23	370	µs	Not including system-level overhead time.
Chip erase time*1	—	10.8	43.2	s	Excludes write time prior to internal erase
Erase/write cycles	10000	—	—	cycle	Average Ta ≤ + 85 °C
Flash memory data hold time	10*2	—	—	year	Average Ta ≤ + 85 °C

*1 : The chip erase time is the sector erase time multiplied across all sectors.

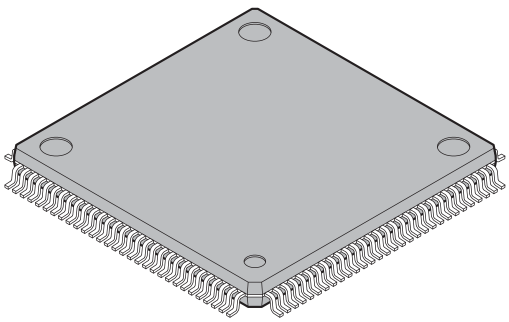
*2 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

■ ORDERING INFORMATION

Part number	Package
MB91F610APMC	120-pin plastic LQFP (FPT-120P-M21)
MB91613PMC	

■ PACKAGE DIMENSION

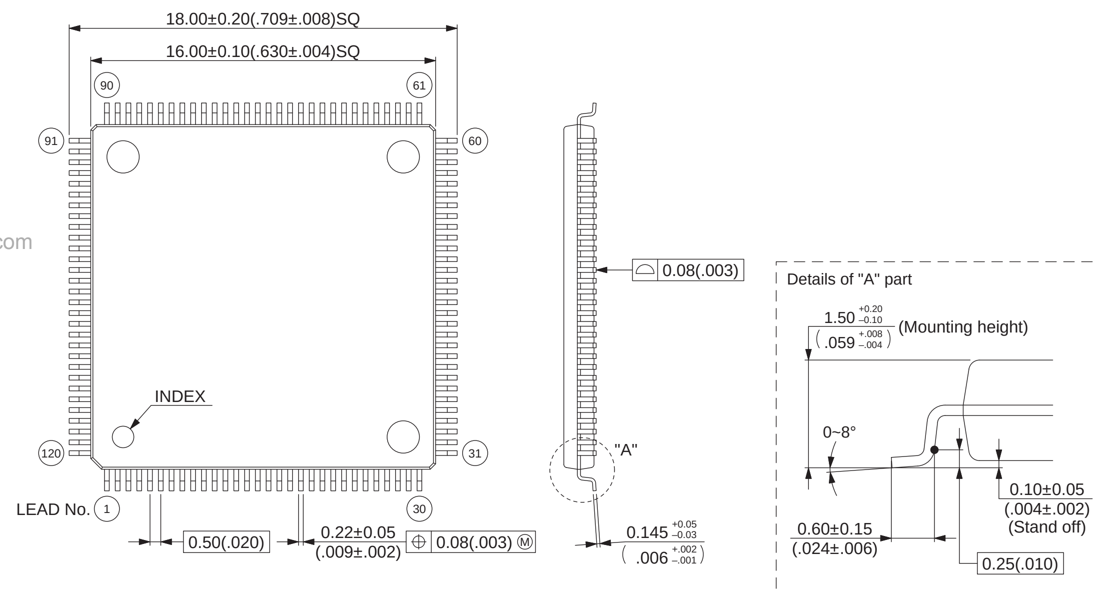
120-pin plastic LQFP



(FPT-120P-M21)

Lead pitch	0.50 mm
Package width × package length	16.0 × 16.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.88 g

120-pin plastic LQFP
(FPT-120P-M21)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Changed the part number. (MB91F610 → MB91F610A) Added “MB91613” to the part number. Changed the terms. (USB function with Mini-HOST → USB function/ HOST) (Mini-HOST → HOST)
4	■ FEATURES	Changed the explanation of “• USB HOST”. (• Support of bulk and interrupt transfer (Only using endpoint1 and endpoint2) → • Support control transfer, bulk transfer, interrupt transfer, and isochronous transfer)
7	■ PIN ASSIGNMENT	Added the note *.
11	■ PIN DESCRIPTION	Changed “I/O circuit type” of the pins number 69, 70 and 71. (L → F, L)
12		Changed “Function” of the pin number 83 to 88, and 92 to 95. (Added “N.C. pin for MASK products.”.)
21	■ I/O CIRCUIT TYPE	Changed “Remarks” of the Type L. (Added “• Flash memory product only”.)
27	■ HANDLING DEVICES	Added “• OSDC output pin”.
31	■ MEMORY SPACE 2.Memory map	Corrected the table. (Flash/ROM → FLASH) (Added 000F 8000_H)
39	■ I/O MAP	Corrected “Initial value after reset”. (FSTR:-------0 → -------1)
43		Corrected “Block” for the line, 0000 0498_H to 0000 $049C_H$. (Changed to “Reserved”.)
64	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed the notation of “Rating Max” for “Input voltage”. (V_{SS} + 4.0 → V_{CC} + 0.3 (≤ 4.0)) Corrected “Remarks” for “Input voltage”. (5 V tolerant*7 → 5 V tolerant) (USB I/O*7 → USB I/O) Changed from “Power consumption” to “Power consumption (Flash product)”. Added “Power consumption (MASK product)”.
65		Corrected the description of *8. (Deleted “ • Note that if the ＋B signal is input at power-on, since the power is supplied through the pin, the power supply voltage may become the voltage at which a power-on reset does not work.”.)

(Continued)

Page	Section	Change Results
67	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) DC Characteristics	Changed from “Power supply current” to “Power supply current (Flash product)”. Changed “Value” for I_{CCO}. (Typ : 150 $\rightarrow$ 100 and 130 $\rightarrow$ 105) (Max : 180 $\rightarrow$ 130)
68		Added “Power supply current (MASK product)”.
69		Added PK0, PK1, $\overline{\text{INIT}}$, MD0, and MD1 to “Pin name" for ““H” level input voltage (hysteresis input)”, and ““L” level input voltage (hysteresis input)”. Added PK0 and PK1 to “Pin name” for ““H” level output voltage”, and ““L” level output voltage”.
71	4. AC Characteristics (1) Main Clock (MCLK) Input Standard	Added the sentence, “When crystal oscillator is connected” to “Remarks” for “Input frequency”. Added the sentence, “When using external clock” to “Remarks” for “Input clock cycle”, and “Input clock pulse width”.
72		Corrected “ • Operating guaranteed range (Not using USB)”. (Changed from “ • Operating guaranteed range” to “ • Operating guaranteed range (Not using USB)”.)
73		Corrected “ • Operating guaranteed range (at using USB)”. (Added *1 to *4 to each value.) (Changed from “VMS” to “PMS” for “ • When the PLL clock is selected”.) (Added the note at the bottom of the page.)
74	(2) Sub Clock (SBCLK) Input Standard	Added the column, “Remarks”. Divided the line, “Input frequency” into two lines, “When crystal oscillator is connected”, and “When using external clock”. Added “Input clock pulse width”, and “Input clock rise time and fall time”. Corrected the table. (Added “< When external clock input>”.) (Deleted “X1” and “X1A”.)
75	(3) Conditions of PLL	Changed from “(3) PLL Oscillation Stabilization Wait Time (LOCK UP Time)” to “(3) Conditions of PLL”. Added the column, “Typ” below “Value”. Added “PLL input clock frequency”, “PLL multiple rate”, and “PLL macro oscillation clock frequency”.
	(5) Reset Input Standards	Added “Reset input rise time and fall time”. Added “V_{IHS}, t_{INITXF}, t_{INITXR}” to the table.
89, 90	5. Electrical Characteristics for the A/D Converter	Added “Compare time”. Corrected the note, *1. (compare time: 0.73 µs $\rightarrow$ compare time: 0.72 µs) Added the note *3.
91, 92		Corrected “ • Definition of 10-bit A/D Converter Terms”. (1LSB $\rightarrow$ 1LSB')

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Page	Section	Change Results
93	■ ELECTRICAL CHARACTERISTICS 6. Electrical Characteristics for the Analog RGB D/A Converter	Corrected “Resolution”. Deleted the description with * at the lower part of the table.
95	7. USB Characteristics	Corrected the note, *3. (Added “at High-State (V_{OH})”.)
98	■ ORDERING INFORMATION	Changed the part number. (MB91F610PMC → MB91F610APMC) Added “MB91613PMC” to the part number.

The vertical lines marked in the left side of the page show the changes.

MEMO

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