BB504C

Build in Biasing Circuit MOS FET IC
VHF&UHF RF Amplifier

HITACHI

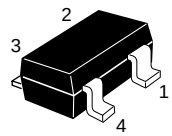
ADE-208-983D (Z)
5th. Edition
Dec. 2000

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise; NF = 1.0 dB typ. at f = 200 MHz,NF =1.75 dB typ. at f =900 MHz
- High gain; PG = 30 dB typ. at f = 200 MHz, PG = 22 dB typ. at f = 900 MHz
- Withstanding to ESD;
  Build in ESD absorbing diode. Withstand up to 200 V at C = 200 pF, Rs = 0 conditions.
- Provide mini mold packages; CMPAK-4 (SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Notes: 1. Marking is “DS–”.
2. BB504C is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

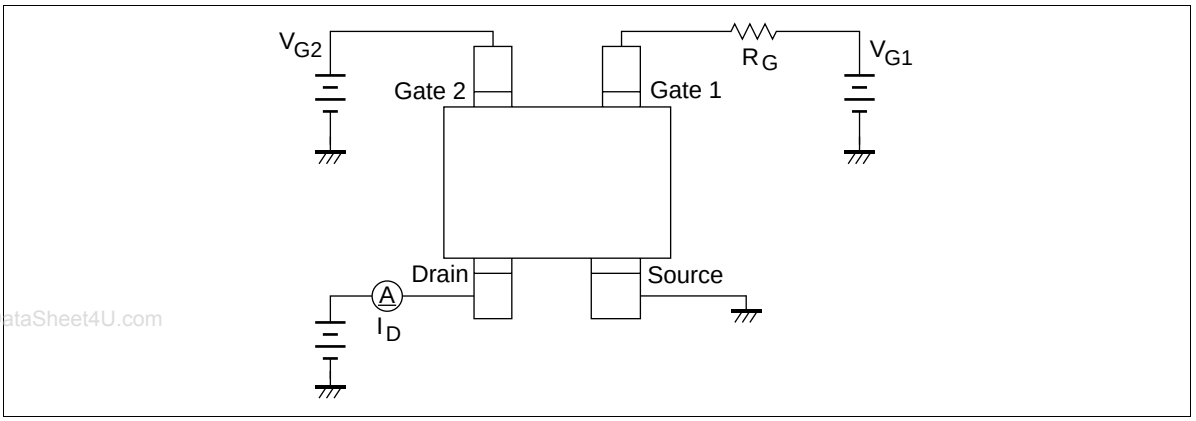
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 –0	V
Gate2 to source voltage	V_{G2S}	+6 –0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

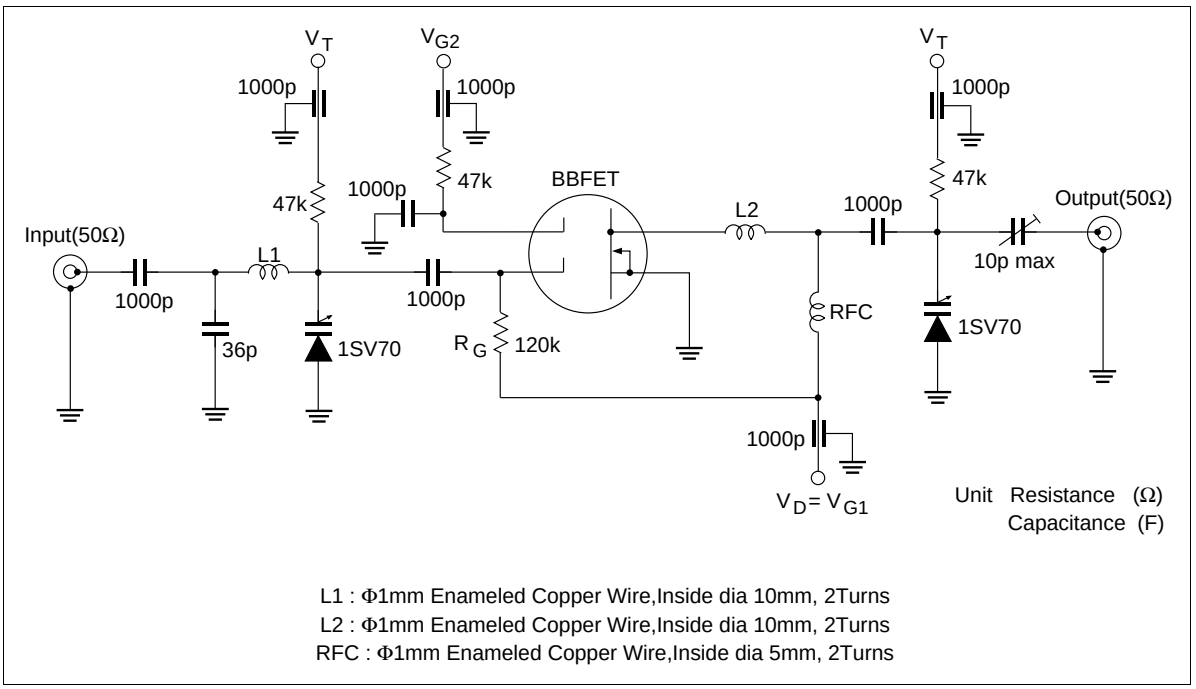
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.6	0.85	1.1	V	V_{DS} = 5V, V_{G2S} = 4V, I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.6	0.85	1.1	V	V_{DS} = 5V, V_{G1S} = 5V, I_D = 100µA
Drain current	$I_{D(op)}$	13	16	19	mA	V_{DS} = 5V, V_{G1} = 5V V_{G2S} = 4V, R_G = 120kΩ
Forward transfer admittance	$\|y_{fs}\|$	24	29	34	mS	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} =4V R_G = 120kΩ, f = 1kHz
Input capacitance	c_{iss}	1.7	2.1	2.5	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	1.0	1.4	1.8	pF	V_{G2S} =4V, R_G = 120kΩ
Reverse transfer capacitance	c_{rss}	—	0.027	0.05	pF	f = 1MHz
Power gain (1)	PG	25	30	—	dB	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V, R_G = 120kΩ
Noise figure (1)	NF	—	1.0	1.8	dB	f = 200MHz
Power gain (2)	PG	17	22	—	dB	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V, R_G = 120kΩ
Noise figure (2)	NF	—	1.75	2.3	dB	f = 900MHz

Test Circuits

- **DC Biasing Circuit for Operating Characteristics Items** ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)

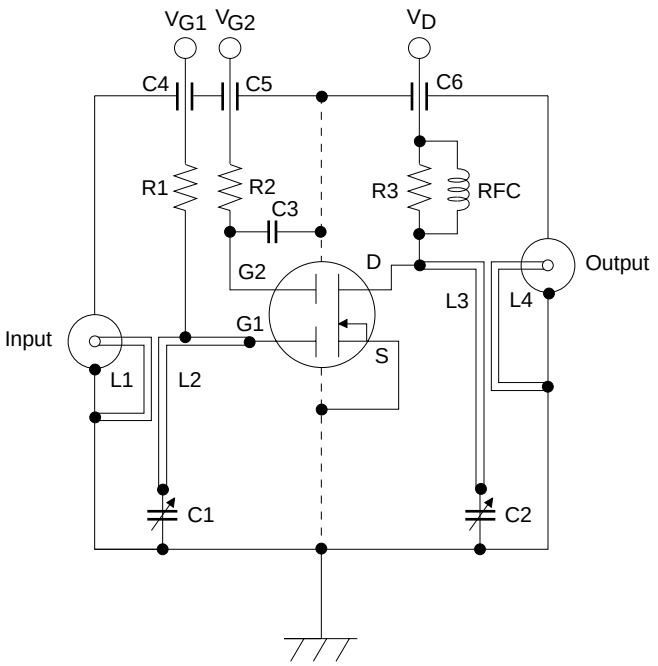


- **200MHz Power Gain, Noise Figure Test Circuit**



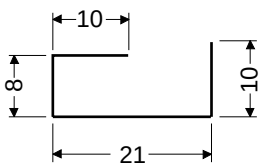
L1 : Φ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
L2 : Φ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
RFC : Φ1mm Enameled Copper Wire,Inside dia 5mm, 2Turns

- **900 MHz Power Gain, Noise Figure Test Circuit**

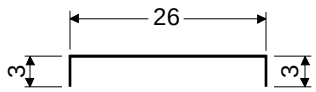


C1, C2 : Variable Capacitor (10pF MAX)
C3 : Disk Capacitor (1000pF)
C4 to C6 : Air Capacitor (1000pF)
R1 : 120 kΩ
R2 : 47 kΩ
R3 : 4.7 kΩ

L1:

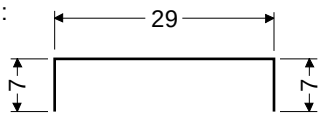


L2:

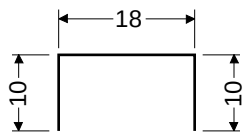


(Φ1mm Copper wire)
Unit:mm

L3:

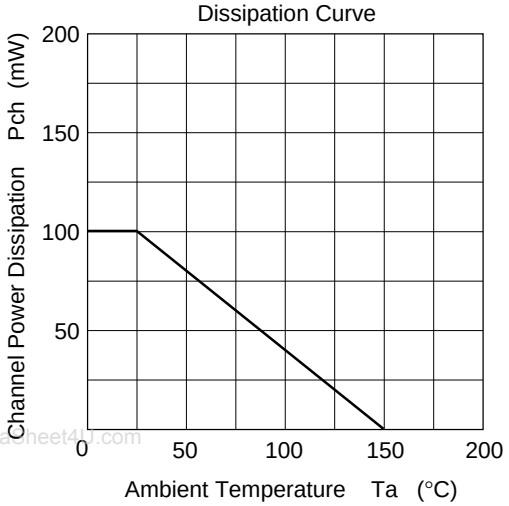


L4:

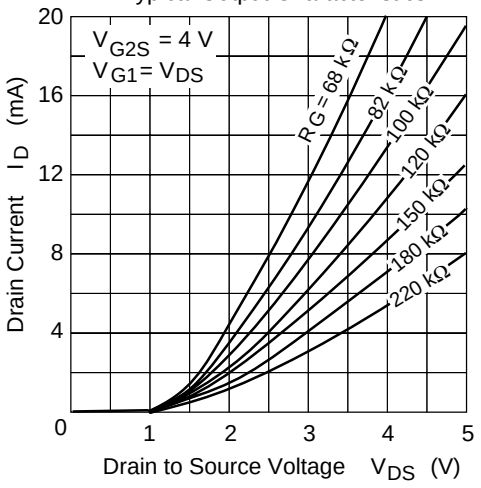


RFC : Φ1mm Copper wire with enamel 4turns inside dia 6mm

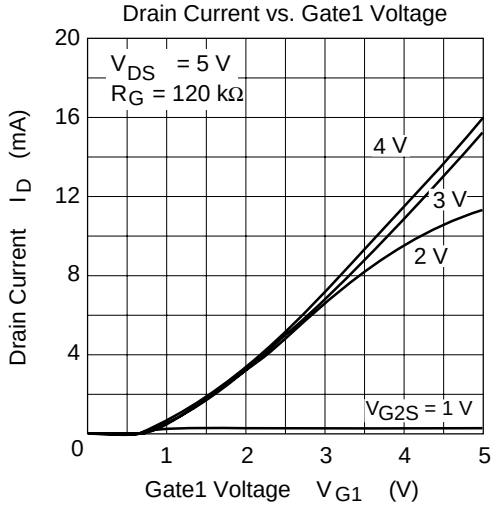
Maximum Channel Power Dissipation Curve



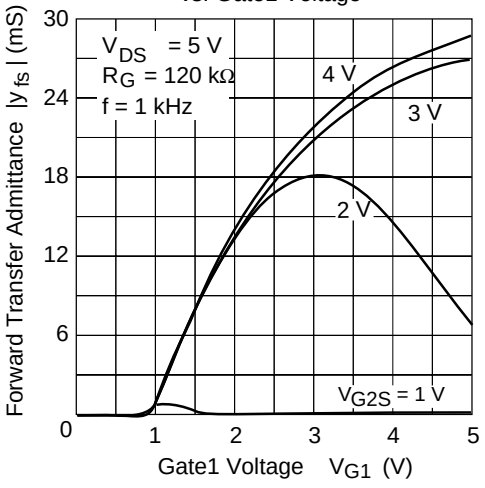
Typical Output Characteristics



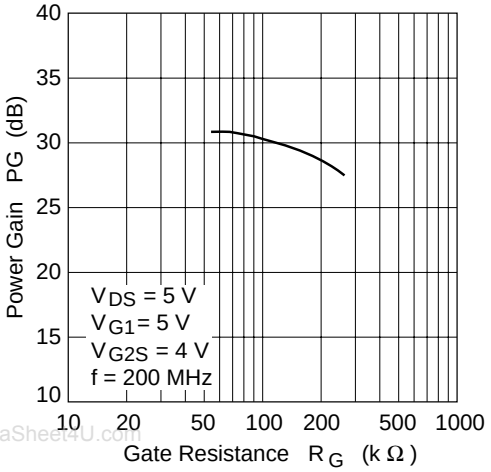
Drain Current vs. Gate1 Voltage



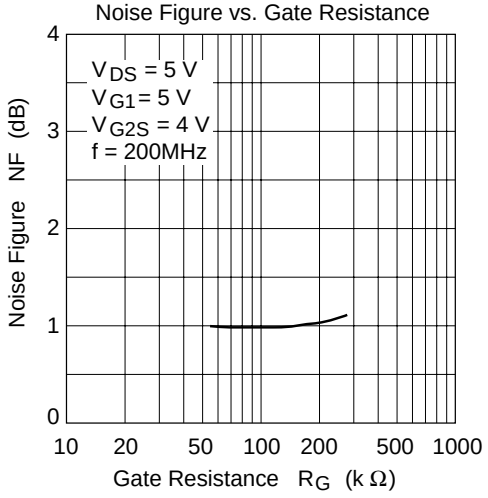
Forward Transfer Admittance vs. Gate1 Voltage



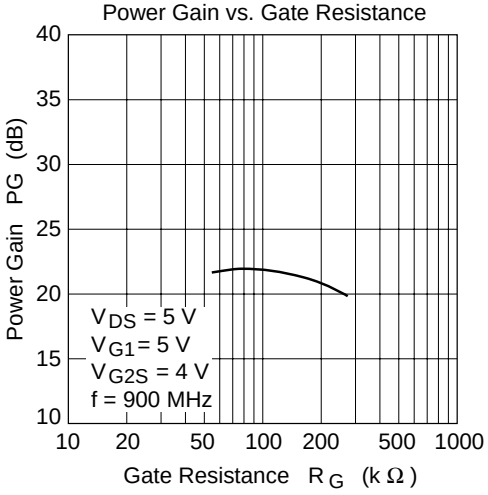
Power Gain vs. Gate Resistance



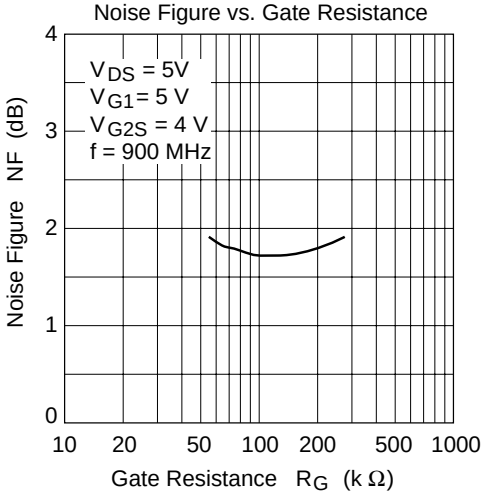
Noise Figure vs. Gate Resistance



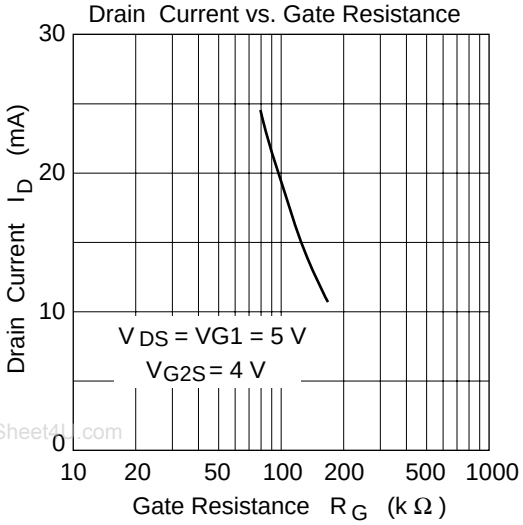
Power Gain vs. Gate Resistance



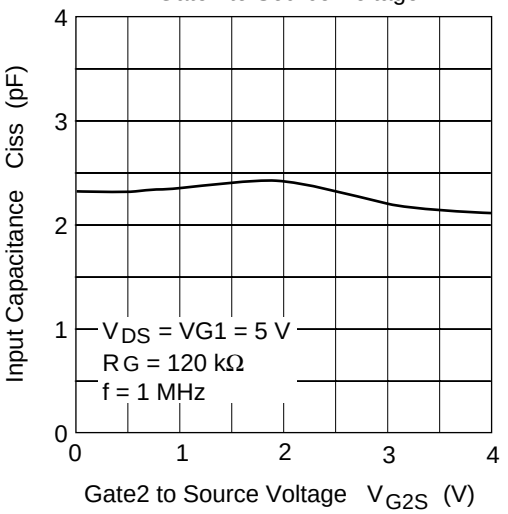
Noise Figure vs. Gate Resistance



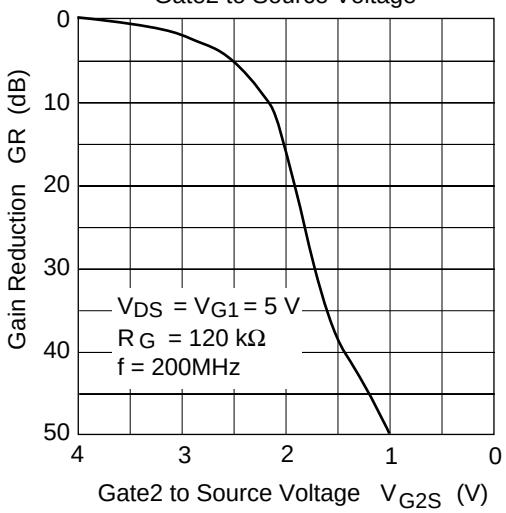
Drain Current vs. Gate Resistance



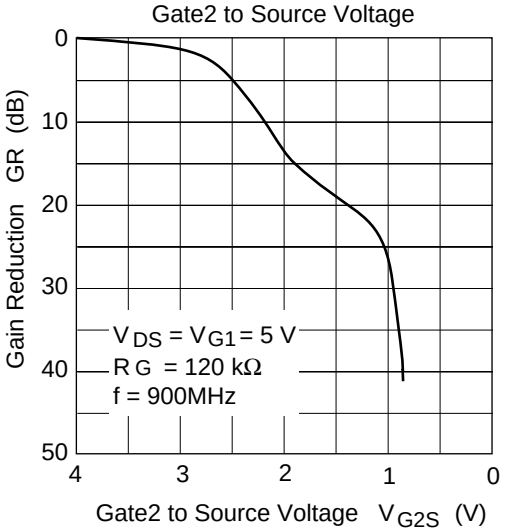
Input Capacitance vs.
Gate2 to Source Voltage



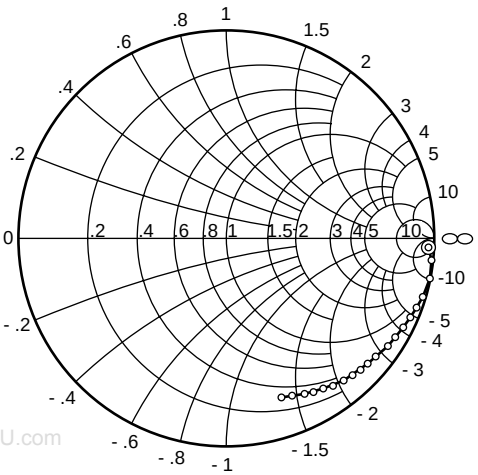
Gain Reduction vs.
Gate2 to Source Voltage



Gain Reduction vs.
Gate2 to Source Voltage



S11 Parameter vs. Frequency

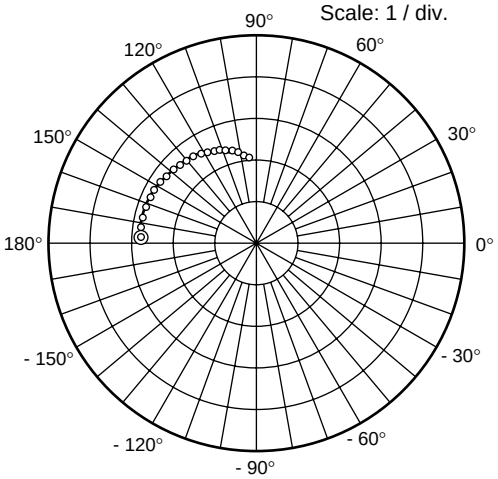


Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 120 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S21 Parameter vs. Frequency

Scale: 1 / div.

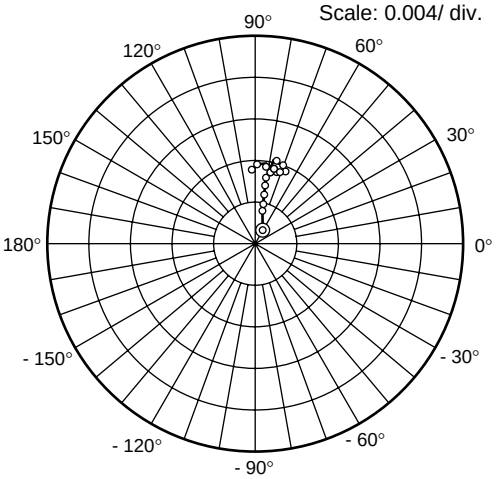


Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 120 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S12 Parameter vs. Frequency

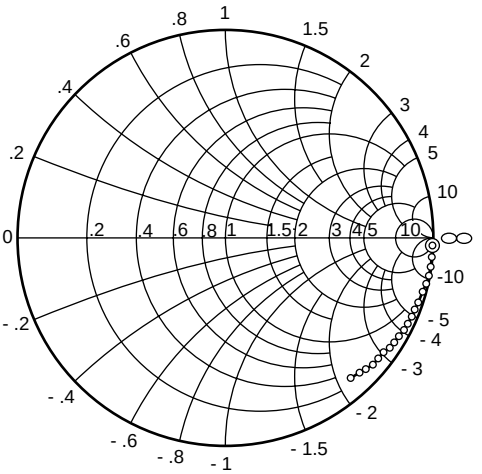
Scale: 0.004/ div.



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 120 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 120 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

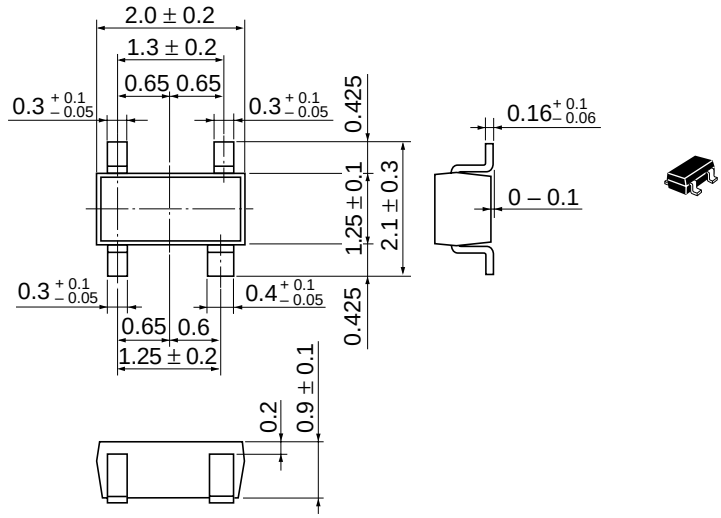
Sparameter (V_{DS} = V_{G1} = 5V, V_{G2S} = 4V, R_G = 120kΩ, Zo = 50Ω)

	S11		S21		S12		S22	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	1.000	-3.3	2.80	175.9	0.00106	58.8	0.990	-2.4
100	0.993	-7.2	2.78	170.9	0.00171	75.7	0.992	-4.7
150	0.991	-10.9	2.77	166.1	0.00253	75.1	0.991	-7.2
200	0.984	-15.0	2.74	161.2	0.00356	77.4	0.987	-9.6
250	0.978	-19.0	2.72	156.5	0.00442	78.2	0.985	-12.2
300	0.970	-22.8	2.68	151.8	0.00485	80.0	0.982	-14.7
350	0.958	-26.7	2.64	147.2	0.00576	74.7	0.978	-17.1
400	0.954	-30.3	2.60	142.7	0.00642	71.7	0.973	-19.6
450	0.945	-33.8	2.56	138.6	0.00689	73.3	0.968	-22.0
500	0.932	-37.5	2.50	134.1	0.00712	71.8	0.963	-24.2
550	0.920	-40.6	2.46	129.8	0.00765	70.7	0.958	-26.7
600	0.910	-44.3	2.41	125.7	0.00804	69.9	0.952	-28.9
650	0.900	-47.5	2.37	121.6	0.00798	69.1	0.947	-31.3
700	0.887	-50.9	2.31	117.8	0.00787	67.8	0.942	-33.4
750	0.870	-54.4	2.27	113.6	0.00785	70.8	0.936	-35.8
800	0.863	-57.6	2.22	110.0	0.00758	73.3	0.929	-37.9
850	0.853	-60.9	2.18	105.8	0.00721	75.2	0.924	-40.3
900	0.839	-63.6	2.12	102.2	0.00694	75.8	0.917	-42.5
950	0.827	-66.5	2.07	98.6	0.00716	88.1	0.912	-44.5
1000	0.819	-70.1	2.04	94.9	0.00667	92.7	0.906	-46.7

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	CMPAK-4(T)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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Colophon 2.0