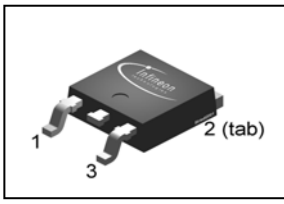
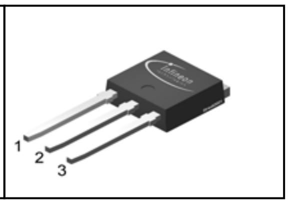
# *OptiMOS*®2 Power-Transistor

### Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC[1] for target applications
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 175 °C operating temperature
- d*v*/d*t* rated

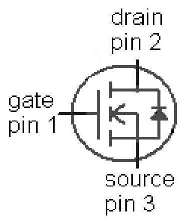
**Product Summary**

| | | |
|---|---|---|
| $V_{DS}$ | 25 | V |
| $R_{DS(on),max}$ (SMD version) | 13 | mΩ |
| $I_D$ | 30 | A |

| P-TO252-3-11 | P-TO251-3-21 |
|---|---|
|  |  |








| Type | Package | Ordering Code | Marking |
|---|---|---|---|
| IPD13N03LA | P-TO252-3-11 | Q67042-S4159 | 13N03LA |
| IPU13N03LA | P-TO251-3-21 | Q67042-S4160 | 13N03LA |

**Maximum ratings,** at $T_j$=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous drain current | $I_D$ | $T_C$=25 °C[2] | 30 | A |
| | | $T_C$=100 °C | 30 | |
| Pulsed drain current | $I_{D,pulse}$ | $T_C$=25 °C[3] | 210 | |
| Avalanche energy, single pulse | $E_{AS}$ | $I_D$=24 A, $R_{GS}$=25 Ω | 60 | mJ |
| Reverse diode d*v*/d*t* | d*v*/d*t* | $I_D$=30 A, $V_{DS}$=20 V, d*i*/d*t*=200 A/µs, $T_{j,max}$=175 °C | 6 | kV/µs |
| Gate source voltage[4] | $V_{GS}$ | | ±20 | V |
| Power dissipation | $P_{tot}$ | $T_C$=25 °C | 46 | W |
| Operating and storage temperature | $T_j$, $T_{stg}$ | | -55 ... 175 | °C |
| IEC climatic category; DIN IEC 68-1 | | | 55/175/56 | |

[1] J-STD20 and JESD22

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Thermal characteristics** | | | | | | |
| Thermal resistance, junction - case | $R_{thJC}$ | | - | - | 3.2 | K/W |
| SMD version, device on PCB | $R_{thJA}$ | minimal footprint | - | - | 75 | |
| | | 6 $cm^2$ cooling area[5)] | - | - | 50 | |

**Electrical characteristics,** at $T_j$=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | min. | typ. | max. | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}$=0 V, $I_D$=1 mA | 25 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=20 µA | 1.2 | 1.6 | 2 | |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$=25 V, $V_{GS}$=0 V, $T_j$=25 °C | - | 0.1 | 1 | µA |
| | | $V_{DS}$=25 V, $V_{GS}$=0 V, $T_j$=125 °C | - | 10 | 100 | |
| Gate-source leakage current | $I_{GSS}$ | $V_{GS}$=20 V, $V_{DS}$=0 V | - | 10 | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$=4.5 V, $I_D$=20 A | - | 17.5 | 21.9 | mΩ |
| | | $V_{GS}$=4.5 V, $I_D$=20 A, SMD version | - | 17.7 | 22.1 | |
| | | $V_{GS}$=10 V, $I_D$=30 A | - | 10.8 | 13.0 | |
| | | $V_{GS}$=10 V, $I_D$=30 A, SMD version | - | 10.7 | 12.8 | |
| Gate resistance | $R_G$ | | - | 0.9 | - | Ω |
| Transconductance | $g_{fs}$ | $\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, $I_D$=30 A | 18 | 36 | - | S |

2) Current is limited by bondwire; with an $R_{thJC}$=3.2 K/W the chip is able to carry 47 A.

3) See figure 3

4) $T_{j,max}$=150 °C and duty cycle $D$<0.25 for $V_{GS}$<-5 V

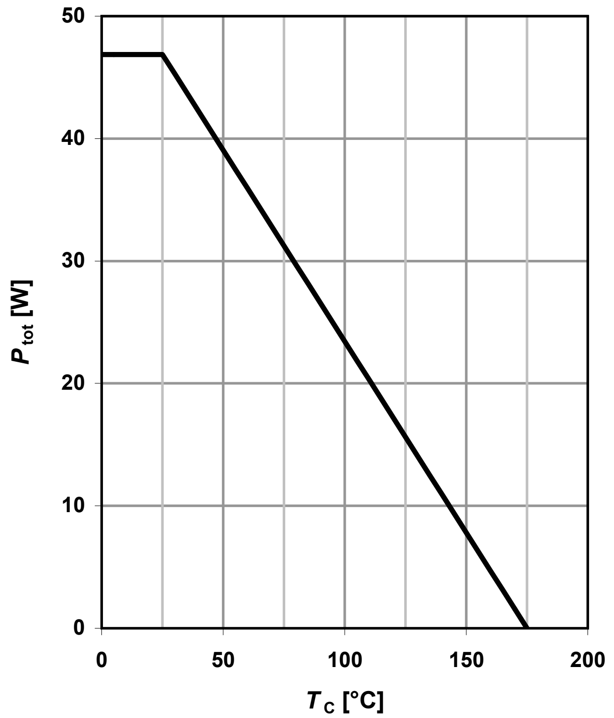
5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 $cm^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Dynamic characteristics** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0 V, $V_{DS}$=15 V, $f$=1 MHz | - | 784 | 1043 | pF |
| Output capacitance | $C_{oss}$ | | - | 303 | 402 | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 41 | 62 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=15 V, $V_{GS}$=10 V, $I_D$=15 A, $R_G$=2.7 Ω | - | 5.4 | 8 | ns |
| Rise time | $t_r$ | | - | 4.6 | 7 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 15 | 23 | |
| Fall time | $t_f$ | | - | 2.6 | 3.9 | |
| Gate Charge Characteristics[6)] | | | | | | |
| Gate to source charge | $Q_{gs}$ | $V_{DD}$=15 V, $I_D$=15 A, $V_{GS}$=0 to 5 V | - | 3 | 4 | nC |
| Gate charge at threshold | $Q_{g(th)}$ | | - | 1.3 | 1.7 | |
| Gate to drain charge | $Q_{gd}$ | | - | 1.8 | 2.7 | |
| Switching charge | $Q_{sw}$ | | - | 3 | 5 | |
| Gate charge total | $Q_g$ | | - | 6 | 8 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 3.4 | - | V |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | $V_{DS}$=0.1 V, $V_{GS}$=0 to 5 V | - | 6 | 7 | nC |
| Output charge | $Q_{oss}$ | $V_{DD}$=15 V, $V_{GS}$=0 V | - | 7 | 9 | |
| **Reverse Diode** | | | | | | |
| Diode continous forward current | $I_S$ | $T_C$=25 °C | - | - | 30 | A |
| Diode pulse current | $I_{S,pulse}$ | | - | - | 210 | |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$=0 V, $I_F$=30 A, $T_j$=25 °C | - | 0.95 | 1.2 | V |
| Reverse recovery charge | $Q_{rr}$ | $V_R$=15 V, $I_F$=$I_S$, $di_F/dt$=400 A/µs | - | - | 10 | nC |

6) See figure 16 for gate charge parameter definition

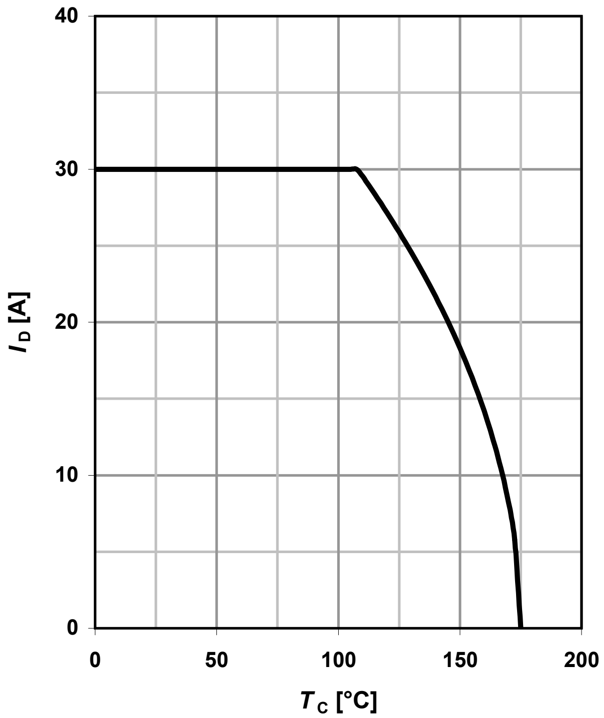
**1 Power dissipation**

$P_{tot}$=f($T_C$)




**2 Drain current**

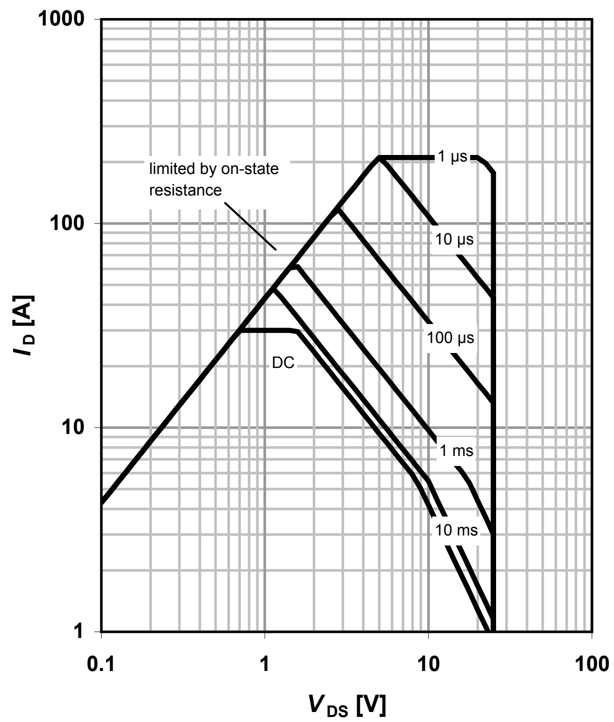
$I_D$=f($T_C$); $V_{GS}$≥10 V




**3 Safe operation area**

$I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0

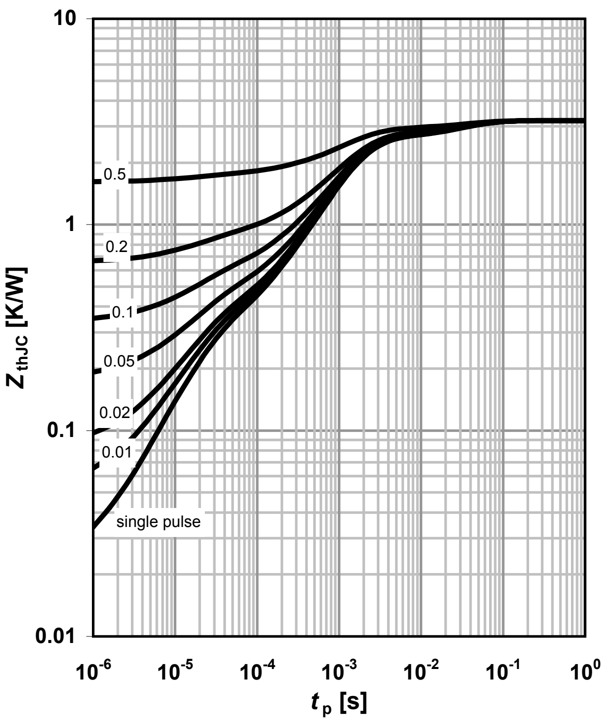
parameter: $t_p$




**4 Max. transient thermal impedance**

$Z_{thJC}$=f($t_p$)

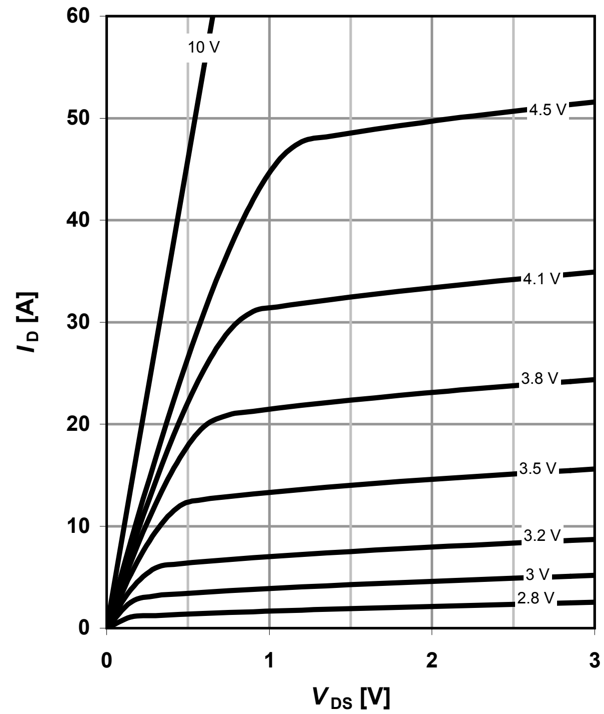
parameter: $D$=$t_p$/$T$



**5 Typ. output characteristics**

$I_D$=f($V_{DS}$); $T_j$=25 °C

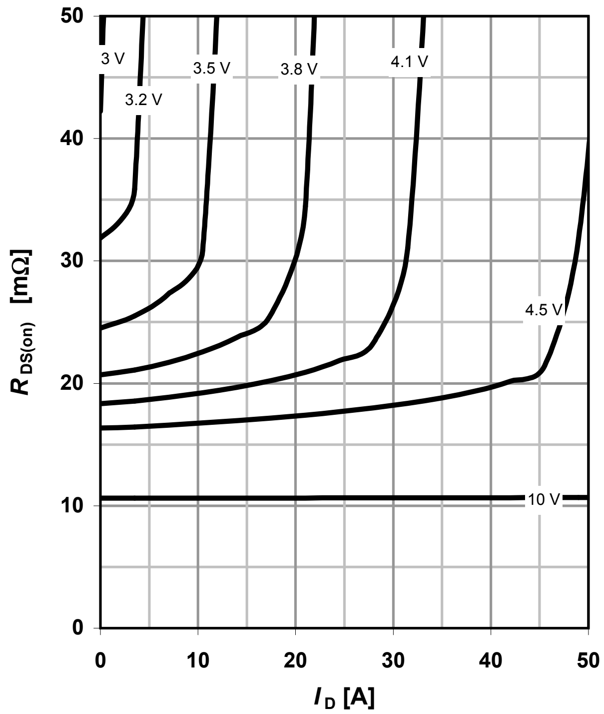
parameter: $V_{GS}$




**6 Typ. drain-source on resistance**

$R_{DS(on)}$=f($I_D$); $T_j$=25 °C

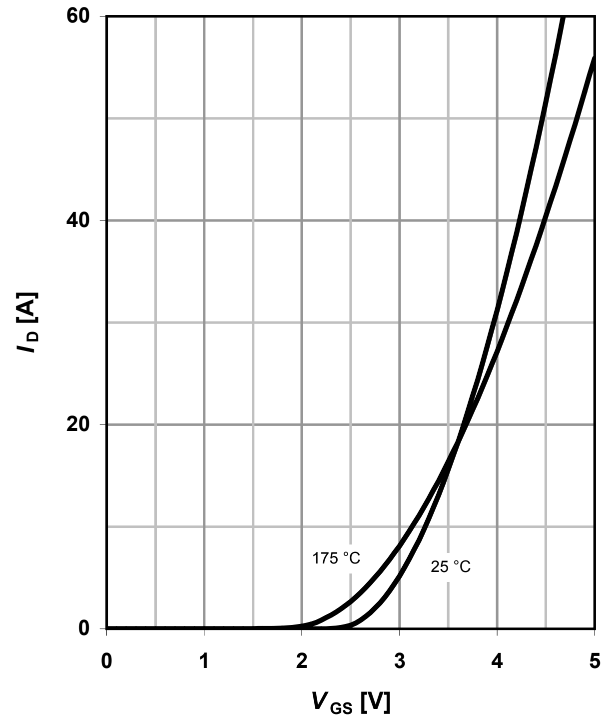
parameter: $V_{GS}$




**7 Typ. transfer characteristics**

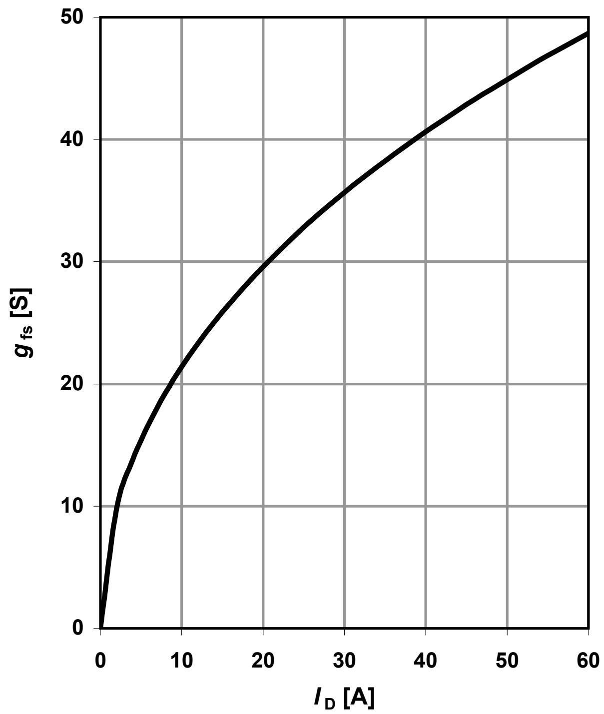
$I_D$=f($V_{GS}$); $|V_{DS}|$>2$|I_D|R_{DS(on)max}$

parameter: $T_j$



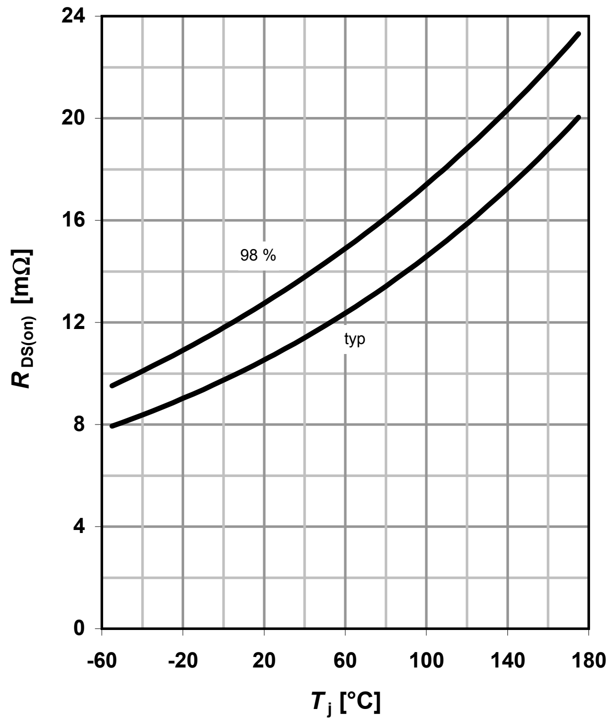

**8 Typ. forward transconductance**

$g_{fs}$=f($I_D$); $T_j$=25 °C



**9 Drain-source on-state resistance**

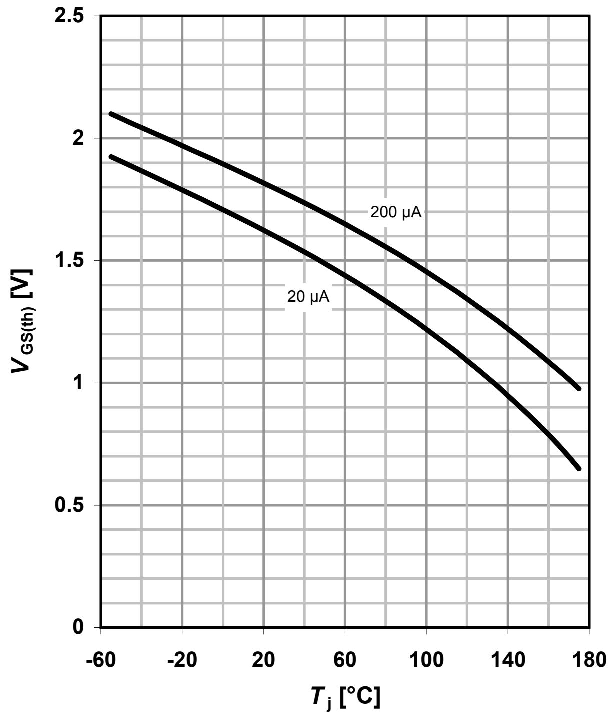
$R_{DS(on)}$=f($T_j$); $I_D$=30 A; $V_{GS}$=10 V




**10 Typ. gate threshold voltage**

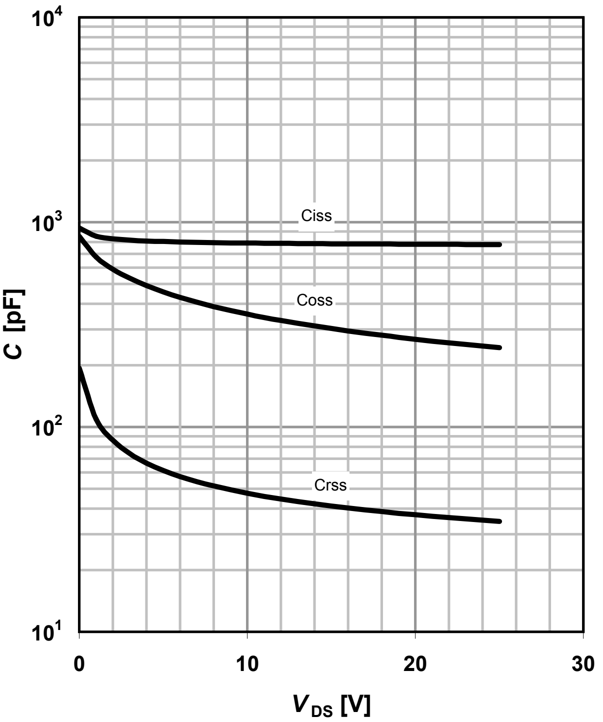
$V_{GS(th)}$=f($T_j$); $V_{GS}$=$V_{DS}$

parameter: $I_D$




**11 Typ. Capacitances**

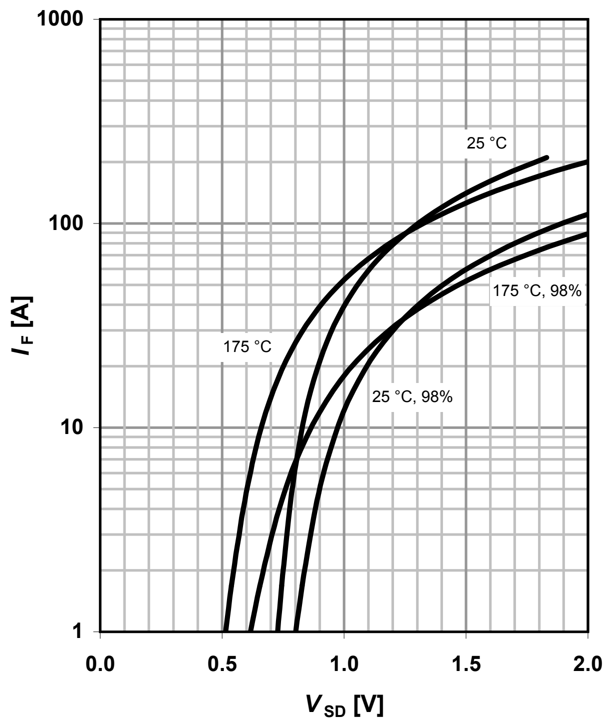
$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz




**12 Forward characteristics of reverse diode**

$I_F$=f($V_{SD}$)

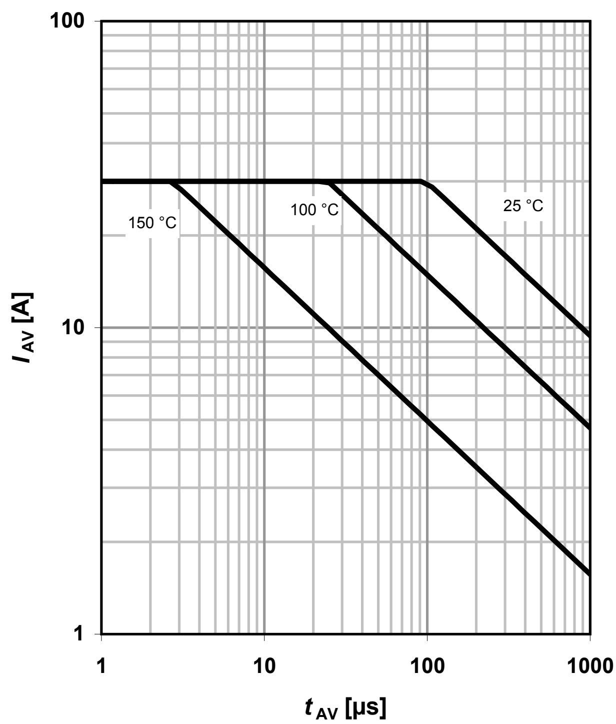
parameter: $T_j$



**13 Avalanche characteristics**

$I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω

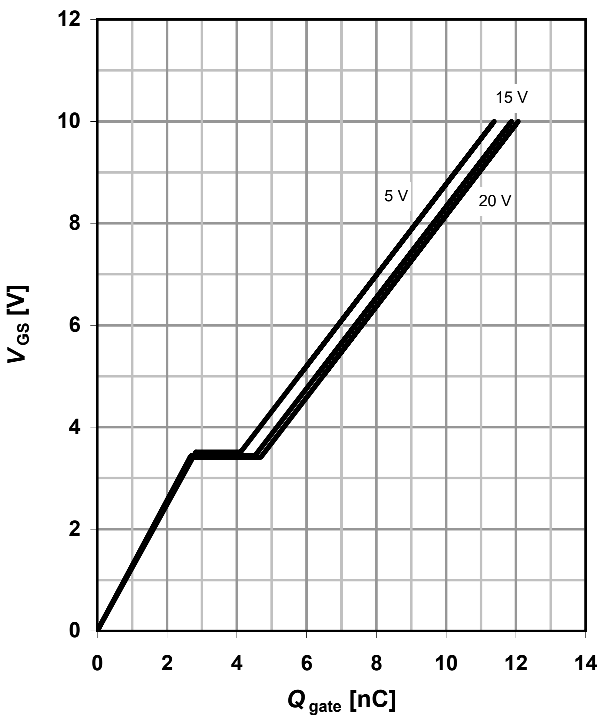
parameter: $T_{j(start)}$




**14 Typ. gate charge**

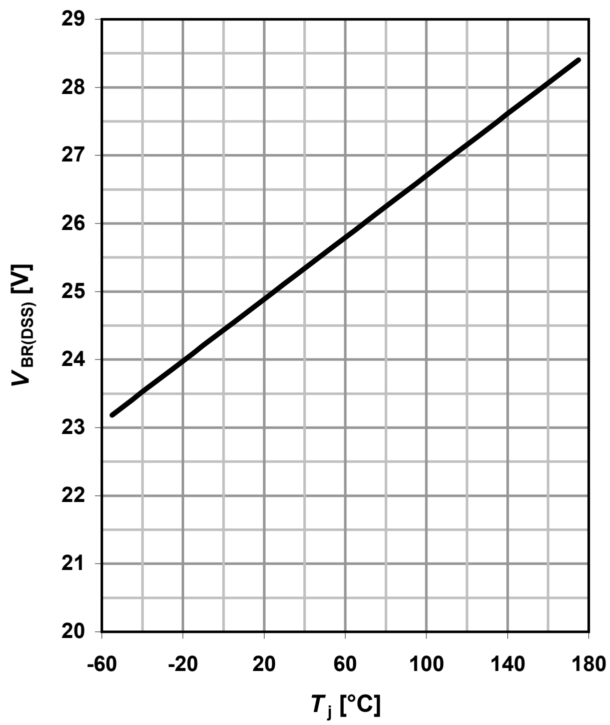
$V_{GS}$=f($Q_{gate}$); $I_D$=25 A pulsed

parameter: $V_{DD}$

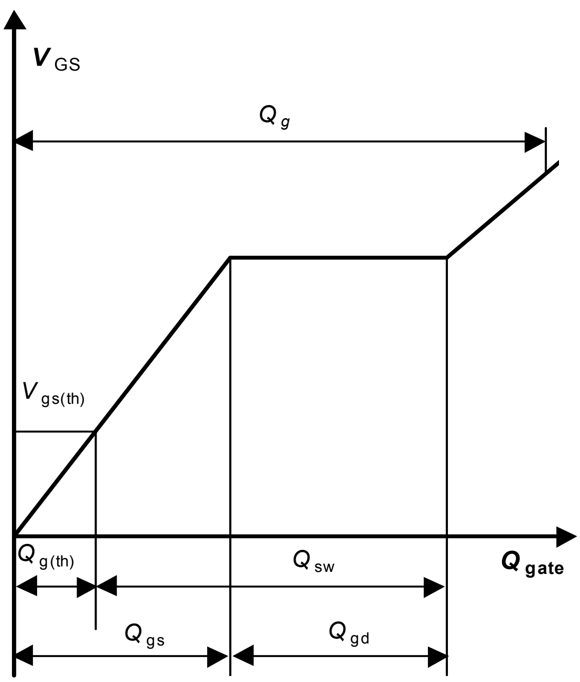



**15 Drain-source breakdown voltage**

$V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA

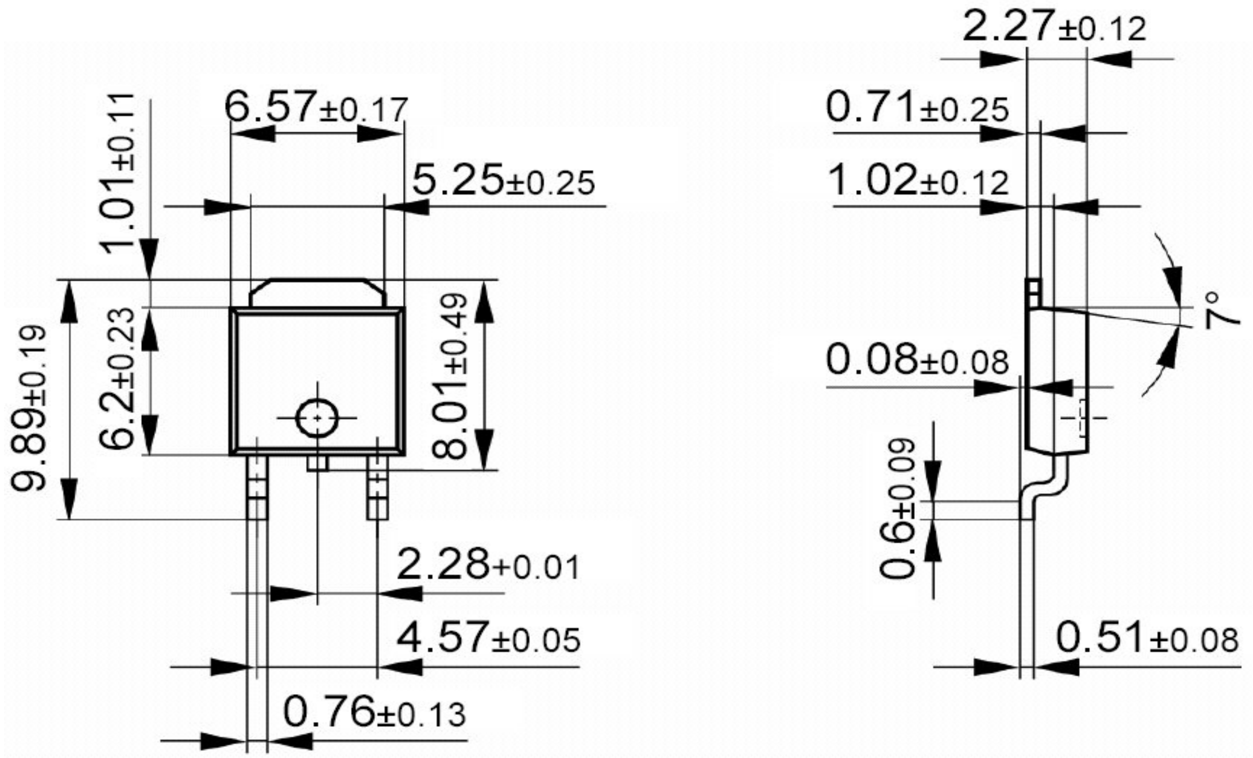



**16 Gate charge waveforms**

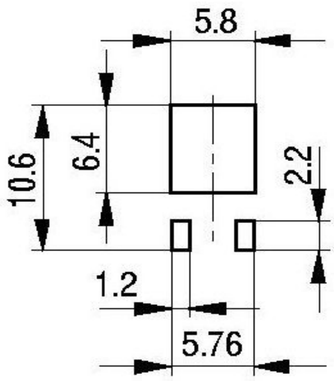


**Package Outline**

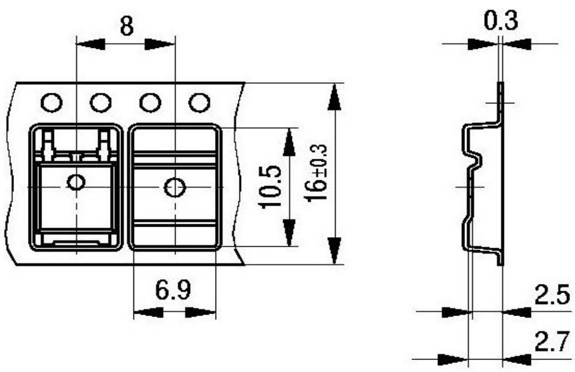
**P-TO252-3-11: Outline**




**Footprint:**



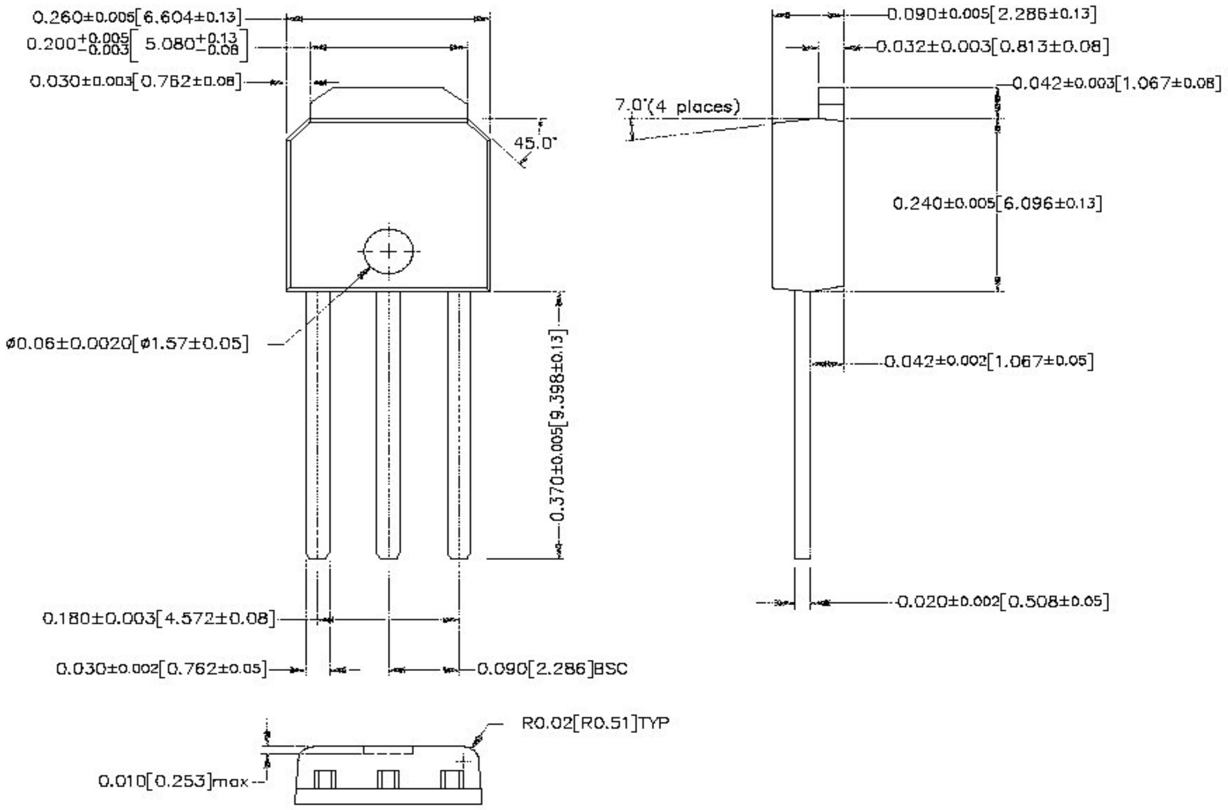

**Packaging:**




Dimensions in mm

**Package Outline**

**P-TO251-3-21: Outline**




Dimensions in inch [mm]

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