MCP8021/2

3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode, Op Amps

Features

- AEC-Q100 Grade 0 Qualified
- Supply Current:
  - Sleep mode: 5 µA Typical
  - Standby mode: <330 µA (MCP8021)
  - Standby mode, op amps off: <330 µA (MCP8022)
  - Standby mode, op amps on: <1300 µA (MCP8022)
- Three Half-Bridge Drivers Configured to Drive External High-Side NMOS and Low-Side NMOS MOSFETs:
  - Independent input control for high-side and low-side NMOS MOSFET gate drives
  - Typical peak output current: 0.5A @ 12V
  - Shoot-through protection
  - Overcurrent and short-circuit protection
- Fixed Output Linear Regulator:
  - 3.3V or 5.0V @ 70 mA
  - True current foldback
- Internal Band Gap Reference
- Three Operational Amplifiers (MCP8022)
- Dedicated WAKE Pin for Sleep Mode Recovery
- Dedicated $\overline{\text{FAULT}}$ Pin
- Single Wire UART Communications
- Supply Voltage Range: 4V-40V
- Operational Voltage Range: 6.25V-29V
- Gate Drive Undervoltage Lockout: 4.5V
- Supply Voltage Undervoltage Shutdown: 4.5V
- Supply Voltage Undervoltage Lockout (UVLO): 6.25V
- Overvoltage Lockout (OVLO): 29V
- Overvoltage Shutdown: 41V
- Transient (100 ms) Voltage Tolerance: 48V
- Extended Temperature Range (T_A): -40°C to +150°C
- Thermal Shutdown

Applications

- Automotive Fuel, Water, Ventilation Motors
- Home Appliances
- Permanent Magnet Synchronous Motor (PMSM) Control
- Hobby Aircraft, Boats, Vehicles

Description

The MCP8021/2 devices are 3-phase Brushless DC (BLDC) power modules containing three integrated half-bridge drivers, capable of driving three external NMOS/NMOS transistor pairs. The three half-bridge drivers are capable of delivering a peak output current of 0.5A at 12V for driving high-side and low-side NMOS MOSFET transistors. The drivers have shoot-through, overcurrent and short-circuit protection. A Sleep mode has been added to achieve a typical “key off” quiescent current of 5 µA.

The MCP8021/2 devices integrate a 3.3V or 5.0V LDO regulator for host and peripheral power, an overtemperature sensor and user-configurable functions.

The user-configurable functions are: dead time, blanking time, op amp enable/disable during standby, enable/disable Sleep mode, enable/disable overcurrent detection and enable/disable gate drive undervoltage protection.

The on-board 3.3V or 5.0V dropout voltage regulators are capable of delivering 70 mA of current. The voltage option is selected by part number.

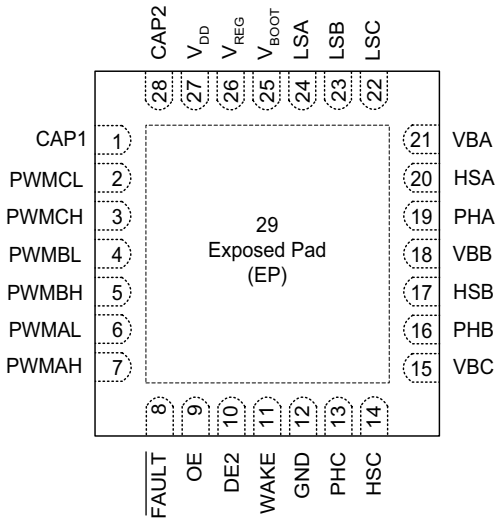
The MCP8022 device adds three independent operational amplifiers for general use.

The MCP8021/2 operation is specified over a temperature range of -40°C to +150°C.

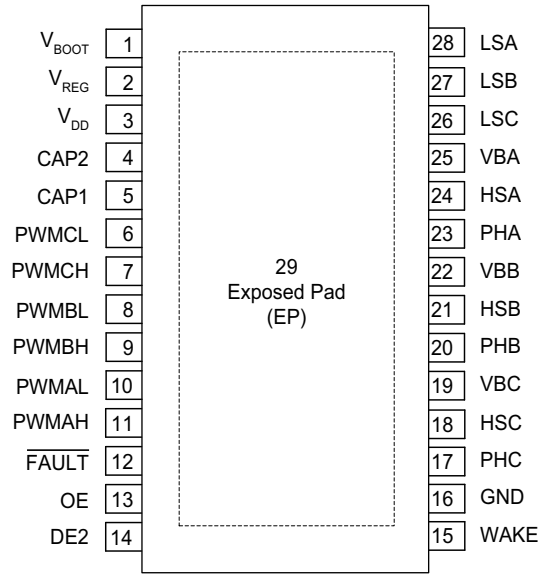
Package options for the MCP8021 include 28-lead 5x5 mm VQFN and 28-lead TSSOP-EP. Package options for the MCP8022 include 40-lead 5x5 mm VQFN and 38-lead TSSOP-EP.

Package Types – MCP8021

5 mm x 5 mm QFN-28*



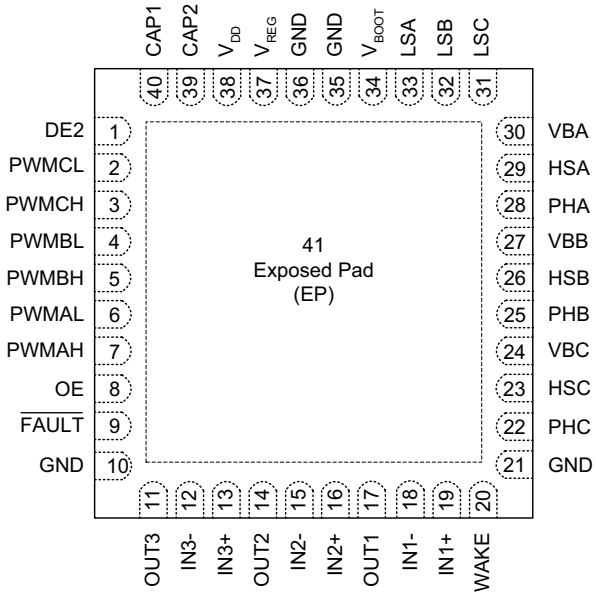
4.4 mm TSSOP-28*



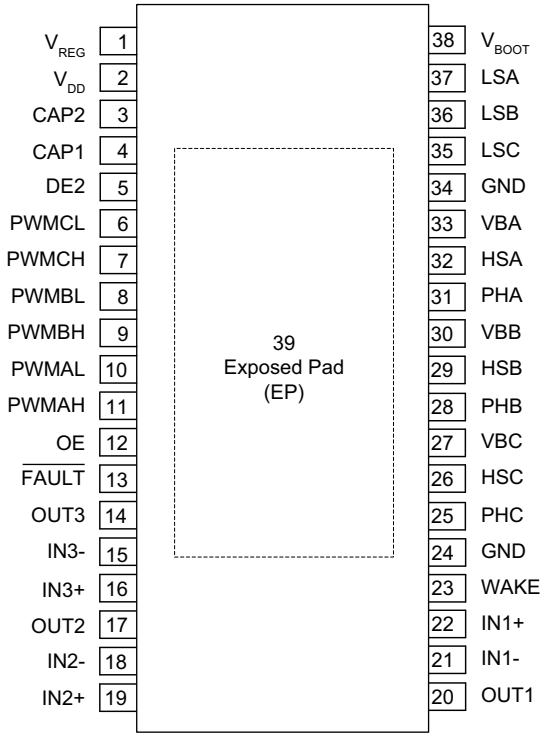
*Includes Exposed Thermal Pad (EP), see Table 3-1.

Package Types – MCP8022

5 mm x 5 mm QFN-40*

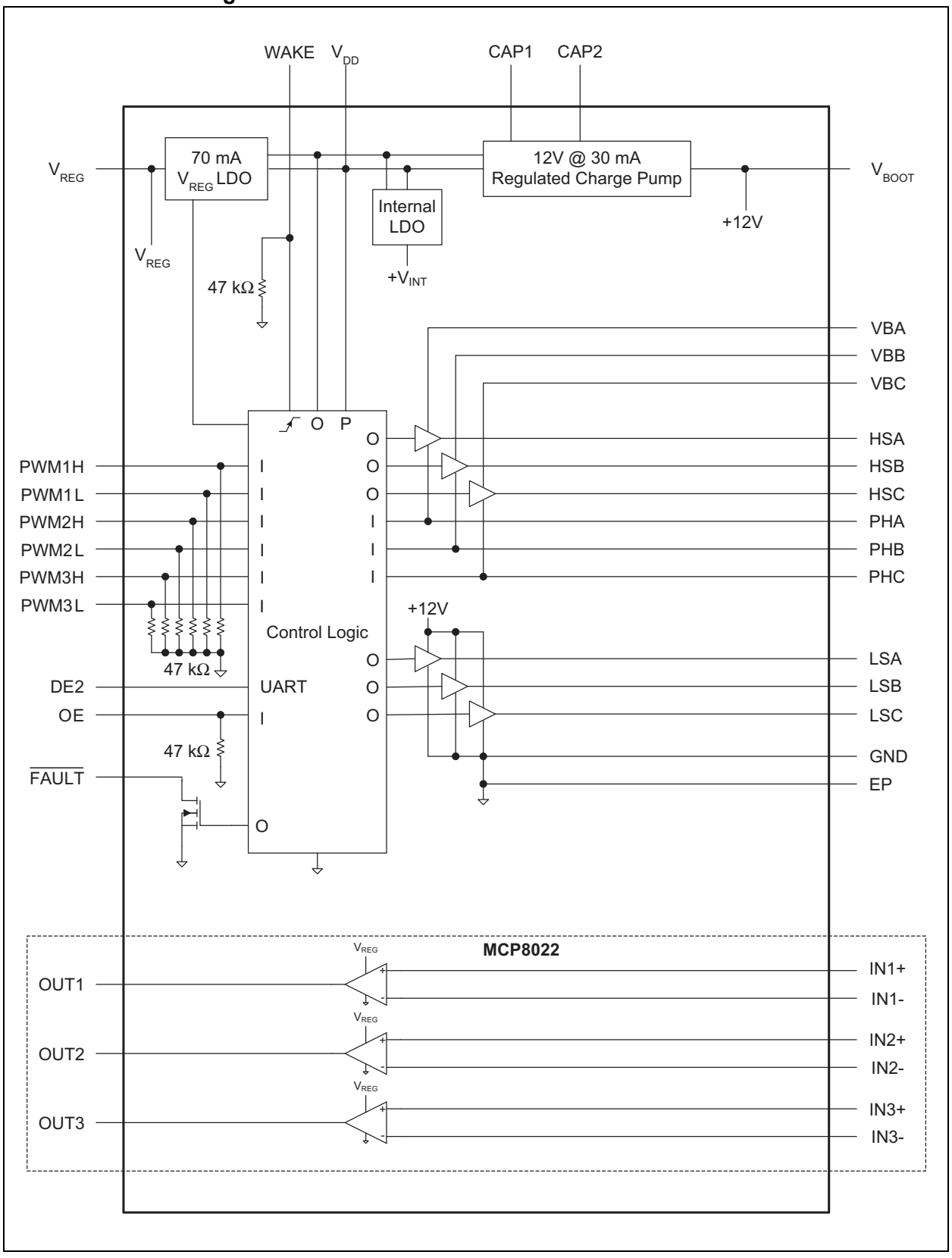


4.4 mm TSSOP-38*

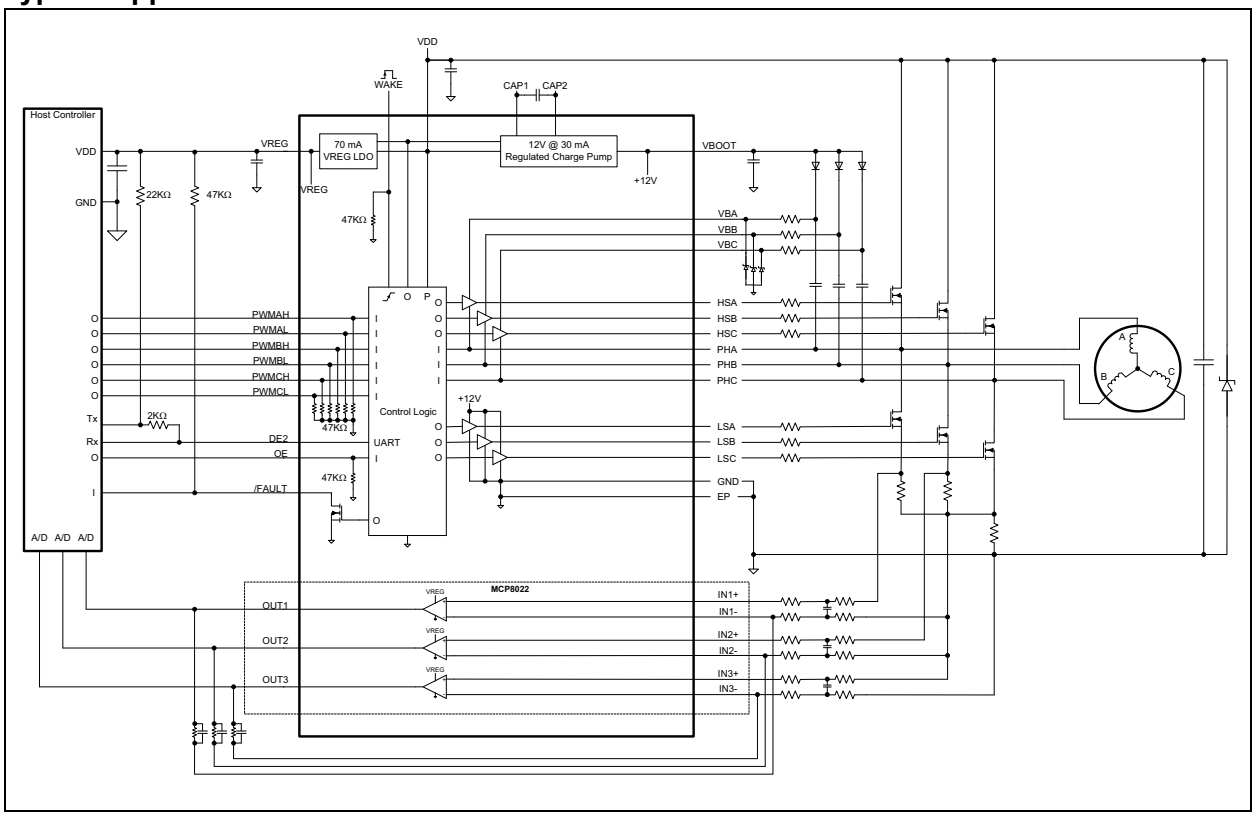


*Includes Exposed Thermal Pad (EP), see Table 3-1.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input Voltage, V_{DD} .....(GND – 0.3V) to +46.0V
V_{DD}, V_{BOOT}, PHx, VBx, WAKE Input Voltage, <100 ms Transient.....+48.0V
Internal Power Dissipation.....Internally Limited
Operating Ambient Temperature Range.....-40°C to +150°C
Operating Junction Temperature **(Note 2)** .....-40°C to +160°C
Transient Junction Temperature **(Note 1)**.....+170°C
Storage Temperature **(Note 2)** .....-55°C to +150°C
Digital I/O ..... -0.3V to 5.5V
Low-Voltage Analog I/O..... -0.3V to 5.5V
V_{BOOT}, VBx, WAKE .....(GND – 0.3V) to +44.0V
PHx, HSx .....(GND – 5.5V) to +44.0V
LSx .....(GND – 0.3V) to +13.2V
ESD and Latch-up Protection:
All Pins.....≥2 kV HBM
Corner Pins ..... ≥750V CDM
All Other Pins ..... ≥500V CDM
Latch-up Protection – All Pins ..... >100 mA

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Transient junction temperatures should not exceed one second in duration. Sustained junction temperatures above +170°C may impact the device reliability.

2: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum +160°C rating. Sustained junction temperatures above +150°C can impact the device reliability and ROM data retention.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, V_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Operating Voltage	V_{DD}	4.5	—	40.0	V	V_{REG} active
		6.0	—	29.0		Driver output active
		—	—	40.0		Sleep mode, V_{REG} inactive
Transient Maximum Voltage	V_{DDmax}	—	—	48.0	V	t < 100 ms
Input Supply Current (MCP8021)	I_{SUP}	—	5	15	µA	Sleep mode, T_J = +25°C
		—	180	330		Standby, OE = 0V
		—	950	—		Active, V_{DD} > 13,5V, OE > $V_{DIG\_HI\_TH}$
		—	1100	—		Active, V_{DD} = 6V, T_J = +25°C

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).
2: Limits by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, V_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Supply Current (MCP8022)	I_{SUP}	—	5	15	µA	Sleep mode, T_J = +25°C
		—	200	350		Standby, OPAMP = 1, OE = 0V
		—	800	1300		Standby, OPAMP = 0, OE = 0V
		—	1450	—		Active, V_{DD} > 13,5V, OE > $V_{DIG\_HI\_TH}$
		—	1600	—		Active, OE > $V_{DIG\_HI\_TH}$, V_{DD} = 7V, T_J = +25°C
Bias Generator						
+12V Regulated Charge Pump (V_{BOOT})						
Charge Pump Current	I_{CP}	20	—	—	mA	V_{DD} = 9.0V **(Note 2)**
Charge Pump Start	CP_{START}	12.50	12.75	—	V	Falling
Charge Pump Stop	CP_{STOP}	—	13.25	13.50	V	Rising
Charge Pump Frequency	CP_{FSW}	—	76.80	—	kHz	V_{DD} = 9.0V
		—	0	—		V_{DD} = 13.5V
Charge Pump Switch Resistance	CP_{RDSON}	—	14	—	Ω	R_{DSON} sum of high side and low side
Output Voltage	V_{BOOT}	—	12	—	V	$V_{DD} \geq$ 13.5V, I_{OUT} = 30 mA
		9	12	—		7V ≤ V_{DD} < 13.5V, C_{PUMP} = 150 nF, I_{OUT} = 20 mA
		9	—	—		6.25V ≤ V_{DD} < 7V, C_{PUMP} = 260 nF, I_{OUT} = 15 mA
Output Voltage Tolerance	$\lvert TOLV_{OUT12} \rvert$	—	—	4.0	%	I_{OUT} = 30 mA
Output Current	I_{BOOT}	30	—	—	mA	Average current
Output Current Limit	$I_{BOOTLIMIT}$	50	60	75	mA	Average current
Output Voltage Temperature Coefficient	TCV_{OUT12}	—	50	—	ppm/°C	**Note 2**
Line Regulation	$\lvert \Delta V_{OUT} / (V_{OUT} \times \Delta) \rvert$	—	0.1	0.5	%/V	13V < V_{DD} < 19V, I_{OUT} = 30 mA
Load Regulation	$\lvert \Delta V_{OUT} / V_{OUT} \rvert$	—	0.2	1.0	%	I_{OUT} = 0.1 mA to 30 mA
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, I_{OUT} = 10 mA **(Note 2)**
Output Capacitor Capacitance Range	CV_{BOOT}	4.7	—	30	µF	Ceramic, Tantalum, Electrolytic **(Note 2)**
Output Capacitor ESR Range	$CESR_{VBOOT}$	0.010	—	1.0	Ω	**Note 2**
V_{BOOT} Ready Threshold	V_{12SM_PG}	—	50	—	$\%V_{BOOT}$	State machine V_{BOOT} Power Good threshold to move to next state **(Note 2)**

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).
2: Limits by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, V_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
+3.3V/+5V Linear Regulator (V_{REG})						
Output Voltage	V_{REG}	—	—	—	V	V_{DD} = 6V, I_{OUT} = 70 mA
		4.8	5	5.2		V_{REG} = 5V
		3.168	3.3	3.432		V_{REG} = 3.3V
Output Voltage Tolerance	$\|TOLV_{REG}\|$	—	—	4.0	%	
Output Current	I_{OUT}	70	—	—	mA	Average current
Output Foldback Current Corner	I_{FOLD}	80	95	110	mA	Average current
Output Foldback Current Limit	I_{FOLD_LIM}	—	10	—	mA	R_{LOAD} = 10 mΩ
Line Regulation	$\|\Delta V_{OUT}/(V_{OUT} \times \Delta V_{DD})\|$	—	0.1	0.5	%/V	6V < V_{DD} < 19V, I_{OUT} = 70 mA
Load Regulation	$\|\Delta V_{OUT}/V_{OUT}\|$	—	0.2	1.0	%	I_{OUT} = 0.1 mA to 70 mA
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, I_{OUT} = 10 mA **(Note 2)**
Output Capacitor Capacitance Range	CV_{REG}	4.7	—	30	µF	Ceramic, Tantalum, Electrolytic **(Note 2)**
Output Capacitor ESR Range	$CESR_{VREG}$	0.010	—	1.0	Ω	**Note 2**
Voltage Supervisor						
V_{REG} Undervoltage Fault Inactive	$VREGUVF_{INACT}$	—	92	—	$\%V_{REG}$	V_{REG} rising
V_{REG} Undervoltage Fault Active	$VREGUVF_{ACT}$	—	88	—	$\%V_{REG}$	V_{REG} falling
V_{REG} Undervoltage Fault Hysteresis	$VREGUVF_{HYS}$	—	4	—	$\%V_{REG}$	
V_{DD} Undervoltage Lockout Inactive	$UVLO_{INACT}$	—	6.0	6.25	V	Rising
V_{DD} Undervoltage Lockout Active	$UVLO_{ACT}$	5.1	5.5	—	V	Falling
V_{DD} Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	—	0.5	—	V	
V_{DD} Undervoltage Shutdown Active	$UVSHDN_{ACT}$	4.0	4.25	4.5	V	V_{DD} < $UVSHDN_{ACT}$
V_{DD} Undervoltage Shutdown Inactive	$UVSHDN_{INACT}$	$UVLO_{INACT}$			V	V_{DD} > $UVLO_{INACT}$
V_{DD} Overvoltage Lockout Active	$OVLO_{ACT}$	—	32.0	33.0	V	V_{DD} rising
V_{DD} Overvoltage Lockout Inactive	$OVLO_{INACT}$	29.0	30.0	—	V	V_{DD} falling
V_{DD} Overvoltage Lockout Hysteresis	$OVLO_{HYS}$	—	2.0	—	V	
V_{DD} Overvoltage Shutdown Active	$OVSHDN_{ACT}$	—	42.5	44	V	V_{DD} > $OVSHDN_{ACT}$
V_{DD} Overvoltage Shutdown Inactive	$OVSHDN_{INACT}$	$OVLO_{INACT}$			V	V_{DD} < $OVSHDN_{INACT}$

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).
2: Limits by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, V_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Supervisor						
Thermal Warning Temperature	T_{WARN}	—	72	—	$\%T_{SD}$	Rising temperature (+115°C)
Thermal Warning Hysteresis	ΔT_{WARN}	—	15	—	°C	Falling temperature
Thermal Shutdown Temperature	T_{SD}	160	170	—	°C	Rising temperature **(Note 2)**
Thermal Shutdown Hysteresis	ΔT_{SD}	—	25	—	°C	Falling temperature
Motor Control Unit						
Gate Output Drivers						
Output Driver Source Current	I_{SOURCE}	0.3	0.5	—	A	V_{DD} = 12V, HS[A:C], LS[A:C] **(Note 2)**
Output Driver Sink Current	I_{SINK}	0.5	—	—	A	V_{DD} = 12V, HS[A:C], LS[A:C] **(Note 2)**
Output Driver Source Resistance	R_{DSON}	—	14	26	Ω	I_{OUT} = 10 mA, HS[A:C], LS[A:C]
Output Driver Sink Resistance	R_{DSON}	—	14	26	Ω	I_{OUT} = 10 mA, HS[A:C], LS[A:C]
Output Driver Fault Blanking	t_{BLANK}	500		4000	ns	Set in CFG2[1:0] bits
		—	4000	—		00 – Default
		—	2000	—		01
		—	1000	—		10
		—	500	—		11
Output Driver UVLO Threshold	V_{DUVLO}	4	—	4.5	V	Configuration Register 0 (bit 3 = 0)
Output Driver PWM Dead Time	t_{PWM_DEAD}	250		2000	ns	Set in CFG2[4:2] bits
		—	2000	—		000 – Default
		—	1750	—		001
		—	1500	—		010
		—	1250	—		011
		—	1000	—		100
		—	750	—		101
		—	500	—		110
		—	250	—		111
Output Driver Propagation Delay Time On	$t_{GATE\_PROP\_ON}$	—	40	—	ns	From PWMxy active to HSx/LSx > 10%
Output Driver Propagation Delay Time Off	$t_{GATE\_PROP\_OFF}$	—	40	—	ns	From PWMxy inactive to HSx/LSx < 90%
Output Driver HS Drive Voltage	V_{HS}	4.5	12	13.5	V	With respect to Phase pin **(Note 2)**
		-5.5	—	—		With respect to ground **(Note 2)**
Output Driver LS Drive Voltage	V_{LS}	4.5	12	13.5	V	With respect to ground **(Note 2)**
Output Driver Short-Circuit Protection Threshold (High Side: V_{DD} – VPHX) (Low Side: VPHX – P_{GND})	D_{SC_THR}	0.250	—	1.000	V	Set in CFG0 register
		—	0.250	—		00 – Default
		—	0.500	—		01
		—	0.750	—		10
		—	1.000	—		11

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).
2: Limits by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, V_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Driver Short-Circuit and Undervoltage Debounce Filter Time	T_{SC_DLY}	—	—	—	ns	C_{LOAD} = 1000 pF, V_{DD} = 12V
		230 ns	—	530 ns		Detection after filtering **(Note 2)**
Power-up or Sleep to Standby	t_{POWER}	—	5	—	ms	I_{VREG} = 70 mA
Standby to Motor Operational	t_{MOTOR}	—	35	—	µs	OE high-low-high transition < 1 ms Fault clearing pulse
		—	5	10	ms	OE low-high transition, standby state to operational **(Note 2)**
		—	—	15	ms	OE low-high transition, standby state to operational if V_{BOOT} fails to reach V_{12SM_PG}
Fault to Driver Output Turn-Off	T_{FAULT_OFF}	—	—	—	µs	C_{LOAD} = 1000 pF, V_{DD} = 12V, time after Fault occurs **(Note 2)**
		—	0.420	1.0		XOCP
		—	2.4	4.0		OVLO
		—	4.2	6.0		All other Faults
OE Low to Driver Output Turn-Off	T_{DEL_OFF}	—	3.0	3.6	µs	C_{LOAD} = 1000 pF, V_{DD} = 12V, time after OE = Low **(Note 2)**
OE Low to Standby State	$t_{STANDBY}$	1.0	—	1.35	ms	Time after OE = Low, SLEEP bit = 0
OE Low to Sleep State	t_{SLEEP}	1.0	—	1.35	ms	Time after OE = Low, SLEEP bit = 1
OE Fault Clearing Pulse	t_{FAULT_CLR}	1	—	900	µs	OE high-low-high transition time
Operational Amplifiers (MCP8022)						
Input Offset Voltage	V_{OS}	-10	—	+10	mV	V_{CM} = 0V
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	V_{CM} = 0V **(Note 2)**
Input Bias Current	I_B	-1	—	+1	µA	
Common-Mode Input Range	V_{CMR}	-0.3	—	V_{REG}	V	
Common-Mode Rejection Ratio	CMRR	—	80	—	dB	Freq = 1 kHz, I_{OUT} = 10 µA
Maximum Output Voltage Range	V_{OL}, V_{OH}	0.15	—	V_{REG} – 0.150	V	I_{OUT} = ±200 µA
Slew Rate	SR	—	±7	—	V/µs	Symmetrical, C_{LOAD} = 20 pF
Gain Bandwidth Product	GBWP	4	10.0	—	MHz	**(Note 2)**
I/O Ports						
Digital Interface						
Digital Input/Output	$DIGITAL_{I/O}$	0	—	5.5	V	**(Note 2)**
Digital Open-Drain Low Voltage	$DIGITALV_{I/O}$	—	—	50	mV	I_{LOAD} = 1 mA
Digital Input Rising Threshold	$V_{DIG\_HI\_TH}$	1.26	—	—	V	
Digital Input Falling Threshold	$V_{DIG\_LO\_TH}$	—	—	0.54	V	
Digital Input Hysteresis	V_{DIG_HYS}	—	500	—	mV	
Digital Input Current	I_{DIG}	—	30	100	µA	V_{DIG} = 3.0V
		—	0.2	—		V_{DIG} = 0V
$\overline{FAULT}$ Output Low Voltage (Open-Drain)	V_{FAULT}	—	—	50	mV	I_{FAULT} = 1 mA

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).
2: Limits by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted: T_J = -40°C to +150°C; typical values are for +25°C, V_{DD} = 13.5V, CV_{BOOT} = 4.7 µF, CV_{REG} = 4.7 µF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Pull-Down Resistance	R_{PULLDN}	—	47	—	kΩ	PWM[A:C]H/L, OE, WAKE pins
Analog Interface						
Analog Low-Voltage Input	$ANALOG_{VIN}$	0	—	5.5	V	Excludes high-voltage pins **(Note 2)**
Analog Low-Voltage Output	$ANALOG_{VOUT}$	0	—	V_{REG}	V	Excludes high-voltage pins **(Note 2)**
WAKE Input						
Input Voltage	$WAKE_{I/O}$	0	—	V_{DD}	V	
Input Rising Threshold	$V_{WAKE\_HI\_TH}$	1.26	—	—	V	**(Note 2)**
Input Falling Threshold	$V_{WAKE\_LO\_TH}$	—	—	0.54	V	**(Note 2)**
Input Hysteresis	V_{WAKE_HYS}	—	500	—	mV	
Input Current	I_{WAKE}	—	0.2	—	µA	V_{WAKE} = 0.0V
		—	70	—		V_{WAKE} = 3.3V
		—	106	—		V_{WAKE} = 5.0V
		—	596	—		V_{WAKE} = 28V
Input Pull-Down Resistance	R_{WAKE_PULLDN}	—	47	—	kΩ	
Wake-up Signal Setup Time	t_{WAIT_SETUP}	150	—	—	µs	Minimum time WAKE pin must be logic low before rising edge of wake-up pulse
DE2 Communications						
Baud Rate	BAUD	9120	9600	10080	bps	Half-duplex
Power-up Delay	PU_DELAY	—	1	—	ms	Time from rising $V_{DD} \geq$ 6V to DE2 active
DE2 Sink Current	I_{DE2_SINK}	1	—	—	mA	$V_{DE2} \leq$ 50 mV
DE2 Message Response Time	t_{DE2_RSP}	0	—	1	ms	Time from last received Stop bit to response Start bit
DE2 Host Wait Time	t_{DE2_WAIT}	2.8	—	—	ms	Minimum time for host to wait for response; three packets based on 9600 Baud
DE2 Message Receive Time-out	$DE2_{RCVTOUT}$	—	—	1.45	ms	Time after Start bit received to NACK for no Stop bit
Auto-Baud Detection Window (Break)	$ABUAD_{DET}$	1.29	—	2.00	ms	Window for valid detection of continuous logic low on DE2 link
Auto-Baud Response Delay	$ABAUD_{DLY}$	—	1.00	—	ms	Delay from $ABUAD_{DET}$ to start of sending 0x55 byte
Auto-Baud Complete Delay	$ABAUD_{COMP}$	—	2.00	—	ms	Delay after sending 0x55 byte before exiting auto-baud function
Delay Between Bytes of Multibyte Message from Host	$t_{DE2\_HOST\_MULTI\_DLY}$	—	—	1.3	ms	Delay between message bytes arriving from host

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).
2: Limits by design, not production tested.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges (Note 1)						
Specified Temperature Range	T_A	-40	—	+150	°C	
Operating Temperature Range	T_A	-40	—	+150	°C	
	T_J	-40	—	+160	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Package Thermal Resistance						
5 mm x 5 mm 28-Lead VQFN	θ_{JA}	—	26.8	—	°C/W	4-Layer JC51-7 standard board, natural convection
	θ_{JC}	—	8.3	—		
5 mm x 5 mm 40-Lead VQFN	θ_{JA}	—	27.3	—	°C/W	4-Layer JC51-7 standard board, natural convection
	θ_{JC}	—	8.5	—		
4.4 mm 28-Lead TSSOP-EP, 0.65 mm Pitch	θ_{JA}	—	34	—	°C/W	4-Layer JC51-7 standard board, natural convection
	θ_{JC}	—	5	—		
4.4 mm 38-Lead TSSOP-EP, 0.50 mm Pitch	θ_{JA}	—	34	—	°C/W	4-Layer JC51-7 standard board, natural convection
	θ_{JC}	—	5	—		

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +160°C rating. Sustained junction temperatures above +160°C can impact the device reliability.

ESD, SUSCEPTIBILITY, SURGE AND LATCH-UP TESTING

Parameter	Standard and Test Condition	Value
Input Voltage Surges	ISO 16750-2	28V for 1 minute, 45V for 0.5 seconds
ESD HBM with 1.5 kΩ/100 pF	CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref E JEDEC JS-001-2012	±2 kV
ESD CDM – Corner Pins	ANSI/ESD-STM5.3.1-2009 CDM13073 AEC-Q100-011-Ref_B	±750V Class C4
ESD CDM – All Other Pins	ANSI/ESD-STM5.3.1-2009 CDM13073 AEC-Q100-011-Ref_B	±500V Class C4
Latch-up Susceptibility	AEC Q100-004, 150°C JEDEC JESD78	>100 mA

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

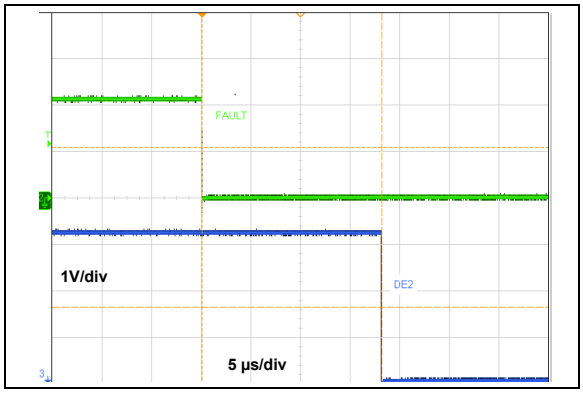


FIGURE 2-1: *Fault Low to DE2 Message Delay.*

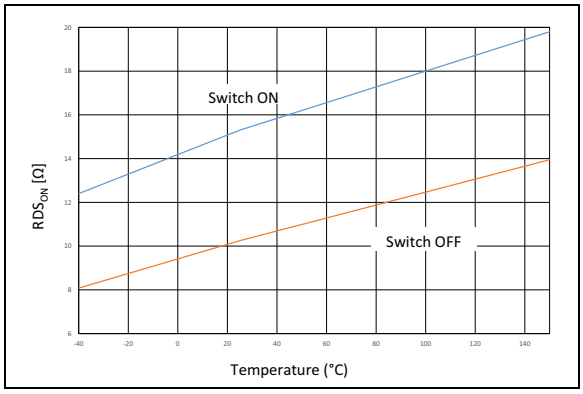


FIGURE 2-4: *Driver R_{DSON} vs. Temperature.*

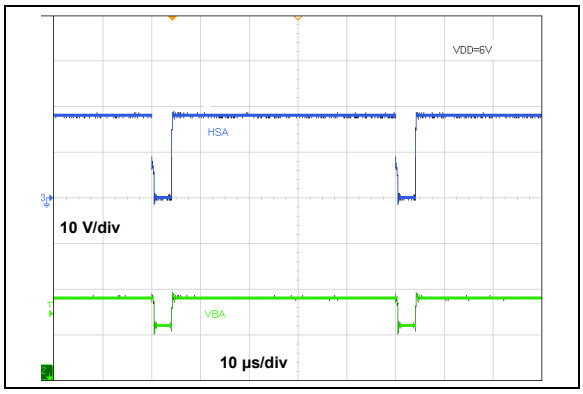


FIGURE 2-2: *Bootstrap Voltage @ 92% Duty Cycle.*

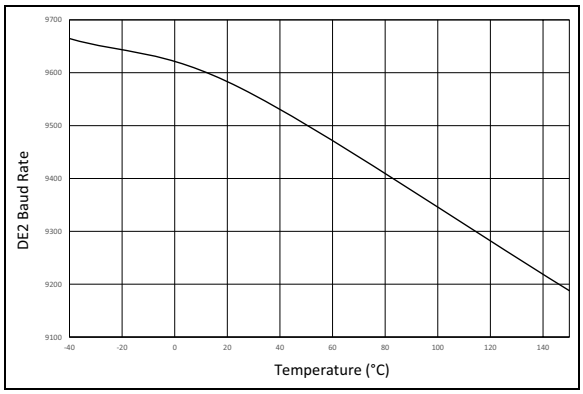


FIGURE 2-5: *Auto-Baud vs. Temperature.*

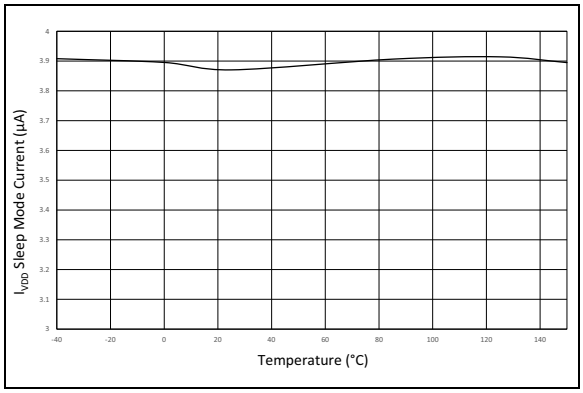


FIGURE 2-3: *Standby Current vs. Temperature (MCP8022).*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1 and Table 3-2.

TABLE 3-1: MCP8021 – PIN FUNCTIONS

28-Lead TSSOP	28-Lead VQFN	Symbol	I/O	Description
1	25	V_{BOOT}	Power	Bootstrap and internal low-side gate drive circuit supply output
2	26	V_{REG}	Power	Linear regulator output
3	27	V_{DD}	Power	Input supply
4	28	CAP2	I/O	Charge pump flying capacitor input
5	1	CAP1	I/O	Charge pump flying capacitor input
6	2	PWMCL	I	Digital input, Phase C low-side control, 47 kΩ pull-down
7	3	PWMCH	I	Digital input, Phase C high-side control, 47 kΩ pull-down
8	4	PWMBL	I	Digital input, Phase B low-side control, 47 kΩ pull-down
9	5	PWMBH	I	Digital input, Phase B high-side control, 47 kΩ pull-down
10	6	PWMAL	I	Digital input, Phase A low-side control, 47 kΩ pull-down
11	7	PWMAH	I	Digital input, Phase A high-side control, 47 kΩ pull-down
12	8	$\overline{FAULT}$	O	Digital output, driver Fault, open-drain
13	9	OE	I	Digital input, device output enable, 47 kΩ pull-down
14	10	DE2	I/O	Digital input/output, half-duplex communications, open-drain
15	11	WAKE	I	HV digital edge-triggered input, device wake-up from Sleep, 47 kΩ pull-down
16	12	P_{GND}	Power	Power 0V reference
17	13	PHC	I/O	Phase C high-side MOSFET driver bias reference
18	14	HSC	O	Phase C high-side N-channel MOSFET gate drive
19	15	VBC	Power	Phase C high-side MOSFET driver bias
20	16	PHB	I/O	Phase B high-side MOSFET driver bias reference
21	17	HSB	O	Phase B high-side N-channel MOSFET gate drive
22	18	VBB	Power	Phase B high-side MOSFET driver bias
23	19	PHA	I/O	Phase A high-side MOSFET driver bias reference
24	20	HSA	O	Phase A high-side N-channel MOSFET gate drive
25	21	VBA	Power	Phase A high-side MOSFET driver bias
26	22	LSC	O	Phase C low-side N-channel MOSFET gate drive
27	23	LSB	O	Phase B low-side N-channel MOSFET gate drive
28	24	LSA	O	Phase A low-side N-channel MOSFET gate drive
EP	EP	P_{GND}	Power	Exposed Pad, connect to power 0V reference (P_{GND})

TABLE 3-2: MCP8022 – PIN FUNCTIONS

40-Lead VQFN	38-Lead TSSOP	Symbol	I/O	Description
1	5	DE2	I/O	Digital input/output, half-duplex communications, open-drain
2	6	PWMCL	I	Digital input, Phase C low-side control, 47 kΩ pull-down
3	7	PWMCH	I	Digital input, Phase C high-side control, 47 kΩ pull-down
4	8	PWMBL	I	Digital input, Phase B low-side control, 47 kΩ pull-down
5	9	PWMBH	I	Digital input, Phase B high-side control, 47 kΩ pull-down
6	10	PWMAL	I	Digital input, Phase A low-side control, 47 kΩ pull-down
7	11	PWMAH	I	Digital input, Phase A high-side control, 47 kΩ pull-down
8	12	OE	I	Digital input, device output enable, 47 kΩ pull-down
9	13	$\overline{\text{FAULT}}$	O	Digital output, driver Fault, open-drain
10	—	P_{GND}	Power	Power 0V reference
11	14	OUT3	O	Operational Amplifier 3 output
12	15	IN3-	I	Operation Amplifier 3 inverting input
13	16	IN3+	I	Operation Amplifier 3 noninverting input
14	17	OUT2	O	Operational Amplifier 2 output
15	18	IN2-	I	Operation Amplifier 2 inverting input
16	19	IN2+	I	Operation Amplifier 2 noninverting input
17	20	OUT1	O	Operational Amplifier 1 output
18	21	IN1-	I	Operation Amplifier 1 inverting input
19	22	IN1+	I	Operation Amplifier 1 noninverting input
20	23	WAKE	I	HV digital edge-triggered input, device wake-up from Sleep, 47 kΩ pull-down
21	24	P_{GND}	Power	Power 0V reference
22	25	PHC	I/O	Phase C high-side MOSFET driver bias reference
23	26	HSC	O	Phase C high-side N-channel MOSFET gate drive
24	27	VBC	Power	Phase C high-side MOSFET driver bias
25	28	PHB	I/O	Phase B high-side MOSFET driver bias reference
26	29	HSB	O	Phase B high-side N-channel MOSFET gate drive
27	30	VBB	Power	Phase B high-side MOSFET driver bias
28	31	PHA	I/O	Phase A high-side MOSFET driver bias reference
29	32	HSA	O	Phase A high-side N-channel MOSFET gate drive
30	33	VBA	Power	Phase A high-side MOSFET driver bias
—	34	P_{GND}	Power	Power 0V reference
31	35	LSC	O	Phase C low-side N-channel MOSFET gate drive
32	36	LSB	O	Phase B low-side N-channel MOSFET gate drive
33	37	LSA	O	Phase A low-side N-channel MOSFET gate drive
34	38	VBOOT	Power	Bootstrap and internal low-side gate drive circuit supply output
35	—	P_{GND}	Power	Power 0V reference
36	—	P_{GND}	Power	Power 0V reference
37	1	VREG	Power	Linear regulator output
38	2	V_{DD}	Power	Input supply
39	3	CAP2	I/O	Charge pump flying capacitor input
40	4	CAP1	I/O	Charge pump flying capacitor input
EP	EP	P_{GND}	Power	Exposed Pad, connect to power 0V reference (P_{GND})

3.1 Communications Port (DE2)

Open-drain communications node. The DE2 communications is a half-duplex, 9600 baud, 8-bit, no parity communications link. The open-drain DE2 pin must be pulled high by an external pull-up resistor. The pin has a minimum drive capability of 1 mA with a V_{DE2} of ≤50 mV when driving low.

3.2 Low-Side PWM Inputs (PWMAL, PWMBL, PWMCL)

Digital PWM inputs for low-side driver control. Each input has a 47 kΩ pull-down to ground. The PWM signals may contain dead-time timing or the system may use the CFG2 Configuration register to set the dead time.

3.3 High-Side PWM Inputs (PWMAH, PWMBH, PWMCH)

Digital PWM inputs for high-side driver control. Each input has a 47 kΩ pull-down to ground. The PWM signals may contain dead-time timing or the system may use the CFG2 Configuration register to set the dead time.

3.4 Output Enable Input (OE)

The Output Enable input pin is used to enable/disable the output driver and the on-board functions. When OE is high, all device functions are enabled. When OE is low, the device operates in Standby or Sleep mode. When Standby mode is active, the V_{BOOT} output supply and charge pump are disabled. The operational amplifiers in the MCP8022 are also disabled if the OPAMP bit in the CFG0 Configuration register is set. The high-side and low-side gate drive outputs are all set to a low state within 100 ns of OE going low. The device transitions to Standby or Sleep mode, 1 ms after OE goes low.

The OE pin may be used to clear any hardware Faults. When a Fault occurs, the OE input may be used to clear the Fault by setting the pin low and then high again. The Fault is cleared by the rising edge of the OE signal if the hardware Fault is no longer active.

The OE pin is used to enable Sleep mode when the SLEEP bit in the CFG0 Configuration register is set to a '1'. OE must be low for a minimum of 1 ms before the transition to Standby or Sleep mode will occur. This allows time for OE to be toggled, to clear any Faults, without going into Sleep mode.

The OE pin has an internal 47 kΩ pull-down to ground.

3.5 Fault Output ($\overline{FAULT}$)

Fault output pin. The latched open-drain output will go low while a Fault is active. Table 4-4 shows the Faults that cause the $\overline{FAULT}$ pin to go low. The pin will stay low until the Fault is inactive and the OE pin is toggled, from low-to-high, to clear the internal Fault latch.

The $\overline{FAULT}$ pin is able to sink 1 mA of current while maintaining less than a 50 mV drop across the output.

The $\overline{FAULT}$ pin will also be active (low) upon initial power-up until the state machine completes the V_{REG} state. This may be used to signal an external host that the driver is ready.

3.6 Power Ground (P_{GND}), Exposed Pad (EP)

Device ground. The PCB ground traces should be short, wide and form a 'Star' pattern to the power source. The Exposed Pad (EP) must be soldered to the PCB. The PCB area below the EP should be a copper pour with thermal vias to help transfer heat away from the device.

3.7 Operational Amplifier Outputs (OUT1, OUT2, OUT3) (MCP8022)

Operational amplifier outputs. These general purpose amplifiers may be used for current sense gain. The amplifiers are disabled when OE = 0 and the OPAMP bit in the CFG0 Configuration register is set.

3.8 Operational Amplifier Inputs (IN1+/-, IN2+/-, IN3+/-) (MCP8022)

Operational amplifier inverting and noninverting inputs. Used in conjunction with the corresponding amplifier OUTx pin to set amplifier gain. The amplifiers are disabled in Standby mode when OE = 0 and the OPAMP bit in the CFG0 Configuration register is set.

3.9 Wake Input (WAKE)

The WAKE pin has an internal 47 kΩ pull-down to ground.

The device will awaken from Sleep mode, on the rising edge of the WAKE pin, after detecting a low state lasting $>t_{WAIT\_SETUP}$ on the pin. The WAKE pin is capable of operating at voltage levels up to V_{DD}.

3.10 Motor Phase Inputs (PHA, PHB, PHC)

Phase signals from the motor. These signals provide high-side N-channel MOSFET driver bias reference and Back EMF sense input. The phase signals are also used with the bootstrap capacitors to provide a high-side gate drive via the VBx inputs.

3.11 High-Side N-MOSFET Gate Driver Outputs (HSA, HSB, HSC)

High-side N-channel MOSFET gate drive signal. Connect to the gate of the external MOSFETs. A resistor and gate-to-source capacitor may be used between these pins and the MOSFET gates to limit phase node slew rate and MOSFET current.

3.12 Bootstrap Inputs (VBA, VBB, VBC)

High-side MOSFET driver bias. Connect these pins between the bootstrap charge pump diode cathode and the bootstrap charge pump capacitor. The V_{BOOT} output is used to provide the bootstrap supply voltage at the diode anodes. The phase signals are connected to the other side of the bootstrap charge pump capacitors. The bootstrap capacitors charge to V_{BOOT} when the phase signals are pulled low by the low-side drivers. When the low-side drivers turn off and the high-side drivers turn on, the phase signal is pulled to V_{DD}, causing the bootstrap voltage to rise to V_{DD} + 12V.

3.13 Low-Side N-MOSFET Gate Driver Outputs (LSA, LSB, LSC)

Low-side N-channel MOSFET drive signal. Connect to the gate of the external MOSFETs. A resistor and gate-to-source capacitor may be used between these pins and the MOSFET gates to limit current and slew rate.

3.14 Bootstrap Supply (V_{BOOT})

Bootstrap supply voltage regulator output. The V_{BOOT} regulator output may be used to power external devices, such as Hall effect sensors or amplifiers. The regulator output requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the V_{BOOT} pin as is practical. A minimum capacitance of 4.7 µF is required to ensure stable operation of the V_{BOOT} circuit. Larger capacitances may be used to increase transient performance. The V_{BOOT} regulator is supplied by the internal charge pump when the charge pump is active. When the charge pump is inactive, the V_{BOOT} regulator is supplied by V_{DD}.

The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.15 +3.3V or +5V LDO (V_{REG})

The V_{REG} pin may be a +3.3V or a +5V Low Dropout (LDO) voltage regulator output, depending on device part number. The V_{REG} LDO may be used to power external devices, such as Hall effect sensors, amplifiers or host processors. The V_{REG} LDO is enabled when the device is not in Sleep mode and the supply voltage is above the device shutdown voltage. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the V_{REG} pin as is practical. For most applications, a minimum 4.7 µF of capacitance will ensure stable operation of the LDO circuit. Larger capacitances may be used to increase transient performance.

The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.16 Power Supply Input (V_{DD})

Connect V_{DD} to the main supply voltage. This voltage should be the same as the motor voltage. The driver overcurrent and overvoltage shutdown features are relative to the V_{DD} pin. When the V_{DD} voltage is separate from the motor voltage, the overcurrent and overvoltage protection features may not be available.

The V_{DD} voltage must not exceed the maximum operating limits of the device. Connect a bulk capacitor close to this pin for good load step performance and transient protection. The actual capacitance should be equal to or larger than the sum of the capacitors attached to the driver supply outputs. The attached capacitors are the V_{REG}, V_{BOOT} and VBx (three bootstrap capacitors), and the charge pump capacitances.

EQUATION 3-1: V_{DD} BULK CAPACITOR CALCULATION

$$CV_{DD} \geq CV_{REG} + CV_{BOOT} + (3 \times CV_{BX}) + C_{CAPx}$$

The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield lower voltage drop, better noise and PSRR performance at high frequency.

3.17 Charge Pump Flying Capacitor (CAP1, CAP2)

Charge pump flying capacitor connection. Connect the charge pump capacitor across these two pins. The charge pump flying capacitor supplies the power for the V_{BOOT} voltage regulator when the charge pump is active.

4.0 DETAILED DESCRIPTION

4.1 State Diagrams

4.1.1 MCP8021/2 STATE DIAGRAM

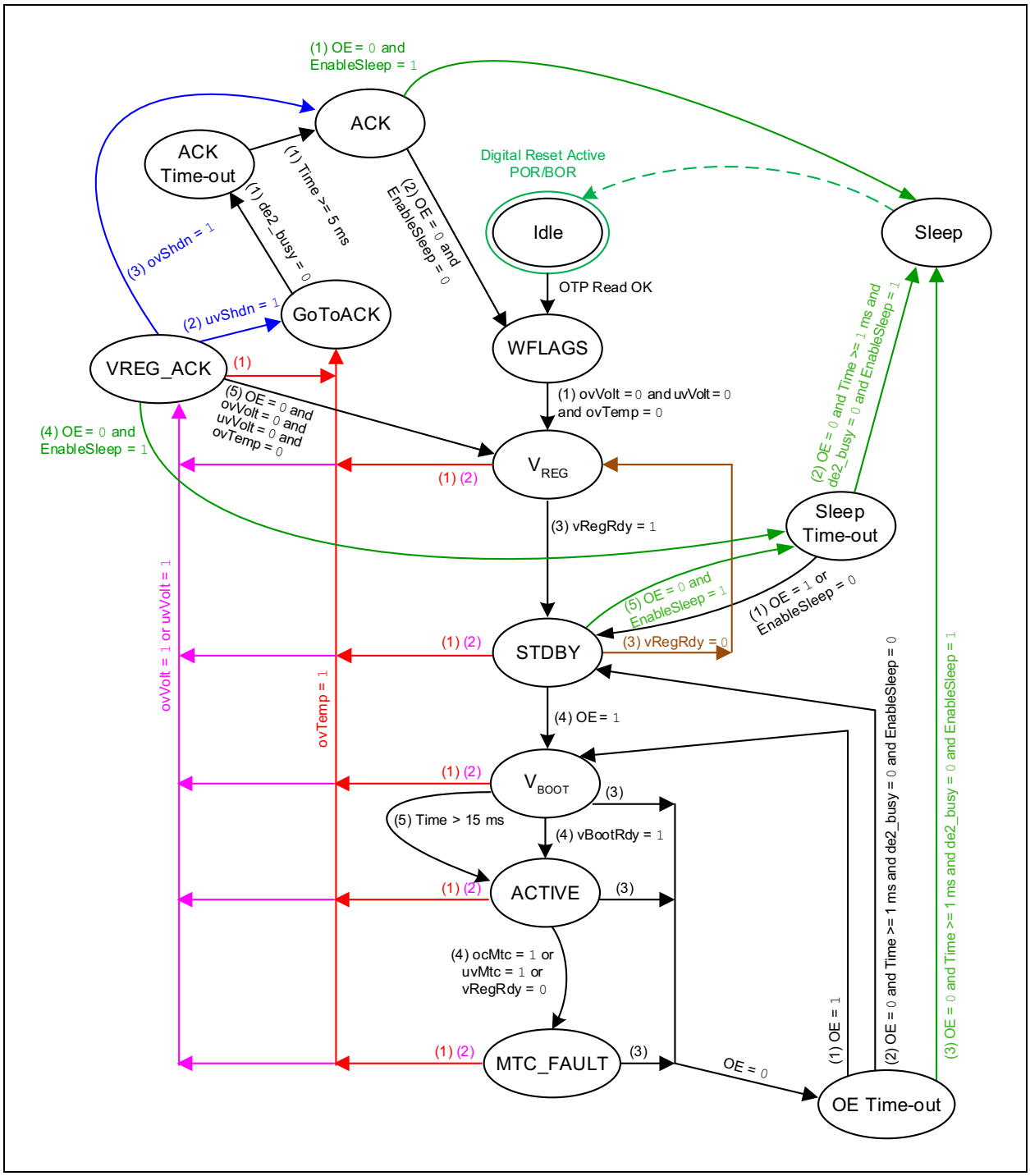


FIGURE 4-1: *MCP8021/2 State Machine.*

4.1.2 DE2 RECEIVE AND AUTO-BAUD SEQUENCE

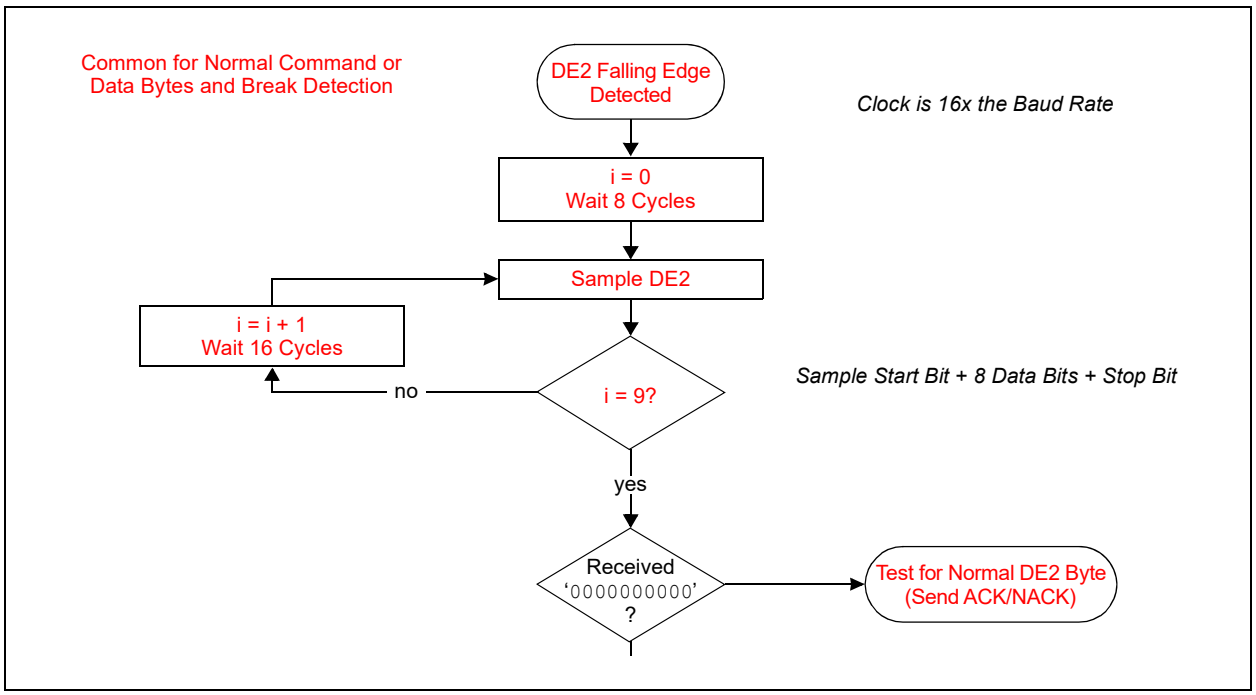


FIGURE 4-2: *DE2 Data Reception and Auto-Baud Rate Sequence (Part 1).*

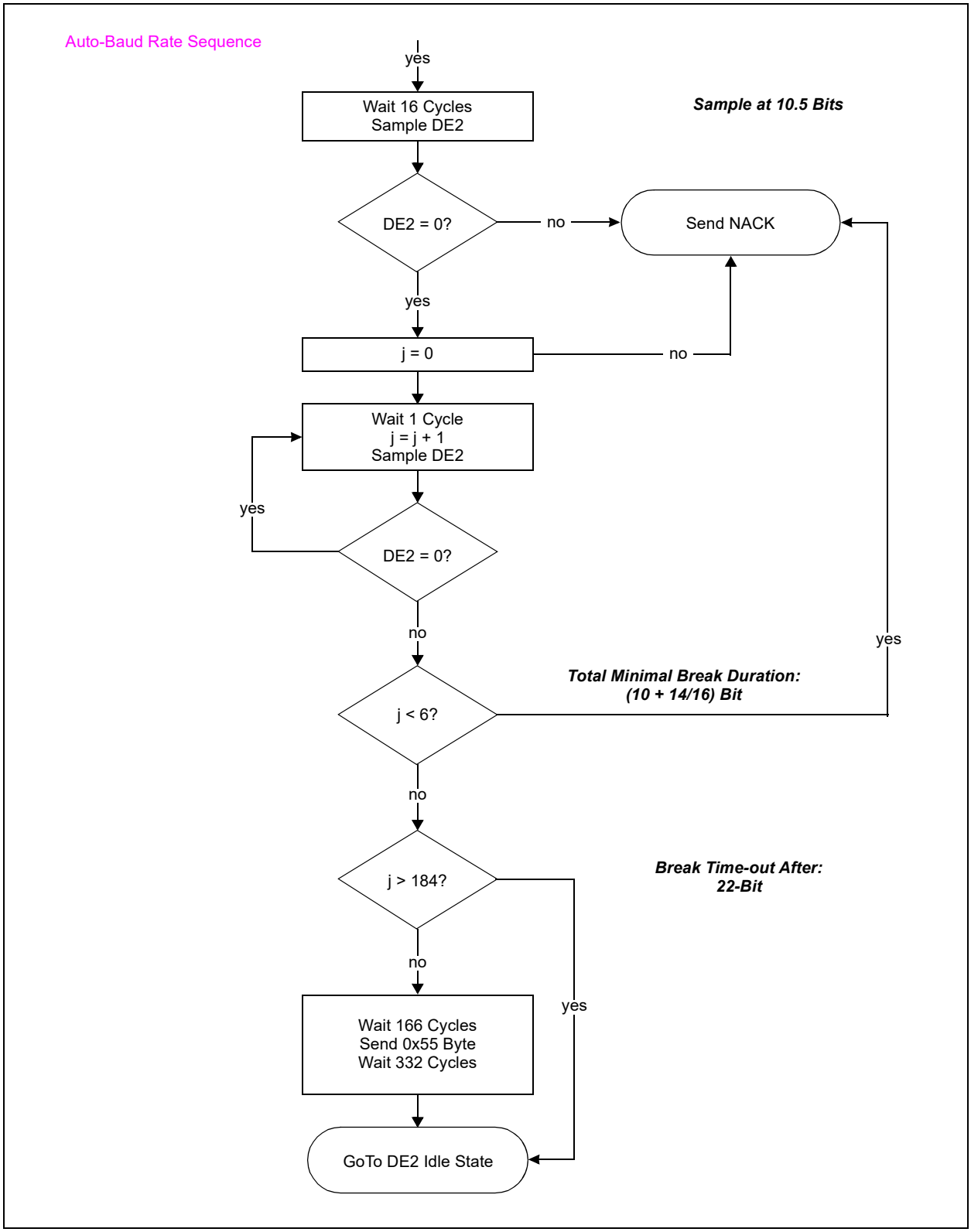


FIGURE 4-3: *DE2 Data Reception and Auto-Baud Rate Sequence (Part 2).*

4.2 Bias Generator

The internal bias generator controls several voltage rails. Two fixed output Low Dropout linear regulators, internal bias supply LDOs and a charge pump are controlled through the bias generator. In addition, the bias generator performs supervisory functions.

4.2.1 CHARGE PUMP

An unregulated charge pump is utilized to boost the input to the V_{BOOT} voltage regulator during low input supply voltage conditions. When the input bias to the device (V_{DD}) drops below the CP_{START} voltage, the charge pump is activated. When activated, 2 x V_{DD} is presented to the input of the V_{BOOT} regulator. The charge pump is capable of maintaining a V_{BOOT} output of +9V @ 15 mA for a V_{DD} supply voltage of 5.25V to 7V. The charge pump is capable of maintaining a V_{BOOT} output of +12V @ 20 mA for a supply input voltage of 7V to 13.5V. The charge pump is disabled and bypassed at V_{DD} voltages above 13.5V, allowing an output voltage of +12V @ 30 mA.

The typical charge pump flying capacitor is a 0.1 µF to 1.0 µF ceramic capacitor.

4.2.2 V_{BOOT} VOLTAGE REGULATOR

The V_{BOOT} voltage regulator rail is used to supply bias voltage for the integrated 3-phase power MOSFET bridge drivers.

The regulator is capable of supplying 30 mA of external load current. The regulator has a minimum overcurrent limit of 40 mA.

The regulator gets its power from the integrated charge pump. When operating at supply voltages (V_{DD}) that are above +13.5V, the integrated charge pump will be disabled and the V_{DD} supply will power the V_{BOOT} voltage regulator. The V_{BOOT} regulator output may be lower than the designed voltage, while operating in the V_{DD} range of +12.5V to +13.0V, due to the dropout voltage of the regulator.

The V_{BOOT} regulator requires an output capacitor, connected from V_{BOOT} to GND, to stabilize the internal control loop and to sustain the bootstrap capacitor energy. A minimum of 4.7 µF ceramic output capacitance is required for the V_{BOOT} voltage regulator output; 10 µF is recommended when switching large MOSFET gate loads. The output capacitor forces a time delay between setting the OE pin high (to transition from Standby mode to Active mode) and the V_{BOOT} regulator voltage output rising above the voltage required to set an internal VBootReady flag. The PWM inputs must not be activated while the V_{BOOT} output is charging the output capacitors to the VBootReady voltage (typically 6.0V). The time required before allowing the PWM inputs to become active, after setting OE high to transition from Standby mode to Active mode, is dependent on output capacitance, any extra loads and supply voltage ramp-up time. The user should allow a minimum time of 0.94 ms for the V_{BOOT} output voltage to rise above the VBootReady voltage. A voltage of 6V and supply current of 30 mA may be used for this delay estimation. See Equation 4-1.

EQUATION 4-1: OE PIN HIGH TO V_{BOOT} READY

$$dt = (C \times dV)/(I)$$
$$dt = (4.7\ \mu F \times 6V)/(30\ mA)$$
$$dt = 0.94\ ms$$

There is a time-out function that allows the state machine to move from V_{BOOT} to active after 15 ms, regardless of the V_{BOOT} ready voltage. This time-out function prevents the driver from hanging up if the V_{BOOT} voltage is overloaded.

There is also a capacitive voltage divider formed by the three bootstrap capacitors and the V_{BOOT} capacitor. The V_{BOOT} capacitor should be selected so that when the V_{BOOT} supply is active and the bootstrap capacitors are charged, the voltage at the bootstrap capacitors will be greater than the driver undervoltage shutdown voltage, 4.5V. For a system with V_{BOOT} = 12V, V_{MIN} = 4.5V and N = 3 x 1 µF $C_{BOOTSTRAP}$ capacitors charging at the same time, the desired CV_{BOOT} capacitor is 1.8 µF (see Equation 4-2). Since the V_{BOOT} supply requires a 4.7 µF capacitor, a 4.7 µF capacitor should be used. The initial voltage seen by the bootstrap capacitors using a 4.7 µF V_{BOOT} capacitor will be 7.32V. See Equation 4-3.

EQUATION 4-2: V_{BOOT} CAPACITOR

$$CV_{BOOT} = \frac{(N \times C_{BOOTSTRAP})}{(V_{BOOT}) \div (V_{MIN}) - 1}$$

EQUATION 4-3: BOOTSTRAP VOLTAGE

$$V_{BOOTSTRAP} = \frac{(V_{BOOT} \times CV_{BOOT})}{((CV_{BOOT} + N \times C_{BOOTSTRAP})}$$

The V_{BOOT} output is disabled when the driver transitions to Standby or Sleep mode.

Table 4-4 shows the Faults that will also disable the V_{BOOT} voltage regulator.

4.2.3 V_{REG} LOW DROPOUT LINEAR REGULATOR (LDO)

The V_{REG} LDO is used to bias an external microcontroller, the internal operational amplifiers and the gate control logic.

The V_{REG} LDO is capable of supplying 70 mA of external load current. The regulator has a minimum overcurrent limit of 80 mA. When the regulator current exceeds the overcurrent limit, the regulator will enter a True Current and Voltage Foldback mode based upon load impedance. As the load impedance decreases towards zero ohms, the regulator output current and voltage will also decrease until the final foldback current and voltage are attained.

When the regulator output voltage drops below the V_{REG} undervoltage limit, the VREGUVF undervoltage Fault bit will be set in the STAT1 register. The regulator will remain active during the Fault. Table 4-1 shows the registers and bits associated with Faults.

The V_{REG} LDO will be disabled when the V_{DD} supply voltage undervoltage Fault occurs. The V_{REG} LDO will be re-enabled when the conditions in **Section 4.3.1 "Voltage Supervisor"** are met.

A minimum of 4.7 µF ceramic output capacitance is required for the V_{REG} LDO; 10 µF is recommended to increase transient performance when a host microcontroller is attached.

The V_{REG} LDO is disabled while the system is in Sleep mode.

4.3 Supervisor

The bias generator incorporates a voltage supervisor and a temperature supervisor.

4.3.1 VOLTAGE SUPERVISOR

The voltage supervisor protects the device, external power MOSFETs and the external microcontroller from damage due to overvoltage or undervoltage of the input supply, V_{DD}.

In the event of an undervoltage condition, $V_{DD} < UVLO_{ACT}$, or overvoltage condition, $V_{DD} > OVLO_{ACT}$, or V_{REG} LDO undervoltage condition, $V_{REG} < VREGUVF_{ACT}$, the gate drivers, charge pump and V_{BOOT} regulator are switched off. The bias generator, communication port, operational amplifiers and the remainder of the motor control unit remain active. The failure state is flagged on the $\overline{FAULT}$ pin and a DE2 status message is sent.

In extreme overvoltage conditions, $V_{DD} > OVSHDN_{ACT}$, the V_{REG} LDO will be shut down as soon as pin OE is set to a low level. The OVSHDN status flag in the STAT0 register will be set and will remain set until the register is read by a host. The DE2 communications link will be disabled together with the V_{REG} LDO. No Fault message will be sent to the host because the device must shut down immediately to prevent high-voltage damage. The V_{REG} LDO will be re-enabled when the V_{DD} supply voltage drops below the overvoltage lockout value, $OVLO_{INACT}$.

In the event of a severe undervoltage condition, $V_{DD} < UVSHDN_{ACT}$, the entire device will shut down except for the minimal circuitry required for a Power-on Reset recovery. A UVSHDN Fault will be set. The V_{REG} output will be turned off and pulled low to create a "clean" shutdown of an attached host processor. The undervoltage shutdown condition is a latched state. The state machine will be restarted from the Power-on Reset state when either of the following two conditions are met:

1. V_{DD} power is cycled.
2. V_{DD} rises above $UVLO_{INACT}$ (6.0V).

4.3.2 TEMPERATURE SUPERVISOR

An integrated temperature sensor self-protects the device circuitry. If the temperature rises above the overtemperature shutdown threshold, all device functions are turned off except for those required to send a DE2 Fault message. A Fault will be generated and a DE2 Fault message will be sent. The functions required to send the DE2 Fault message will then be shut down if pin OE is set to a low level. Active operation resumes when the temperature has cooled down below a set hysteresis value and the Fault has been cleared by toggling the OE pin from a logic low to a logic high.

It is desirable to signal the microcontroller with a warning message before the overtemperature threshold is reached. When the Thermal Warning Temperature (T_{WARN}) set point is exceeded, a warning message will be sent to the host microcontroller. The warning message has no effect upon driver operation. The microcontroller may then take appropriate actions to reduce the temperature rise. The method to signal the microcontroller is through the DE2 pin.

4.4 Output Enable (OE)

The Output Enable (OE) pin allows the device outputs to be disabled by external control. The Output Enable pin has three modes of operation.

4.4.1 FAULT CLEARING STATE

The OE pin is used to clear any Faults and re-enable the driver. After toggling the OE pin low-to-high, the system requires a minimum time period to re-enable and start up all of the driver blocks. The start-up time is approximately 35 µs. The maximum pulse time for the high-low-high transition to clear the Faults should be less than 900 µs to prevent the system from transitioning through Standby mode. If the high-low-high transition is longer than 1 ms, the device will start up from the Standby state.

Any Fault status bits that are set will be cleared by the low-to-high transition of the OE pin, if and only if, the Fault condition has ceased to exist. If the Fault condition still exists, the active Fault status bit will remain active. No additional Fault messages will be sent for a Fault that remains active.

4.4.2 STANDBY STATE

Standby state is entered when the OE pin goes low for longer than 1 ms and the SLEEP Configuration bit is inactive. When Standby mode is entered, the following subsystems are disabled:

- High-side gate drives (HSA, HSB, HSC) forced low
- Low-side gate drives (LSA, LSB, LSC) forced low
- V_{BOOT} LDO
- Charge pump
- Operational amplifiers if CFG0[6] = `1` **(MCP8022)**

The V_{REG} LDO, operational amplifiers (if CFG0[6] = `0`) and DE2 communications stay active.

The total current consumption of the device when OE is inactive (device disabled) stays within the “Standby mode input quiescent current” limits specified in the device characteristics table.

4.4.3 SLEEP MODE

Sleep mode is entered when both a `SLEEP` command is sent to the device via DE2 communications and the OE pin is low. The two conditions may occur in any order. The transition to Sleep mode occurs after the last of the two conditions occurs. The SLEEP bit in the CFG0 Configuration register indicates when the device should transition to a low-power mode. The device will operate normally until the OE pin is transitioned low by an external device. At that point in time, the SLEEP bit value determines whether the device transitions to Standby mode or low-power Sleep mode. The supply current (I_{SUP}) during Sleep mode will typically be 5 µA. When Sleep mode is activated, most functions will be shut off, including the V_{REG} LDO. Only the Power-on Reset monitor and minimal state machine will remain active to detect a wake-up event. This indicates that the host processor will be shut down if the host is using the V_{REG} LDO regulator for power. The device will stay in the low-power Sleep mode until either of the following conditions is met:

- The WAKE pin transitions high after being in a low state lasting longer than t_{WAIT_SETUP}
- Power is cycled

The MCP8021/2 devices are not required to retain configuration data while in Sleep mode. When exiting Sleep mode, the host should send a new configuration message to configure the device if the default configuration values are not desired. The same configuration sequence used during power-up may be used when exiting Sleep mode.

When activated, Sleep mode will always be entered regardless of any active Fault. This allows a transition to Sleep mode when the host is powered by the V_{REG} LDO and the regulator is in an unreliable state. The SLEEP bit in the Configuration register will be ignored at power-up until the system has enabled the V_{REG} LDO and the V_{REG} LDO has entered regulation.

4.5 Faults

4.5.1 FAULT PIN OUTPUT ($\overline{FAULT}$)

The $\overline{FAULT}$ pin is used as a Fault indicator. The pin is capable of sinking a minimum of 1 mA of current while maintaining less than 50 mV of voltage across the output. An external pull-up resistor to the logic supply is required.

The open-drain $\overline{FAULT}$ pin transitions low when a Fault occurs. Table 4-1 lists the Faults that activate the $\overline{FAULT}$ signal. Warnings do not activate the $\overline{FAULT}$ signal; Table 4-2 lists the warnings.

4.5.2 FAULT HANDLING SEQUENCE

When a Fault occurs, the following steps will occur in sequence.

1. The gate drive outputs will be immediately turned off.
2. The $\overline{FAULT}$ pin output will go low.
3. A message will be sent via the DE2 communications link if, and only if, the Fault is not a V_{DD} overvoltage shutdown ($OVSHDN_{ACT}$).
4. The V_{REG} LDO will be disabled immediately if the Fault is a V_{DD} overvoltage shutdown ($OVSHDN_{ACT}$) or a V_{DD} undervoltage shutdown ($UVSHDN_{ACT}$) Fault.
5. The V_{REG} LDO will be disabled 5 ms after the DE2 message has been sent for an overtemperature shutdown (OT_{SHDN}) Fault.

4.5.3 FAULT INDICATOR

A “FAULT” indicator bit resides in the STAT0 register. The bit is the logical ‘OR’ of all of the Fault bits in the two status registers. Warnings are not included in the FAULT indicator bit.

The FAULT bit will allow the user to read the STAT0 register in order to determine if a Fault is present in the system. If the bit is set, then the user may request the STAT1 message and interrogate the bits of both status messages to determine what Faults exist.

The Faults that are logically OR’d together to generate the FAULT bit are as follows:

- STAT0:OTPF
- STAT0:UVLOF
- STAT0:OVLOF
- STAT1:REGUVF
- STAT1:XUVLOF
- STAT1:XOCPF

TABLE 4-1: FAULTS

Fault	DE2 Message
Fault Active (‘OR’ of all Faults)	0x85 0x01
Overtemperature	0x85 0x04
V_{DD} Input Undervoltage	0x85 0x08
V_{DD} Input Overvoltage	0x85 0x10
V_{REG} Output Undervoltage	0x86 0x01
External MOSFET Undervoltage Lockout	0x86 0x04
External MOSFET Overcurrent Detection	0x86 0x08

TABLE 4-2: WARNINGS

Fault	DE2 Message
Temperature Warning	0x85 0x02

4.5.4 POWER CONTROL STATUS (PCON)

The PCON[2:0] (STAT0[7:5]) bits are power control status bits that may be used to determine the cause of a shutdown. They are not Fault latches. The V_{DD} overvoltage shutdown Fault is an internally latched Fault that does not have a latched Fault bit in the STAT0 or STAT1 register. That is because the device will be shut down immediately upon entering the overvoltage Fault condition. When power is back within the device operating range, and the V_{REG} supply is re-enabled, the host will be able to read the STAT0 register to determine the reason for a power cycle. The PCON power status bits will contain the cause of the power cycle. Table 4-3 lists the power status register bits in the STAT0 register.

TABLE 4-3: POWER STATUS

PCON Status Bits [7:5]	DE2 Message
Overtemperature Shutdown (OTSHDN) Occurred	0x85 0xA0
V_{DD} Overvoltage Shutdown (OVSHDN) Occurred	0x85 0x80
Sleep Occurred	0x85 0x60
V_{DD} Undervoltage Shutdown (UVSHDN) Occurred	0x85 0x40
Power-on Reset (POR) Occurred	0x85 0x20
Normal Operation	0x85 0x00

4.5.4.1 Internal Function Block Status

Table 4-4 shows the effects of the OE pin, Faults and the SLEEP bit upon the functional status of the internal blocks of the MCP8021/2.

4.5.4.2 Start-up/$\overline{\text{FAULT}}$ Pin State

During device start-up or Power-on Reset (POR), the $\overline{\text{FAULT}}$ pin will stay active (low) to indicate to the host that the device is initializing. The $\overline{\text{FAULT}}$ pin will stay active until the state machine powers up the V_{REG} LDO and completes the V_{REG} state. After the V_{REG} LDO is powered up, the $\overline{\text{FAULT}}$ pin logic checks the state of all of the latched FAULT bits. If any FAULT bit is still active, the $\overline{\text{FAULT}}$ pin will stay active and remain low.

TABLE 4-4: INTERNAL FUNCTION BLOCK STATUS

System State	Fault	Conditions	Sleep Latch	V_{REG} LDO	V_{BOOT} LDO	Motor Drivers	DE2	Op Amps (MCP8022)	Internal UVLO, OVLO, OTP
Sleep		OE = 0, SLEEP = 1	W	—	—	—	—	—	—
Standby		OE = 0, SLEEP = 0	—	A	—	—	A	C	A
Operating		OE = 1, $\overline{FAULT}$ = 1	—	A	A	A	A	A	A
Faults $\overline{FAULT}$ = 0	Driver OTPF	T_J Temperature > +160°C	—	—	—	—	D	—	A
	V_{DD}UVLO	$V_{DD} \leq UVLO_{INACT}$	—	A	—	—	A	A	A
	V_{DD}UVSHDN	$V_{DD} \leq UVSHDN_{INACT}$	—	-	—	—	E	-	—
	V_{DD}OVLO	$V_{DD} \geq OVLO_{INACT}$	—	A	—	—	A	A	A
	V_{DD}OVSHDN	$V_{DD} \geq OVSHDN_{INACT}$	—	-	—	—	—	—	A
	V_{REG} LDO UVF	$V_{REG} \leq$ 88% V_{REG}	—	A	—	—	A	A	A
	MOSFET UVLO	$V_{HS[A:C]} < V_{DUVLO}$ $V_{LS[A:C]} < V_{DUVLO}$	—	A	A	—	A	A	A
	MOSFET OCPF	$V_{Drain\ Source}$ > EXTOC[1:0] setting	—	A	A	—	A	A	A
Warnings $\overline{FAULT}$ = 1	Driver temperature	T_J Temperature > 72% T_{SD_MIN} (+115°C for +160°C driver OTP)	—	A	A	A	A	A	A
Power Status	Configuration lost if Power-on Reset, wake from Sleep or recover from V_{DD} undervoltage shutdown occurred	Set at initial power-up, when $V_{DD} < UVSHDN_{ACT}$ or when waking from Sleep	—	A	A	A	A	A	A

Legend: — = Inactive (Off); A = Active (On); C = Configurable; D = Inactive (Off) 5 ms after sent Fault message; E = Inactive (Off); R = Receiver Only; W = Wake-up (from Sleep); OCPF = Overcurrent Protection; OTPF = Overtemperature Protection; UVLO = Undervoltage Lockout; OVLO = Overvoltage Lockout; UVF = Undervoltage Fault; UVSHDN = Undervoltage Shutdown; OVSHDN = Overvoltage Shutdown

4.6 Motor Control Unit

The motor control unit is comprised of the following:

- External Drive for a 3-Phase Bridge with NMOS/NMOS MOSFET Pairs
- MOSFET Driver Undervoltage Lockout
- External MOSFET Short-Circuit Current
- $\overline{\text{FAULT}}$ Pin Output
- Cross Conduction Protection
- Programmable Dead Time
- Programmable Blanking Time
- Three General Purpose Operational Amplifiers **(MCP8022)**

4.6.1 EXTERNAL DRIVE FOR A 3-PHASE BRIDGE WITH NMOS/NMOS MOSFET PAIRS

Each motor phase is driven with external NMOS/NMOS MOSFET pairs. These are controlled by a low-side and a high-side gate driver. The gate drivers are controlled by the digital input pins, PWM[A:C]H/L. A logic high turns the associated gate driver on and a logic low turns the associated gate driver off. The PWM[A:C]H/L digital inputs are equipped with internal pull-down resistors.

The low-side gate drivers are biased by the V_{BOOT} regulator output, referenced to ground. The high-side gate drivers are a floating drive biased by a bootstrap capacitor circuit. The bootstrap capacitor is charged by the V_{BOOT} regulator whenever the accompanying low-side MOSFET is turned on.

The high-side and low-side driver outputs all go to a low state whenever there is a Fault, when OE = `0` for more than 1 ms or when Sleep mode is active, regardless of the PWM[A:C]H/L inputs.

4.6.2 MOSFET GATE DRIVE UNDERVOLTAGE LOCKOUT (UVLO)

The MOSFET gate drive undervoltage lockout Fault detection monitors the available voltage used to drive the external MOSFET gates. The Fault detection is only active while the driver is actively driving the external MOSFET gate. Any time the driver bias voltage is below the gate drive undervoltage lockout threshold (V_{DUVLO}) for a time longer than specified by the t_{DUVLO} parameter, the driver will not turn on when commanded on. A driver Fault will be indicated to the host microcontroller on the $\overline{\text{FAULT}}$ open-drain output pin and also via a DE2 communications `Status_1` message. This is a latched Fault. Clearing the Fault requires either removal of device power or disabling and re-enabling the device via the device Output Enable (OE) input. The EXTUVLO bit in the CFG0 register is used to enable or disable the driver undervoltage lockout feature. This protection feature prevents the external MOSFETs from being controlled with a gate voltage not suitable to fully enhance the device.

4.6.3 EXTERNAL MOSFET SHORT-CIRCUIT CURRENT

Short-circuit protection monitors the voltage across the external MOSFETs during an on condition. The high-side driver voltage is measured from V_{DD} to PH[A:C]. The low-side driver voltage is measured from PH[A:C] to ground. If a monitored voltage rises above a user-configurable threshold after the driver HS[A:C] or LS[A:C] output voltage has been driven high, all drivers will be turned off. A driver Fault will be indicated to the host microcontroller on the open-drain $\overline{\text{FAULT}}$ output pin and also via a DE2 communications `Status_1` message. This is a latched Fault. Clearing the Fault requires either removal of device power or toggling the OE input pin low-to-high. This protection feature helps detect internal motor failures, such as winding to case shorts.

Note:	The driver short-circuit protection is dependent on application parameters. A configuration message is provided for a set number of threshold levels. The MOSFET gate drive UVLO and short-circuit protection features have the option to be disabled.

The short-circuit voltage may be set via a DE2 `Set_Cfg_0` message. The EXTOC[1:0] bits of the CFG0 register are used to select the voltage level for the short-circuit comparison. If a monitored voltage differential between V_{DD} and PH[A:C], or between PH[A:C] and P_{GND}, exceeds the selected voltage level when the MOSFET gate drive is active, a Fault will be triggered. The selectable voltage levels are 250 mV, 500 mV, 750 mV and 1000 mV. The EXTSC bit of the CFG0 register is used to enable or disable the MOSFET driver short-circuit detection.

4.6.4 GATE CONTROL LOGIC

The gate control logic enables level shifting of the digital inputs, polarity control and cross conduction protection.

4.6.4.1 Cross Conduction Protection

If both MOSFETs in the same half-bridge are commanded on by the digital PWM inputs, both will be turned off.

4.6.4.2 Programmable Dead Time

The gate control logic employs a break-before-make dead-time delay that is programmable. A configuration message is provided to configure the driver dead time. The programmable dead times range from 250 ns to 2000 ns (default) in 250 ns increments. The dead time allows the PWM inputs to be direct inversions of each other and still allow proper motor operation. The dead time internally modifies the PWMH/L gate drive timing to prevent cross conduction. The DRVDT[2:0] bits of the CFG2 register are used to set the dead-time value.

4.6.4.3 Programmable Blanking Time

A configuration message is provided to configure the driver current limit blanking time. The blanking time allows the driver to ignore any current spikes that may occur when switching the driver outputs. The allowable blanking times are 500 ns, 1 µs, 2 µs and 4 µs (default). The blanking time will start after the dead-time circuitry has timed out. The DRVBL[1:0] bits of the CFG2 register are used to set the blanking time value.

The blanking time also affects the driver undervoltage lockout. The driver undervoltage lockout latches the external MOSFET undervoltage lockout Fault if the undervoltage condition lasts longer than the time specified by the t_{DUVLO} parameter. The t_{DUVLO} parameter takes into account the blanking time if blanking is in progress.

4.6.5 OPERATIONAL AMPLIFIERS (MCP8022)

Three operational amplifiers are present in the MCP8022 device. The operational amplifiers are available for general purpose use by the external system circuitry.

The operational amplifiers are enabled whenever the device is powered and not in Sleep mode. The user may also select the state of the operational amplifiers for Standby mode. When the OE input is set low long enough for the system to enter Standby mode, the operational amplifiers may be enabled or disabled, depending on the value of the CFG0[6] Configuration bit. When the CFG0[6] bit is '0', the operational amplifiers will be enabled during Standby mode. When the CFG0[6] bit is '1', the operational amplifiers will be disabled during Standby mode. This allows the system to reduce power consumption without transitioning to Sleep mode.

The V_{REG} regulator provides the bias supply for the operational amplifiers. The amplifiers are capable of operating when the V_{REG} regulator output voltage drops due to the supply voltage (V_{DD}) dropping. The corresponding amplifier output voltage limits will be reduced accordingly. The output voltage range is capable of providing 200 µA of current from 0.150V to V_{REG} – 0.150V. The input voltage range is -0.3V to 3.3V.

4.7 Motor Control

The commutation loop of a BLDC motor control is a Phase-Locked Loop (PLL), which locks to the rotor's position. Note that this inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. An outer speed loop changes the rotor velocity and the commutation loop locks to the rotor's position to commutate the phases at the correct times.

4.7.1 SIX-STEP SENSORLESS MOTOR CONTROL

Many control algorithms can be implemented with the MCP8021/2 in conjunction with a microcontroller. The following discussion provides a starting point for implementing the MCP8021 or MCP8022 in a sensorless control application of a 3-phase motor. The motor is driven by energizing two windings at a time and sequencing the windings in a six-step per electrical revolution method. This method leaves one winding unenergized at all times. The voltage (Back EMF or BEMF) on that unenergized winding can be monitored to determine the rotor position.

4.7.1.1 Start-up Sequence

When the motor being driven is at rest, the BEMF voltage is equal to zero. The motor needs to be rotating for the BEMF sensor to lock onto the rotor position and commutate the motor. The recommended start-up sequence is to bring the rotor from rest, up to a speed fast enough to allow BEMF sensing. Motor operation is comprised of five modes: Disabled mode, Bootstrap mode, Lock or Align mode, Ramp mode and Run mode. Refer to the commutation state machine in Table 4-5. The order in which the microcontroller steps through the commutation state machine determines the direction that the motor rotates.

4.7.1.2 Disabled Mode (OE = 0)

When the driver output is disabled (OE = 0), all of the MOSFET driver outputs are set low.

4.7.1.3 Bootstrap Mode

The high-side driver obtains the high-side biasing voltage from the V_{BOOT} LDO, bootstrap diode and bootstrap capacitor. The bootstrap capacitors must first be charged before the high-side drives may be used. The bootstrap capacitors are all charged by activating all three low-side drivers. The active low-side drivers pull their respective phase nodes low, charging the bootstrap capacitors to the V_{BOOT} LDO voltage. The three low-side drivers should be active for at least 1.2 ms per 1 µF of bootstrap capacitance. This assumes a 12V voltage change and 30 mA (10 mA per phase) of current coming from the V_{BOOT} LDO.

4.7.1.4 Lock Mode

Before the motor can be started, the rotor should be in a known position. In Lock mode, the microcontroller drives Phase B low and Phases A and C high. This aligns the rotor 30 electrical degrees before the center of the first commutation state. Lock mode must last long enough to allow the motor and its load to settle into this position.

4.7.1.5 Ramp Mode

At the end of Lock mode, Ramp mode is entered. In Ramp mode, the microcontroller steps through the commutation state machine, increasing the step rate linearly, until a minimum speed is reached that will result in a usable BEMF voltage. Ramp mode is an open-loop commutation. No knowledge of the rotor position is used.

4.7.1.6 Run Mode

At the end of Ramp mode, Run mode is entered. In Run mode, the Back EMF sensor is enabled and commutation is now under the control of the Phase-Locked Loop. Motor speed can be regulated by an outer speed control loop.

TABLE 4-5: COMMUTATION STATE MACHINE

State	Outputs						BEMF Phase
	HSA	HSB	HSC	LSA	LSB	LSC	
OE = 0	OFF	OFF	OFF	OFF	OFF	OFF	N/A
BOOTSTRAP	OFF	OFF	OFF	ON	ON	ON	N/A
LOCK	ON	OFF	ON	OFF	ON	OFF	N/A
1	ON	OFF	OFF	OFF	OFF	ON	Phase B
2	OFF	ON	OFF	OFF	OFF	ON	Phase A
3	OFF	ON	OFF	ON	OFF	OFF	Phase C
4	OFF	OFF	ON	ON	OFF	OFF	Phase B
5	OFF	OFF	ON	OFF	ON	OFF	Phase A
6	ON	OFF	OFF	OFF	ON	OFF	Phase C

4.7.1.7 PWM Speed Control

The inner commutation loop is a Phase-Locked Loop, which locks to the rotor's position. This inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. The outer speed loop changes the rotor velocity and the inner commutation loop locks to the rotor's position to commutate the phase at the correct times.

The outer speed loop pulse width modulates the motor drive inverter to produce the desired wave shape and voltage at the motor. The inductance of the motor then integrates this PWM pattern to produce the desired average current, thus controlling the desired torque and speed of the motor. For a trapezoidal BLDC motor drive with six-step commutation, the PWM is used to generate the average voltage to produce the desired motor current and motor speed.

There are two basic methods to PWM the inverter switches. The first method returns the reactive energy in the motor inductance to the source by reversing the voltage on the motor winding during the current decay period. This method is referred to as fast decay or chop-chop. The second method circulates the reactive current in the motor with minimal voltage applied to the inductance. This method is referred to as slow decay or chop-coast.

The preferred control method employs a chop-chop PWM for any situations where the motor is being accelerated, either positively or negatively. For improved efficiency, chop-coast PWM is employed during steady-state conditions. The chop-chop speed loop is implemented by hysteretic control, fixed off-time control or Average Current mode control of the motor current. This makes for a very robust controller, since the motor current is always in instantaneous control. The motor speed presented to the chop-chop loop is reduced by approximately 9%. A fixed frequency PWM that only modulates the high-side switches implements the chop-coast loop. The chop-coast loop is presented with the full motor speed, so if it is able to control the speed, the chop-chop loop will never be satisfied and will remain saturated. The chop-chop remains able to assume full control if the motor torque is exceeded, either through a load change or a change in speed that produces acceleration torque. The chop-coast loop will remain saturated, with the chop-chop loop in full control, during start-up and acceleration to full speed. The bandwidth of the chop-coast loop is set to be slower than the chop-chop loop so that any transients will be handled by the chop-chop loop and the chop-coast loop will only be active in steady-state operation.

4.8 DE2 Communication Port

A half-duplex 9600 baud UART interface is available to communicate with an external host. The port is used to configure the MCP8021/2 and also for status and Fault messages.

4.8.1 COMMUNICATIONS INTERFACE

A single wire, half-duplex, 9600 baud, 8-bit bidirectional communications interface is implemented using the open-drain DE2 pin. The interface consists of eight data bits, one Stop bit and one Start bit. The implementation of the interface is described in the following sections.

The DE2 interface is an open-drain interface. The open-drain output is capable of sinking a minimum of 1 mA of current while maintaining less than 50 mV at the output.

A 5K resistor should typically be used between the host transmit pin and the MCP8021/2 DE2 pin to allow the MCP8021/2 to drive the DE2 line low when the host TX pin is at an active-high level.

The auto-baud frequency is temperature-dependent, as illustrated in Figure 2-5. To establish proper DE2 communication, it is recommended to synchronize the host frequency by proceeding the auto-baud function alternatively, as described in **Section 4.8.5 "Auto-Baud Function"**. The time from receiving the last bit of a command message to sending the first bit of the response message ranges from t_{DE2_RSP} to t_{DE2_WAIT}, corresponding to 0 µs to 3.125 ms. The host should refrain from sending additional messages until the previously requested message has been received in order to prevent overwriting the driver response message.

4.8.2 PACKET FORMAT

Every internal driver status change will cause the driver to send a message to the microcontroller. The interface uses a standard UART baud rate of 9600 bits per second.

In the DE2 protocol, the transmitter and the receiver do not share a clock signal. A clock signal does not emanate from one transmitter to the other receiver. Due to this reason, the protocol is asynchronous. The protocol uses only one line to communicate, so the transmit/receive packet must be done in Half-Duplex mode. A new transmit message is allowed only when a complete packet has been transmitted and responded to.

The host must listen to the DE2 line in order to check for contentions. In case of contention, the host must release the line and wait for at least three packet length times before initiating a new transfer.

Figure 4-4 illustrates a basic DE2 data packet.

4.8.3 PACKET TIMING

While no data are being transmitted, a logic '1' must be placed on the open-drain DE2 line by an external pull-up resistor. A data packet is composed of one Start bit, which is always a logic '0', followed by eight data bits and a Stop bit. The Stop bit must always be a logic '1'. It takes ten bits to transmit a byte of data.

The device detects the Start bit by detecting the transition from logic '1' to logic '0' (note that while the data line is Idle, the logic level is high). Once the Start bit is detected, the next data bit's "center" can be assured to be 24 ticks minus 2 (worst-case synchronizer uncertainty) later. From then on, every next data bit center is 16 clock ticks later. Figure 4-5 illustrates this point.

4.8.4 MESSAGE HANDLING

The driver will not transition to Sleep mode while a message is being received. If a message reception is in progress before the OE = 0 to Sleep mode transition delay (t_{SLEEP}) times out, the message will be fully received and the contents applied to the Configuration registers if applicable. The SLEEP bit will then be checked and the system enters Sleep mode if the SLEEP bit is still active.

4.8.5 AUTO-BAUD FUNCTION

The MCP8021/2 devices provide an auto-baud feature that allows a host, communicating on the DE2 communications link, to determine the actual baud rate being used by the MCP8021/2 device. The feature allows the host to request a 0x55 byte transmission from the MCP8021/2. The host then determines the MCP8021/2 baud rate and adjusts the host internal Baud Rate Generator (BRG) to match the MCP8021/2 baud rate.

The DE2 pin is used to trigger the auto-baud feature. The host sets the DE2 signal to a logic low for a period of time (auto-baud Break window) that ranges between 1.29 ms and 2.0 ms. The host then releases the DE2 pin back to the host UART control. The host UART then raises the DE2 pin to a logic high value. The MCP8021/2 driver will respond with a standard NACK ('0b00nnnnnn', where 'nnnnnn' are the six Least Significant bits (LSbs) received) if the DE2 link was held low for less than 1.29 ms and the byte was not interpreted as a valid command. The MCP8021/2 driver will ignore the current message if the DE2 link is held low for more than 2.0 ms.

If the driver receives a valid auto-baud request in the allotted time frame, the driver will enter an Auto-Baud state, indicating an auto-baud message has been requested. When the auto-baud function is activated, the DE2 subsystem will disable sending all unsolicited messages to the host. The auto-baud request must not be proceeded before a message was sent by the host after a Power-on Reset.

If the internal Auto-Baud state is set, the driver will wait for a minimum of 0.86 ms and a maximum of 1.19 ms. After the wait time has expired, a 0x55 data byte will be immediately sent on the DE2 link by the driver.

The driver will wait 2.00 ms after sending the 0x55 baud rate data over the DE2 link before transmitting any other messages. The driver will then exit the Auto-Baud state and resume normal DE2 operations. The 2.00 ms wait is needed to allow the host to complete the auto-baud verification and update the host UART Baud Rate Generator.

The MCP8021/2 device will always monitor the DE2 link for a logic low before attempting to transmit.

The MCP8021/2 device will preempt all DE2 communications upon receiving a logic low on the DE2 link which lasts longer than ten bit times at 9600 baud (Break sequence).

The MCP8021/2 device will wait for a period up to 2 ms for the DE2 link to change to a logic high state after the initial detection of a logic low on the DE2 link. If the DE2 link fails to rise to a logic high level within 2 ms of the initial logic low level, the auto-baud message will be canceled and no message will be sent. The auto-baud function will then be complete.

The driver will send any pending unsolicited messages after the auto-baud function has finished.

4.8.6 MESSAGING INTERFACE

A command byte will always have the Most Significant bit (MSb) 7 set to '1'. Bits 6 and 5 are reserved for future use and should be set to '0'. Bits[4:0] are used for commands. That allows for 32 possible commands.

4.8.6.1 Host to MCP8021/2

Messages sent from the host to the MCP8021/2 devices consist of either one or two 8-bit bytes. The first byte transmitted is the command byte. The second byte transmitted, if required, is the data for the command.

If a multibyte command is sent to the MCP8021/2 devices and no second byte is received by the MCP8021/2 devices, then a "Command Not Acknowledged" message will be sent back to the host after. The host must start sending the 2nd byte of a two-byte command within 1 ms of completion of the first byte to prevent a NACK message. Once the second byte Start bit is received, the MCP8021/2 internal receiver logic will handle the reception of the data byte. If the data byte Stop bit is not received within the expected reception time for the last received bit, the MCP8021/2 will respond with a NACK message.

4.8.6.2 MCP8021/2 to Host

A solicited response byte from the MCP8021/2 devices will always echo the command byte with bit 7 set to '0' (response) and with bit 6 set to '1' for Acknowledged (ACK) or '0' for Not Acknowledged (NACK). The second byte, if required, will be the data for the host command. Any command that causes an error or is not supported will receive a NACK response.

The MCP8021/2 may send unsolicited command messages to the host controller. All messages to the host controller do not require a response from the host controller.

4.8.7 MESSAGES

4.8.7.1 SET_CFG_0

There is a SET_CFG_0 message that is sent by the host to the MCP8021/2 devices to configure the devices. The SET_CFG_0 message may be sent to the devices at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_0 message. The SET_CFG_0 message format is indicated in Table 4-6. The response is indicated in Table 4-7.

4.8.7.2 GET_CFG_0

There is a GET_CFG_0 message that is sent by the host to the MCP8021/2 devices to retrieve the device Configuration register. The GET_CFG_0 message format is indicated in Table 4-6. The response is indicated in Table 4-7.

4.8.7.3 STATUS_0 and STATUS_1

There is a STATUS_0 and STATUS_1 message that is sent by the host to the MCP8021/2 devices to retrieve the device STAT0 and STAT1 registers. Unsolicited STATUS_0 and STATUS_1 messages may also be sent to the host by the MCP8021/2 devices to inform the host of status changes. The unsolicited STATUS_0 and STATUS_1 messages will only be sent when a status bit changes to an active state. The STATUS_0 and STATUS_1 message format is indicated in Table 4-6. The response is indicated in Table 4-7.

When a STATUS_0 or STATUS_1 message is sent to the host in response to a new Fault becoming active, the FAULT bit will be cleared, either by the host issuing a STATUS_0 or STATUS_1 request message, or by the host toggling the OE pin low then high. The FAULT bit will stay active and not be cleared if the Fault condition still exists at the time the host attempted to clear the Fault.

The PCON bits of the STAT0 register will be set every time the device restarts due to various events (see Table 4-3). When the driver resumes operation, a single unsolicited STATUS_0 message will be sent to the host indicating a Reset has occurred. The message will be sent five milliseconds (5 ms) after the V_{REG} LDO has reached its active state. The host should check the PCON bits to determine the cause of the power cycle. In all cases, the configuration data may have been lost and should be re-sent to the driver. The PCON flags are reset by a host STATUS_0 request message. If the host misses the unsolicited STATUS_0 message at start-up, the host may manually request the status by sending a STATUS_0 message to the driver. The PCON bits of the STAT0 register will contain the source of the Power-on Reset until the STAT0 register is requested by the host.

4.8.7.4 SET_CFG_2

There is a SET_CFG_2 message that is sent by the host to the MCP8021/2 devices to configure the driver current limit blanking time. The SET_CFG_2 message may be sent to the devices at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_2 message. The SET_CFG_2 message format is indicated in Table 4-6. The response is indicated in Table 4-7.

4.8.7.5 GET_CFG_2

There is a GET_CFG_2 message that is sent by the host to the MCP8021/2 devices to retrieve the device Configuration Register #2. The GET_CFG_2 message format is indicated in Table 4-6. The response is indicated in Table 4-7.

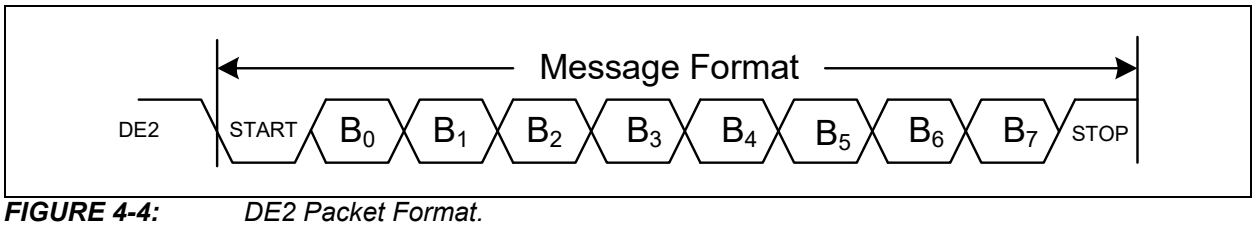


FIGURE 4-4: *DE2 Packet Format.*

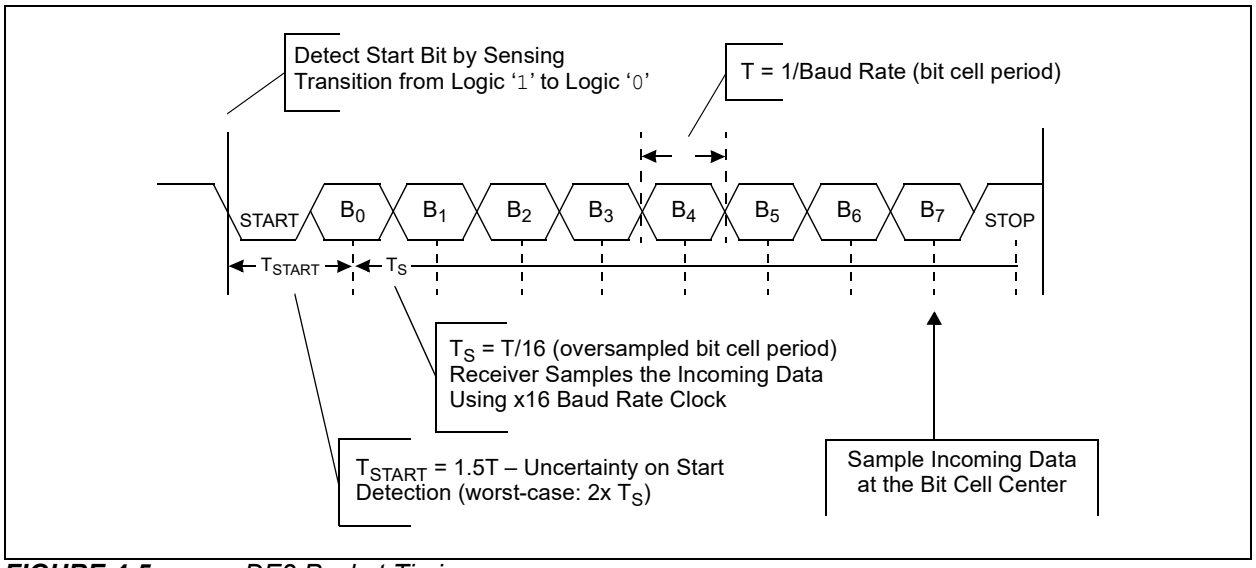


FIGURE 4-5: *DE2 Packet Timing.*

TABLE 4-6: DE2 COMMUNICATION COMMANDS FROM HOST TO MCP8021/2

Command	Byte	Bit	Value	Description
SET_CFG_0	1		10000001 (81h)	Set Configuration Register 0
	2	7	0	Reserved
		6	0	Reserved **(MCP8021)**
			0	Enable operational amplifiers in Standby mode (default) **(MCP8022)**
			1	Disable operational amplifiers in Standby mode **(MCP8022)**
		5	0	System enters Standby mode when OE = 0, SLEEP = 0 for more than 1 ms
			1	System enters Sleep mode when OE = 0, SLEEP = 1 for more than 1 ms
		4	0	Reserved
		3	0	Enable external MOSFET undervoltage lockout (default)
			1	Disable external MOSFET undervoltage lockout
		2	0	Enable external MOSFET short-circuit detection (default)
			1	Disable external MOSFET short-circuit detection
		1:0	00	Set external MOSFET overcurrent limit to 0.250V (default)
			01	Set external MOSFET overcurrent limit to 0.500V
			10	Set external MOSFET overcurrent limit to 0.750V
			11	Set external MOSFET overcurrent limit to 1.000V
GET_CFG_0	1		10000010 (82h)	Get Configuration Register 0
STATUS_0	1		10000101 (85h)	Get Status Register 0
STATUS_1	1		10000110 (86h)	Get Status Register 1
SET_CFG_2	1		10000111 (87h)	Set Configuration Register 2
	2	7:5	00h	Reserved
		4:2	—	Driver dead time (for PWMH /PWML inputs)
			000	2000 ns (default)
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	—	Driver blanking time (ignore switching current spikes)
			00	4 µs (default)
			01	2 µs
			10	1 µs
			11	500 ns
GET_CFG_2	1		10001000 (88h)	Get Configuration Register 2
GET_REV_ID	1		10010000 (90h)	Get device hardware revision

TABLE 4-7: DE2 COMMUNICATION MESSAGES FROM MCP8021/2 TO HOST

MESSAGE	BYTE	BIT	VALUE	DESCRIPTION
SET_CFG_0	1	7:0	00000001 (01h)	Command not Acknowledged (response)
			01000001 (41h)	Command Acknowledged (response)
	2	7	0	Reserved
		6	0	Reserved **(MCP8021)**
			0	Operational amplifiers enabled in Standby mode (default) **(MCP8022)**
			1	Operational amplifiers disabled in Standby mode **(MCP8022)**
		5	0	System enters Standby mode when OE = 0, SLEEP = 0 for more than 1 ms
			1	System enters Sleep mode when OE = 0, SLEEP = 1 for more than 1 ms
		4	0	Reserved
		3	0	External MOSFET undervoltage lockout enabled (default)
			1	External MOSFET undervoltage lockout disabled
		2	0	External MOSFET short-circuit detection enabled (default)
			1	External MOSFET short-circuit detection disabled
		1:0	00	0.250V external MOSFET overcurrent limit (default)
			01	0.500V external MOSFET overcurrent limit
			10	0.750V external MOSFET overcurrent limit
			11	1.000V external MOSFET overcurrent limit
GET_CFG_0	1	7:0	00000010 (02h)	Command not Acknowledged (response)
			01000010 (42h)	Command Acknowledged (response)
	2	7	0	Reserved
		6	0	Reserved **(MCP8021)**
			0	Operational amplifiers enabled in Standby mode **(MCP8022)**
			1	Operational amplifiers disabled in Standby mode **(MCP8022)**
		5	0	System enters Standby mode when OE = 0, SLEEP = 0 for more than 1 ms
			1	System enters Sleep mode when OE = 0, SLEEP = 1 for more than 1 ms
		4	0	Reserved
		3	0	External MOSFET undervoltage lockout enabled
			1	External MOSFET undervoltage lockout disabled
		2	0	External MOSFET short-circuit detection enabled
			1	External MOSFET short-circuit detection disabled
		1:0	00	0.250V external MOSFET overcurrent limit
			01	0.500V external MOSFET overcurrent limit
			10	0.750V external MOSFET overcurrent limit
			11	1.000V external MOSFET overcurrent limit

TABLE 4-7: DE2 COMMUNICATION MESSAGES FROM MCP8021/2 TO HOST (CONTINUED)

MESSAGE	BYTE	BIT	VALUE	DESCRIPTION
STATUS_0	1	7:0	00000101 (05h)	Command not Acknowledged (response)
			01000101 (45h)	Command Acknowledged (response)
			10000101 (85h)	Command sent to host (unsolicited)
	2	7:5	101	Overtemperature Shutdown (OTSHDN) occurred
			100	Overvoltage Shutdown (OVSHDN) occurred
			011	Sleep Shutdown (SLEEP) occurred
			010	Undervoltage Shutdown (UVSHDN) occurred
			001	Power-on Reset (POR) occurred
			000	Normal operation
		4	1	Input Overvoltage (OVLOF), V_{DD} > 32V
		3	1	Input Undervoltage (UVLOF), V_{DD} < 5.5V
		2	1	Overtemperature (OTPF), T_J > +160°C
		1	1	Overtemperature Warning (OTPW), T_J > +115°C
		0	0	No Fault condition exists
			1	A Fault condition exists
STATUS_1	1	7:0	00000110 (06h)	Command not Acknowledged (response)
			01000110 (46h)	Command Acknowledged (response)
			10000110 (86h)	Command sent to host (unsolicited)
	2	7:4	0	Reserved
		3	1	External MOSFET Overcurrent (XOCPF) detected
		2	1	External MOSFET Undervoltage Lockout (XUVLOF)
		1	0	Reserved
		0	1	V_{REG} LDO Undervoltage Fault (VREGUVF)
SET_CFG_2	1	7:0	00000111 (07h)	Command not Acknowledged (response)
			01000111 (47h)	Command Acknowledged (response)
	2	7:5	00h	Reserved
		4:2	—	Driver dead time (for PWMH /PWML inputs)
			000	2000 ns (default)
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	—	Driver blanking time (ignore Faults)
			00	4000 ns (default)
			01	2000 ns
			10	1000 ns
			11	500 ns

TABLE 4-7: DE2 COMMUNICATION MESSAGES FROM MCP8021/2 TO HOST (CONTINUED)

MESSAGE	BYTE	BIT	VALUE	DESCRIPTION
GET_CFG_2	1	7:0	00001000 (08h)	Command not Acknowledged (response)
			01001000 (48h)	Command Acknowledged (response)
	2	7:5	00h	Reserved
		4:2	—	Driver dead time (for PWMH /PWML inputs)
			000	2000 ns
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	—	Driver blanking time (ignore Faults)
			00	4000 ns
			01	2000 ns
			10	1000 ns
			11	500 ns
GET_REV_ID	1	7:0	00010000 (10h)	Command not Acknowledged (response)
			01010000 (50h)	Command Acknowledged (response)
	2	7:3	00h	Reserved
		2:0	00h-07h	Device hardware revision

4.9 Register Definitions

REGISTER 4-1: CFG0: CONFIGURATION REGISTER 0

U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	OPAMP(1)	SLEEP	—	EXTUVLO	EXTSC	EXTOC1	EXTOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **OPAMP:** International Operational Amplifier Power-Down **(MCP8022)**(1)
- 1 = Disables operational amplifiers during Standby mode
- 0 = Enables operational amplifiers during Standby mode

bit 5 **SLEEP:** Sleep Mode

Bit may only be changed while in Standby mode.
- 1 = System enters Sleep mode when OE = 0
- 0 = System enters Standby mode when OE = 0

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXTUVLO:** External MOSFET Undervoltage Lockout
- 1 = Disables
- 0 = Enables

bit 2 **EXTSC:** External MOSFET Short-Circuit Detection
- 1 = Disables
- 0 = Enables

bit 1-0 **EXTOC[1:0]:** External MOSFET Overcurrent Limit Value
- 00 = Overcurrent limit set to 0.250V
- 01 = Overcurrent limit set to 0.500V
- 10 = Overcurrent limit set to 0.750V
- 11 = Overcurrent limit set to 1.000V

Note 1: The OPAMP bit has no effect on MCP8021.

REGISTER 4-2: CFG2: CONFIGURATION REGISTER 2

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DRVDT2	DRVDT1	DRVDT0	DRVBL1	DRVBL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **DRVDT[2:0]:** Driver Dead-Time Selection
000 = 2000 ns
001 = 1750 ns
010 = 1500 ns
011 = 1250 ns
100 = 1000 ns
101 = 7500 ns
110 = 500 ns
111 = 250 ns

bit 1-0 **DRVBL[1:0]:** Driver Blanking Time Selection
Bit may only be changed while in Standby mode.
00 = 4000 ns
01 = 2000 ns
10 = 1000 ns
111 = 500 ns

REGISTER 4-3: STAT0: STATUS REGISTER 0

R-0	R-0	R-1	R-0	R-0	R-0	R-0	R-0
PCON2	PCON1	PCON0	OVLOF	UVLOF	OTPF	OTPW	FAULT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **PCON[2:0]:** Power Control Status (configuration lost if non-zero value)
- 101 = Overtemperature Shutdown (OTSHDN) occurred
- 100 = Overvoltage Shutdown (OVSHDN) occurred
- 011 = Sleep (SLEEP) shutdown occurred
- 010 = Undervoltage Shutdown (UVSHDN) occurred
- 001 = Power-on Reset (POR) occurred
- 000 = Normal operation

bit 4 **OVLOF:** Input Overvoltage Lockout Fault
- 1 = V_{DD} input voltage > 32V
- 0 = V_{DD} input voltage < 32V

bit 3 **UVLOF:** Input Undervoltage Fault
- 1 = V_{DD} input voltage < 5.5V
- 0 = V_{DD} input voltage > 5.5V

bit 2 **OTPF:** Overtemperature Protection Fault
- 1 = Device junction temperature is > +160°C
- 0 = Device junction temperature is < +160°C

bit 1 **OTPW:** Overtemperature Protection Warning
- 1 = Device junction temperature is > +115°C
- 0 = Device junction temperature is < +115°C

bit 0 **FAULT:** Fault Status
- 1 = At least one Fault is active
- 0 = No active Faults

REGISTER 4-4: STAT1: STATUS REGISTER 1

U-0	U-0	U-0	U-0	R-0	R-0	U-0	R-0
—	—	—	—	XOCPF	XUVLOF	—	VREGUVF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **XOCPF:** External MOSFET Overcurrent Protection Fault
Only Valid when EXTSC (CFG0[2]) = 0.
1 = External MOSFET V_{DS} > EXTOC[1:0] (CFG0[1:0]) value
0 = External MOSFET V_{DS} < EXTOC[1:0] (CFG0[1:0]) value

bit 2 **XUVLOF:** External MOSFET Gate Drive Undervoltage Fault
Only Valid when EXTUVLO (CFG0[3]) = 0.
1 = HSx output voltage < V_{DUVLO}
0 = HSx output voltage > V_{DUVLO}

bit 1 **Unimplemented:** Read as '0'

bit 0 **VREGUVF:** V_{REG} LDO Undervoltage Fault
1 = V_{REG} LDO output voltage < 88% of target V_{REG}
0 = V_{REG} LDO output voltage > 92% of target V_{REG}

REGISTER 4-5: REV_ID: HARDWARE REVISION ID

U-0	U-0	U-0	U-0	U-0	R-0/1	R-0/1	R-0/1
—	—	—	—	—	REVID2	REVID1	REVID0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **REVID[2:0]:** Device Revision

5.0 APPLICATION INFORMATION

5.1 Component Calculations

5.1.1 CHARGE PUMP CAPACITORS

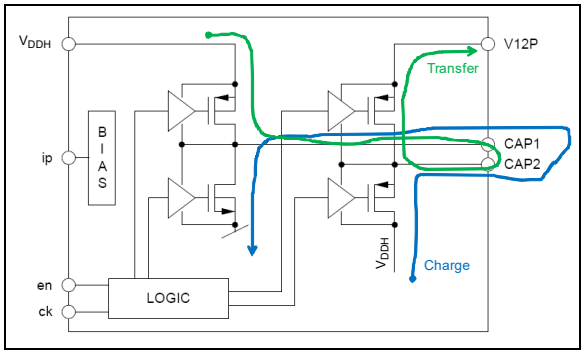


FIGURE 5-1: *Charge Pump.*

Let:

- I_{OUT} = 20 mA
- f_{CP} = 75 kHz (charge/discharge in one cycle)
- 50% duty cycle
- V_{DDH} = 5.5V (worst case)
- R_{DSON} = 7.5Ω (R_{PMOS}), 3.5Ω (R_{NMOS})
- V12P = 2 × V_{DDH} (ideal)
- C_{ESR} = 20 mΩ (ceramic capacitors)
- V_{DROP} = 100 mV (V_{OUT} ripple)
- T_{CHG} = T_{DCHG} = 0.5 × 1/75 kHz = 6.67 µs

5.1.1.1 Flying Capacitor

The flying capacitor should be chosen to charge to a minimum of 95% (3τ) of V_{DDH} within one half of a switching cycle.

- 3 × τ = T_{CHG}
- τ = T_{CHG}/3
- RC = T_{CHG}/3
- C = T_{CHG}/(R × 3)
- C = 6.67 µs/([7.5Ω + 3.5Ω + 0.02Ω] × 3)
- C = 202 nF

Choose a 180 nF capacitor.

5.1.1.2 Charge Pump Output Capacitor

Solve for the charge pump output capacitance, connected between V12P and ground, that will supply the 20 mA load for one switch cycle. The V_{BOOT} LDO pin on the MCP8021/2 is the "V12P" pin referenced in the calculations.

- C = I_{OUT} × dt/dV
- C = I_{OUT} × 13.3 µs/(V_{DROP} + I_{OUT} × C_{ESR})
- C = 20 mA × 13.3 µs/(0.1V + 20 mA × 20 mΩ)
- C ≥ 2.65 µF

For stability reasons, the V_{BOOT} LDO and V_{REG} LDO capacitors must be at least 4.7 µF, so choose: C ≥ 4.7 µF.

5.1.1.3 Charging Path (Flying Capacitor Across CAP1 and CAP2)

- V_{CAP} = V_{DDH} × (1 – $e^{-T/\tau}$)
- V_{CAP} = 5.5V × (1 – $e^{-[6.67\ \mu s/([7.5\Omega + 3.5\Omega + 20\ m\Omega] \times 180\ nF)]}$)

V_{CAP} = 5.31V available for transfer on the first cycle.

5.1.1.4 Transfer Path (Flying and Output Capacitors)

- V12P = V_{DDH} + V_{CAP} – I_{OUT} × dt/C
- V12P = 5.5V + 5.31V – (20 mA × 6.67 µs/180 nF)
- V12P = 10.066V

5.1.1.5 Calculate the Flying Capacitor Voltage Drop in One Cycle While Supplying 20 mA

- dV = I_{OUT} × dt/C
- dV = 20 mA × 6.67 µs/180 nF
- dV = 0.741V @ 20 mA

The second and subsequent transfer cycles will have a higher voltage available for transfer, since the capacitor is not completely depleted with each cycle. V_{CAP} will then be V_{CAP} – dV after the first transfer, plus V_{DDH} – (V_{CAP} – dV) times the RC constant. This repeats for each subsequent cycle, allowing a larger charge pump capacitor to be used if the system will tolerate several charge transfers before requiring full output voltage and current.

Repeating **Section 5.1.1.3 "Charging Path (Flying Capacitor Across CAP1 and CAP2)"** for the second cycle (and subsequent by recalculating for each new value of V_{CAP} after each transfer):

- V_{CAP} = (V_{CAP} – dV) + (V_{DDH} – (V_{CAP} – dV)) (1 – $e^{-T/t}$)
- V_{CAP} = (5.31V – 0.741V) + (5.5V – (5.31V – 0.741V)) × (1 – $e^{-[6.67\ \mu s/([7.5W + 3.5W + 20\ mW] \times 180\ nF)]}$)
- V_{CAP} = 4.567V + 0.934V × 0.96535

V_{CAP} = 5.468V available for transfer on second cycle.

5.1.1.6 Charge Pump Results

The maximum charge pump flying capacitor value is 202 nF to maintain a 95% voltage transfer ratio on the first charge pump cycle. Larger capacitor values may be used, but they will require more cycles to charge to maximum voltage. The minimum required output capacitor value is 2.65 µF to supply 20 mA for 13.3 µs with a 100 mV drop. A larger output capacitor may be used to cover losses due to capacitor tolerance over temperature, capacitor dielectric and PCB losses.

These are approximate calculations. The actual voltages may vary due to incomplete charging or discharging of capacitors per cycle due to load changes. The charge pump calculations assume the charge pump is able to charge up the external boot cap within a few cycles.

5.1.2 BOOTSTRAP CAPACITOR

The high-side driver bootstrap capacitor needs to power the high-side driver and gate for 1/3 of the motor electrical period for a 3-phase BLDC motor operating in Six-Step mode.

Let:

MOSFET Driver Current	=	300 mA
PWM Period	=	50 µs (20 kHz)
Minimum Duty Cycle	=	1% (500 ns)
Maximum Duty Cycle	=	99% (49.5 µs)
V_{IN}	=	12V
Minimum Gate Drive Voltage	=	8V (V_{GS})
Total Gate Charge	=	130 nC (80A MOSFET)
Allowable V_{GS} Drop (V_{DROP})	=	3V
Switch R_{DSON}	=	100 mW
Driver Internal Bias Current	=	20 µA (I_{BIAS})

Solve for the smallest capacitance that can supply:

- 130 nC of charge to the MOSFET gate
- 1 Megohm gate source resistor current
- Driver bias current and switching losses

Q_{MOSFET}	=	130 nC
$Q_{RESISTOR}$	=	$[(V_{GS}/R) \times T_{ON}]$
Q_{DRIVER}	=	$(I_{BIAS} \times T_{ON})$
T_{ON}	=	49.5 µs (99% DC) for worst case
$Q_{RESISTOR}$	=	$Q_{RESISTOR}$
Q_{DRIVER}	=	20 µA × 49.5 µs = 0.99 nC

Sum all of the energy requirements:

- $C = (Q_{MOSFET} + Q_{RESISTOR} + Q_{DRIVER})/V_{DROP}$
- C = (130 nC + 0.594 nC + 0.99 nC)/3V
- C = 43.86 nF

Choose a bootstrap capacitor value that is larger than 43.86 nF.

5.2 Device Protection

5.2.1 MOSFET VOLTAGE SUPPRESSION

When a motor shaft is rotating and power is removed, the magnetism of the motor components will cause the motor to act like a generator. The current that was flowing into the motor will now flow out of the motor. As the motor magnetic field decays, the generator output will also decay. The voltage across the generator terminals will be proportional to the generator current and circuit impedance of the generator circuit. If the power supply is part of the return path for the current and the power supply is disconnected, then the voltage at the generator terminals will increase until the current flows. This voltage increase must be handled externally to the driver. A voltage suppression device may be used to clamp the motor terminal voltage to a level that will not exceed the maximum system operating voltage during the high-voltage transients. A voltage suppressor circuit may be connected from power ground to the motor power supply rail to create a path for the motor current when the supply is disconnected (Figure 5-2). The PCB traces must be capable of carrying the motor current with minimum voltage and temperature rise.

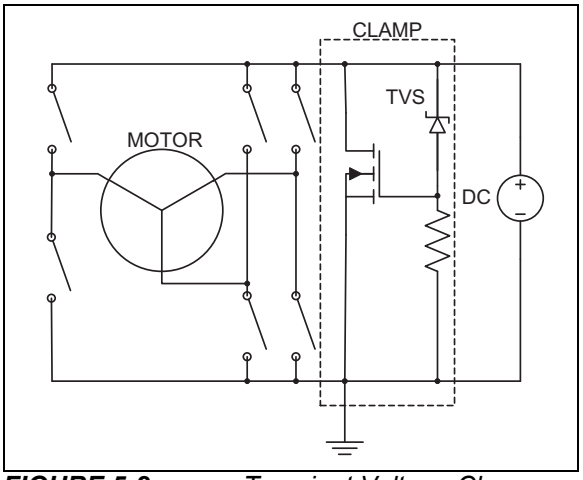


FIGURE 5-2: *Transient Voltage Clamp.*

An additional method is to inactivate the high-side drivers and to activate the low-side drivers. This allows current to flow through the low-side external MOSFETs and prevents the voltage from increasing at the power supply terminals.

5.2.2 BOOTSTRAP VOLTAGE SUPPRESSION

The pins which handle the highest voltage during motor operation are the bootstrap pins (VBx). The bootstrap pin voltage is typically V_{BOOT} (12V) higher than the associated phase voltage. When the high-side MOSFET is conducting, the phase pin voltage is typically at V_{DD} and the bootstrap pin voltage is typically at V_{DD} + 12V. When the phase MOSFETs switch, current induced voltage transients occur on the phase pins. These currents are caused by the MOSFET body diode reverse recovery and MOSFET turn-on/turn-off times. Those induced voltages cause the bootstrap pin voltages to also increase. Depending on the magnitude of the phase pin voltage, the bootstrap pin voltage may exceed the safe operating voltage of the device. The current induced transients may be reduced by slowing down the turn-on and turn-off times of the MOSFETs. The external MOSFETs may be slowed down by adding a 10 to 100 ohm resistor in series with the gate drive. A 3.3 nF to 10 nF ceramic capacitor may be added that connects each MOSFET gate and source terminal. The added capacitance slows down the switching times of the MOSFET while allowing the gate resistance to remain small enough to keep the gate clamped off. The added capacitance also results in a lower slew rate of the phase node and limits the shoot-through current caused by the body diode reverse recovery.

The high-side MOSFETs may also be slowed down by inserting a 10Ω to 25Ω resistor between each bootstrap pin and the associated bootstrap diode capacitor junction. Another 25Ω to 50Ω resistor is then added between the gate drive and the MOSFET gate. This results in a high-side turn-on resistance of 25Ω plus the series gate resistor. The high-side turn-off resistance only consists of the series gate resistance and allows for a faster shut-off time. Care must be taken to make sure the voltage drop across the bootstrap pin resistor does not cause an external MOSFET undervoltage Fault.

When a system motor power supply voltage clamp is not used, 33V or 36V transzorbs may be connected from each bootstrap pin (VBx) to the ground. This will ensure that the bootstrap voltage does not exceed the absolute maximum voltage allowed on the pins. The resistors connected between the bootstrap pins and the bootstrap diode/capacitor junctions, mentioned in the previous paragraph, may also be used in order to limit the transzorb current and reduce the transzorb package size.

5.2.3 FLOATING GATE SUPPRESSION

The gate drive pins may float when the supply voltage is lost or an overvoltage situation shuts down the driver. When an overvoltage condition exists, the driver high-side and low-side outputs are tri-state. Each external MOSFET that is connected to the gate driver should have a gate-to-source resistor to bleed off any charge that may accumulate due to the tri-state. This will help prevent inadvertent turn-on of the MOSFET.

Figure 5-3 shows the location of the overvoltage transzorbs (or equivalent circuits), gate resistors, bootstrap resistors and gate-to-source resistors.

5.2.4 MOSFET BODY DIODE REVERSE RECOVERY SNUBBER

When motor current is flowing through the external MOSFET body diodes and the complimentary MOSFET of the phase pair turns on, the body diode reverse recovery creates a momentary short circuit until the reverse recovery time is complete. When the body diode reverse recovery is complete, the current path is opened, causing the phase node voltage to slew rapidly towards ground or V_{DD} levels. The rapid slew rate may cause an inversion of the gate-to-source voltage on the MOSFET that is turning on and result in that MOSFET turning off.

The fast slew rate may also cause ringing on the phase node and also the sense resistor if the turn-off is too fast.

The first remedy for the low-side turn-off is to slow down the MOSFET gate-to-source turn-off. That causes the R_{DSON} of the low-side MOSFET to gradually increase as the gate voltage drops and the low-side MOSFET slowly turns off. The slow turn-off allows the phase voltage, generated by the motor current flowing through the low-side MOSFET R_{DSON}, to slowly rise towards the positive motor supply level.

The same scenario is also valid for turning on the low-side MOSFET when the high-side MOSFET has just been turned off and current was flowing from the high side into the motor.

The MOSFET body diode reverse recovery situation occurs when the low-side MOSFETs are turned on while the motor current is flowing to the positive source through the high-side MOSFET body diode. The diode reverse recovery time allows a short circuit to exist between the positive supply and the low-side MOSFET drain until the high-side diode is reverse biased and the reverse recovery time has elapsed. The first remedies above should be used to slow the switching speeds of the MOSFETs. Then, a snubber is added to each MOSFET to fine-tune the phase node slew rate and eliminate any further transients. Adding a drain-to-source snubber slows down the slew rate of the phase node and results in a more controlled excursion of the phase node voltage. The snubber consists of a resistor and a capacitor connected in series between the drain and source of the MOSFET. The resistor is chosen to keep the initial snubber voltage below a few volts when peak motor current is flowing through the body diode. The capacitor is then chosen to provide an RC time constant longer than the MOSFET body diode reverse recovery time. A 0.1Ω resistor is typically used, along with a 0.1 µF capacitor to provide an RC of 10 ns.

The power dissipated by the capacitor is calculated by applying Equation 5-1.

EQUATION 5-1: SNUBBER CAPACITOR POWER DISSIPATION

$$P_{DISS} = 2 \times \pi \times f \times C \times V^2 \times Dissipation\ Factor$$

Where:

f = PWM Frequency
C = Capacitance
V = Motor Voltage
$Dissipation\ Factor = 2 \times p \times f \times C \times ESR = ESR/X_C$

The capacitor and resistor form factors are chosen to handle the dissipated power.

5.2.5 MOTOR CURRENT SENSE CIRCUITRY

A sense resistor in series with the bridge ground return provides a current signal for feedback. This resistor should be non-inductive to minimize ringing from high di/dt. Any inductance in the power circuit represents potential problems in the form of additional voltage stress and ringing, as well as increasing switching times. While impractical to eliminate, careful layout and bypassing will minimize these effects. The output stage should be as compact as heat sinking will allow, with wide, short traces carrying all pulsed currents. Each half-bridge should be separately bypassed with a low ESR/ESL capacitor, decoupling it from the rest of the circuit. Some layouts will allow the input filter capacitor to be split into three smaller values and serve double duty as the half-bridge bypass capacitors.

5.2.6 AUTO-BAUD CODE EXAMPLE

Example 5-1 is a dsPIC® DSC code example using the auto-baud function.

EXAMPLE 5-1: dsPIC® AUTO-BAUD EXAMPLE

```
/* create autobaud function using dsPIC built-in BREAK function
   * Fcy = Fosc/2
   * U1BRG_9600 = U1BRG = (Fcy/(16 * Baudrate)) - 1 where default Baudrate = 9600
   * Baudrate = FCY / ((U1BRG + 1) * 16)
   */
   U1MODEbits.ABAUD = 0;                // stop the ABAUD counter
   U1MODEbits.UARTEN = 1;               // enable UART
   U1STAbits.UTXEN = 1;                 // Transmit enabled, UxTX pin controlled by UARTx
   while(U1STAbits.UTXBF);              // Wait for transmit buffer to empty
   while(!U1STAbits.TRMT);              // wait for last byte to finish transmitting
   U1STAbits.UTXBRK = 1;                // Send BREAK command
   U1TXREG = 0x00;                      // Dummy write to start BREAK command
   while (U1STAbits.UTXBRK);            // wait for completion of BREAK sequence
   while (!U1STAbits.TRMT);             // wait for last break bit to transmit
   U1RXREG = 0;                         // reset UART - Required to abort sync
   U1RXREG = 1;                         // enable UART
   __delay_us(100);                     // make sure DE2 link is ready
   U1MODEbits.ABAUD = 1;                // start the ABAUD counter upon receipt of next byte (0x55)
   __delay_ms(5);                       // wait for ABAUD to complete
   if (U1MODEbits.ABAUD) __delay_ms(5);   // wait another 5 ms if ABAUD is not complete
                                        // NewBaudrate = FCY / ((U1BRG + 1) * 16);
                                        // new baudrate
   if (!U1MODEbits.ABAUD)               // verify calculated baud rate is valid.
                                        // If not, use default 9600 baud rate.
   {                                    // verify new baud clock is within limits of U1BRG_9600 +/- 5%
         if ((U1BRG > U1BRG_9600_MINUS_5_PERCENT)  &&
             (U1BRG < U1BRG_9600_PLUS_5_PERCENT))
         {
                                        // success, use new baudrate generator value
   }
         else
         {
                                        // failed, reload default 9600 baud rate clock
             U1BRG = U1BRG_9600;
         }
   }
   else
   {
                                        // Autobaud never completed, reload default 9600 baud rate clock
         U1MODEbits.ABAUD = 0;          // stop the ABAUD counter
         U1BRG = U1BRG_9600;
   }
```

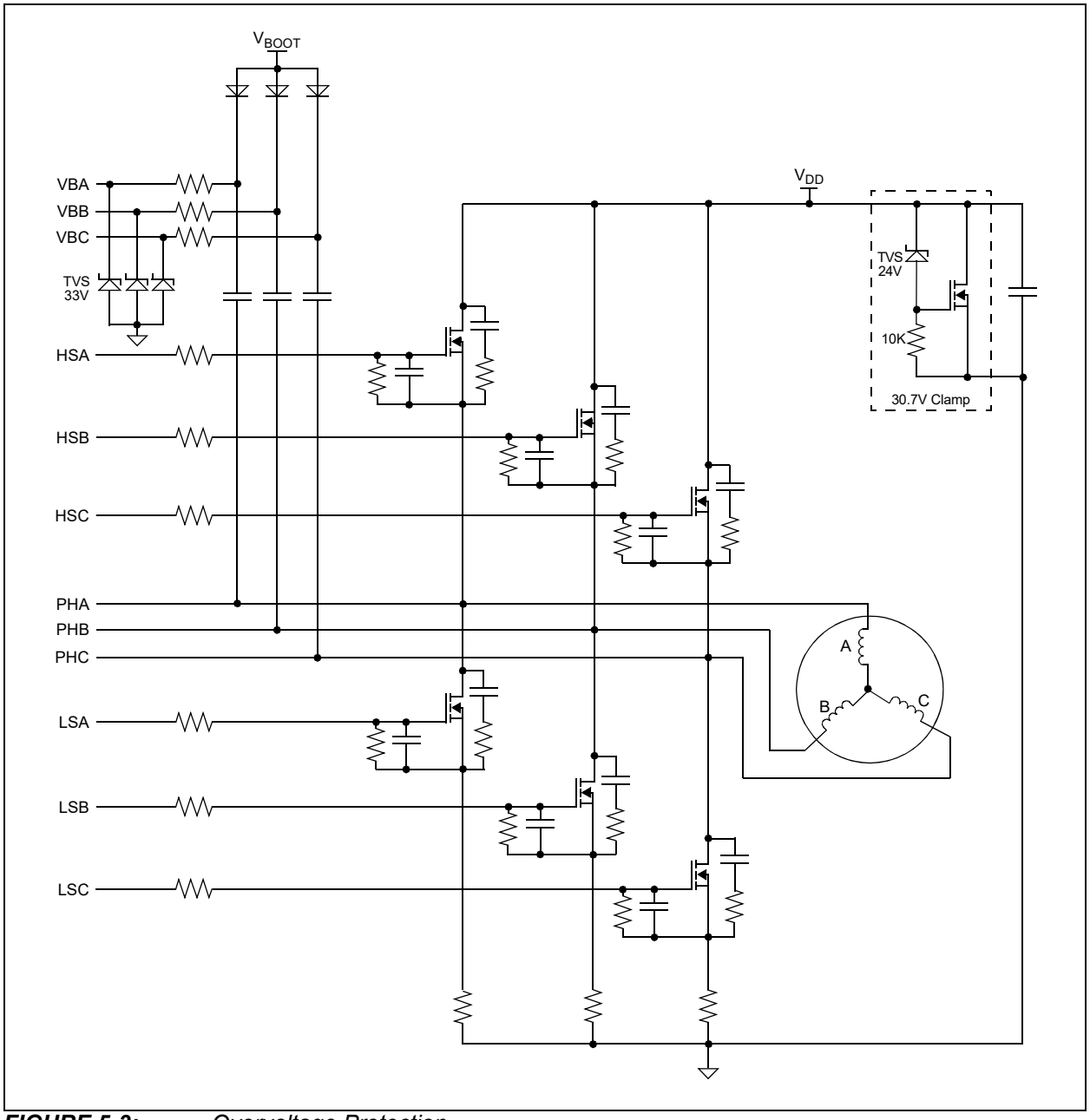


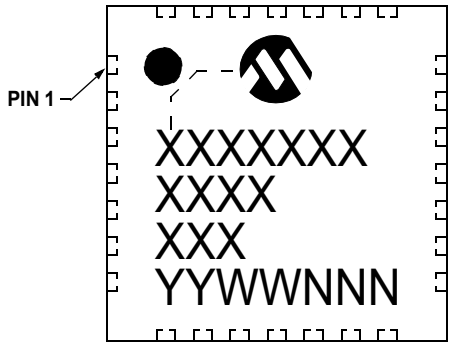
FIGURE 5-3: *Overvoltage Protection.*

6.0 PACKAGE INFORMATION

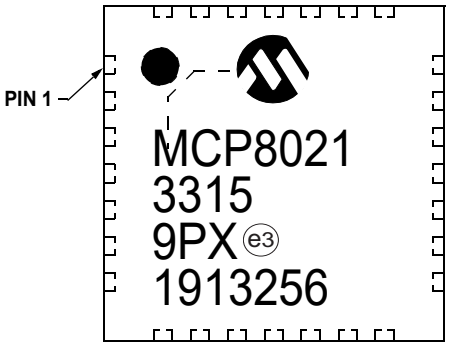
6.1 Package Marking Information

MCP8021

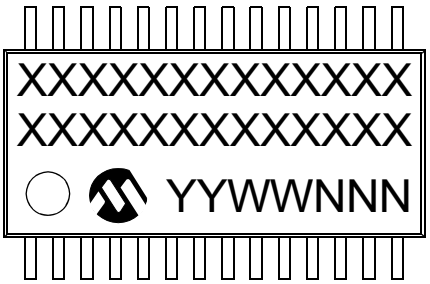
28-Lead VQFN (5x5 mm)



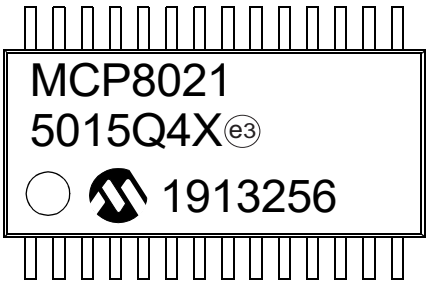
Example



28-Lead TSSOP (4.4 mm)



Example

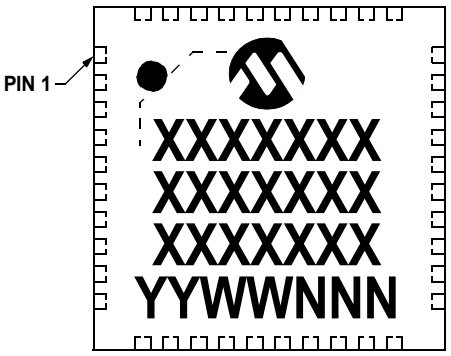


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

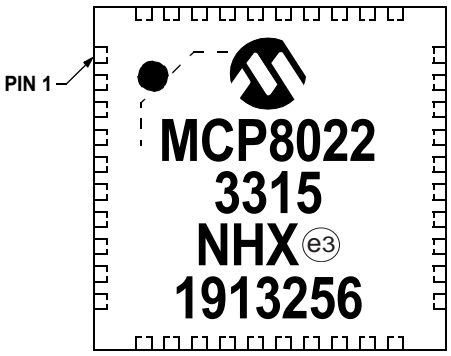
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP8022

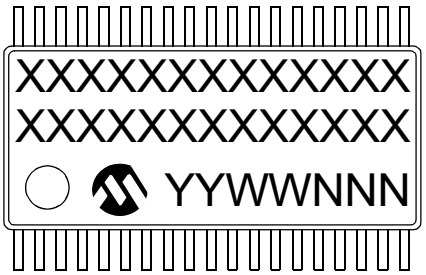
40-Lead VQFN (5x5 mm)



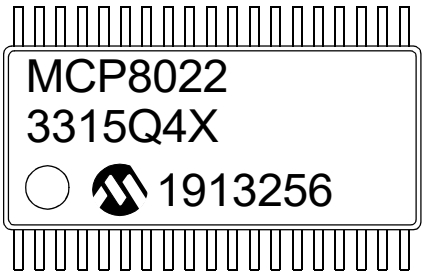
Example



38-Lead TSSOP (4.4 mm)

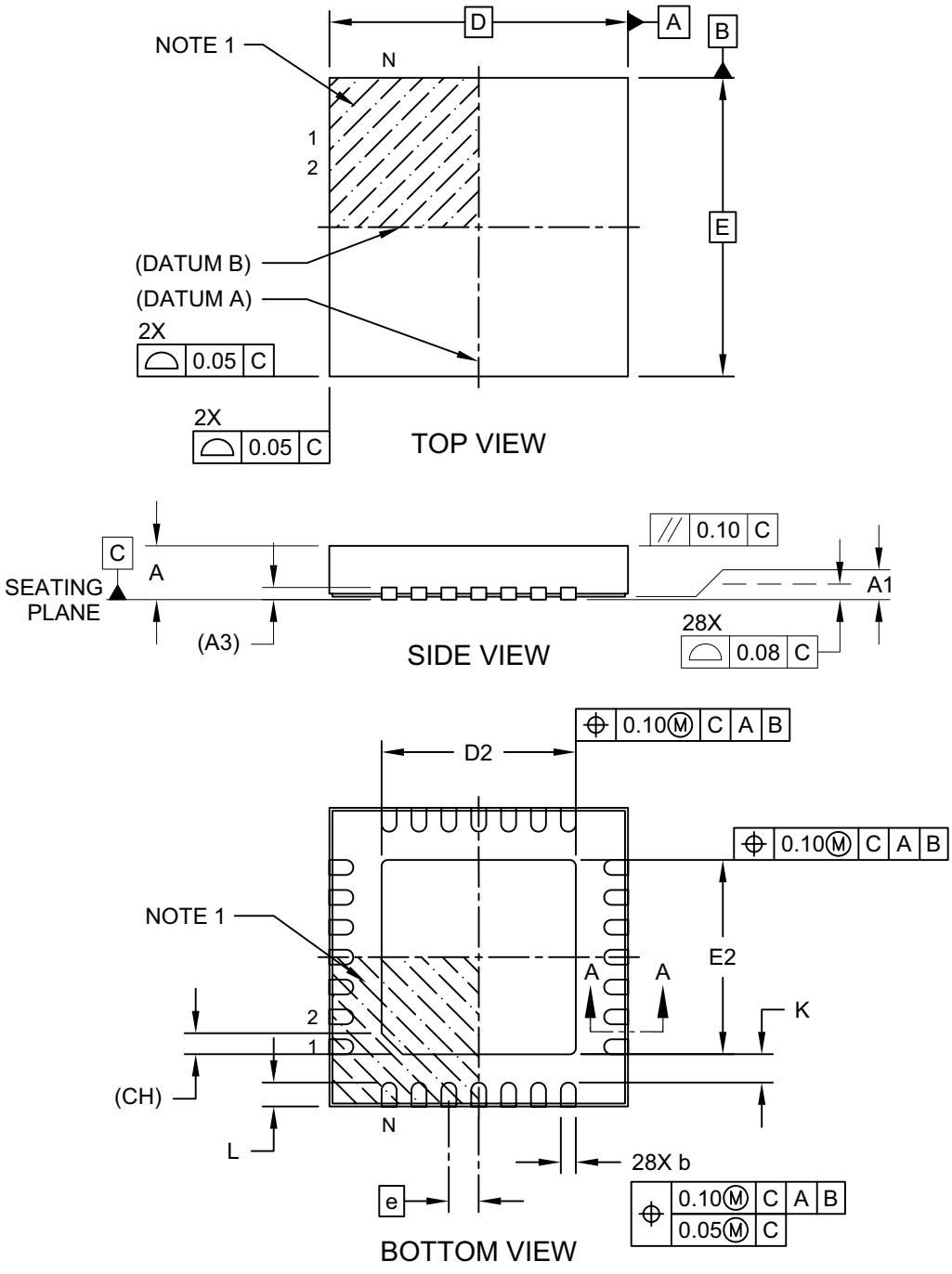


Example



28-Lead Very Thin Plastic Quad Flat, No Lead Package (9PX) - 5x5 mm Body [VQFN] With Stepped Wettable Flanks, 3.25x3.25mm Exposed Pad

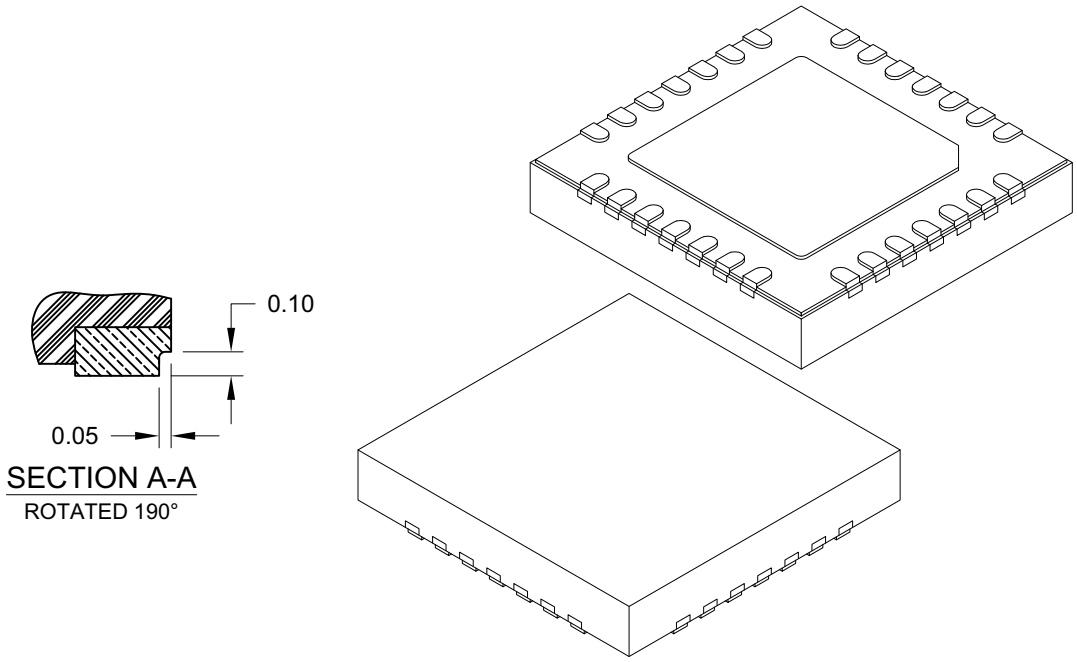
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-426A Sheet 1 of 2

28-Lead Very Thin Plastic Quad Flat, No Lead Package (9PX) - 5x5 mm Body [VQFN] With Stepped Wettable Flanks, 3.25x3.25mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Exposed Pad Chamfer	CH		0.35 REF	

Notes:

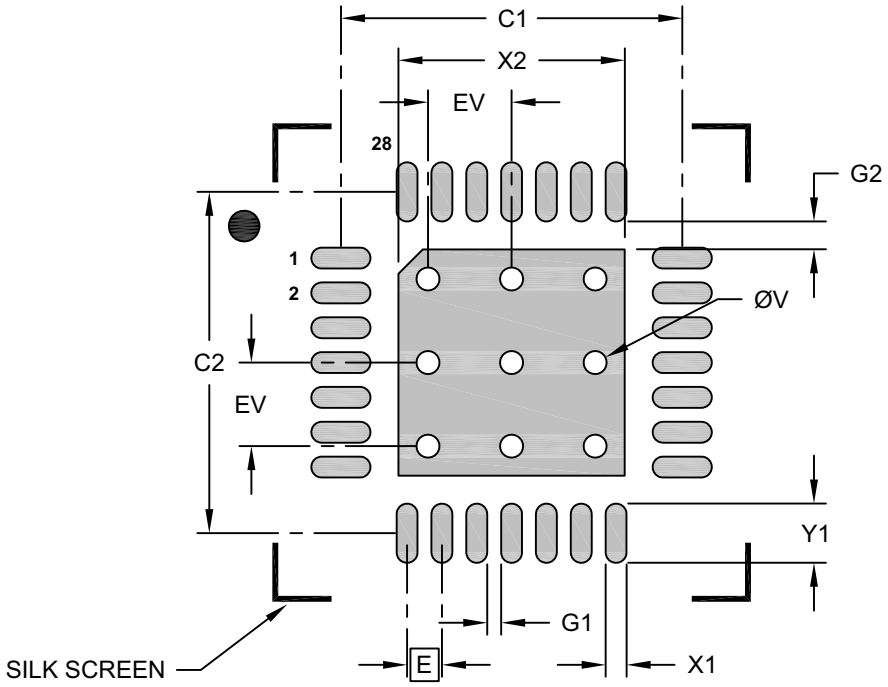
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-426A Sheet 2 of 2

28-Lead Very Thin Plastic Quad Flat, No Lead Package (9PX) - 5x5 mm Body [VQFN] With Stepped Wettable Flanks, 3.25x3.25mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		3.25	
Contact Pad Spacing	C2		3.25	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			0.85
Contact Pad to Contact Pad (X24)	G1	0.20		
Contact Pad to Center Pad (X28)	G2	0.40		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

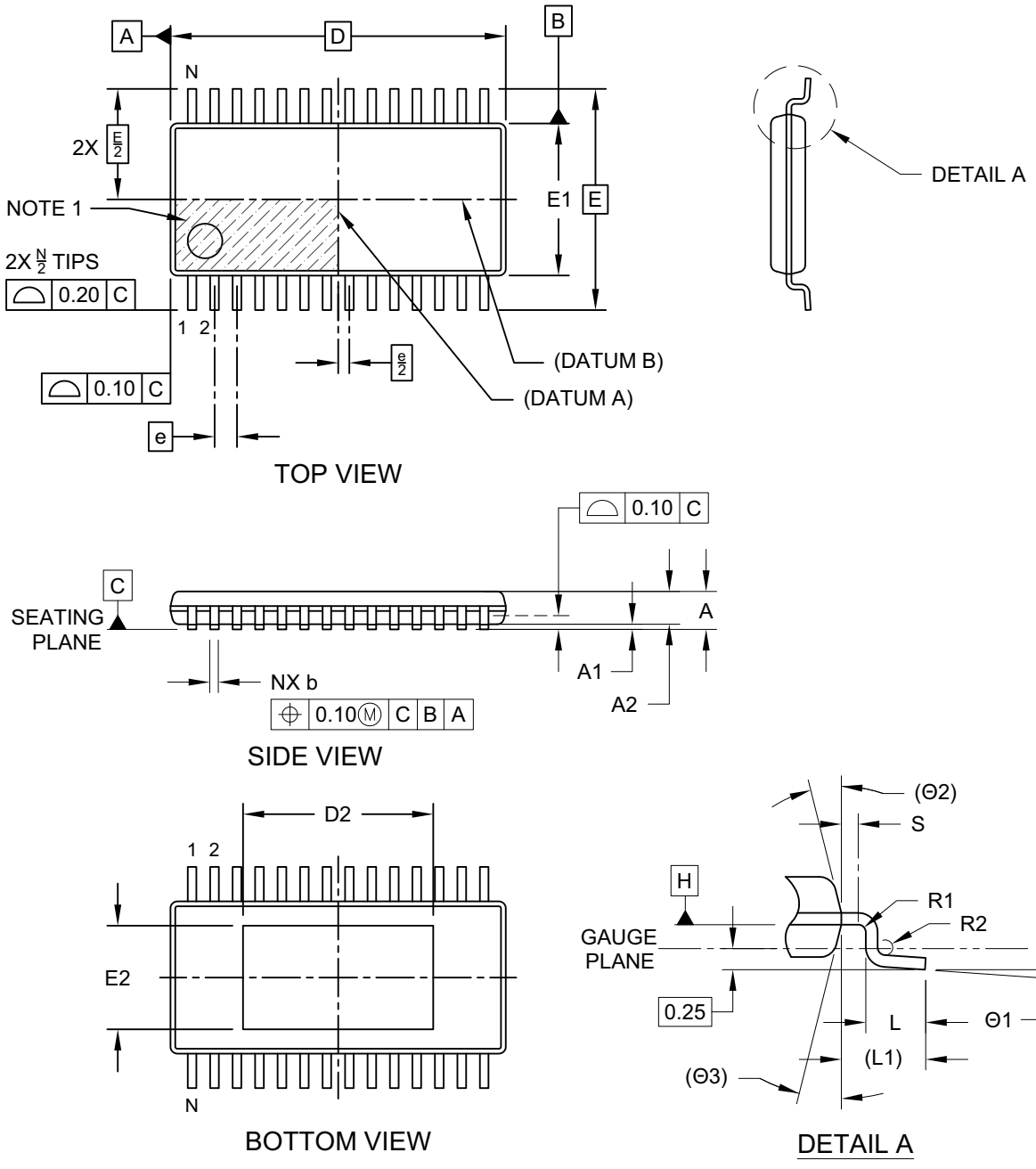
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2426A

28-Lead Thin Shrink Small Outline Package (ST) - 4.4 mm Body [TSSOP] With 5.5x3.0 mm Exposed Pad

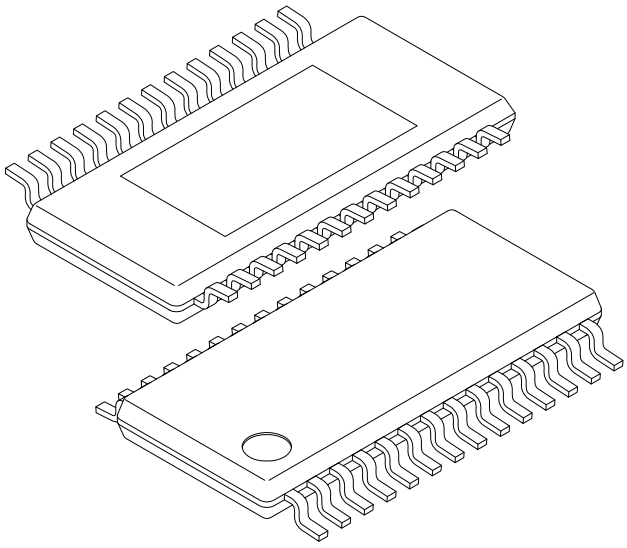
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-055A Sheet 1 of 2

28-Lead Thin Shrink Small Outline Package (ST) - 4.4 mm Body [TSSOP] With 5.5x3.0 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Standoff	A1	0.05	-	0.15
Terminal Thickness	A2	0.85	0.90	0.95
Overall Length	D		9.70 BSC	
Exposed Pad Length	D2	5.40	5.50	5.60
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Exposed Pad Width	E2	2.90	3.00	3.10
Terminal Width	b	0.19	-	0.30
Terminal Length	L	0.50	0.60	0.70
Terminal Shoulder	S	0.20	-	-
Terminal Bend Radius	R1	0.09	-	-
Terminal Bend Radius	R2	0.09	-	-
Terminal Foot Angle	Θ1	0°	-	8°
Mold Draft Angle	Θ2		14° REF	
Mold Draft Angle	Θ3		14° REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

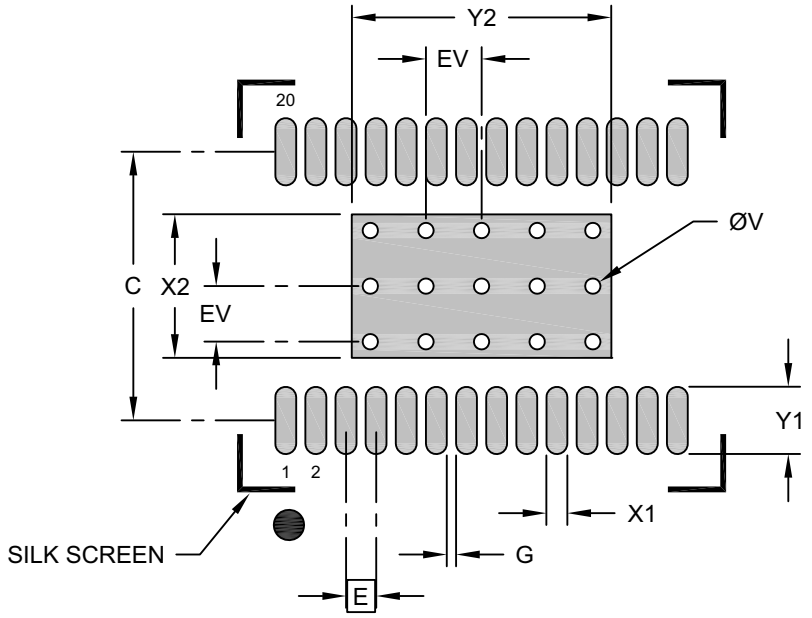
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-055A Sheet 2 of 2

28-Lead Thin Shrink Small Outline Package (ST) - 4.4 mm Body [TSSOP] With 5.5x3.0 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Center Pad Width	X2			3.10
Center Pad Length	Y2			5.60
Contact Pad Spacing	C		5.80	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.45
Contact Pad to Pad (X26)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

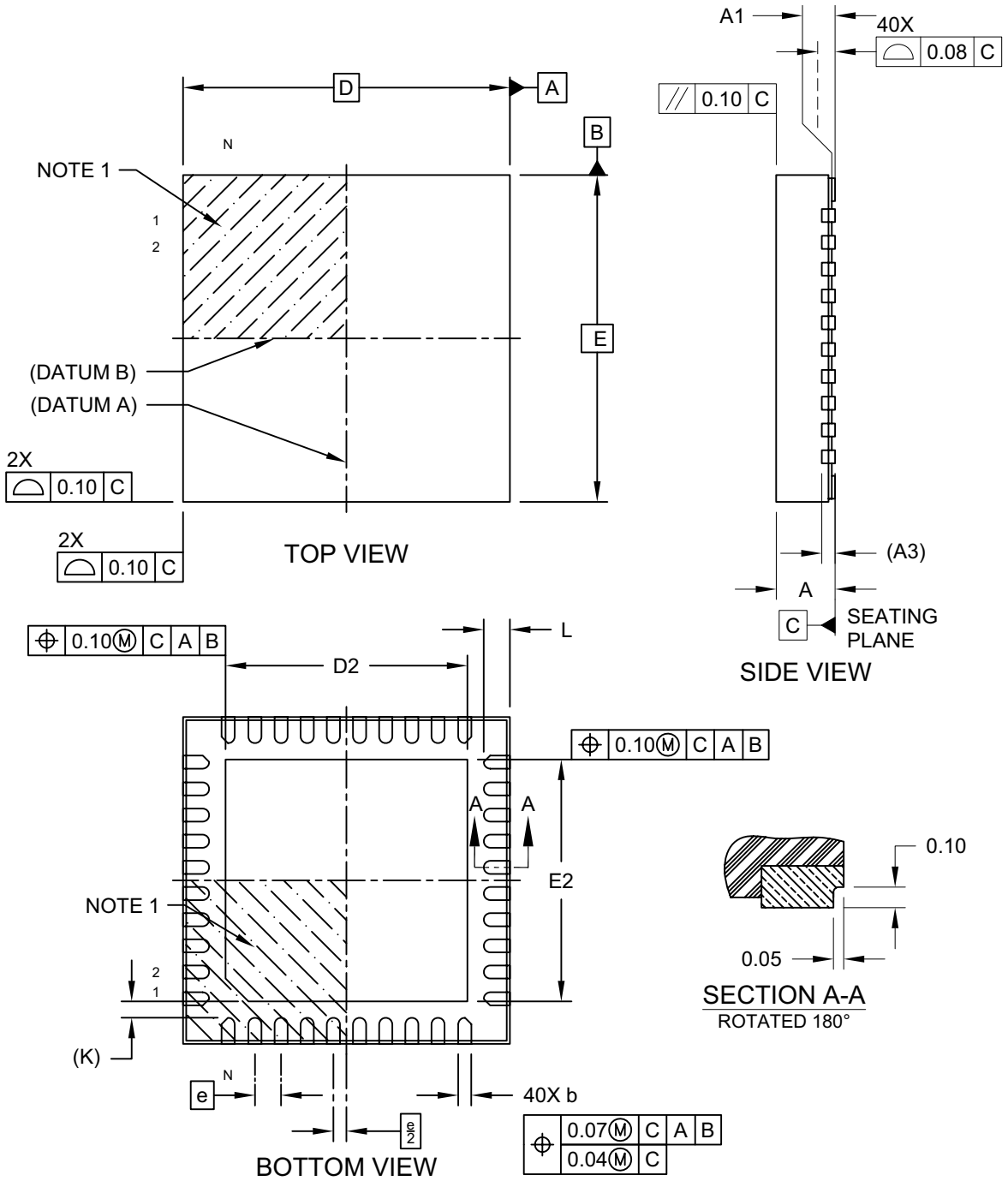
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2055A

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

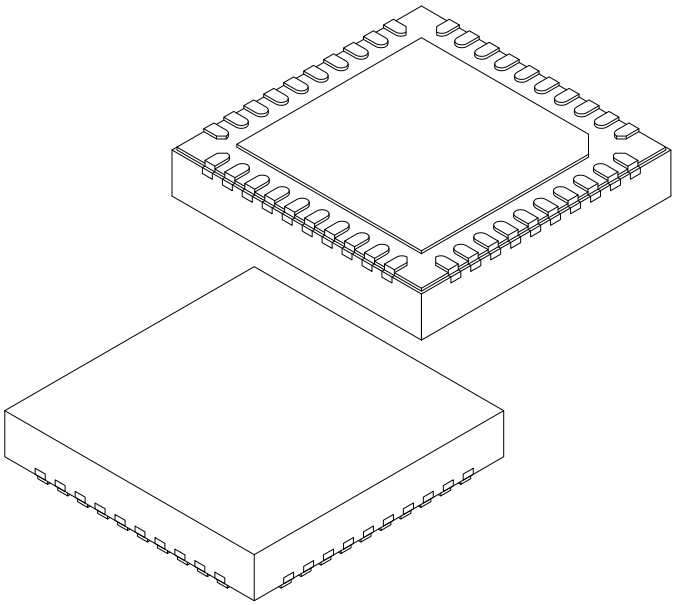
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-425A Sheet 1 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

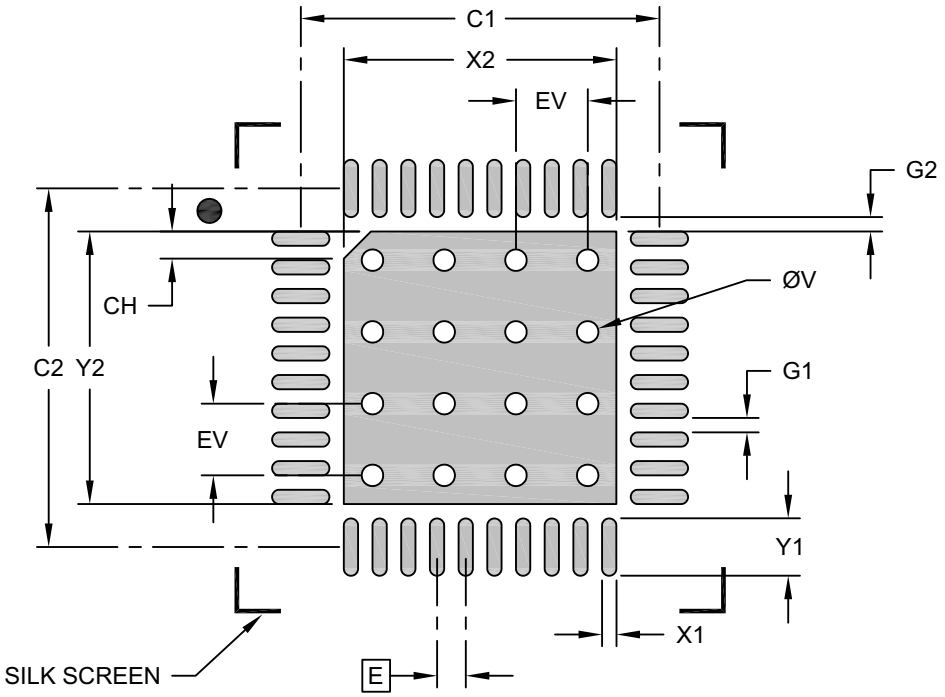
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-425A Sheet 2 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Chamfer	CH		0.38	
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.80
Contact Pad to Pad (X36)	G1	0.20		
Contact Pad to Center Pad (X40)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

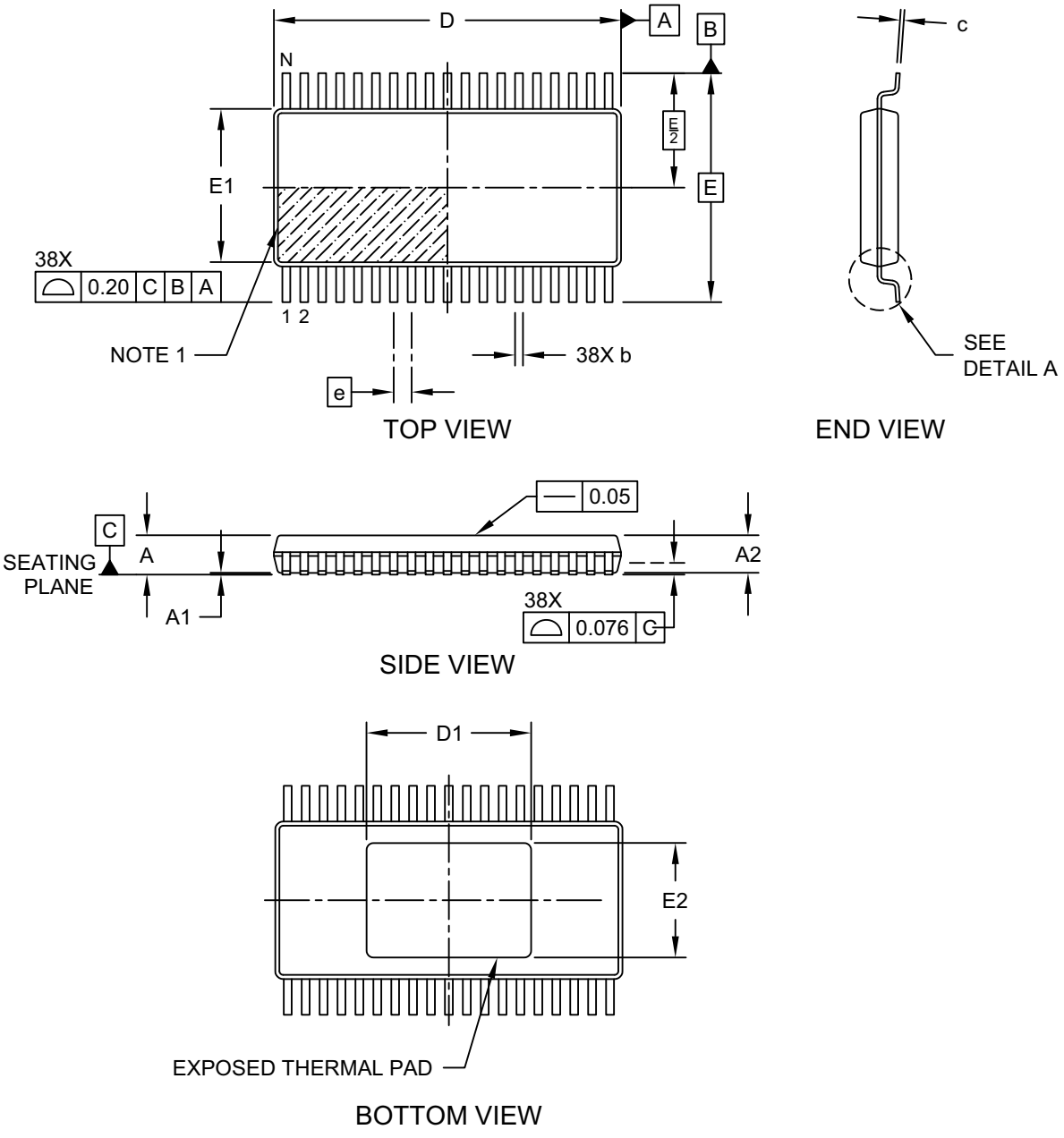
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2425A

38-Lead Thin Shrink Small Outline Package (SBX) - 4.4 mm Body [TSSOP] With 4.6x 3.2 mm Exposed Pad

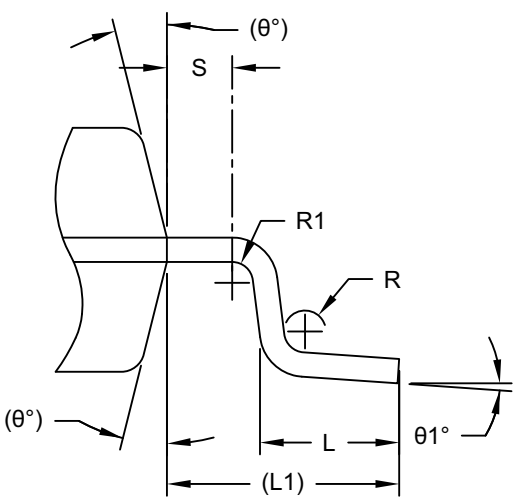
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



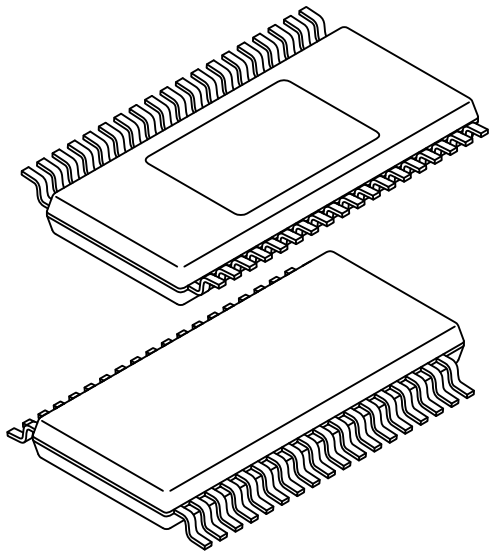
Microchip Technology Drawing C04-424A Sheet 1 of 2

38-Lead Thin Shrink Small Outline Package (SBX) - 4.4 mm Body [TSSOP] With 4.6x 3.2 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		38	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.10
Standoff	A1	0.05	-	0.15
Terminal Thickness	A2	0.85	0.90	0.95
Overall Length	D	9.60	9.70	9.80
Exposed Pad Length	D1	4.50	4.60	4.70
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.60
Exposed Pad Width	E2	3.10	3.20	3.30
Terminal Width	b	0.17	-	0.27
Terminal Width	c	0.09	-	0.20
Terminal Length	L	0.50	0.60	0.70
Terminal Length	L1		1.00 REF	
Lead Shoulder	S	0.20	-	-
Terminal Foot Angle	θ1	0°	-	8°
Mold Draft Angle	θ		14° REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

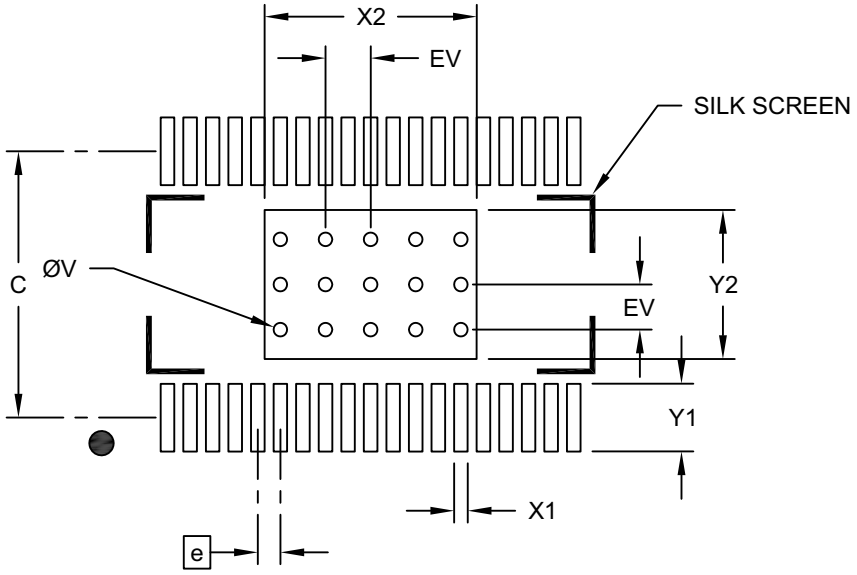
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-424A Sheet 2 of 2

38-Lead Thin Shrink Small Outline Package (SBX) - 4.4 mm Body [TSSOP] With 4.6x 3.2 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			4.70
Center Pad Length	Y2			3.30
Contact Pad Spacing	C		5.90	
Contact Pad Width (X38)	X1			0.30
Contact Pad Length (X38)	Y1			1.50
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2424A

APPENDIX A: REVISION HISTORY

Revision A (July 2020)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-XXXX	X	/XX
Device	Tape and Reel Option	Output Voltage	Temperature Range	Package

Device:	MCP8021	= 3-Phase BLDC Motor Gate Driver (VQFN-28, TSSOP-28)
	MCP8021T	= S-Phase BLDC Motor Gate Driver, Tape and Reel (VQFN-28, TSSOP-28)
	MCP8022	= 3-Phase BLDC Motor Gate Driver (VQFN-40, TSSOP-38)
	MCP8022T	= S-Phase BLDC Motor Gate Driver, Tape and Reel (VQFN-40, TSSOP-38)
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel(1)
Output Voltage Option:	3315	= 3.3V
	5015	= 5.0V
Temperature Range:	H	= -40°C to +125°C (High)
	E	= -40°C to +150°C (Extended)
Package:	9PX	= 28-Lead VQFN
	Q4X	= 28-Lead TSSOP
	NHX	= 40-Lead VQFN
	SBX	= 38-Lead TSSOP

Examples:

a) MCP8021-5015E/9PX: 5.0V Output Voltage, Extended Temperature, 28-Lead 5x5 VQFN Package

b) MCP8021-5015H/9PX: 5.0V Output Voltage, High Temperature, 28-Lead 5x5 VQFN Package

c) MCP8021T-5015E/9PX: Tape and Reel, 5.0V Output Voltage, Extended Temperature, 28-Lead 5x5 VQFN Package

d) MCP8021T-5015H/9PX: 5.0V Output Voltage, Tape and Reel, High Temperature, 40-Lead 5x5 VQFN Package

e) MCP8021-3315E/Q4X: 3.3V Output Voltage, Extended Temperature, 28-Lead 4.4 TSSOP Package

f) MCP8022-5015E/NHX: 5.0V Output Voltage, Extended Temperature, 40-Lead 5x5 VQFN Package

g) MCP8022T-3315H/SBX Tape and Reel, 3.3V Output Voltage, High Temperature, 38-Lead 4.4 TSSOP Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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