3817 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3817 group is 8-bit microcomputer based on the 740 family core technology.

The 3817 group is designed mainly for VCR timer/function control, and include six 8-bit timers, a fluorescent display automatic display circuit, a PWM function, and an 8-channel A-D converter.

The various microcomputers in the 3817 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3817 group, refer to the section on group expansion.

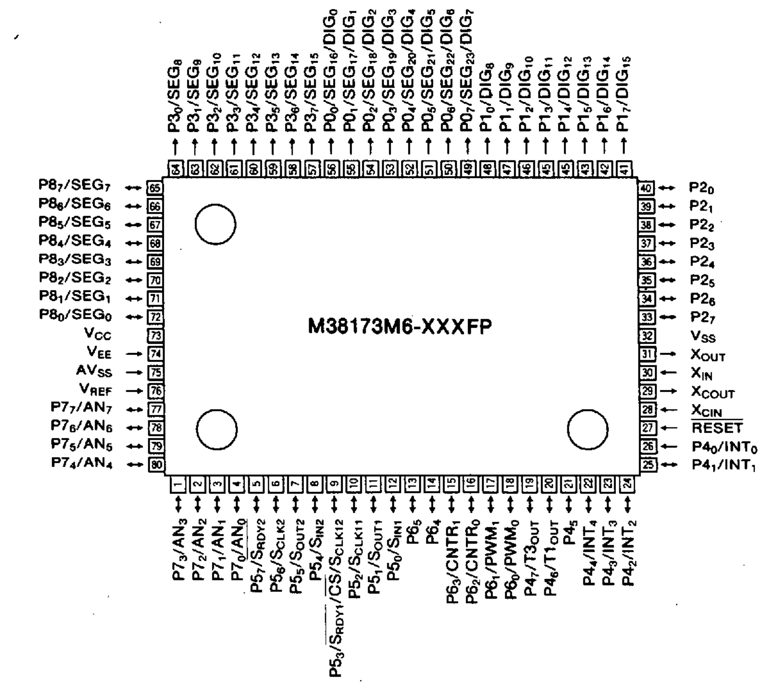
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .... 0.63μs (at 6.3MHz oscillation frequency)
- Memory size
  ROM .... 4K to 60K bytes
  RAM .... 192 to 1024 bytes
- Programmable input/output ports 45
- High-breakdown-voltage output ports 32
- Interrupts .... 18 sources, 15 vectors
- Timers .... 8-bit×6
- Serial I/O .... Clock-synchronized 8-bit×2 (Serial I/O1 has an automatic data transfer function)
- PWM output circuit .... 14-bit×1
  8-bit×1 (also functions as timer 6)
- A-D converter .... 8-bit×8 channels
- Fluorescent display function
  Segments .... 8 to 24
  Digits .... 4 to 16
- 2 Clock generating circuit
  Clock (X_{IN}-X_{OUT}) .... Internal feedback resistor
  Sub-clock (X_{CIN}-X_{COUT}) .... Without internal feedback resistor
- Power source voltage .... 4.0 to 5.5V
- Power dissipation
  In high-speed mode 38mW
  (at 6.3MHz oscillation frequency)
  In low-speed mode 300μW
  (at 32kHz oscillation frequency)
- Operating temperature range .... −10 to +85℃

APPLICATIONS

VCRs, tuners, musical instruments, office automation, etc.

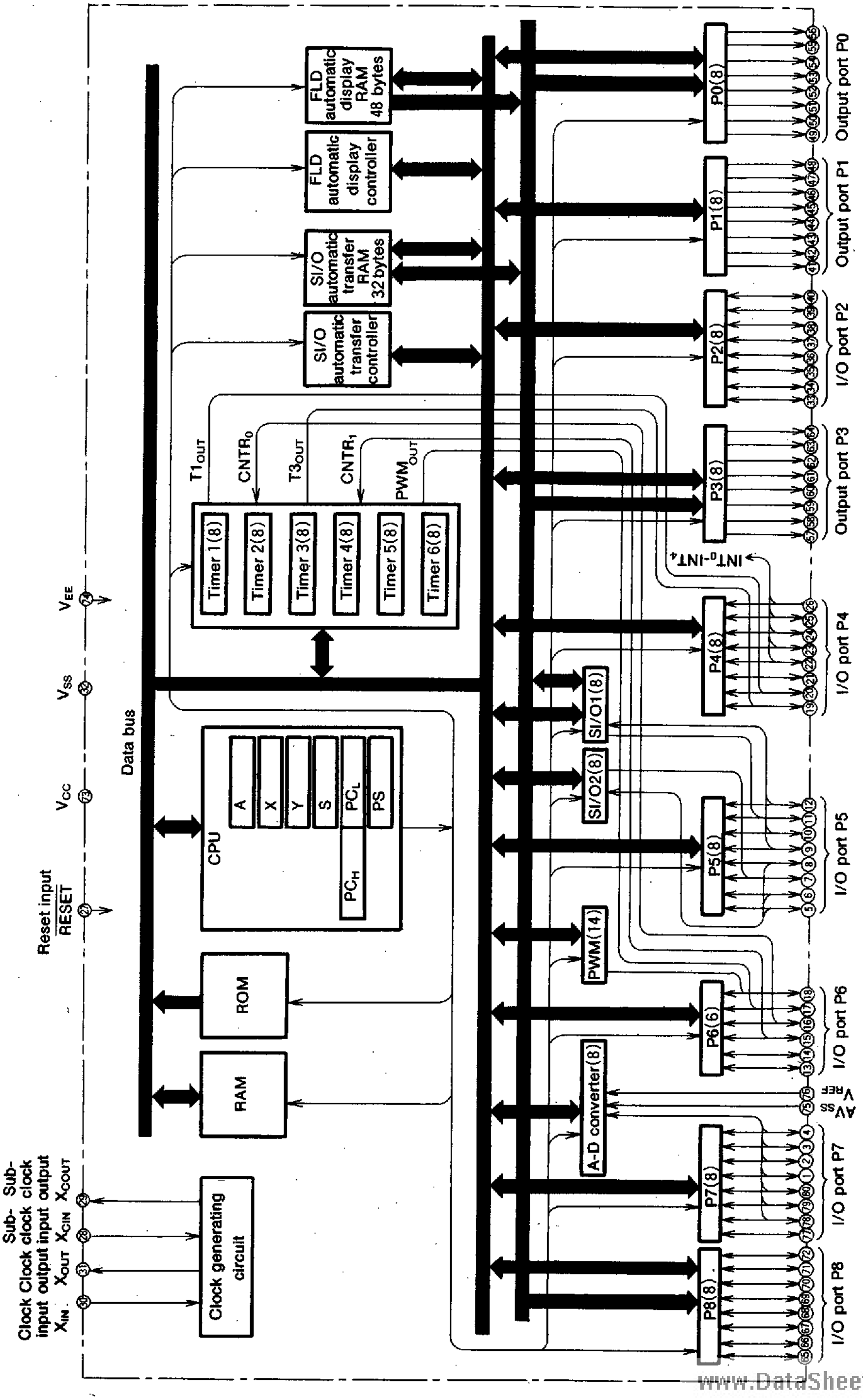
PIN CONFIGURATION (TOP VIEW)



Package type : 80P6N-A

80-pin plastic molded QFP

FUNCTIONAL BLOCK DIAGRAM (Package : 80P6N-A)



PIN DESCRIPTION

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 4.0 to 5.5V to V_{CC}, and 0V to V_{SS}.	
V_{EE}	Pull-down power input	• Applies voltage supplied to pull-down resistors of ports P0, P1 and P3.	
V_{REF}	Analog reference voltage	• Reference voltage input pin for A-D converter	
AV_{SS}	Analog power source	• GND input pin for A-D converters • Connect to V_{SS}.	
$\overline{RESET}$	Reset input	• Reset input pin for active "L"	
X_{IN}	Clock input	• Input and output signals for the internal clock generating circuit. • It consist of internal feedback resistor. • Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. • This clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
X_{CIN}	Sub-clock input	• Input and output signals for the sub-clock generating circuit. • It consist of without internal feedback resistor. • Connect a ceramic resonator or quartz-crystal oscillator and external feedback resistor between the X_{CIN} and X_{COUT} pins. • If an external clock is used, connect the clock source to the X_{CIN} pin and leave the X_{COUT} pin open. • This clock can also be used as the oscillating source of system clock.	
X_{COUT}	Sub-clock output		
$P0_0/SEG_{16}/DIG_0$-$P0_7/SEG_{23}/DIG_7$	Output port P0	• 8-bit output port • The output structure is high-breakdown-voltage P-channel open drain with internal pull-down resistors connected between the output and the V_{EE} pin. • At reset this port is set to V_{EE} pin level.	• FLD automatic display pins
$P1_0/DIG_8$-$P1_7/DIG_{15}$	Output port P1	• 8-bit output port with the same function as port P0	• FLD automatic display pins
$P2_0$-$P2_7$	I/O port P2	• 8-bit CMOS I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • At reset this port is set to input mode. • TTL compatible input level • CMOS 3-state output structure	
$P3_0/SEG_8$-$P3_7/SEG_{15}$	Output port P3	• 8-bit output port with the same function as port P0	• FLD automatic display pins
$P4_0/INT_0$	Input port $P4_0$	• 1-bit CMOS input pin.	• External interrupt input pin
$P4_1/INT_1$-$P4_4/INT_4$	I/O port P4	• 7-bit CMOS I/O port with the same function as port P2 • CMOS compatible input level • CMOS 3-state output structure	• External interrupt input pins
$P4_5$			
$P4_6/T1_{OUT}$, $P4_7/T3_{OUT}$			• Timer 1, Timer 3 output pin

PIN DESCRIPTION

Pin	Name	Function	Alternate Function
$P5_0/S_{IN1}$, $P5_1/S_{OUT1}$, $P5_2/S_{CLK11}$, $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$	I/O port P5	• 8-bit I/O port with the same function as port P2 • N-channel open drain output structure • CMOS compatible input level • Keep the input voltage of this port between 0V and V_{CC}.	• Serial I/O1 I/O pins
$P5_4/S_{IN2}$, $P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$, $P5_7/\overline{S_{RDY2}}$			• Serial I/O2 I/O pins
$P6_0/PWM_0$	I/O port P6	• 6-bit CMOS I/O port with the same function as port P2 • CMOS compatible input level • CMOS 3-state output structure	• 14-bit PWM output pin
$P6_1/PWM_1$			• 8-bit PWM output pin
$P6_2/CNTR_0$, $P6_3/CNTR_1$			• Timer 2, Timer 4 input pins
$P6_4$, $P6_5$			
$P7_0/AN_0$-$P7_7/AN_7$	I/O port P7	• 8-bit CMOS I/O port with the same function as port P2 • CMOS compatible input level • CMOS 3-state output structure	• A-D conversion input pins
$P8_0/SEG_0$-$P8_7/SEG_7$	I/O port P8	• 8-bit I/O port with the same function as port P2 • P-channel open drain output structure • CMOS compatible input level • Please note that this port does not have internal pull-down resistors.	• FLD automatic display pins

PART NUMBERING

Product M3817 3 M 6 - XXX FP

- Package type
  - FP : 80P6N-A package
  - FS : 80D0 package
- ROM number
  - Omitted in some types
- ROM/PROM size
  - 1 : 4096 bytes
  - 2 : 8192 bytes
  - 3 : 12288 bytes
  - 4 : 16384 bytes
  - 5 : 20480 bytes
  - 6 : 24576 bytes
  - 7 : 28672 bytes
  - 8 : 32768 bytes
  - 9 : 36864 bytes
  - A : 40960 bytes
  - B : 45056 bytes
  - C : 49152 bytes
  - D : 53248 bytes
  - E : 57344 bytes
  - F : 61440 bytes
  - The first 128 bytes and the last 2 bytes of ROM are reserved areas; they cannot be used.
- Memory type
  - M : Mask ROM version
  - E : EPROM or One Time PROM version
- RAM size
  - 0 : 192 bytes
  - 1 : 256 bytes
  - 2 : 384 bytes
  - 3 : 512 bytes
  - 4 : 640 bytes
  - 5 : 768 bytes
  - 6 : 896 bytes
  - 7 : 1024 bytes

GROUP EXPANSION

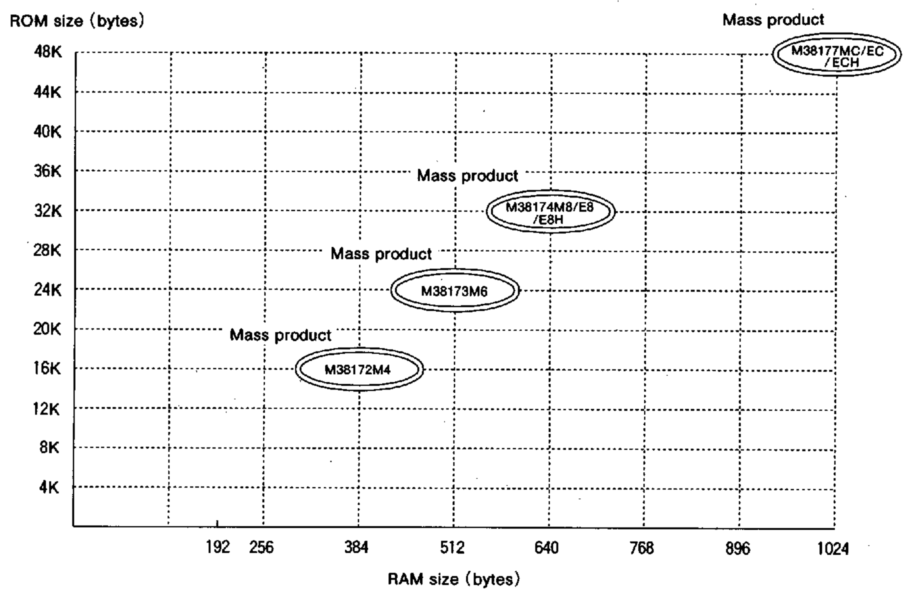
Mitsubishi plans to expand the 3817 group as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions

(2) ROM/PROM size ································16K to 48K bytes
RAM size ···384 to 1024 bytes

(3) Packages
80P6N-A ··················· 0.8mm-pitch plastic molded QFP
80D0 ··············· 0.8mm-pitch window type ceramic LCC (EPROM version)

Memory Expansion Plan



Currently supported products are listed below. **As of May 1996**

Product	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38172M4-XXXFP	16384(16254)	384	80P6N-A	Mask ROM version
M38173M6-XXXFP	24576(24446)	512		Mask ROM version
M38174M8-XXXFP	32768(32638)	640		Mask ROM version
M38174E8-XXXFP				One Time PROM version
M38174E8FP				One Time PROM version (blank)
M38174E8FS			80D0	EPROM version
M38174E8HXXXFP			80P6N-A	One Time PROM version
M38174E8HFP				One Time PROM version (blank)
M38174E8HFS			80D0	EPROM version
M38177MC-XXXFP	49152(49022)	1024	80P6N-A	Mask ROM version
M38177EC-XXXFP				One Time PROM version
M38177ECFP				One Time PROM version (blank)
M38177ECFS			80D0	EPROM version
M38177ECHXXXFP			80P6N-A	One Time PROM version
M38177ECHFP				One Time PROM version (blank)
M38177ECHFS			80D0	EPROM version

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 3817 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL and DIV instruction can be used.

CPU MODE REGISTER

The CPU mode register is allocated at address $003B_{16}$.

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

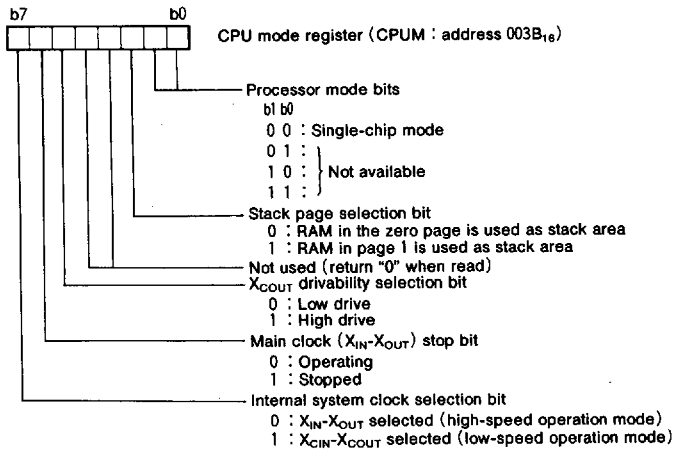


Fig. 1 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}

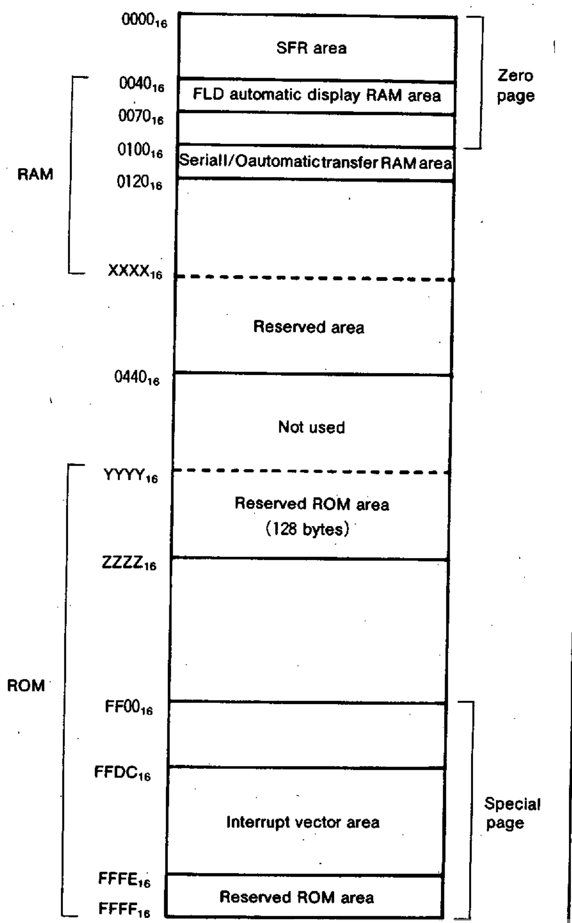


Fig. 2 Memory map diagram

Address	Register	Address	Register
0000_{16}	Port P0 (P0)	0020_{16}	Timer 1 (T1)
0001_{16}		0021_{16}	Timer 2 (T2)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 3 (T3)
0003_{16}		0023_{16}	Timer 4 (T4)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 5 (T5)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 6 (T6)
0006_{16}	Port P3 (P3)	0026_{16}	
0007_{16}		0027_{16}	Timer 6 PWM register (T6PWM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer 12 mode register (T12M)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 34 mode register (T34M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	Timer 56 mode register (T56M)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	PWM control register (PWMCON)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	PWM register (upper)(PWMH)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	PWM register (lower)(PWML)
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}	Port P8 (P8)	0030_{16}	A-D control register (ADCON)
0011_{16}	Port P8 direction register (P8D)	0031_{16}	A-D conversion register (AD)
0012_{16}		0032_{16}	Port P0 segment/digit switching register (P0SDR)
0013_{16}		0033_{16}	Port P1 digit/port switching register (P1DPR)
0014_{16}		0034_{16}	Port P8 segment/port switching register (P8SPR)
0015_{16}		0035_{16}	Key-scan blanking register (KSCN)
0016_{16}		0036_{16}	FLDC mode register (FLDM)
0017_{16}		0037_{16}	FLD data pointer (FLDDP)
0018_{16}	Serial I/O automatic transfer data pointer (SIODP)	0038_{16}	High-breakdown-voltage port control register (HVPC)
0019_{16}	Serial I/O1 control register (SIO1CON)	0039_{16}	
$001A_{16}$	Serial I/O automatic transfer control register (SIOAC)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	Serial I/O1 register (SIO1)	$003B_{16}$	CPU mode register (CUPM)
$001C_{16}$	Serial I/O automatic transfer interval register (SIOAI)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS
Direction Registers

The 3817 group has 45 programmable I/O pins arranged in six I/O ports (ports P2 and P4 to P8). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

High-Breakdown-Voltage Output Ports

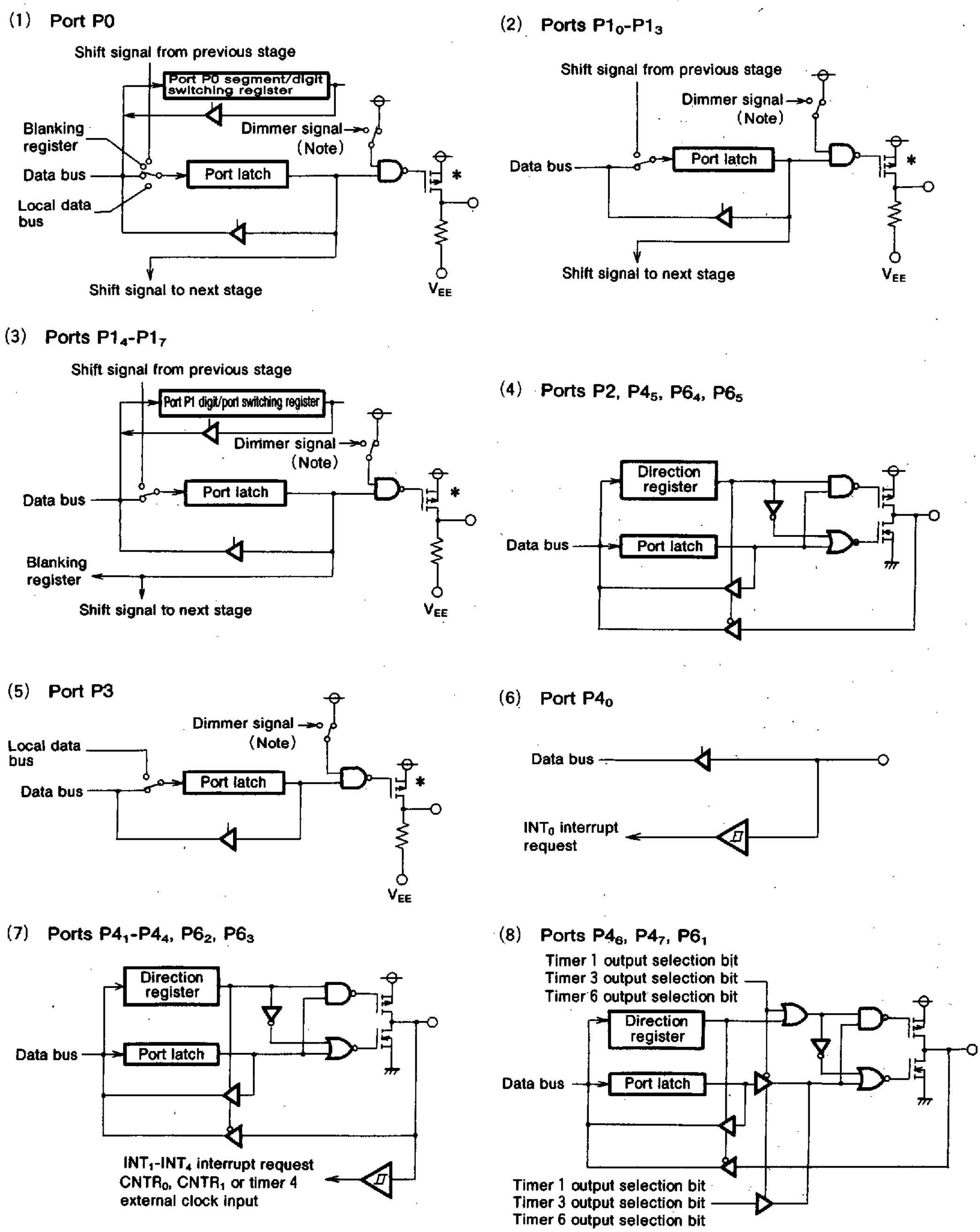
The 3817 group has four ports with high-breakdown-voltage pins (ports P0, P1, P3, P8). The high-breakdown-voltage ports have P-channel open drain output with a breakdown voltage of $V_{CC}-40V$. Each pin in Ports P0, P1, and P3 has an internal pull-down resistor connected to V_{EE}. Port P8 has no internal pull-down resistors, so that connect an external resistor to each port. At reset, the P-channel output transistor of each port latch is turned off, so it becomes V_{EE} level ("L") by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register (address 0038_{16}) slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
$P0_0/SEG_{16}/DIG_0$-$P0_7/SEG_{23}/DIG_7$	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Port P0 segment/digit switching register High-breakdown-voltage port control register	(1)
$P1_0/DIG_8$-$P1_3/DIG_{11}$	Port P1	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(2)
$P1_4/DIG_{12}$-$P1_7/DIG_{15}$					FLDC mode register Port P1 digit/port switching register High-breakdown-voltage port control register	(3)
$P2_0$-$P2_7$	Port P2	Input/output, individual bits	TTL level input CMOS 3-state output			(4)
$P3_0/SEG_8$-$P3_7/SEG_{15}$	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(5)
$P4_0/INT_0$	Port P4	Input	CMOS compatible input level	External interrupt input	Interrupt edge selection register	(6)
$P4_1/INT_1$-$P4_4/INT_4$		Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input	Interrupt edge selection register	(7)
$P4_5$						(4)
$P4_6/T1_{OUT}$, $P4_7/T3_{OUT}$				Timer output	Timer 12 mode register Timer 34 mode register	(8)
$P5_0/S_{IN1}$, $P5_1/S_{OUT1}$, $P5_2/S_{CLK1}$, $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$	Port P5	Input/output, individual bits	CMOS compatible input level N-channel open-drain output	Serial I/O1 function I/O	Serial I/O1 control register Serial I/O automatic transfer control register	(9) (10) (11)
$P5_4/S_{IN2}$, $P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$, $P5_7/\overline{S_{RDY2}}$				Serial I/O2 function I/O	Serial I/O2 control register	(9) (10) (11)
$P6_0/PWM_0$	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	14-bit PWM output	PWM control register PWML register PWMH register	(12)
$P6_1/PWM_1$				8-bit PWM output	Timer 56 mode register Timer6 PWM register	(8)
$P6_2/CNTR_0$, $P6_3/CNTR_1$				Timer 2, Timer 4 input	Interrupt edge selection register	(7)
$P6_4$, $P6_5$						(4)
$P7_0/AN_0$-$P7_7/AN_7$	Port P7	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input	A-D control register	(13)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
$P8_0/SEG_0$-$P8_7/SEG_7$	Port P8	Input/output, individual bits	CMOS compatible input level High-breakdown-voltage P-channel open-drain output without pull-down resistor	FLD automatic display function	FLDC mode register Port P8 segment/port switching register High-breakdown-voltage port control registor	(14)

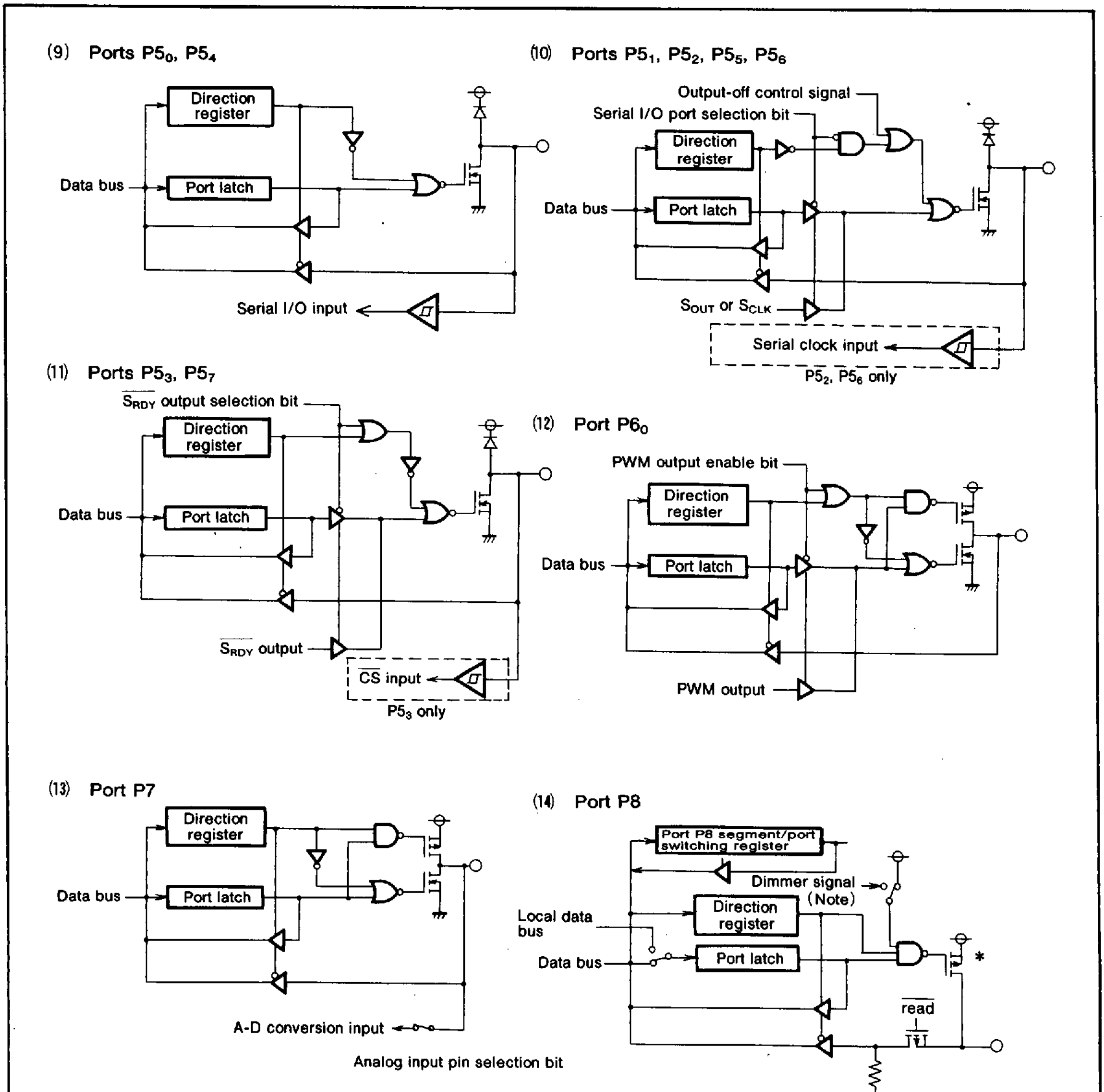
Note 1. For details of how to use double-function ports as function I/O ports, refer to the applicable sections.
2. Make sure that the input level at each pin is either 0V or V_{CC} during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.



* : High-breakdown-voltage P-channel transistor

Note. The dimmer signal sets the Toff timing.

Fig. 4 Port block diagram (1)



* : High-breakdown-voltage P-channel transistor

Note. The dimmer signal sets the Toff timing.

Fig. 5 Port block diagram (2)

INTERRUPTS

Interrupts occur by eighteen sources: five external, twelve internal, and one software.

Interrupt Control

Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".
Interrupt enable bits can be set or cleared by software.
Interrupt request bits can be cleared by software, but cannot be set by software.
The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.
When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

When an interrupt is received, the contents of the program counter and processor' status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

When the active edge of an external interrupt (INT_0-INT_4) is changed or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;
(1) Disable the external interrupt which is selected.
(2) Change the active edge selection.
(3) Clear the interrupt request bit which is selected to "0".
(4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
Serial I/O1	5	$FFF5_{16}$	$FFF4_{16}$	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O automatic transfer				At completion of the last data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	$FFF3_{16}$	$FFF2_{16}$	At completion of data transfer	
Timer 1	7	$FFF1_{16}$	$FFF0_{16}$	At timer 1 underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	STP release timer underflow
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
Timer 4	10	$FFEB_{16}$	$FFEA_{16}$	At timer 4 underflow	
Timer 5	11	$FFE9_{16}$	$FFE8_{16}$	At timer 5 underflow	
Timer 6	12	$FFE7_{16}$	$FFE6_{16}$	At timer 6 underflow	
INT_3	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt valid when INT_4 interrupt is selected (active edge selectable)
A-D converter				At completion of A-D conversion	Valid when A-D interrupt is selected
FLD blanking	15	$FFE1_{16}$	$FFE0_{16}$	At falling of final digit	Valid when FLD blanking interrupt is selected
FLD digit				At rising of each digit	Valid when FLD digit interrupt is selected
BRK instruction	16	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1. Vector addresses contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

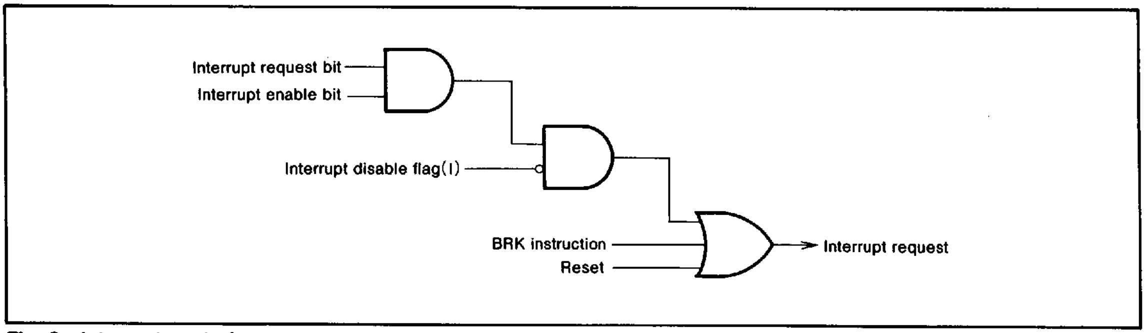


Fig. 6 Interrupt control

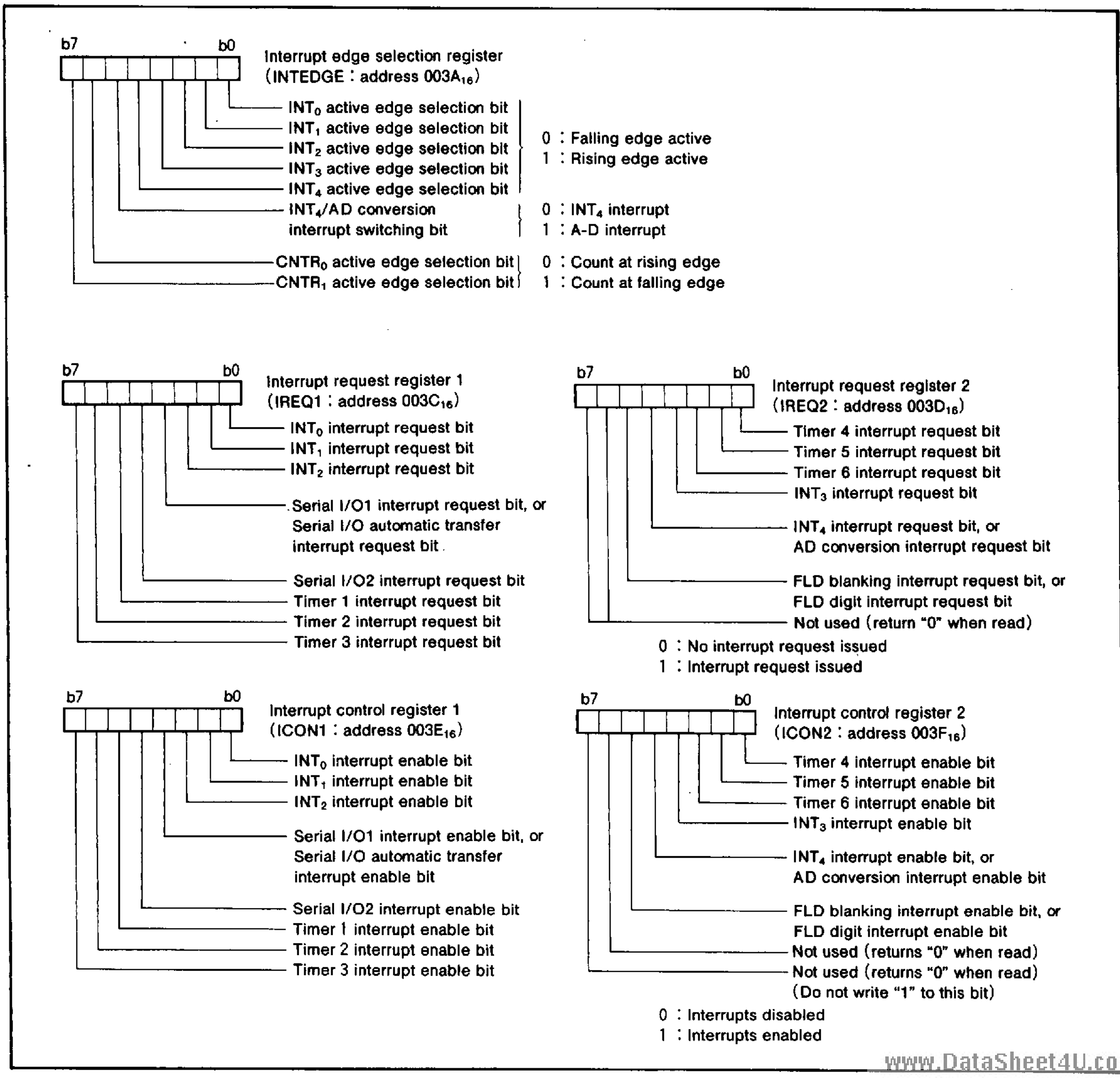


Fig. 7 Structure of interrupt-related registers

TIMERS

The 3817 group has six built-in timers : timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6. All timers are count down. When the timer reaches "00_{16}", at the next count pulse the contents of the corresponding timer latch is loaded into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to "1".
Note that the system clock ϕ can be set to either high-speed mode or low-speed mode by the CPU mode register.

Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.
Timer 1 can also output a rectangular waveform from the $P4_6/T1_{OUT}$ pin. The waveform changes polarity each time timer 1 overflows.
The active edge of the external signal $CNTR_0$ can be set by the interrupt edge selection register.
When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to "FF_{16}", and timer 2 is set to "01_{16}".

Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.
Timer 3 can also output a rectangular waveform from the $P4_7/T3_{OUT}$ pin. The waveform changes polarity each time timer 3 overflows.
The active edge of the external signal $CNTR_1$ can be set by the interrupt edge selection register.

Timer 5 and Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.
Timer 6 can also output a rectangular waveform from the $P6_1/PWM_1$ pin. The waveform changes polarity each time timer 6 overflows.

Timer 6 PWM_1 Mode

Timer 6 can also output a rectangular waveform of n cycles high and m cycles low. The n is the value set in timer latch 6 (address 0025_{16}) and m is the value in the timer 6 PWM register (address 0027_{16}). If n is "0", the PWM output is "L", if m is "0" and n is not "0", then the PWM output is "H". In PWM mode, interrupts are generated at the rising edge of the PWM_1 output.

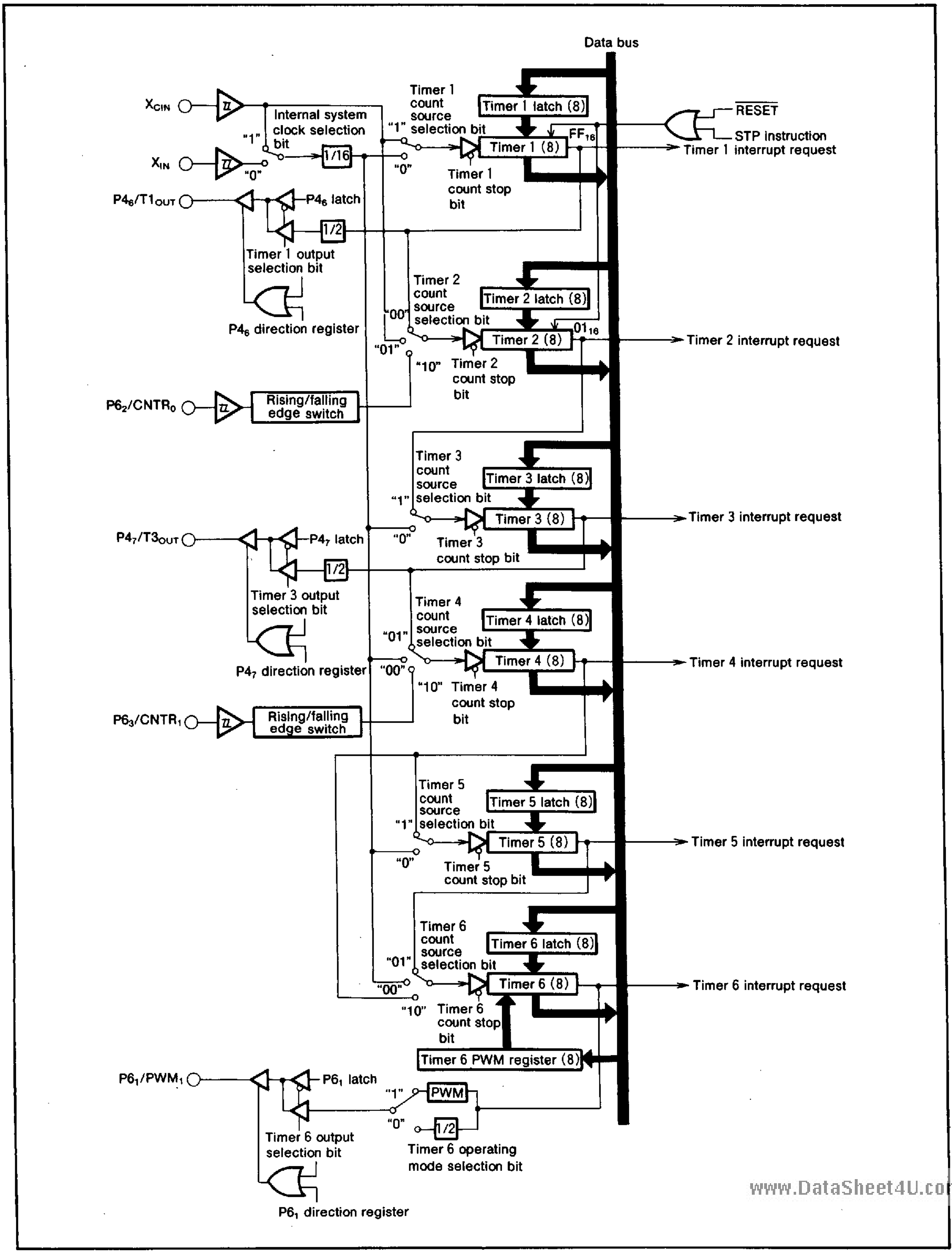


Fig. 8 Timer block diagram

Timer 12 mode register (T12M : address 0028_{16}) (b7 … b0)

- b0: Timer 1 count stop bit
  - 0 : Operating
  - 1 : Stopped
- b1: Timer 2 count stop bit
  - 0 : Operating
  - 1 : Stopped
- b2: Timer 1 count source selection bit
  - 0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$
  - 1 : $f(X_{CIN})$
- b3: Not used (returns "0" when read)
- b5, b4: Timer 2 count source selection bits (b5 b4)
  - 0 0 : Timer 1 underflow
  - 0 1 : $f(X_{CIN})$
  - 1 0 : External count input $CNTR_0$
  - 1 1 : Not available
- b6: Timer 1 output selection bit ($P4_6$)
  - 0 : I/O port
  - 1 : Timer 1 output
- b7: Not used (returns "0" when read)

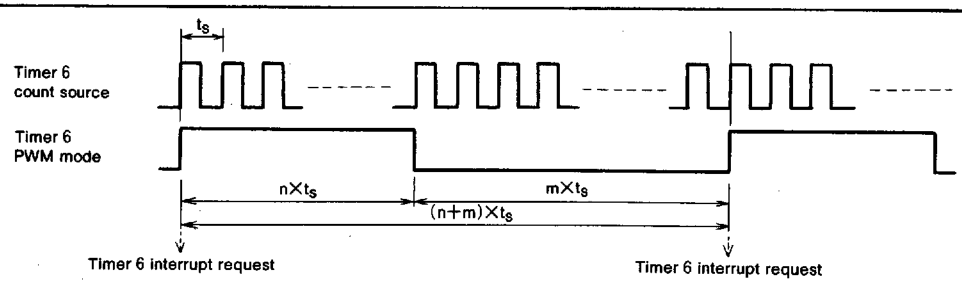
Timer 34 mode register (T34M : address 0029_{16}) (b7 … b0)

- b0: Timer 3 count stop bit
  - 0 : Operating
  - 1 : Stopped
- b1: Timer 4 count stop bit
  - 0 : Operating
  - 1 : Stopped
- b2: Timer 3 count source selection bit
  - 0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$
  - 1 : Timer 2 underflow
- b3: Not used (returns "0" when read)
- b5, b4: Timer 4 count source selection bits (b5 b4)
  - 0 0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$
  - 0 1 : Timer 3 underflow
  - 1 0 : External count input $CNTR_1$
  - 1 1 : Not available
- b6: Timer 3 output selection bit ($P4_7$)
  - 0 : I/O port
  - 1 : Timer 3 output
- b7: Not used (returns "0" when read)

Timer 56 mode register (T56M : address $002A_{16}$) (b7 … b0)

- b0: Timer 5 count stop bit
  - 0 : Operating
  - 1 : Stopped
- b1: Timer 6 count stop bit
  - 0 : Operating
  - 1 : Stopped
- b2: Timer 5 count source selection bit
  - 0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$
  - 1 : Timer 4 underflow
- b3: Timer 6 operation mode selection bit
  - 0 : Timer mode
  - 1 : PWM mode
- b5, b4: Timer 6 count source selection bits (b5 b4)
  - 0 0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$
  - 0 1 : Timer 5 underflow
  - 1 0 : Timer 4 underflow
  - 1 1 : Not available
- b6: Timer 6 (PWM_1) output selection bit ($P6_1$)
  - 0 : I/O port
  - 1 : Timer 6 output
- b7: Not used (returns "0" when read) (Do not write "1" to this bit)

Fig. 9 Structure of timer-related registers



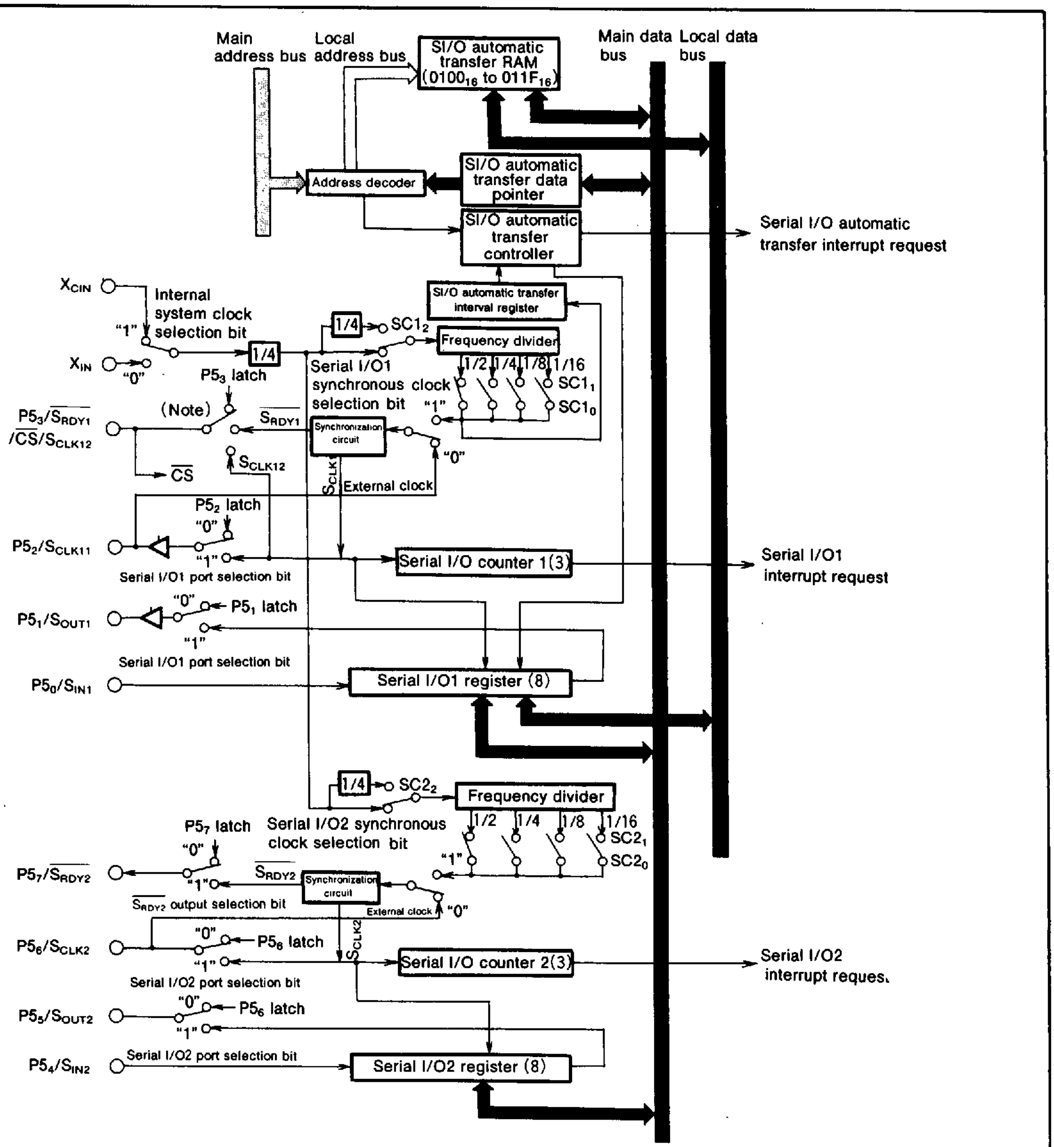
Note. If the value set in timer 6 is n and the value set in the timer 6 PWM register is m, a PWM waveform with duty cycle $n/(n+m)$ and period $(n+m)\times t_S$ is output (where is t_S the frequency of the timer 6 count source).

Fig. 10 Timing in timer 6 PWM_1 mode

SERIAL I/O

The 3817 group has two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).
Serial I/O1 has a built-in automatic transfer function.Normal serial operation can be set via the serial I/O automatic transfer control register (address $001A_{16}$).

Serial I/O2 can only be used in normal operation mode.
The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (addresses 0019_{16} and $001D_{16}$).



Note. Selection is by the synchronization clock selection bit, the $\overline{S_{RDY1}}$ output selection bit, and the serial I/O1 port selection bit of the serial I/O1 control register, and the automatic transfer control bit and synchronization clock output pin selection bit of the serial I/O automatic transfer control register.

Fig. 11 Serial I/O block diagram

Serial I/O Control Registers (SIO1CON, SIO2CON) 0019_{16}, $001D_{16}$

Each of the serial I/O control registers (addresses 0019_{16} and $001D_{16}$) contains seven bits that select various control parameters of the serial I/O function.

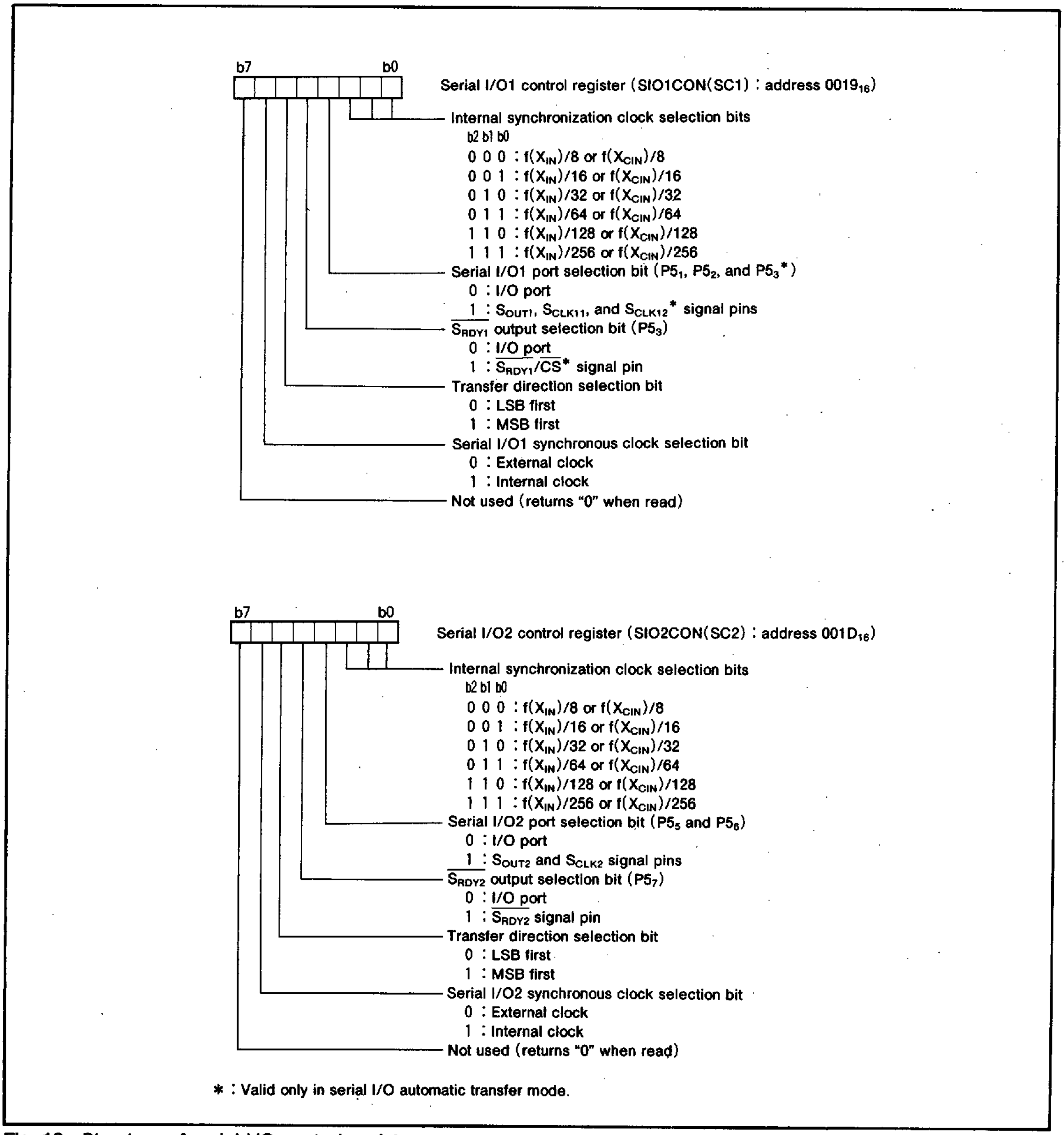


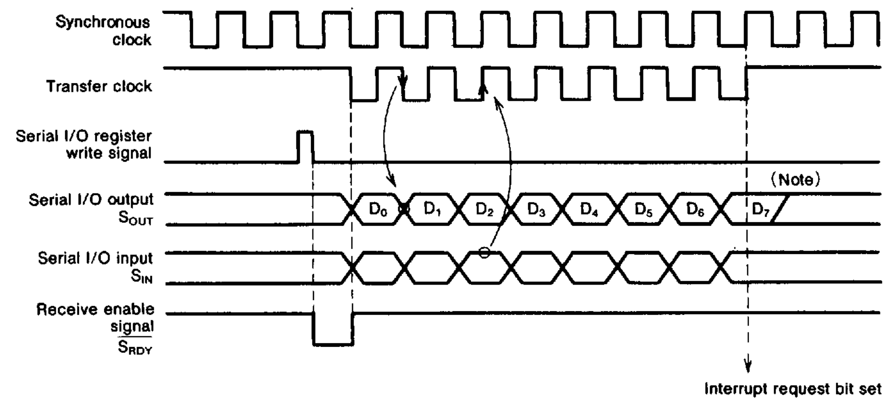
Fig. 12 Structure of serial I/O control registers

Serial I/O Ordinary Mode

Either an internal clock or an external clock can be selected as the synchronous clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, for selecting of six clocks.

If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address $001B_{16}$ or $001F_{16}$). After eight bits have been transferred, the S_{OUT} pin goes to high impedance.

If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift during inputting the transfer clock is. In this case, note that the S_{OUT} pin does not go to high impedance state at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.



Note. If internal clock is selected, the S_{OUT} pin is at high impedance after transfer ends.

Fig. 13 Serial I/O timing in normal mode (for LSB first)

Serial I/O Automatic Transfer Mode

The serial I/O1 function has an automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address $001A_{16}$).

The following memory spaces are added to the circuits used for the serial I/O1 function in ordinary mode, to enable automatic transfer mode:

- 32 bytes of serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O control register (address 0019_{16}) in the same way as for the serial I/O ordinary mode. However, note that when external clock is selected and bit 4 (the $\overline{S_{RDY1}}$ output selection bit) of the serial I/O1 control register "1", port $P5_3$ becomes the $\overline{CS}$ input pin by setting.

Serial I/O Automatic Transfer Control Register (SIOAC) $001A_{16}$

The serial I/O automatic transfer control register (address $001A_{16}$) contains four bits that select various control parameters for automatic transfer.

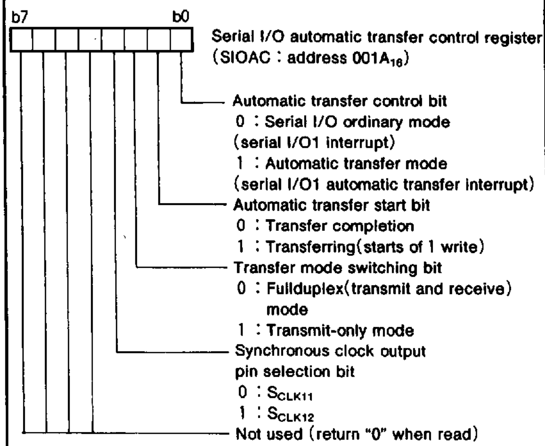


Fig. 14 Structure of serial I/O automatic transfer control register

Serial I/O Automatic Transfer Data Pointer (SIODP) 0018_{16}

The serial I/O automatic transfer data pointer (address 0018_{16}) contains five bits that indicate addresses in serial I/O automatic transfer RAM (each address in memory is actually the value in the serial I/O automatic transfer data pointer plus 0100_{16}).

Set the serial I/O automatic transfer data pointer to (the number of transfer data−1), to specify the storage position of the start of data.

Address \ Bit	7	6	5	4	3	2	1	0
0100_{16}								
0101_{16}								
0102_{16}								
⋮				⋮				
$011D_{16}$								
$011E_{16}$								
$011F_{16}$								

Fig. 15 Bit allocation of serial I/O automatic transfer RAM

Serial I/O Automatic Transfer RAM

The serial I/O automatic transfer RAM is the 32 bytes from address 0100_{16} to address $011F_{16}$.

Setting of Serial I/O Automatic Transfer Data

When data is stored in the serial I/O automatic transfer RAM, it is stored with the start of the data at the address set by the serial I/O automatic transfer data pointer and the end of the data at address 0100_{16}.

Serial I/O Automatic Transfer Interval Register (SIOAI) $001C_{16}$

The serial I/O automatic transfer interval register (address $001C_{16}$) consists of a 5-bit counter that determines the transfer interval Ti during automatic transfer.

If a value n is written to the serial I/O automatic transfer interval register, a value of $Ti = (n + 2) \times Tc$ is generated, where Tc is the length of one bit of the transfer clock. However, note that this transfer interval setting is only valid when internal clock has been selected as the clock source.

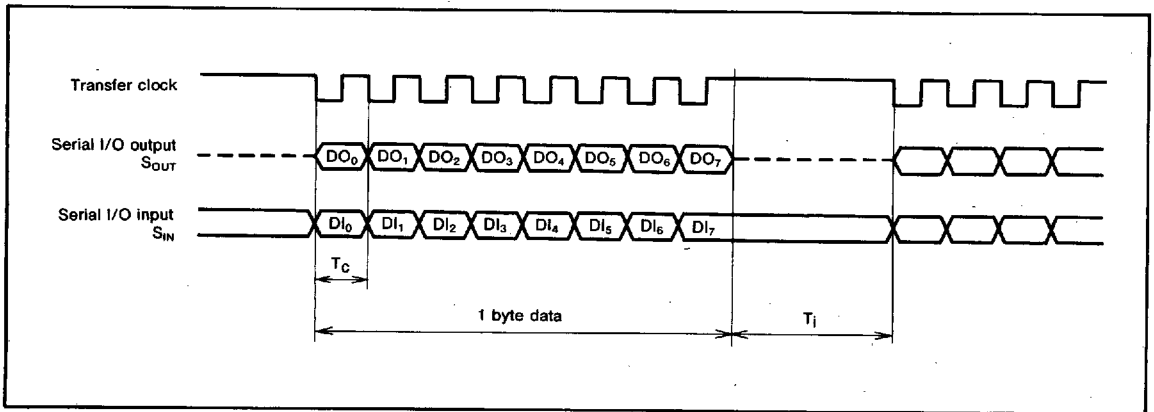


Fig. 16 Serial I/O automatic transfer interval timing

Setting of Serial I/O Automatic Transfer Timing

Use the serial I/O1 control register (address 0019_{16}) and the serial I/O automatic transfer interval register (address $001C_{16}$) to set the timing of serial I/O automatic transfer.

The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval.

This setting of transfer interval is valid only when internal clock is selected as the clock source.

Start of Serial I/O Automatic Transfer

Automatic transfer mode is set by writing "1" to bit 0 of the serial I/O automatic transfer control register (address $001A_{16}$), then automatic transfer starts when "1" is written to that bit. Bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" to it is one way to complete automatic transfer.

Operation in Serial I/O Automatic Transfer Modes

There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes.

Operation in Fullduplex Mode

In fullduplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is sent in sequence and simultaneously receive data is written to the automatic transfer RAM, in accordance with the serial I/O automatic transfer data pointer.

The transfer timing of each bit is the same as in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted. If internal clock is selected, the transfer clock remains at "H" for the time set by the serial I/O automatic transfer interval register, then the data at the next address indicated by the serial I/O automatic transfer data pointer is transferred. If external clock is selected, the setting of the automatic transfer interval register is invalid, so the user must ensure that the transfer clock is controlled externally.

Data transfer ends when the contents of the serial I/O automatic transfer pointer reach "00_{16}". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

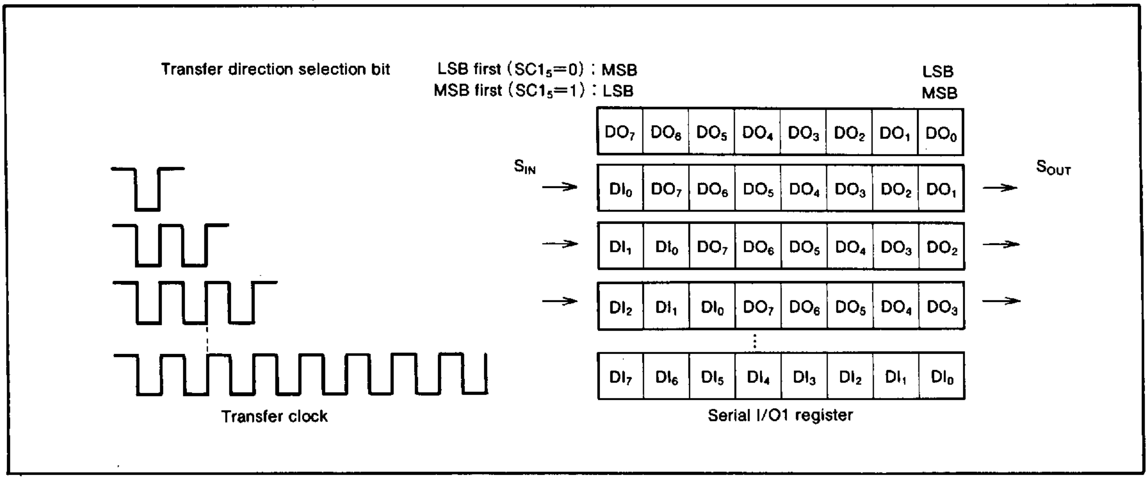


Fig. 17 Serial I/O1 register in fullduplex mode

If Internal Clock is Selected

If internal clock is selected, the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin can be used as the $\overline{S_{RDY1}}$ pin by setting the $SC1_4$ bit to "1".
If internal clock is selected, the $P5_3$ pin can be used as the synchronization clock output pin S_{CLK12} by setting the $SIOAC_3$ bit to "1". In this case, the S_{CLK11} pin is at high impedance.
Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ and $P5_2/S_{CLK11}$ pins by setting bit 3 ($SC1_3$), bit 4 ($SC1_4$), and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_{16}) and bit 3 ($SIOAC_3$) of the serial I/O automatic transfer control register (address $001A_{16}$). (Refer to Table 2.)

If using the S_{CLK11} and S_{CLK12} pins for switching, set the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin to $P5_3$ by setting the $SC1_4$ bit to "0", and set the $P5_3$ direction register to input mode.
Make sure that the $SIOAC_3$ bit is switched after automatic transfer is completed, while the transfer clock is still "H".

Table 2. S_{CLK11} and S_{CLK12} selection

$SC1_6$	$SC1_4$	$SC3_3$	$SIOAC_3$	$P5_2/S_{CLK11}$	$P5_3/S_{CLK12}$
1	0	1	0	S_{CLK11}	$P5_3$
			1	High impedanse	S_{CLK12}

Note. $SC1_3$: Serial I/O1 port selection bit
$SC1_4$: $\overline{S_{RDY1}}$ output selection bit
$SC1_6$: Synchronization clock selection bit
$SIOAC_3$: Synchronization clock output pin selection bit

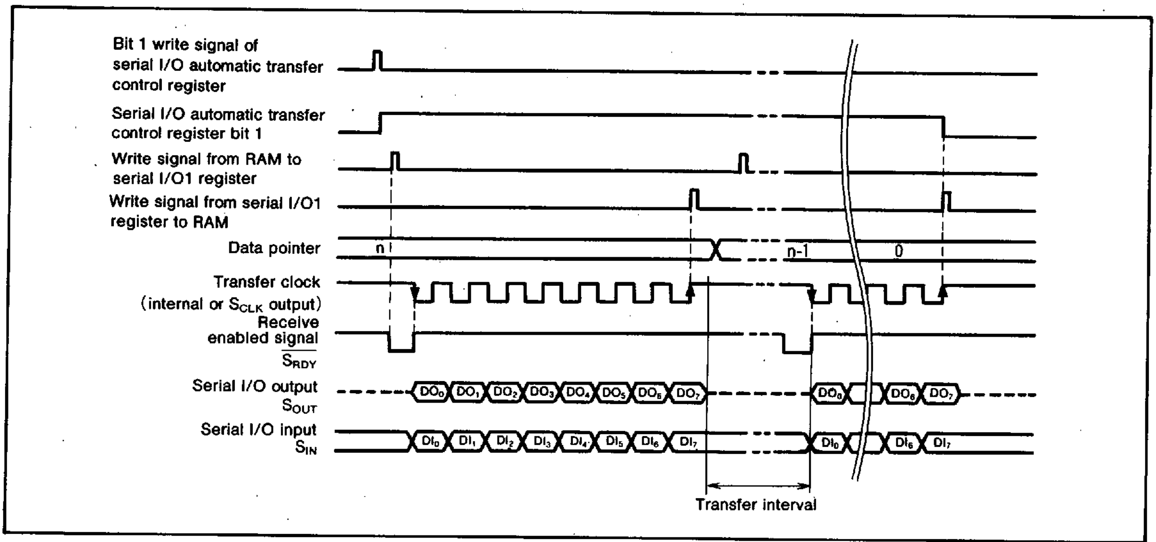


Fig. 18 Timing during serial I/O automatic transfer (internal clock selected, $\overline{S_{RDY}}$ used)

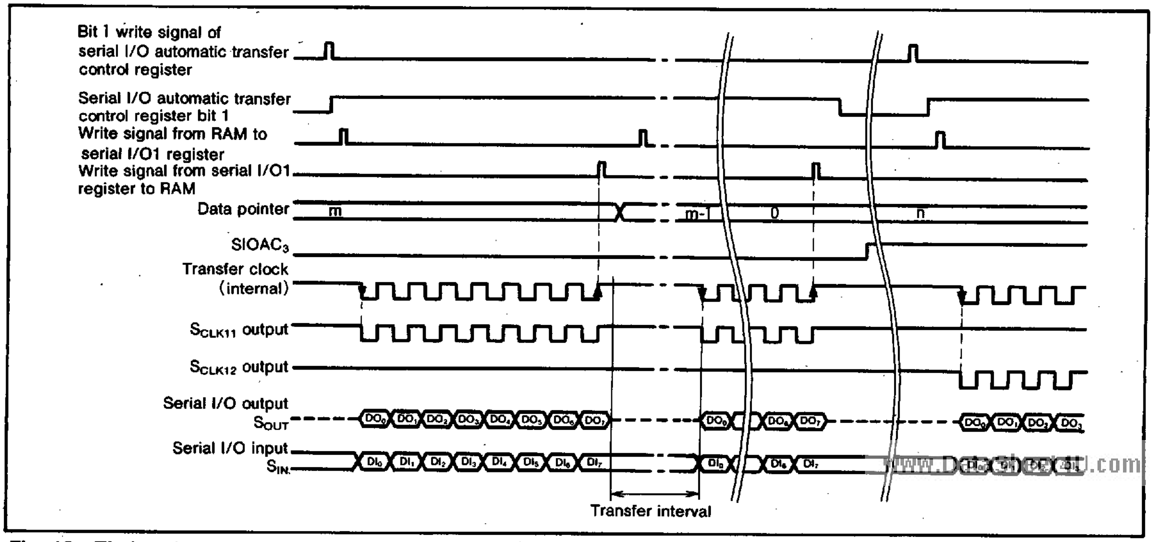


Fig. 19 Timing during serial I/O automatic transfer (internal clock selected, S_{CLK11} and S_{CLK12} used)

If External Clock is Selected

If an external clock is selected, the internal clock and the transfer interval set by the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin S_{OUT} and the internal transfer clock can be controlled from the outside by setting the $\overline{S_{RDY1}}$ and $\overline{CS}$ (input) pins.

When the $\overline{CS}$ input is "L", the S_{OUT} pin and the internal transfer clock are enabled. When the $\overline{CS}$ input is "H", the S_{OUT} pin is at high impedance and the internal transfer clock is at "H".

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin by setting bit 4 ($SC1_4$) and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_{16}) and bit 0 ($SIOAC_0$) of the serial I/O automatic transfer control register (address $001A_{16}$).

Make sure that the $\overline{CS}$ pin switches from "L" to "H" or from "H" to "L" while the transfer clock (S_{CLK} input) is "H" after one byte of data has been transferred.

If external clock is selected, make sure that the external clock goes "L" after at least 9 cycles of the internal system clock ϕ after the start bit is set. Leave at least 11 cycles of the system clock ϕ free for the transfer interval after one byte of data has been transferred.

If $\overline{CS}$ input is not being used, note that the S_{OUT} pin will not go high impedance, even after transfer is completed.

If $\overline{CS}$ input is not being used, or if $\overline{CS}$ is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer. (Note that the automatic transfer interrupt request bit is set and bit 1 of the automatic transfer register is cleared at the point at which the specified number of bytes of data have been transferred.)

Table 3. $P5_3/\overline{S_{RDY1}}/\overline{CS}$ selection

$SC1_6$	$SC1_4$	$SIOAC_0$	$P5_3/\overline{S_{RDY1}}/\overline{CS}$
0	0	X	$P5_3$
	1	0	$\overline{S_{RDY1}}$
		1	$\overline{CS}$

Note. $SC1_4$: $\overline{S_{RDY1}}$ output selection bit
$SC1_6$: Synchronization clock selection bit
$SIOAC_0$: Automatic transfer control bit

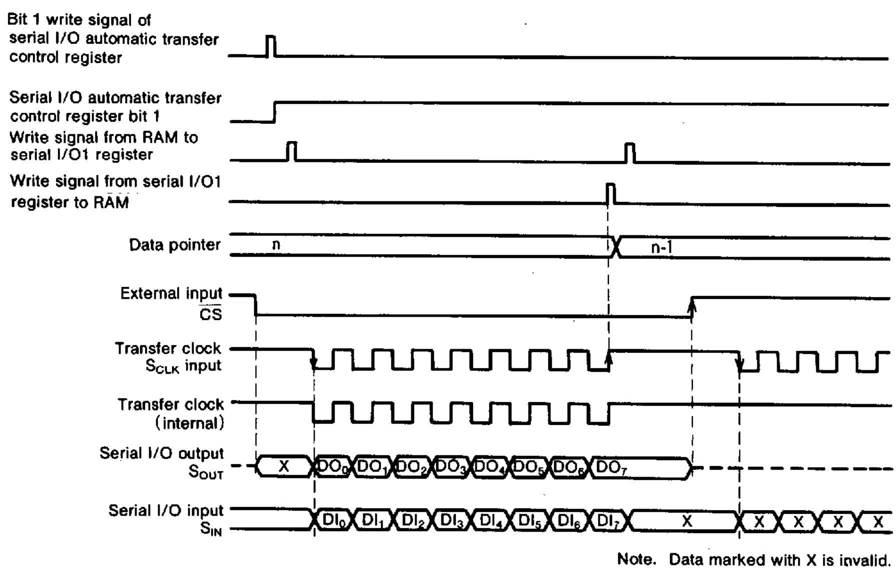


Fig. 20 Timing during serial I/O automatic transfer (external clock selected)

PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

The 3817 group has a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4MHz, the minimum resolution bit width is 500ns and the cycle period is 8192μs. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the X_{IN} clock.

The explanation in the rest of this data sheet assumes $f(X_{IN})$=4MHz.

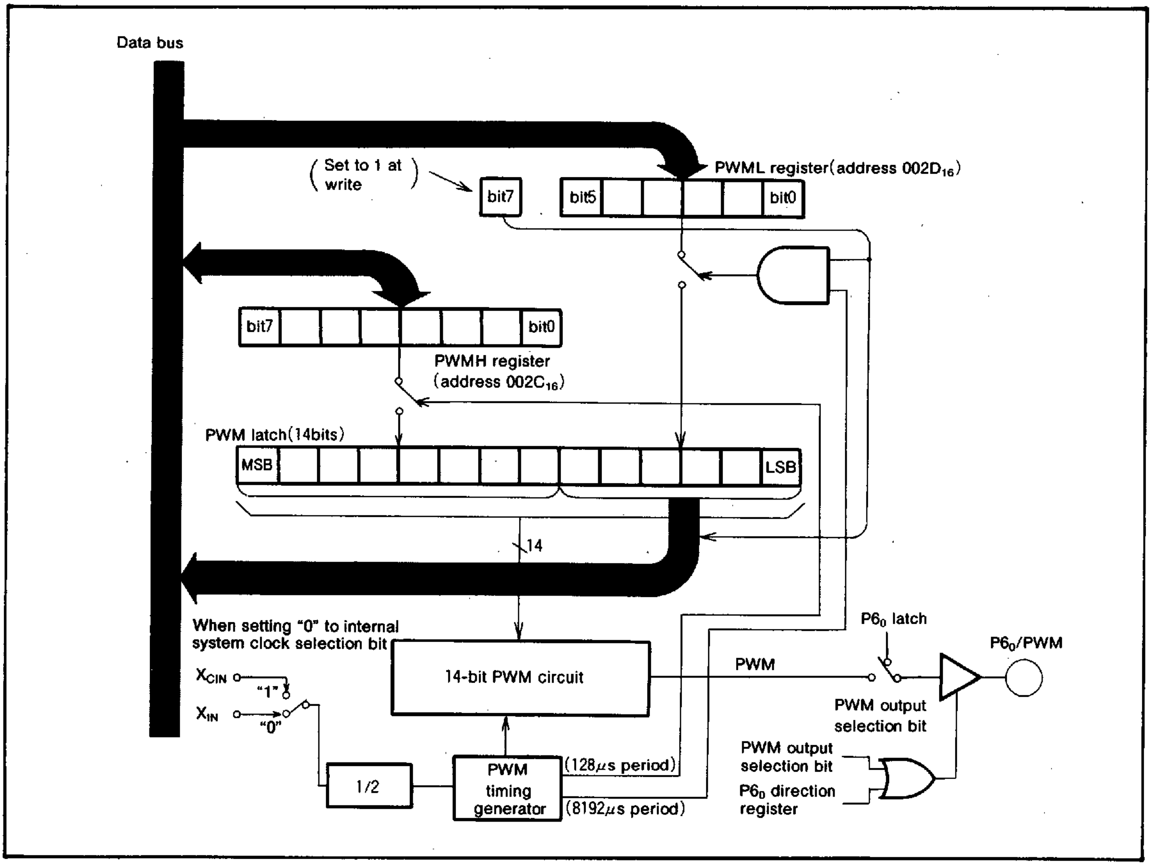


Fig. 21 PWM block diagram

Data Set-up

The PWM output pin also functions as port $P6_0$. Set port $P6_0$ to be the PWM output pin by setting bit 0 of the PWM mode register (address $002B_{16}$). The high-order eight bits of output data are set in the high-order PWM register PWMH (address $002C_{16}$) and the low-order six bits are set in the low-order PWM register PWML (address $002D_{16}$).

Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 8192μs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 128μs). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

Table 4. Relationship between lower 6 bits of data and period set by the ADD bit

Lower 6 Bits of Data(PWML)	Sub-periods tm Lengthened (m =0 to 63)
0 0 0 0 0 0 (LSB)	None
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ……………, 57, 59, 61, 63

PWM Operation

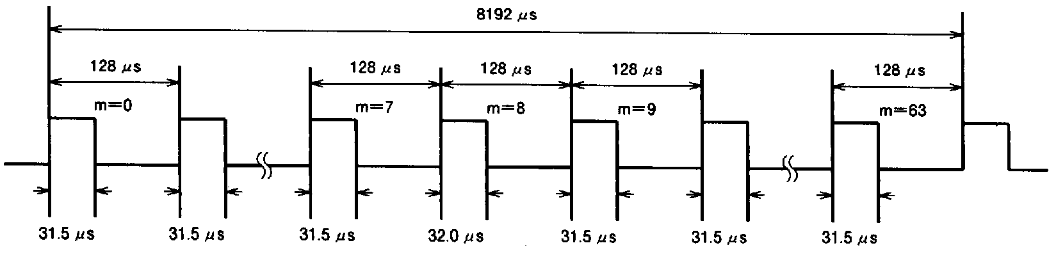
The timing of the 14-bit PWM function is shown in Fig. 24. The 14-bit PWM data is divided into the low-order six bits and the high-order eight bits in the PWM latch.

The high-order eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256× τ (128μs) long. The signal is "H" for a length equal to N times τ, where τ is the minimum resolution (500ns).

The contents of the low-order six bits of data enable the lengthening of the high signal by τ (500ns). As shown in Fig. 21, the six bits of PWML determine which subcycles are lengthened.

As shown in Fig. 24, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the high-order eight bits of the 14-bit data are 03_{16} and the low-order six bits are 05_{16}, the length of the "H"-level output in sub-periods t_8, t_{24}, t_{32}, t_{40}, and t_{56} is 4τ, and its length 3τ in all other sub-periods.



Pulse width modulation register H : 00111111
Pulse width modulation register L : 000101
Sub-periods where "H" pulse width is 32 μs : m = 8, 24, 32, 40, 56
Sub-periods where "H" pulse width is 31.5 μs : m = all other values

Fig. 22 PWM timing

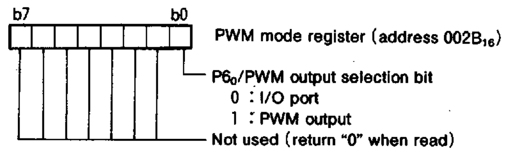


Fig. 23 Structure of PWM mode register

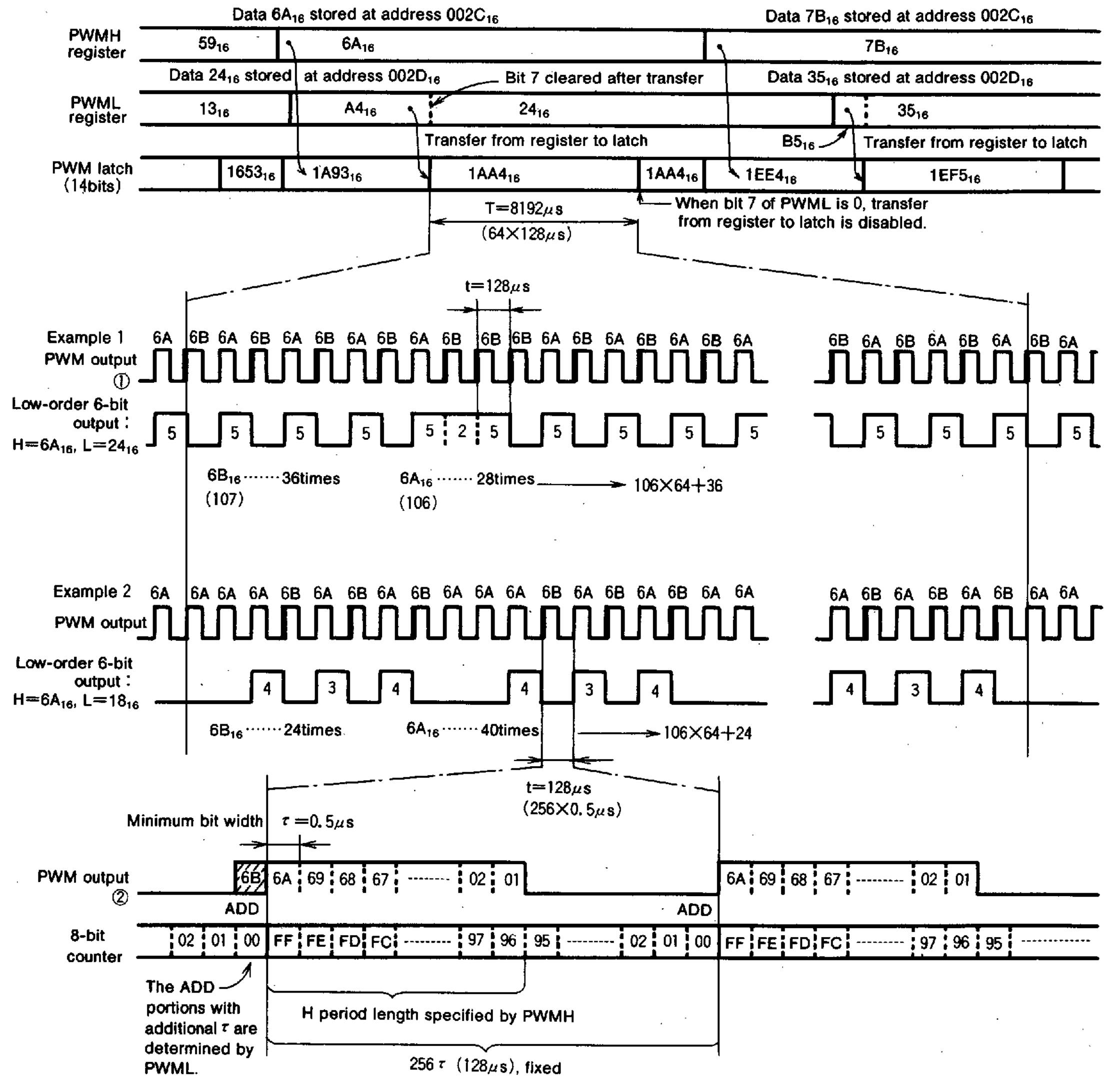


Fig. 24 14-bit PWM timing

A-D CONVERTER

The functional blocks of the A-D converter are described below.

A-D Conversion Register (AD) 0031_{16}

The A-D conversion register is a read-only register that stores the result of an A-D conversion. This register should not be read during an A-D conversion.

A-D Control Register (ADCON) 0030_{16}

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports $P7_7/AN_7$ to $P7_0/AN_0$

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Note that the comparator is constructed linked to a capacitor, so set f (X_{IN}) to at least 500kHz during A-D conversion.

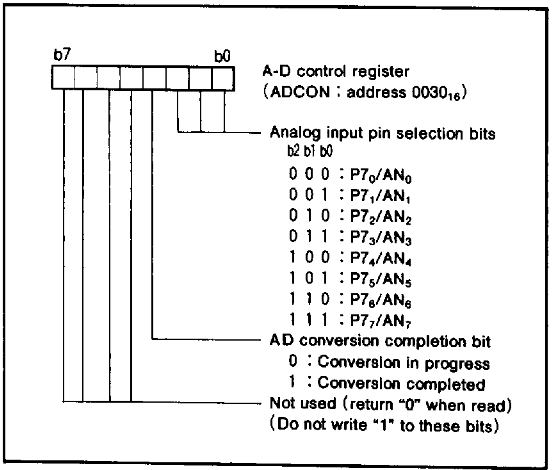


Fig. 25 Structure of A-D control register

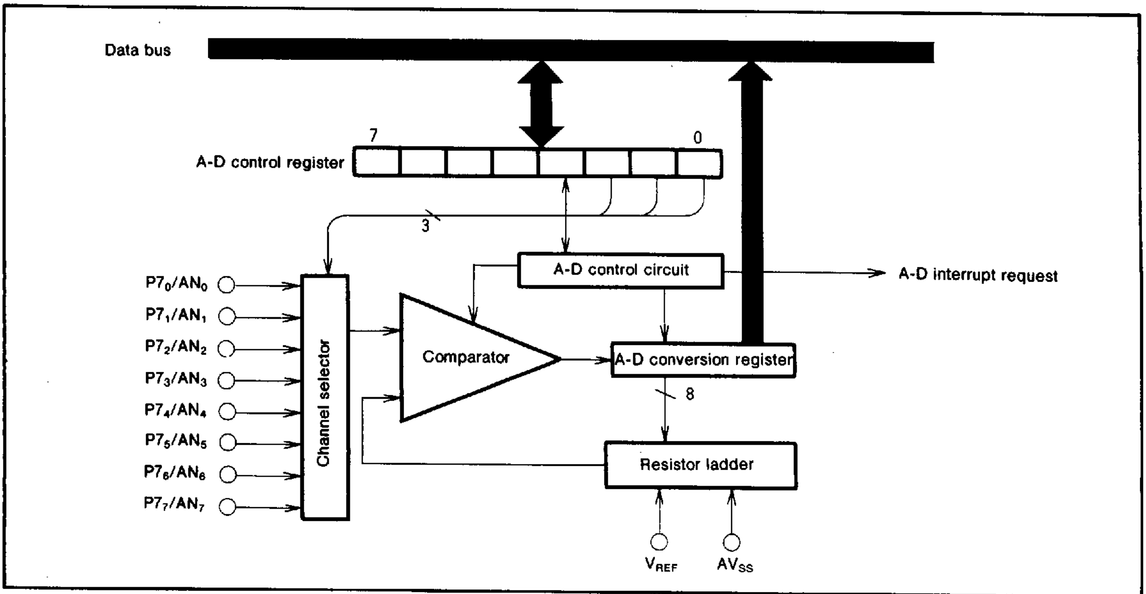


Fig. 26 A-D converter block diagram

FLD CONTROLLER

The 3817 group has fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 24 pins for segments
- 16 pins for digits
- FLDC mode register
- FLD data pointer
- FLD data pointer reload register
- Port P0 segment/digit switching register
- Port P1 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- 48-byte FLD automatic display RAM

Eight to twenty-four pins can be used as segment pins and four to sixteen pins can be used as digit pins.

Note that only 32 pins (maximum) can be used as segment and digit pins.

In the FLD automatic display mode ports $P1_0$ to $P1_3$ function as digit pins DIG_8 to DIG_{11} automatically.

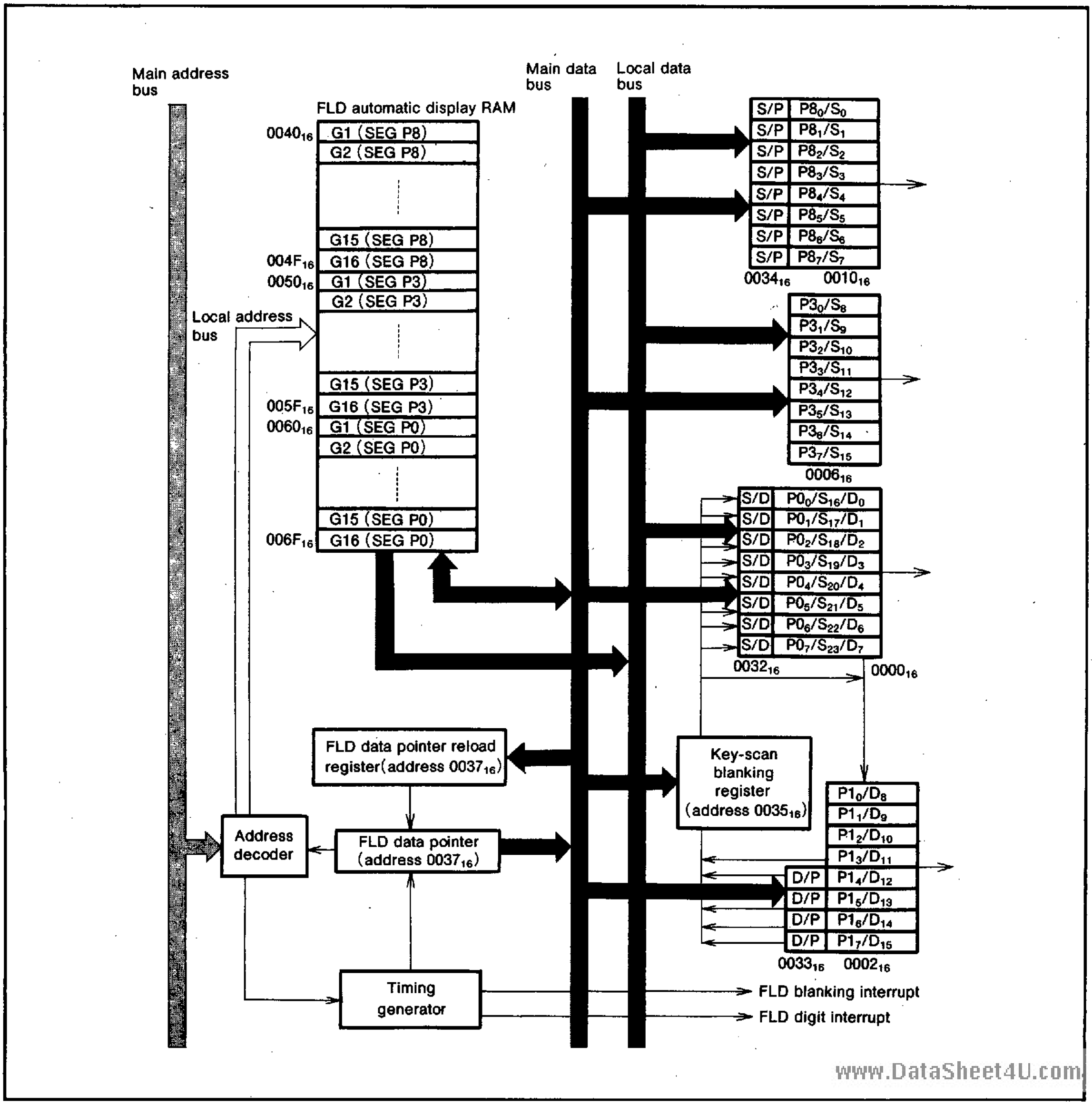


Fig. 27 FLD control circuit block diagram

FLDC Mode Register (FLDM) 0036_{16}

The FLDC mode register (address 0036_{16}) is a seven bit control register which is used to control the FLD automatic display.

Key-scan Blanking Register (KSCN) 0035_{16}

The key-scan blanking register (address 0035_{16}) is a two bit register which sets the blanking period T_{scan} between the last digit and the first digit of the next cycle.

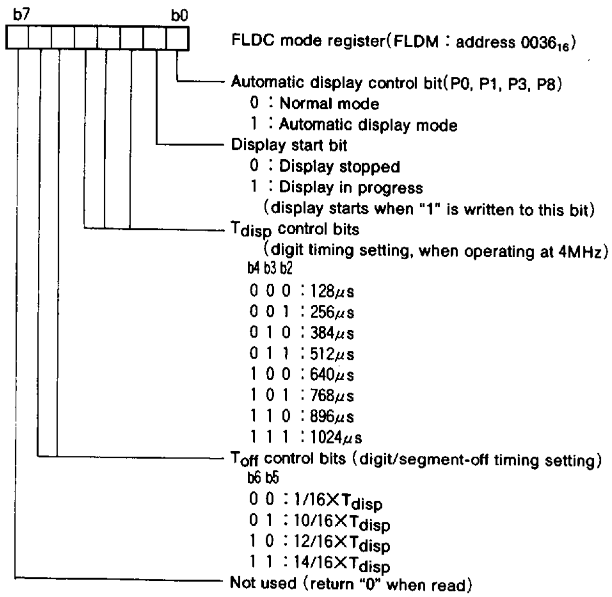


Fig. 28 Structure of FLDC mode register (FLDM)

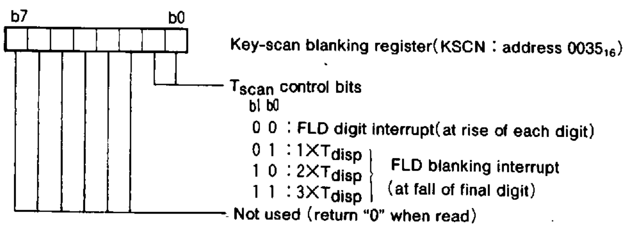


Fig. 29 Structure of key-scan blanking register (KSCN)

FLD Automatic Display Pins

The FLD automatic display function of Ports P0, P1, P3, and P8 is selected by setting the automatic display control bit of the FLDC mode register (address 0036_{16}) to "1".
When using the FLD automatic display mode, set the number of segments and digits for each port.

Table 5. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
$P8_0$-$P8_7$	SEG_0-SEG_7 or $P8_0$-$P8_7$	The individual bits of the Port P8 segment/port switching register (address 0034_{16}) can be used to set each pin to either segment ("1") or normal port input ("0"). (Note)
$P3_0$-$P3_7$	SEG_8-SEG_{15}	None (segment only)
$P0_0$-$P0_7$	SEG_{16}-SEG_{23} or DIG_0-DIG_7	The individual bits of the Port P0 segment/digit switching register (address 0032_{16}) can be used to set each pin to segment ("1") or digit ("0"). (Note)
$P1_0$-$P1_3$	DIG_8-DIG_{11}	None (digit only, use all bits always.)
$P1_4$-$P1_7$	DIG_{12}-DIG_{15} or $P1_4$-$P1_7$	The individual bits of the Port P1 digit/port switching register (address 0033_{16}) can be used to set each pin to digit ("1") or normal port output ("0"). (Note)

Note. Always set digits in sequence.

Number of segments / Number of digits	16 / 4	8 / 12	16 / 10	24 / 8	16 / 16
Port P8 (has Port P8 segment/port switching register)	0 $P8_0$	0 $P8_0$	0 $P8_0$	1 SEG_0	1 SEG_0
	0 $P8_1$	0 $P8_1$	0 $P8_1$	1 SEG_1	1 SEG_1
	0 $P8_2$	0 $P8_2$	0 $P8_2$	1 SEG_2	1 SEG_2
	0 $P8_3$	0 $P8_3$	0 $P8_3$	1 SEG_3	1 SEG_3
	0 $P8_4$	0 $P8_4$	1 SEG_4	1 SEG_4	1 SEG_4
	0 $P8_5$	0 $P8_5$	1 SEG_5	1 SEG_5	1 SEG_5
	0 $P8_6$	0 $P8_6$	1 SEG_6	1 SEG_6	1 SEG_6
	0 $P8_7$	0 $P8_7$	1 SEG_7	1 SEG_7	1 SEG_7
Port P3 (segment only)	SEG_8	SEG_8	SEG_8	SEG_8	SEG_8
	SEG_9	SEG_9	SEG_9	SEG_9	SEG_9
	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}
	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}
	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}
	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}
	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}
	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}
Port P0 (has Port P0 segment/digit switching register)	1 SEG_{16}	0 $DIG_0 \rightarrow G12$	1 SEG_{16}	1 SEG_{16}	0 $DIG_0 \rightarrow G16$
	1 SEG_{17}	0 $DIG_1 \rightarrow G11$	1 SEG_{17}	1 SEG_{17}	0 $DIG_1 \rightarrow G15$
	1 SEG_{18}	0 $DIG_2 \rightarrow G10$	1 SEG_{18}	1 SEG_{18}	0 $DIG_2 \rightarrow G14$
	1 SEG_{19}	0 $DIG_3 \rightarrow G9$	1 SEG_{19}	1 SEG_{19}	0 $DIG_3 \rightarrow G13$
	1 SEG_{20}	0 $DIG_4 \rightarrow G8$	0 $DIG_4 \rightarrow G10$	1 SEG_{20}	0 $DIG_4 \rightarrow G12$
	1 SEG_{21}	0 $DIG_5 \rightarrow G7$	0 $DIG_5 \rightarrow G9$	1 SEG_{21}	0 $DIG_5 \rightarrow G11$
	1 SEG_{22}	0 $DIG_6 \rightarrow G6$	0 $DIG_6 \rightarrow G8$	1 SEG_{22}	0 $DIG_6 \rightarrow G10$
	1 SEG_{23}	0 $DIG_7 \rightarrow G5$	0 $DIG_7 \rightarrow G7$	1 SEG_{23}	0 $DIG_7 \rightarrow G9$
Port P1 (has Port P1 digit/port switching register)	$DIG_8 \rightarrow G4$	$DIG_8 \rightarrow G4$	$DIG_8 \rightarrow G6$	$DIG_8 \rightarrow G8$	$DIG_8 \rightarrow G8$
	$DIG_9 \rightarrow G3$	$DIG_9 \rightarrow G3$	$DIG_9 \rightarrow G5$	$DIG_9 \rightarrow G7$	$DIG_9 \rightarrow G7$
	$DIG_{10} \rightarrow G2$	$DIG_{10} \rightarrow G2$	$DIG_{10} \rightarrow G4$	$DIG_{10} \rightarrow G6$	$DIG_{10} \rightarrow G6$
	$DIG_{11} \rightarrow G1$	$DIG_{11} \rightarrow G1$	$DIG_{11} \rightarrow G3$	$DIG_{11} \rightarrow G5$	$DIG_{11} \rightarrow G5$
	0 $P1_4$	0 $P1_4$	1 $DIG_{12} \rightarrow G2$	1 $DIG_{12} \rightarrow G4$	1 $DIG_{12} \rightarrow G4$
	0 $P1_5$	0 $P1_5$	1 $DIG_{13} \rightarrow G1$	1 $DIG_{13} \rightarrow G3$	1 $DIG_{13} \rightarrow G3$
	0 $P1_6$	0 $P1_6$	0 $P1_6$	1 $DIG_{14} \rightarrow G2$	1 $DIG_{14} \rightarrow G2$
	0 $P1_7$	0 $P1_7$	0 $P1_7$	1 $DIG_{15} \rightarrow G1$	1 $DIG_{15} \rightarrow G1$

Fig. 30 Segment/digit setting example

FLD Automatic Display RAM

The FLD automatic display RAM area is the 48 bytes from address 0040_{16} to $006F_{16}$. The FLD automatic display RAM area can be used to store 3-byte data items for a maximum of 16 digits. Addresses 0040_{16} to $004F_{16}$ are used for P8 segment data, addresses 0050_{16} to $005F_{16}$ are used for P3 segment data, and addresses 0060_{16} to $006F_{16}$ are used for P0 segment data.

FLD Data Pointer and FLD Data Pointer Reload Register

The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment, and the FLD data pointer reload register indicates the address of the first digit of segment P0.

Both the FLD data pointer and the FLD data pointer reload register are allocated to address 0037_{16} and are 6-bits wide. Data written to this address is written to the FLD data pointer reload register, data read from this address is read from the FLD data pointer.

The actual memory address is the value of the data pointer plus 40_{16}.

The contents of the FLD data pointer indicate the first address of segment P0 (the content of the FLD data pointer reload register) at the start of automatic display. The content of the FLD data pointer changes repeatedly as follows: when transferring the segment P0 data to the segment, the content decreases by −16; when transferring the segment P3 data to the segment, it decreases by − 16; when transferring the segment P8 data to the segment, it increases by +31. After it reaches "00_{16}", the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, three bytes of data for the P0, P3, and P8 segments of one digit are transferred.

Address \ Bit	7	6	5	4	3	2	1	0	
0040_{16}	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	← Final digit (final data of segment P8)
0041_{16}	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	
⋮	⋮			⋮					Segment P8 data area
$004E_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	
$004F_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	
0050_{16}	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	← Final digit (final data of segment P3)
0051_{16}	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	
⋮	⋮			⋮					Segment P3 data area
$005E_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	
$005F_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	
0060_{16}	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	← Final digit (final data of segment P0)
0061_{16}	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	
⋮	⋮			⋮					Segment P0 data area
$006E_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	
$006F_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	

Fig. 31 FLD automatic display RAM and bit allocation

Data Setup

When data is stored in the FLD automatic display RAM, the end of segment P8 data is stored at address 0040_{16}, the end of segment P3 data is stored at address 0050_{16}, and the end of segment P0 data is stored at address 0060_{16}. The head of each of the segment P8, P3, and P0 data is stored at an address that is the number of digits−1 away from the corresponding address 0040_{16}, 0050_{16}, 0060_{16}.

Set the value (the number of digits −1) to the low-order four bits of the FLD data pointer reload register. "1" is always written to bit 5, and "0" is always written to bit 4. Note that "0" is always read from bit 5 or 4 during a read.

For 17 segments and 15 digits
(FLD data pointer reload register=14)

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	///	///	///	///	///	///	///	///
0041_{16}	///	///	///	///	///	///	///	///
0042_{16}	///	///	///	///	///	///	///	///
0043_{16}	///	///	///	///	///	///	///	///
0044_{16}	///	///	///	///	///	///	///	///
0045_{16}	///	///	///	///	///	///	///	///
0046_{16}	///	///	///	///	///	///	///	///
0047_{16}	///	///	///	///	///	///	///	///
0048_{16}	///	///	///	///	///	///	///	///
0049_{16}	///	///	///	///	///	///	///	///
$004A_{16}$	///	///	///	///	///	///	///	///
$004B_{16}$	///	///	///	///	///	///	///	///
$004C_{16}$	///	///	///	///	///	///	///	///
$004D_{16}$	///	///	///	///	///	///	///	///
$004E_{16}$	///	///	///	///	///	///	///	///
$004F_{16}$								
0050_{16}	///	///	///	///	///	///	///	///
0051_{16}	///	///	///	///	///	///	///	///
0052_{16}	///	///	///	///	///	///	///	///
0053_{16}	///	///	///	///	///	///	///	///
0054_{16}	///	///	///	///	///	///	///	///
0055_{16}	///	///	///	///	///	///	///	///
0056_{16}	///	///	///	///	///	///	///	///
0057_{16}	///	///	///	///	///	///	///	///
0058_{16}	///	///	///	///	///	///	///	///
0059_{16}	///	///	///	///	///	///	///	///
$005A_{16}$	///	///	///	///	///	///	///	///
$005B_{16}$	///	///	///	///	///	///	///	///
$005C_{16}$	///	///	///	///	///	///	///	///
$005D_{16}$	///	///	///	///	///	///	///	///
$005E_{16}$	///	///	///	///	///	///	///	///
$005F_{16}$								
0060_{16}								///
0061_{16}								///
0062_{16}								///
0063_{16}								///
0064_{16}								///
0065_{16}								///
0066_{16}								///
0067_{16}								///
0068_{16}								///
0069_{16}								///
$006A_{16}$								///
$006B_{16}$								///
$006C_{16}$								///
$006D_{16}$								///
$006E_{16}$								///
$006F_{16}$								

For 24 segments and 8 digits
(FLD data pointer reload register=7)

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	///	///	///	///	///	///	///	///
0041_{16}	///	///	///	///	///	///	///	///
0042_{16}	///	///	///	///	///	///	///	///
0043_{16}	///	///	///	///	///	///	///	///
0044_{16}	///	///	///	///	///	///	///	///
0045_{16}	///	///	///	///	///	///	///	///
0046_{16}	///	///	///	///	///	///	///	///
0047_{16}	///	///	///	///	///	///	///	///
0048_{16}								
0049_{16}								
$004A_{16}$								
$004B_{16}$								
$004C_{16}$								
$004D_{16}$								
$004E_{16}$								
$004F_{16}$								
0050_{16}	///	///	///	///	///	///	///	///
0051_{16}	///	///	///	///	///	///	///	///
0052_{16}	///	///	///	///	///	///	///	///
0053_{16}	///	///	///	///	///	///	///	///
0054_{16}	///	///	///	///	///	///	///	///
0055_{16}	///	///	///	///	///	///	///	///
0056_{16}	///	///	///	///	///	///	///	///
0057_{16}	///	///	///	///	///	///	///	///
0058_{16}								
0059_{16}								
$005A_{16}$								
$005B_{16}$								
$005C_{16}$								
$005D_{16}$								
$005E_{16}$								
$005F_{16}$								
0060_{16}	///	///	///	///	///	///	///	///
0061_{16}	///	///	///	///	///	///	///	///
0062_{16}	///	///	///	///	///	///	///	///
0063_{16}	///	///	///	///	///	///	///	///
0064_{16}	///	///	///	///	///	///	///	///
0065_{16}	///	///	///	///	///	///	///	///
0066_{16}	///	///	///	///	///	///	///	///
0067_{16}	///	///	///	///	///	///	///	///
0068_{16}								
0069_{16}								
$006A_{16}$								
$006B_{16}$								
$006C_{16}$								
$006D_{16}$								
$006E_{16}$								
$006F_{16}$								

Note. /// Shaded areas are not used.

Fig. 32 Example of using the FLD automatic display RAM

Timing Setting

The digit timing (T_{disp}) and digit/segment turn-off timing (T_{off}) can be set by the FLDC mode register (address 0036_{16}). The scan timing (T_{scan}) can be set by the key-scan blanking register (address 0035_{16}).

Note that flickering will occur if the repetition frequency ($1/(T_{disp} \times$ number of digits $+ T_{scan}$)) is an integral multiple of the digit timing T_{disp}.

FLD Start

To perform FLD automatic display, you have to use the following registers.

- Port P0 segment/digit switching register
- Port P1 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- FLD data pointer
- FLDC mode register

Automatic display mode is activated by writing "1" to bit 0 of the FLDC mode register (address 0036_{16}), and the automatic display is started by writing "1" to bit 1.

During automatic display bit 1 always keeps "1", automatic display can be interrupted by writing "0" to bit 1.

If key-scan is to be performed by segment during the key-scan blanking period T_{scan},

1. Write "0" to bit 0 (automatic display control bit) of FLDC mode register (address 0036_{16}).
2. Set the port corresponding to the segment to the normal port.
3. After the key-scan is performed, write "1" (automatic display mode) to bit 0 of FLDC mode register (address 0036_{16}).

Note on performance of key-scan in the above 1 to 3 order.

1. Do not write "0" to bit 1 of FLDC mode register (address 0036_{16}).
2. Do not write "1" to the port corresponding to the digit.

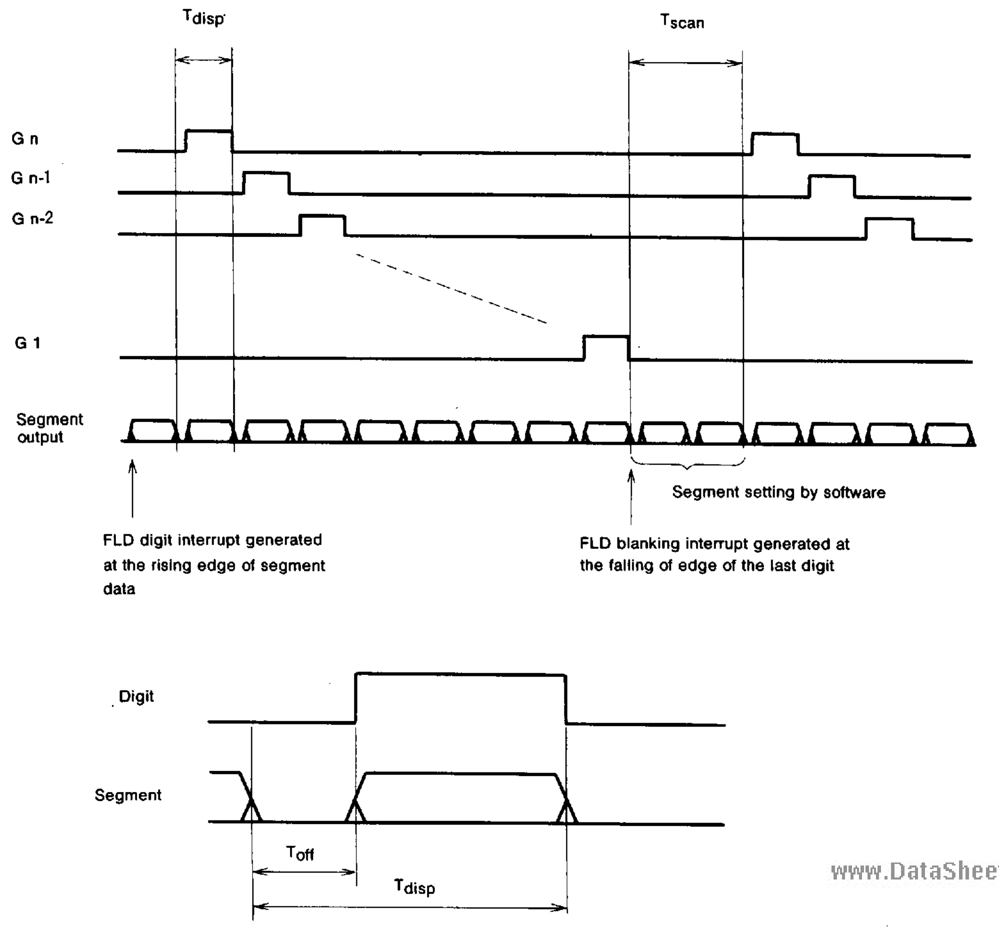


Fig. 33 FLDC timing

RESET CIRCUIT

After a reset, the microcomputer will start in high-speed operation start mode or low-speed operation start mode depending on a mask-programmable option.

High-Speed Operation Start Mode

In high-speed operation start mode, to reset the microcomputer occurs, the $\overline{RESET}$ pin is held at an "L" level for 2μs or more. Then is returned to an "H" level (the power source voltage should be between 4.0V and 5.5V), reset is released. Both the X_{IN} and the X_{CIN} clocks begin oscillating. In order to give the X_{IN} clock time to stabilize, internal operation begins until after 13 X_{IN} clock cycles are completed. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte).

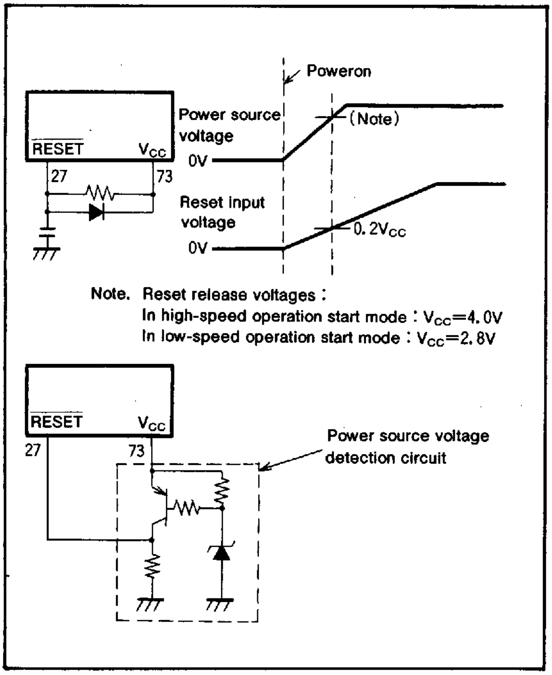


Fig. 34 Poweron reset circuit example

Low-Speed Operation Start Mode

In low-speed operation start mode, to reset the microcomputer occurs, the $\overline{RESET}$ pin is held at a "L" level for 2μs or more. Then is returned to an "H" level (the power source voltage should be between 2.8V and 5.5V). The X_{IN} clock does not begin oscillating. In order to give the X_{CIN} time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the $X_{CIN}/16$ are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte).

If the X_{CIN} clock is stable, reset will complete after approximately 250ms (assuming $f(X_{CIN})$=32.768kHz).

Immediately after a poweron, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.

Note on Use

Make sure that the reset input voltage is less than 0.8V in high-speed operation start mode, or less than 0.5V in low-speed operation start mode.

	Register	Address	Register contents
(1)	Port P0 register	(0000_{16})···	00_{16}
(2)	Port P1 register	(0002_{16})···	00_{16}
(3)	Port P2 register	(0004_{16})···	00_{16}
(4)	Port P2 direction register	(0005_{16})···	00_{16}
(5)	Port P3 register	(0006_{16})···	00_{16}
(6)	Port P4 register	(0008_{16})···	00_{16}
(7)	Port P4 direction register	(0009_{16})···	00_{16}
(8)	Port P5 register	($000A_{16}$)···	00_{16}
(9)	Port P5 direction register	($000B_{16}$)···	00_{16}
(10)	Port P6 register	($000C_{16}$)···	00_{16}
(11)	Port P6 direction register	($000D_{16}$)···	00_{16}
(12)	Port P7 register	($000E_{16}$)···	00_{16}
(13)	Port P7 direction register	($000F_{16}$)···	00_{16}
(14)	Port P8 register	(0010_{16})···	00_{16}
(15)	Port P8 direction register	(0011_{16})···	00_{16}
(16)	Serial I/O1 control register	(0019_{16})···	00_{16}
(17)	Serial I/O automatic transfer control register	($001A_{16}$)···	00_{16}
(18)	Serial I/O automatic transfer interval register	($001C_{16}$)···	00_{16}
(19)	Serial I/O2 control register	($001D_{16}$)···	00_{16}
(20)	Timer 1 register	(0020_{16})···	FF_{16}
(21)	Timer 2 register	(0021_{16})···	01_{16}
(22)	Timer 3 register	(0022_{16})···	FF_{16}
(23)	Timer 4 register	(0023_{16})···	FF_{16}
(24)	Timer 5 register	(0024_{16})···	FF_{16}
(25)	Timer 6 register	(0025_{16})···	FF_{16}
(26)	Timer 12 mode register	(0028_{16})···	00_{16}
(27)	Timer 34 mode register	(0029_{16})···	00_{16}
(28)	Timer 56 mode register	($002A_{16}$)···	00_{16}
(29)	PWM control register	($002B_{16}$)···	00_{16}
(30)	A-D control register	(0030_{16})···	08_{16}
(31)	Port P0 segment/digit switching register	(0032_{16})···	00_{16}
(32)	Port P1 digit/port switching register	(0033_{16})···	00_{16}
(33)	Port P8 segment/port switching register	(0034_{16})···	00_{16}
(34)	Key-scan blanking register	(0035_{16})···	00_{16}
(35)	FLDC mode register	(0036_{16})···	00_{16}
(36)	High-breakdown-voltage port control register	(0038_{16})···	00_{16}
(37)	Interrupt edge selection register	($003A_{16}$)···	00_{16}
(38)	CPU mode register	($003B_{16}$)···	* * 1 0 0 0 0 0
(39)	Interrupt request register 1	($003C_{16}$)···	00_{16}
(40)	Interrupt request register 2	($003D_{16}$)···	00_{16}
(41)	Interrupt control register 1	($003E_{16}$)···	00_{16}
(42)	Interrupt control register 2	($003F_{16}$)···	00_{16}
(43)	Processor status register	(PS)···	× × × × × 1 × ×
(44)	Program counter	(PC_H)···	Contents of address $FFFD_{16}$
		(PC_L)···	Contents of address $FFFC_{16}$

Note. * : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option.
× : Underfined
The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values.

Fig. 35 Internal status at reset

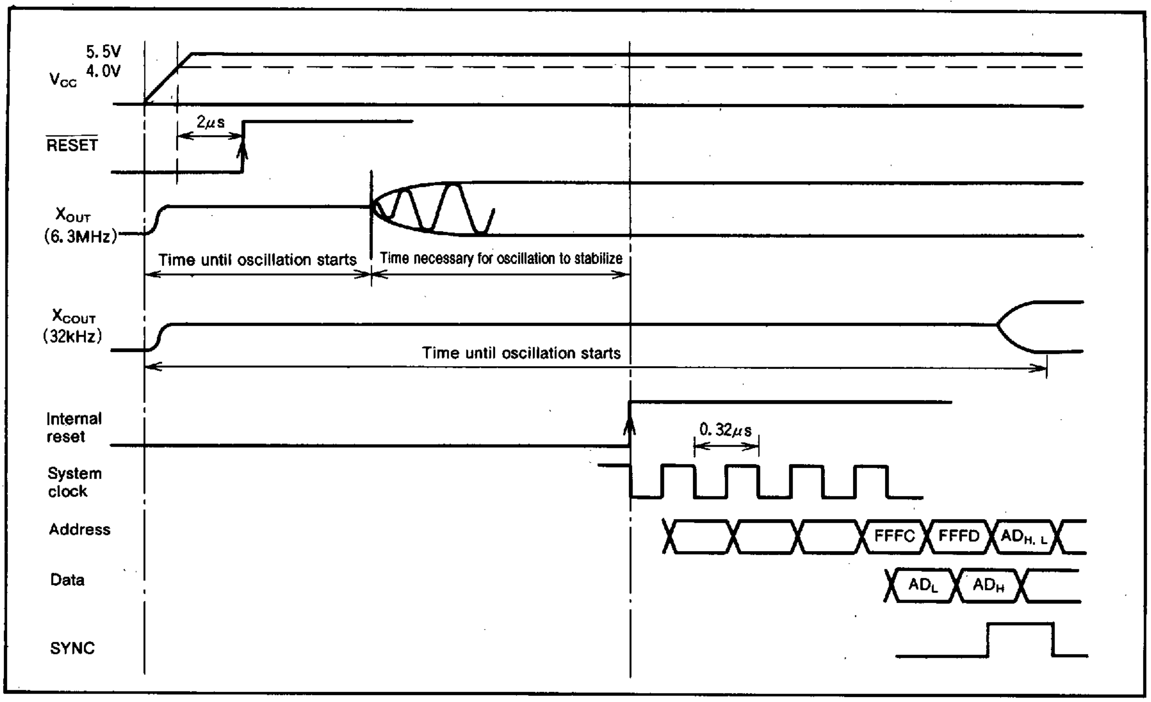


Fig. 36 Reset sequence in high-speed operation mode

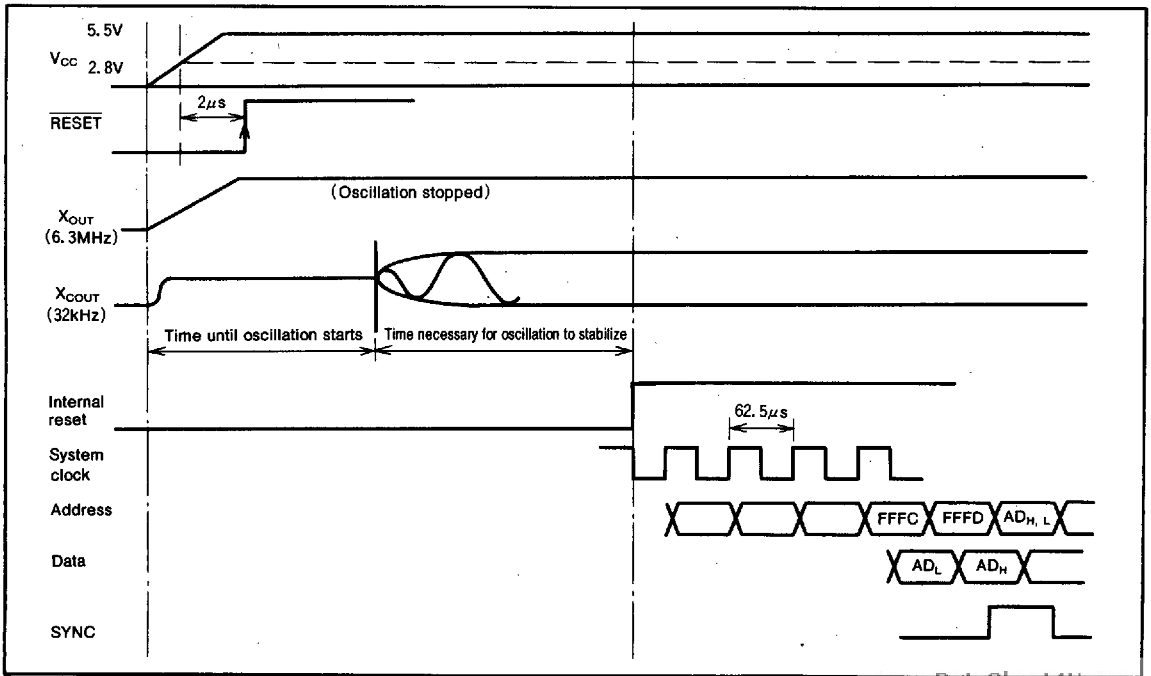


Fig. 37 Reset sequence in low-speed operation mode

CLOCK GENERATING CIRCUIT

To supply a clock signal externally, input to the X_{IN} (X_{CIN}) pin and make the X_{OUT} (X_{COUT}) pin open. If the X_{CIN} clock is not used, connect the X_{CIN} pin to V_{SS}, and leave the X_{COUT} pin open.

Either high-speed operation start mode or low-speed operation start mode can be selected by using a mask option.

High-Speed Operation Start Mode

After reset has completed, the internal clock ϕ is half the frequency of X_{IN}. Immediately after poweron, both the X_{IN} and X_{CIN} clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address $003B_{16}$) to "1".

Low-Speed Operation Start Mode

After reset has completed, the internal clock ϕ is half the frequency of X_{CIN}. Immediately after poweron, only the X_{CIN} clock starts oscillating. To set the internal clock ϕ to high-speed operation mode, first set bit 6 (CM_6) of the CPU mode register (address $003B_{16}$) to "0", the set bit 7 (CM_7) to "0". Note that the program must allow time for oscillation to stabilize.

Oscillation Control

Stop Mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level. Timer 1 is set to "FF_{16}" and timer 2 is set to "01_{16}".

Either X_{IN} or X_{CIN} divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing a STP instruction. Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

Low-Speed Mode

If the internal clock is generated from the sub-clock (X_{CIN}), a low power consumption operation can be entered by stopping only the main clock X_{IN}. To stop the main clock, set bit 6 (CM_6) of the CPU mode register ($003B_{16}$) to "1". When the main clock X_{IN} is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the X_{CIN}-X_{COUT} drivability can be reduced, allowing even lower power consumption (20μA with f(X_{CIN})= 32kHz). To reduce the X_{CIN}-X_{COUT} drivability, clear bit 5 (CM_5) of the CPU mode register ($003B_{16}$) to "0". At reset or when a STP instruction is executed, this bit is set to "1" and strong drivability is selected to help the oscillation to start.

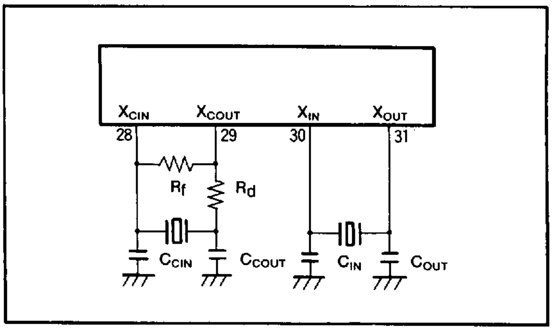


Fig. 38 Ceramic resonator circuit

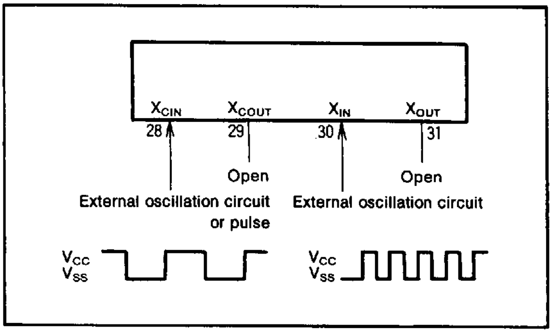
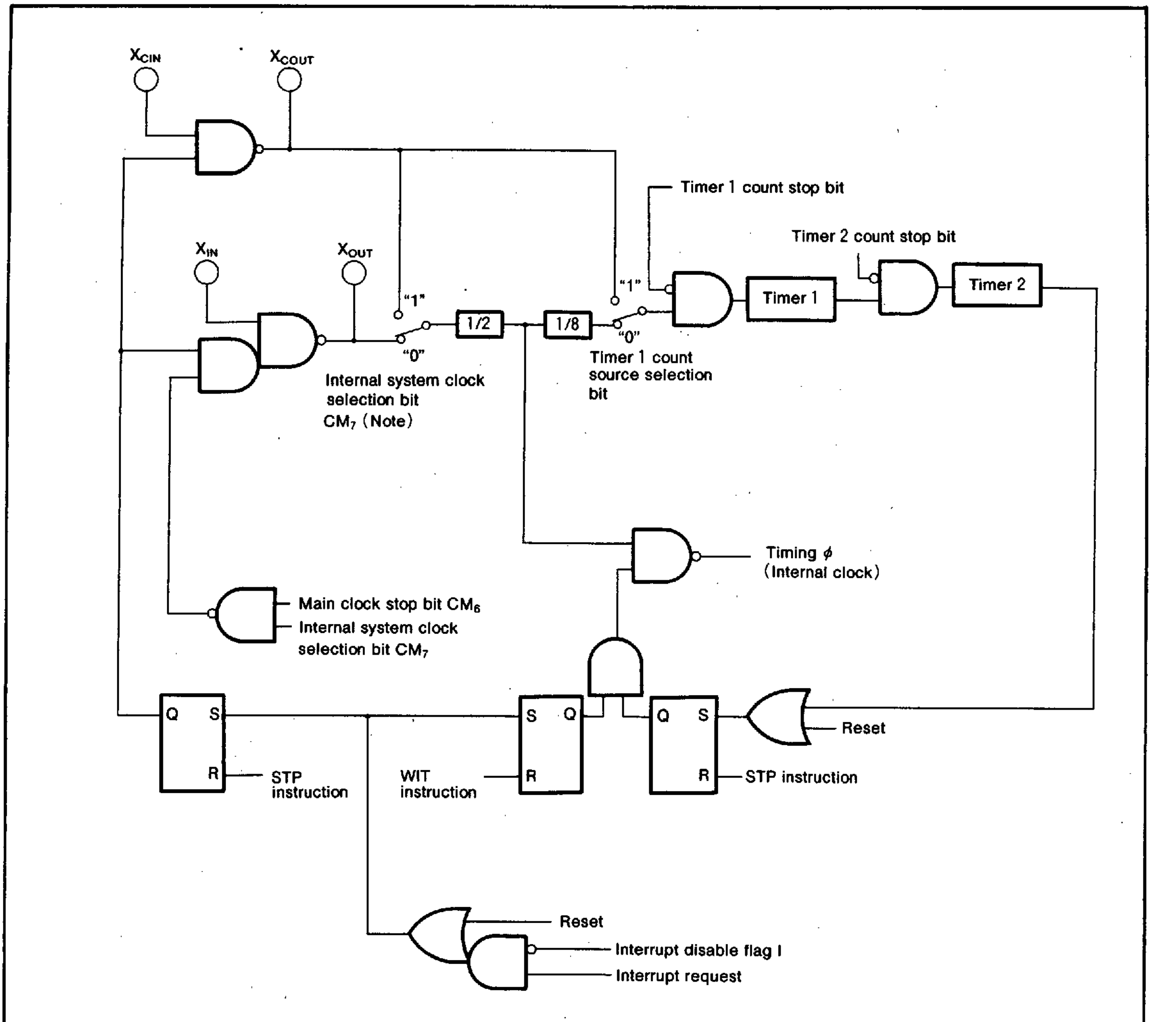
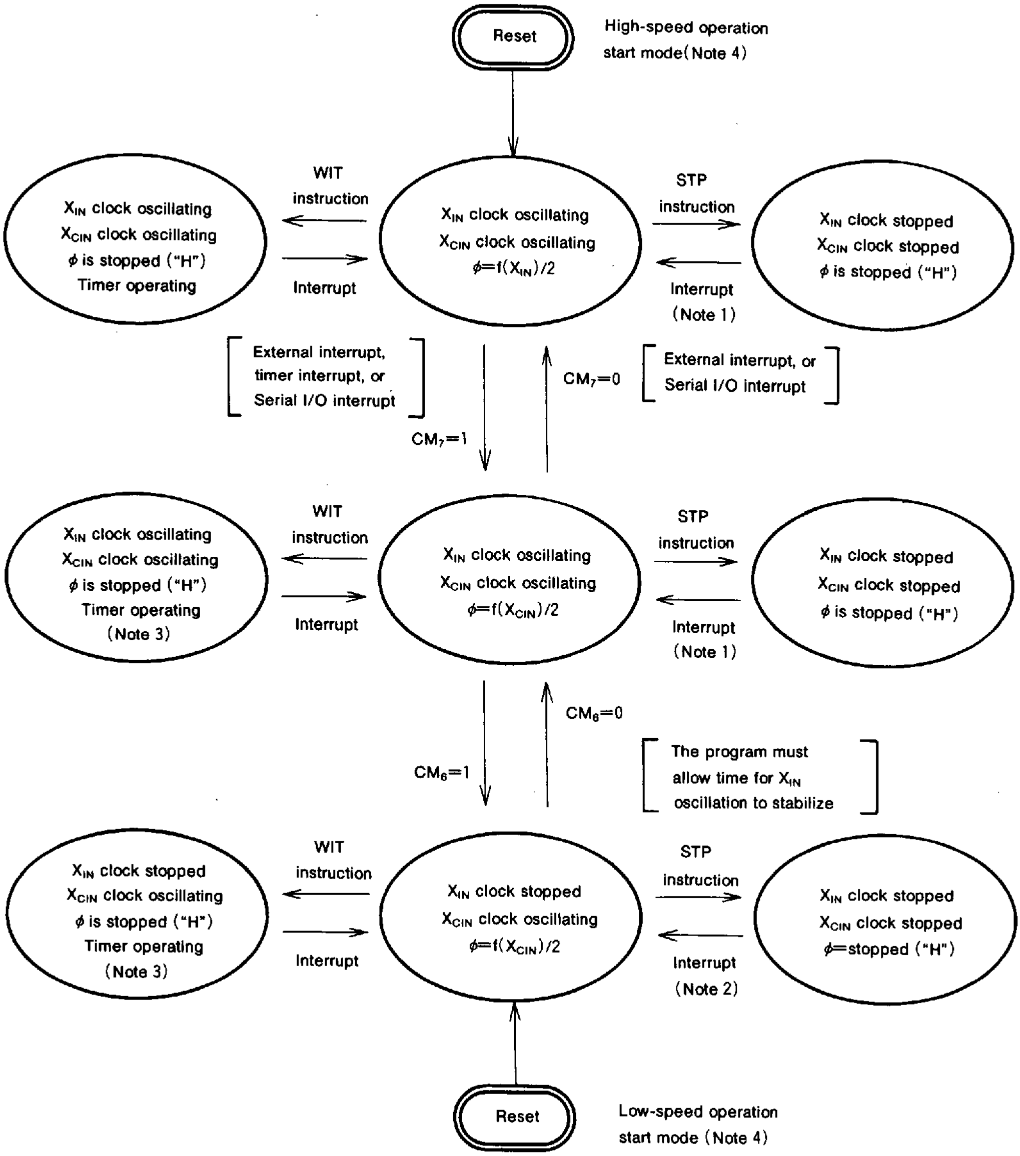


Fig. 39 External clock input circuit



Note. The values of CM_7 and CM_6 at reset are determined by a mask option.

Fig. 40 System clock generation circuit block diagram



The example assumes that 6.3MHz is being applied to the X_{IN} pin and 32kHz to the X_{CIN} pin.

Note 1. When the STP state is ended, a delay of approximately 1.3ms is automatically generated by timer 1 and timer 2.
2. The delay after the STP state ends is approximately 0.25s.
3. If the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is $f(X_{CIN})/16$.
4. Specify this option when ordering a mask ROM version.

Fig. 41 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written.
After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.
The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used :

- the data transfer instruction (LDA, etc.)
- the operation instruction when the index X mode flag (T) is "1"
- the addressing mode which uses the value of a direction register as an index.
- the bit-test instruction (BBC or BBS, etc.) to a direction register
- the read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.
Do not write "1" to bit 0 of the port P4 direction register (address 0009_{16})

Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.
When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.

Instruction Execution Timing

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the X_{IN} or X_{CIN} frequency.

At the STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.
The X_{COUT} drivability selection bit (the CPU mode register) is set to "1" (high drive) in order to start oscillating.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that $f(X_{IN})$ is 500kHz or more during an A-D conversion.
Do not execute the STP or WIT instruction during A-D conversion.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

If required, specify the following option on the Mask Confirmation Form:

- Operation start mode switching option

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 42 is recommended to verify programming.

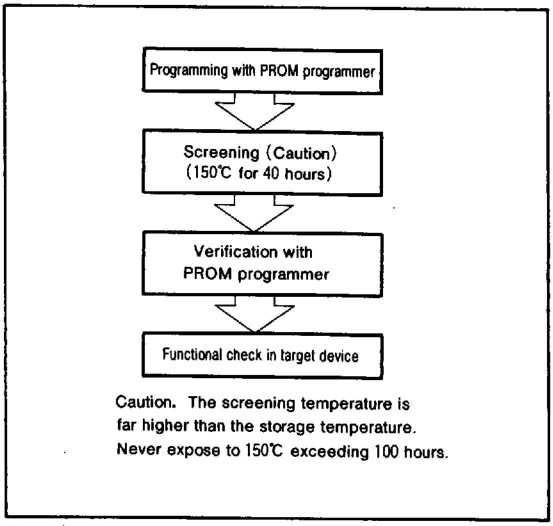


Fig. 42 Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	−0.3 to 7.0	V
V_{EE}	Pull-down power source voltage		V_{CC}−40 to V_{CC}+0.3	V
V_I	Input voltage $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_2$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P4_0$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P8_0$-$P8_7$		V_{CC}−40 to V_{CC}+0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage X_{CIN}		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$		V_{CC}−40 to V_{CC}+0.3	V
V_O	Output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$, X_{OUT}, X_{COUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	600	mW
T_{opr}	Operating temperature		−10 to 85	℃
T_{stg}	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage	High-speed operation mode	4.0	5.0	5.5	V
		Low-speed operation mode	2.8	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{EE}	Pull-down power source voltage		V_{CC}−38		V_{CC}	V
V_{REF}	Reference input voltage (when A-D converter is used)		2		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0-AN_7		0		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$-$P2_7$		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_0$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P8_0$-$P8_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$-$P2_7$		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P4_0$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P8_0$-$P8_7$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=4.0 to 5.5V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 1)			−240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_1$-$P4_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$ (Note 1)			−60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$ (Note 1)			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P6_0$ (Note 1)			3.0	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 1)			−120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_1$-$P4_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$ (Note 1)			−30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$ (Note 1)			50	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P6_0$ (Note 1)			1.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 2)			−40	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$ (Note 2)			−10	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$-$P2_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P4_1$-$P4_7$, $P5_0$-$P5_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$ (Note 2)			3.0	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 3)			−18	mA
$I_{OH(avg)}$	"H" average output current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$ (Note 3)			−5.0	mA
$I_{OL(avg)}$	"L" average output current $P2_0$-$P2_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$ (Note 3)			5.0	mA
$I_{OL(avg)}$	"L" average output current $P4_1$-$P4_7$, $P5_0$-$P5_7$ (Note 3)			5.0	mA
$I_{OL(avg)}$	"L" average output current $P6_0$ (Note 3)			1.5	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers 2 and 4 (duty cycle 50%)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			6.3	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current in an average value measured over 100ms.
4. When the oscillation frequency has a duty cycle of 50%.
5. When using the microcomputer in low-speed operation mode, make sure that the sub-clock input frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$	I_{OH}=−18mA	V_{CC}−2.0			V
V_{OH}	"H" output voltage $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$	I_{OH}=−10mA	V_{CC}−2.0			V
V_{OL}	"L" output voltage $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$	I_{OL}=10mA			2.0	V
V_{OL}	"L" output voltage $P6_0$	I_{OL}=1.5mA			0.5	V
V_{T+}−V_{T-}	Hysteresis INT_0-INT_4, S_{IN1}, S_{IN2}, S_{CLK1}, S_{CLK2}, $CNTR_0$, $CNTR_1$	When using a non-port function		0.4		V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$, X_{IN}	$\overline{RESET}$: V_{CC}=2.8V to 5.5V		0.5		V
V_{T+}−V_{T-}	Hysteresis X_{CIN}			0.5		V
I_{IH}	"H" input current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $P4_0$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $P8_0$-$P8_7$ (Note 1)	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{CIN}	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4		μA
I_{IL}	"L" input current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $P4_0$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $P8_0$-$P8_7$ (Note 1)	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{CIN}	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		−4		μA
I_{LOAD}	Output load current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$	V_{EE}=V_{CC}−36V, V_{OL}=V_{CC}, Output transistors "off"	150	500	900	μA
I_{LEAK}	Output leakage current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$	V_{EE}=V_{CC}−38V, V_{OL}=V_{CC}−38V, Output transistors "off" (Except for reset)			−10	μA
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V

Note 1. Except when reading ports P8.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	Power source current	• High-speed mode $f(X_{IN})$=6.3MHz $f(X_{CIN})$=32kHz Output transistors "off" A-D converter operating			7.5	15	mA
		• High-speed mode $f(X_{IN})$=6.3MHz (in WIT state) $f(X_{CIN})$=32kHz Output transistors "off" A-D converter stopped			1.5		mA
		• Low-speed mode $f(X_{IN})$= stopped, $f(X_{CIN})$=32kHz Low-power dissipation mode set (CM_5=0) Output transistors "off"			60	200	μA
		• Low-speed mode $f(X_{IN})$= stopped $f(X_{CIN})$=32kHz (in WIT state) Low-power dissipation mode set (CM_5=0) Output transistors "off"			20	40	μA
		All oscillation stopped (in STP state) Output transistors "off"	T_a=25℃		0.1	1.0	μA
			T_a=85℃			10	

A-D CONVERTER CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, high-speed operation mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	$V_{CC}=V_{REF}$=5.12V		±1	±2.5	LSB
T_{CONV}	Conversion time		49		50	$t_C(\phi)$
I_{VREF}	Reference input current	V_{REF}=5V	50	150	200	μA
I_{IA}	Analog port input current			0.5	5.0	μA
R_{LADDER}	Ladder resistor			35		kΩ

TIMING REQUIREMENTS (V_{CC} =4.0 to 5.5V, V_{SS} = 0V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width		2			µs
$t_{C(X_{IN})}$	Main clock input cycle time (X_{IN} input)		158			ns
$t_{WH(X_{IN})}$	Main clock input "H" pulse width		40			ns
$t_{WL(X_{IN})}$	Main clock input "L" pulse width		40			ns
$t_{C(X_{CIN})}$	Sub-clock input cycle time (X_{CIN} input)		20			µs
$t_{WH(X_{CIN})}$	Sub-clock input "H" pulse width		5.0			µs
$t_{WL(X_{CIN})}$	Sub-clock input "L" pulse width		5.0			µs
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time		4.0			µs
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, input "H" pulse width		1.6			µs
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, input "L" pulse width		1.6			µs
$t_{WH(INT)}$	INT_0-INT_4 input "H" pulse width		80			ns
$t_{WL(INT)}$	INT_0-INT_4 input "L" pulse width		80			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time		1.0			µs
$t_{WH(S_{CLK})}$	Serial I/O clock input clock "H" pulse width		400			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input clock "L" pulse width		400			ns
$t_{su(S_{CLK}-S_{IN})}$	Serial I/O input setup time		200			ns
$t_{h(S_{CLK}-S_{IN})}$	Serial I/O input hold time		200			ns

SWITCHING CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH(S_{CLK})}$	Serial I/O clock output "H" pulse width	C_L=100pF, R_L=1kΩ	$t_{C(S_{CLK})}/2-160$			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output "L" pulse width	C_L=100pF, R_L=1kΩ	$t_{C(S_{CLK})}/2-160$			ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial I/O output delay time				$0.2t_C$	ns
$t_{v(S_{CLK}-S_{OUT})}$	Serial I/O output hold time		0			ns
$t_{f(S_{CLK})}$	Serial I/O clock output falling time	C_L=100pF, R_L=1kΩ			40	ns
$t_{r(Pch-strg)}$	P-channel high-breakdown voltage output rising time (Note 1)	C_L=100pF, V_{EE}=V_{CC}−36V		55		ns
$t_{r(Pch-weak)}$	P-channel high-breakdown voltage output rising time (Note 2)	C_L=100pF, V_{EE}=V_{CC}−36V		1.8		µs

Note 1. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "0".
2. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "1".

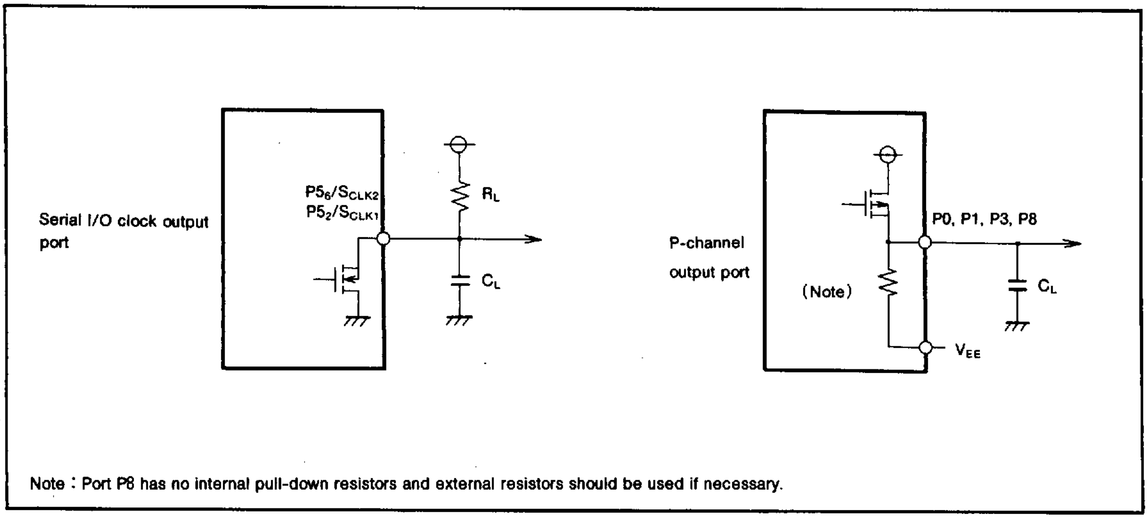


Fig. 43 Output switching characteristics measurement circuit

Timing Chart