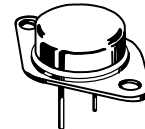


**2N6251**
**15 AMPERE  
 POWER TRANSISTOR  
 NPN SILICON  
 350 VOLTS  
 175 WATTS**

**CASE 1-07  
 TO-204AA  
 (TO-3)**

## High Voltage NPN Silicon Power Transistors

... designed for high voltage inverters, switching regulators and line operated amplifier applications. Especially well suited for switching power supply applications.

- High Voltage Breakdown Rating
- Low Saturation Voltages
- Fast Switching Capability
- High  $E_{S/b}$  Energy Handling Capability

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (1)	$V_{CEO(sus)}$	350	Vdc
Collector-Emitter Voltage (1)	$V_{CER(sus)}$	375	Vdc
Collector-Base Voltage (1)	$V_{CB}$	450	Vdc
Emitter-Base Voltage	$V_{EB}$	6.0	Vdc
Collector Current — Continuous**	$I_C$	15	Adc
— Peak	$I_{CM}$	30	
Base Current — Continuous (1)	$I_B$	10	Adc
— Peak	$I_{BM}$	20	
Emitter Current — Continuous	$I_E$	25	Adc
— Peak	$I_{EM}$	50	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	175	Watts
@ $T_C = 100^\circ\text{C}$		100	
Derate above $25^\circ\text{C}^*$		1.0	$\text{W}/^\circ\text{C}$
Operating and Storage Junction (1) Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	$^\circ\text{C}$

(1) Indicates JEDEC Registered Data.

\*\* JEDEC Registered Value is 10 A, Motorola Guaranteed Value is 15 A.

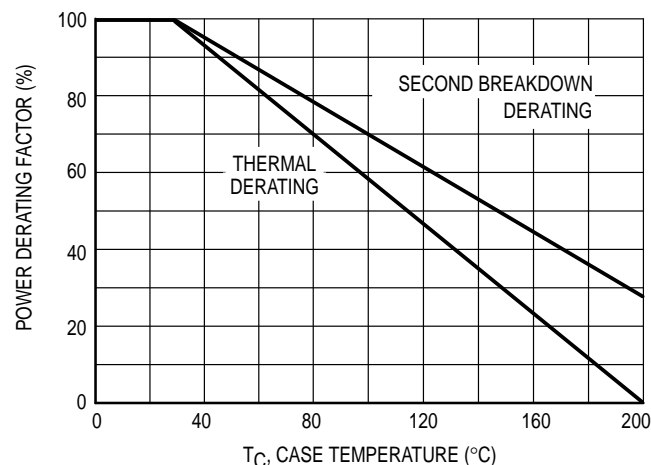


Figure 1. Power Derating

REV 1

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (Table 1) ( $I_C = 200\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	350	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) ( $I_C = 200\text{ mA}$ )	$V_{CER(sus)}$	375	—	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CER}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CER}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEV}$	— —	5.0 10	mAdc
Collector Cutoff Current ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 225\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 300\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	5.0	mAdc
Emitter Cutoff Current ( $V_{EB} = 6.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased $t = 1.0\text{ s}$ (non–repetitive) ( $V_{CE} = 30\text{ V}$ ) ( $V_{CE} = 100\text{ V}$ )	$I_{S/b}$	5.8 0.3	— —	Vdc
Second Breakdown Energy with base reverse biased (Table 1) ( $I_C = 10\text{ A}$ , $V_{BE(off)} = 4.0\text{ Vdc}$ , $L = 50\text{ }\mu\text{H}$ )	$E_{S/b}$	2.5	—	mJ

## ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 10\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$h_{FE}$	6.0	50	—
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1.67\text{ Adc}$ )	$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 10\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 1.25\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 1.67\text{ Adc}$ )	$V_{BE(sat)}$	—	2.5	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	2.5	—	MHz
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## SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Rise Time	$(V_{CC} = 200\text{ Vdc}$ , $I_C = 10\text{ A}$ , Duty Cycle $\leq 2.0\%$ , $t_p = 100\text{ }\mu\text{s}$ ) ( $I_{B1} = I_{B2} = 1.67\text{ Adc}$ )	$t_r$	—	2.0	$\mu\text{s}$
Storage Time		$t_s$	—	3.5	$\mu\text{s}$
Fall Time		$t_f$	—	1.0	$\mu\text{s}$

\* Indicates JEDEC Registered Data.

(1) Measured on a curve tracer (60 Hz full–wave rectified sine wave).

Table 1. Test Conditions for Dynamic Performance

	V <sub>CEO(sus)</sub>	V <sub>CER(sus)</sub>	ES/b	RESISTIVE SWITCHING
INPUT CONDITIONS				
CIRCUIT VALUES	L <sub>coil</sub> = 42 mH R <sub>coil</sub> = 0.7 Ω, f <sub>o</sub> = 60 Hz V <sub>CC</sub> = 0 to 50 V	L <sub>coil</sub> = 14 mH R <sub>coil</sub> = 0.05 Ω V <sub>CC</sub> = 0 to 50 V f <sub>o</sub> = 60 Hz	L <sub>coil</sub> = 50 μH, V <sub>CC</sub> = 11.5 V R <sub>coil</sub> = 0.2 Ω	V <sub>CC</sub> = 200 V R <sub>L</sub> = 20 Ω
TEST CIRCUITS	<p><b>INDUCTIVE TEST CIRCUIT</b></p> <p><b>OUTPUT WAVEFORMS</b></p> <p><math>t_1</math> Adjusted to Obtain <math>I_C</math> <math>t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}</math></p> <p>NOTE: SET <math>I_{C(pk)}</math> TO OBTAIN <math>I_C = 200</math> mA AT <math>V_{CEO(sus)}</math> EQUAL TO RATED VALUE. ADJUST <math>V_{Clamp}</math> VOLTAGE FOR <math>V_{CEO(sus)}</math> RATED VALUE.</p>		<p><b>RESISTIVE TEST CIRCUIT</b></p>	

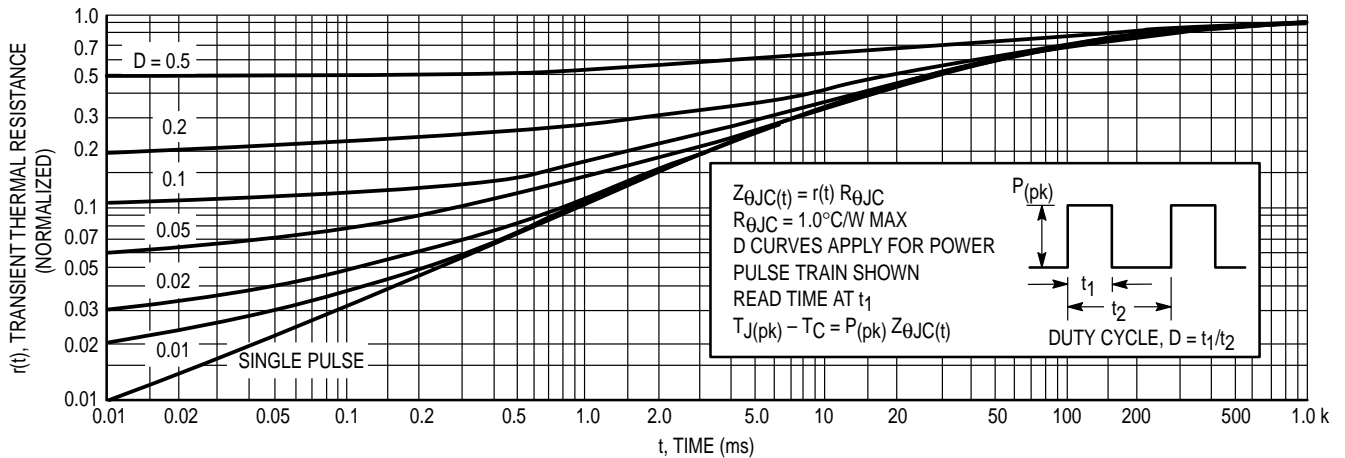


Figure 2. Thermal Response

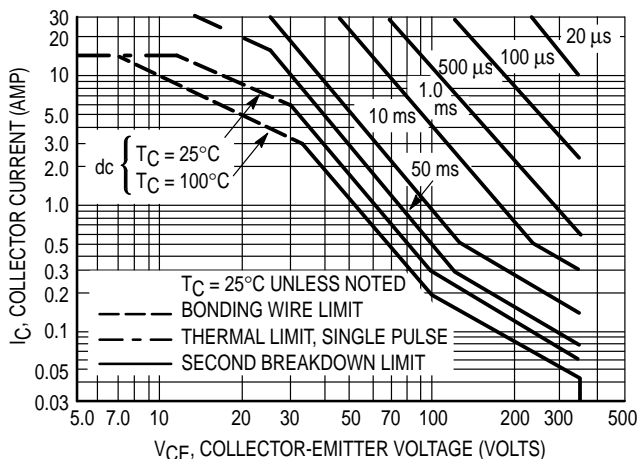


Figure 3. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on  $T_C = 25^\circ\text{C}$ .  $T_J(pk)$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 3 may be found at any case temperature by using the appropriate curve on Figure 1.

$T_J(pk)$  may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

DC CHARACTERISTICS

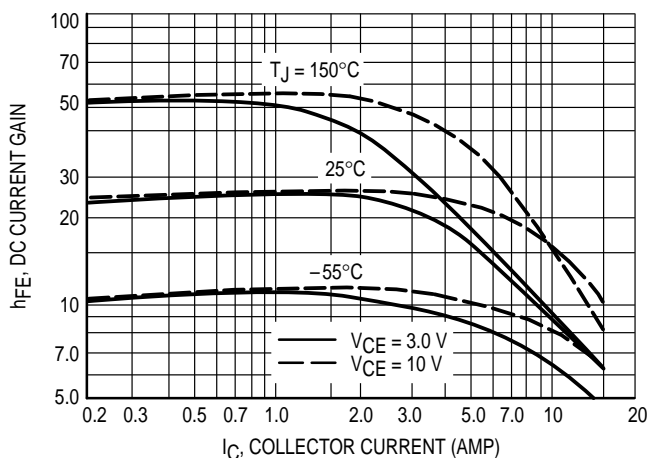


Figure 4. DC Current Gain

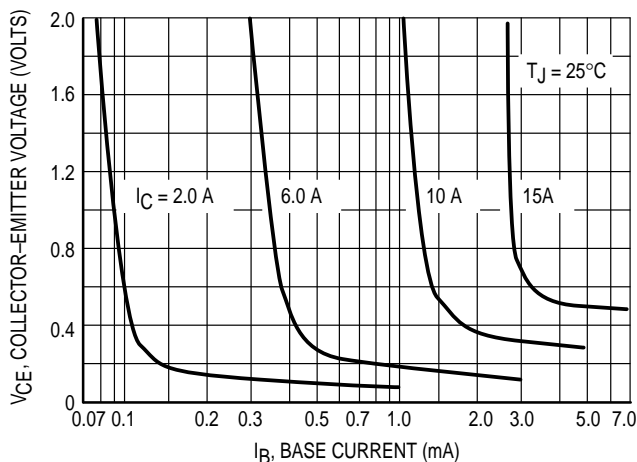


Figure 5. Collector Saturation Region

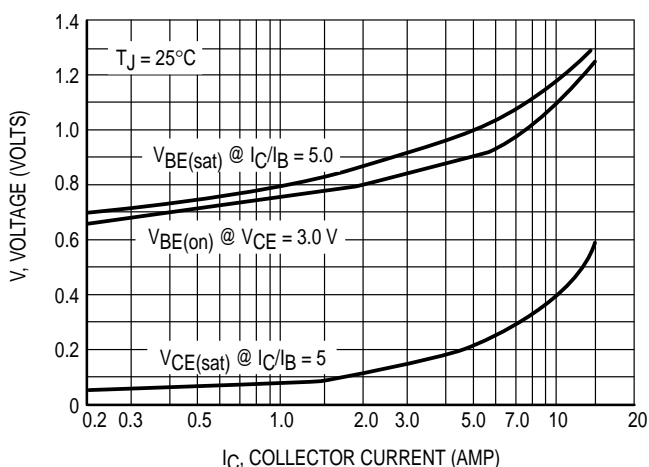


Figure 6. "On" Voltage

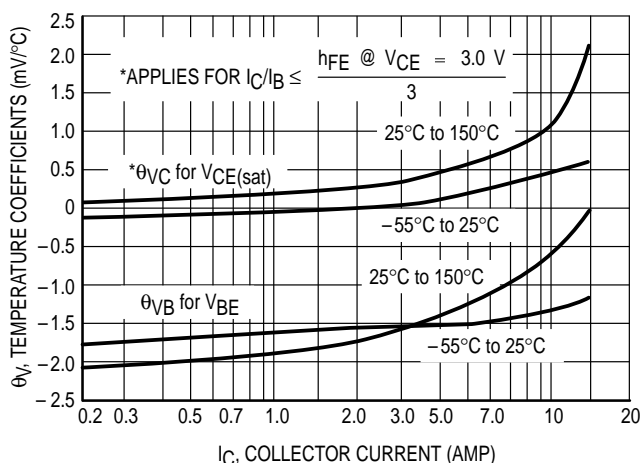


Figure 7. Temperature Coefficients

RESISTIVE SWITCHING PERFORMANCE

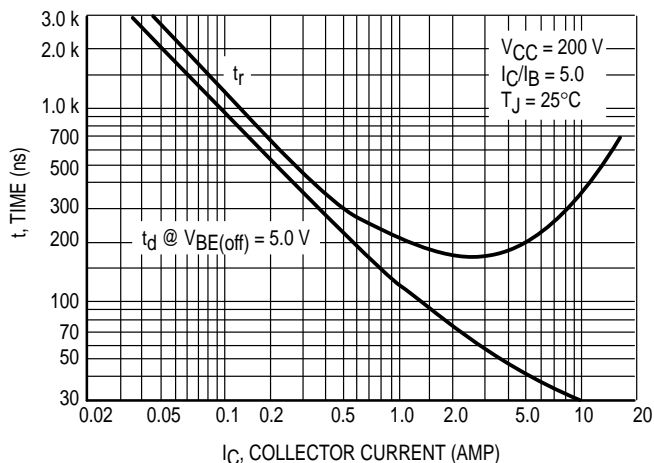


Figure 8. Turn-on Time

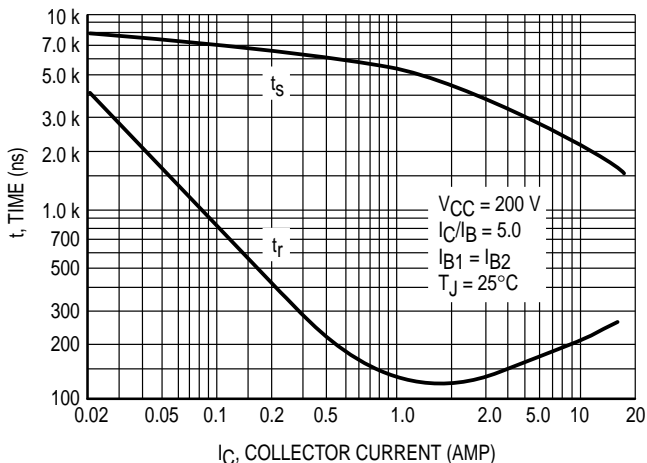
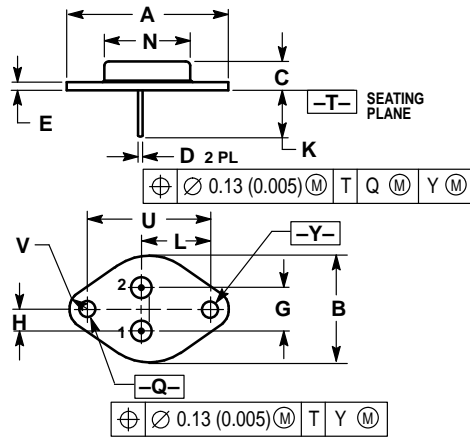


Figure 9. Turn-off Time

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:  
 PIN 1. BASE  
 2. EMITTER  
 CASE: COLLECTOR

CASE 1-07  
 TO-204AA (TO-3)  
 ISSUE Z

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