74AVCH16T245

16-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 01 — 14 October 2009   **Product data sheet**

1. General description

The 74AVCH16T245 is a 16-bit transceiver with bidirectional level voltage translation and 3-state outputs. The device can be used as two 8-bit transceivers or as a 16-bit transceiver. It has dual supplies ($V_{CC(A)}$ and $V_{CC(B)}$) for voltage translation and two 8-bit input-output ports (nAn, nBn) each with its own output enable (n$\overline{OE}$) and send/receive (nDIR) input for direction control. $V_{CC(A)}$ and $V_{CC(B)}$ can be independently supplied at any voltage between 0.8 V and 3.6 V making the device suitable for low voltage translation between any of the following voltages: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V. A HIGH on nDIR selects transmission from nAn to nBn while a LOW on nDIR selects transmission from nBn to nAn. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A and B outputs are in the high-impedance OFF-state. The bus-hold circuitry on the powered-up side always stays active.

The 74AVCH16T245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features

- Wide supply voltage range:
  - ◆ $V_{CC(A)}$: 0.8 V to 3.6 V
  - ◆ $V_{CC(B)}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
  - ◆ 380 Mbit/s ($\geq$ 1.8 V to 3.3 V translation)

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74AVCH16T245

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◆ 200 Mbit/s (≥ 1.1 V to 3.3 V translation)
◆ 200 Mbit/s (≥ 1.1 V to 2.5 V translation)
◆ 200 Mbit/s (≥ 1.1 V to 1.8 V translation)
◆ 150 Mbit/s (≥ 1.1 V to 1.5 V translation)
◆ 100 Mbit/s (≥ 1.1 V to 1.2 V translation)
■ Suspend mode
■ Bus hold on data inputs
■ Latch-up performance exceeds 100 mA per JESD 78 Class II
■ Inputs accept voltages up to 3.6 V
■ I_{OFF} circuitry provides partial Power-down mode operation
■ Multiple package options
■ Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1.   Ordering information

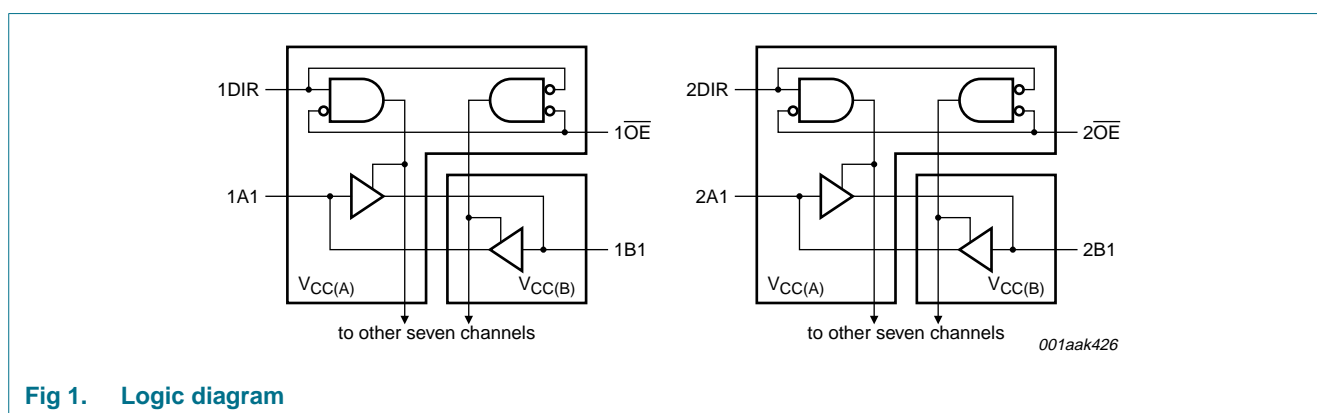| Type number	Package			
	Temperature range	Name	Description	Version
74AVCH16T245DGG	−40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74AVCH16T245DGV	−40 °C to +85 °C	TSSOP48[1]	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1
74AVCH16T245EV	−40 °C to +125 °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm	SOT702-1
74AVCH16T245BQ	−40 °C to +125 °C	HUQFN60U	plastic thermal enhanced ultra thin quad flat package; no leads; 60 terminals; UTLP based; body 4 × 6 × 0.55 mm	SOT1025-1

[1] Also known as TVSOP48.

4. Functional diagram

Fig 1.   Logic diagram
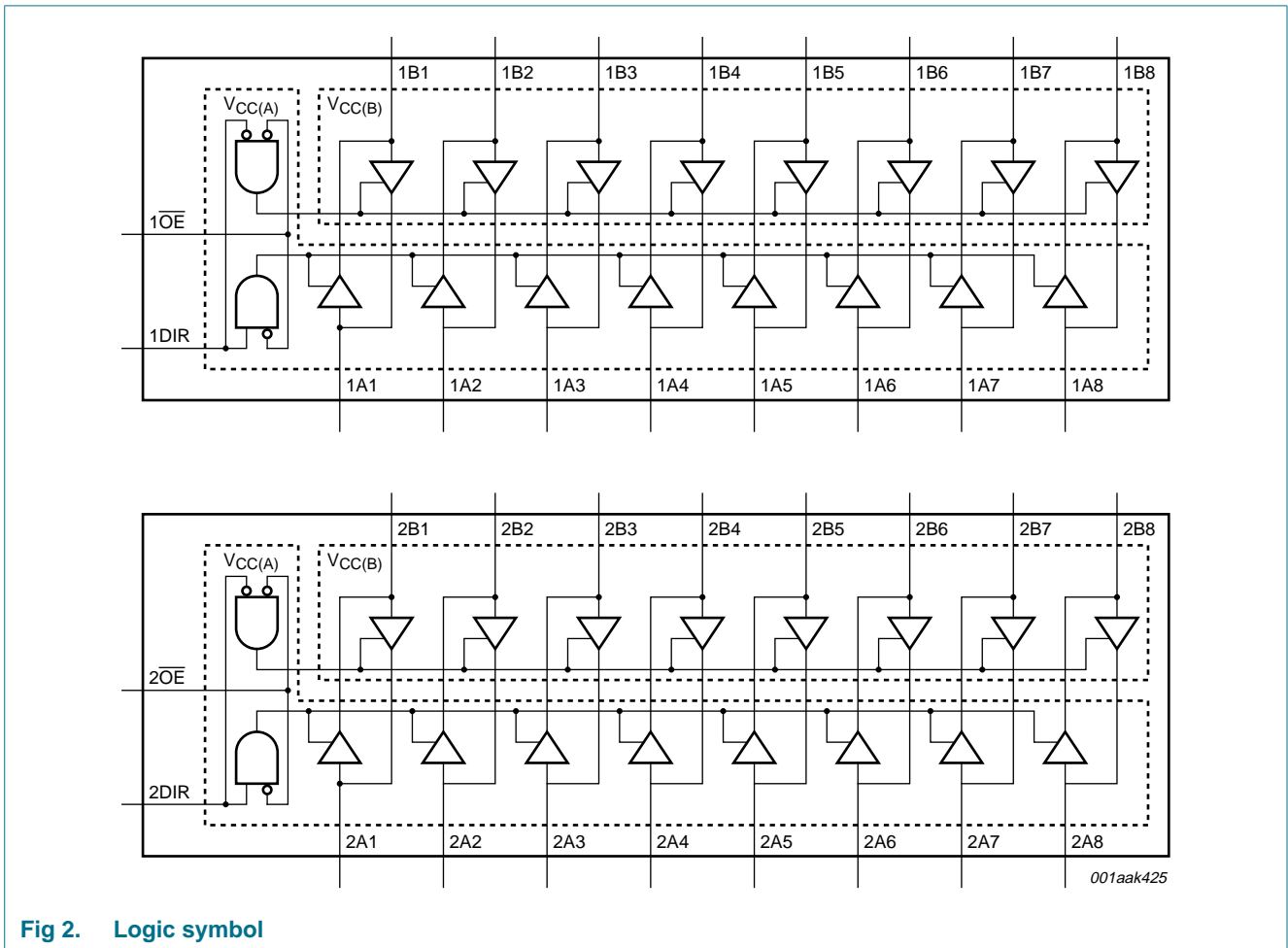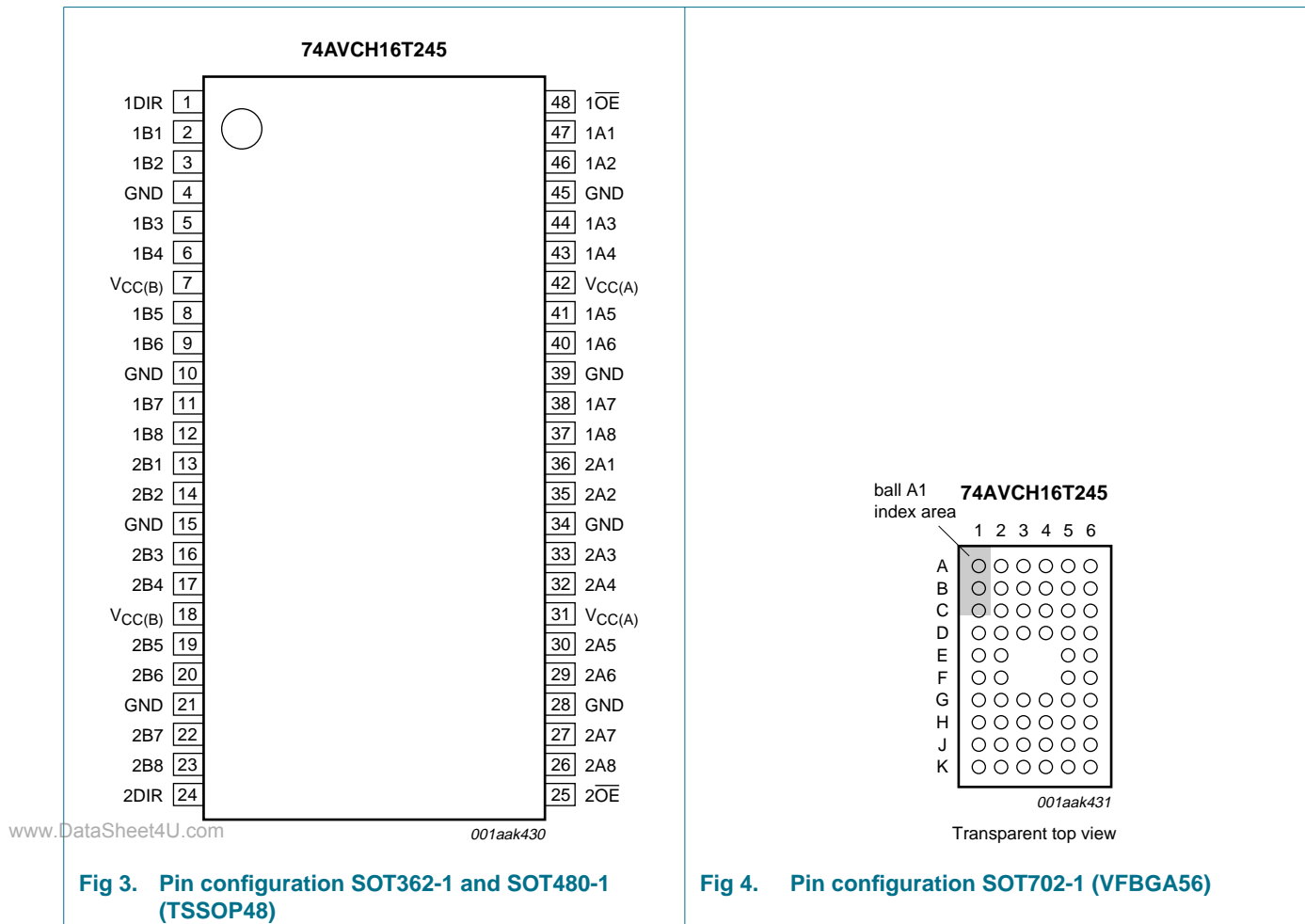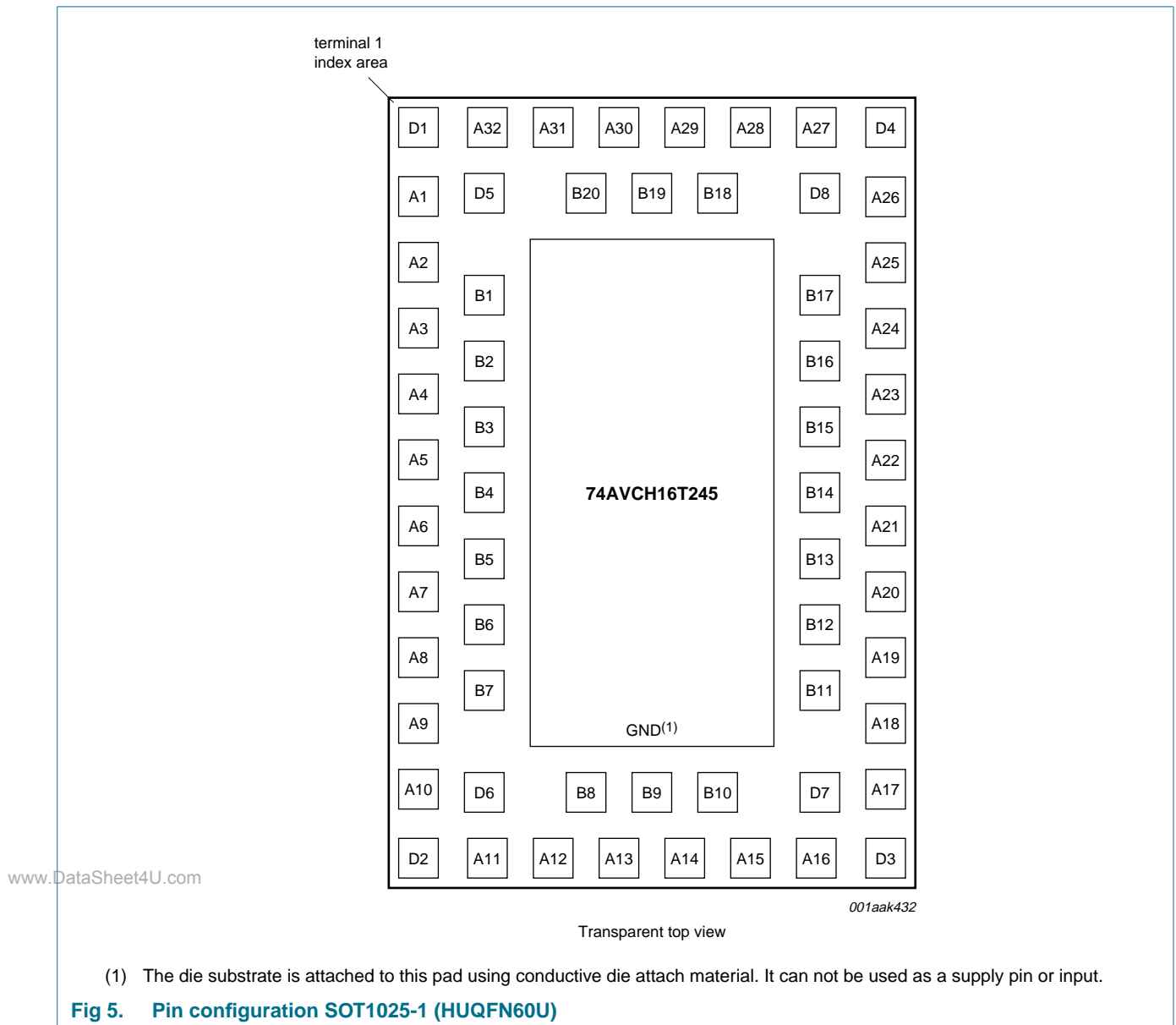
Fig 2.   Logic symbol

5. Pinning information

5.1 Pinning

74AVCH16T245

1DIR [1]	[48] 1$\overline{OE}$
1B1 [2]	[47] 1A1
1B2 [3]	[46] 1A2
GND [4]	[45] GND
1B3 [5]	[44] 1A3
1B4 [6]	[43] 1A4
V$_{CC(B)}$ [7]	[42] V$_{CC(A)}$
1B5 [8]	[41] 1A5
1B6 [9]	[40] 1A6
GND [10]	[39] GND
1B7 [11]	[38] 1A7
1B8 [12]	[37] 1A8
2B1 [13]	[36] 2A1
2B2 [14]	[35] 2A2
GND [15]	[34] GND
2B3 [16]	[33] 2A3
2B4 [17]	[32] 2A4
V$_{CC(B)}$ [18]	[31] V$_{CC(A)}$
2B5 [19]	[30] 2A5
2B6 [20]	[29] 2A6
GND [21]	[28] GND
2B7 [22]	[27] 2A7
2B8 [23]	[26] 2A8
2DIR [24]	[25] 2$\overline{OE}$

001aak430

Fig 3. Pin configuration SOT362-1 and SOT480-1 (TSSOP48)

ball A1 index area   **74AVCH16T245**

1 2 3 4 5 6

A B C D E F G H J K

001aak431

Transparent top view

Fig 4.   Pin configuration SOT702-1 (VFBGA56)

terminal 1 index area

Transparent top view

001aak432

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5.   Pin configuration SOT1025-1 (HUQFN60U)

5.2 Pin description

Table 2. Pin description

Symbol	Pin			Description
	SOT362-1 and SOT480-1	**SOT702-1**	**SOT1025-1**	
1DIR, 2DIR	1, 24	A1, K1	A30, A13	direction control
1B1 to 1B8	2, 3, 5, 6, 8, 9, 11, 12	B2, B1, C2, C1, D2, D1, E2, E1	B20, A31, D5, D1, A2, B2, B3, A5	data input or output
2B1 to 2B8	13, 14, 16, 17, 19, 20, 22, 23	F1, F2, G1, G2, H1, H2, J1, J2	A6, B5, B6, A9, D2, D6, A12, B8	data input or output
GND[1]	4, 10, 15, 21, 28, 34, 39, 45	B3, D3, G3, J3, J4, G4, D4, B4	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
$V_{CC(B)}$	7, 18	C3, H3	A1, A10	supply voltage B (nBn inputs are referenced to $V_{CC(B)}$)
1$\overline{OE}$, 2$\overline{OE}$	48, 25	A6, K6	A29, A14	output enable input (active LOW)
1A1 to 1A8	47, 46, 44, 43, 41, 40, 38, 37	B5, B6, C5, C6, D5, D6, E5, E6	B18, A28, D8, D4, A25, B16, B15, A22	data input or output
2A1 to 2A8	36, 35, 33, 32, 30, 29, 27, 26	F6, F5, G6, G5, H6, H5, J6, J5	A21, B13, B12, A18, D3, D7, A15, B10	data input or output
$V_{CC(A)}$	31, 42	C4, H4	A17, A26	supply voltage A (nAn, n$\overline{OE}$ and nDIR inputs are referenced to $V_{CC(A)}$)
n.c.	-	A2, A3, A4, A5, K2, K3, K4, K5	A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19	not connected

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table[1]

Supply voltage	Input		Input/output[3]	
$V_{CC(A)}$, $V_{CC(B)}$	n$\overline{OE}$[2]	nDIR[2]	nAn[2]	nBn[2]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND[3]	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The nAn, nDIR and n$\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The nBn input circuit is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

7. Limiting values

Table 4.   Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			−0.5	+4.6	V
$V_{CC(B)}$	supply voltage B			−0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		−50	-	mA
V_I	input voltage		[1]	−0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		−50	-	mA
V_O	output voltage	Active mode	[1][2][3]	−0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode	[1]	−0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			−100	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C;				
		TSSOP48 package	[4]	-	500	mW
		VFBGA56 package	[5]	-	1000	mW
		HUQFN60U package	[5]	-	1000	mW

[1]   The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] V_{CCO} + 0.5 V should not exceed 4.6 V.

[4]   Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

[5]   Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5.   Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			0.8	3.6	V
$V_{CC(B)}$	supply voltage B			0.8	3.6	V
V_I	input voltage			0	3.6	V
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode		0	3.6	V
T_{amb}	ambient temperature			−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8$ V to 3.6 V	[2]	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

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9. Static characteristics

Table 6.   Typical static characteristics at T_{amb} = 25 °C[1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −1.5 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 0.8 V		-	0.69	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 1.5 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 0.8 V		-	0.07	-	V
I_I	input leakage current	nDIR, n$\overline{OE}$ input; V_I = 0 V or 3.6 V; $V_{CC(A)}$ = $V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.025	±0.25	μA
I_{BHL}	bus hold LOW current	A or B port; V_I = 0.42 V; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.2 V	[3]	-	26	-	μA
I_{BHH}	bus hold HIGH current	A or B port; V_I = 0.78 V; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.2 V	[4]	-	−24	-	μA
I_{BHLO}	bus hold LOW overdrive current	A or B port; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.2 V	[5]	-	27	-	μA
I_{BHHO}	bus hold HIGH overdrive current	A or B port; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.2 V	[6]	-	−26	-	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = $V_{CC(B)}$ = 3.6 V	[7]	-	±0.5	±2.5	μA
		suspend mode A port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	[7]	-	±0.5	±2.5	μA
		suspend mode B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	[7]	-	±0.5	±2.5	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA
C_I	input capacitance	nDIR, n$\overline{OE}$ input; V_I = 0 V or 3.3 V; $V_{CC(A)}$ = $V_{CC(B)}$ = 3.3 V		-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; V_O = 3.3 V or 0 V; $V_{CC(A)}$ = $V_{CC(B)}$ = 3.3 V		-	4.5	-	pF

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[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3]   The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL} max.

[4]   The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH} min.

[5]   An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.

[6]   An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.

[7]   For I/O ports, the parameter I_{OZ} includes the input leakage current.

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Table 7.   Static characteristics [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input					
		V_{CCI} = 0.8 V	$0.70V_{CCI}$	-	$0.70V_{CCI}$	-	V
		V_{CCI} = 1.1 V to 1.95 V	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		V_{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V_{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, n$\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	2	-	2	-	V
V_{IL}	LOW-level input voltage	data input					
		V_{CCI} = 0.8 V	-	$0.30V_{CCI}$	-	$0.30V_{CCI}$	V
		V_{CCI} = 1.1 V to 1.95 V	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		V_{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V_{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, n$\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	-	$0.30V_{CC(A)}$	-	$0.30V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 µA; $V_{CC(A)}$ = $V_{CC(B)}$ = 0.8 V to 3.6 V	V_{CCO} − 0.1	-	V_{CCO} − 0.1	-	V
		I_O = −3 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.1 V	0.85	-	0.85	-	V
		I_O = −6 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.4 V	1.05	-	1.05	-	V
		I_O = −8 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.65 V	1.2	-	1.2	-	V
		I_O = −9 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 2.3 V	1.75	-	1.75	-	V
		I_O = −12 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 3.0 V	2.3	-	2.3	-	V

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Table 7. **Static characteristics** *...continued*[1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 100$ µA; $V_{CC(A)} = V_{CC(B)} = 0.8$ V to 3.6 V	-	0.1	-	0.1	V
		$I_O = 3$ mA; $V_{CC(A)} = V_{CC(B)} = 1.1$ V	-	0.25	-	0.25	V
		$I_O = 6$ mA; $V_{CC(A)} = V_{CC(B)} = 1.4$ V	-	0.35	-	0.35	V
		$I_O = 8$ mA; $V_{CC(A)} = V_{CC(B)} = 1.65$ V	-	0.45	-	0.45	V
		$I_O = 9$ mA; $V_{CC(A)} = V_{CC(B)} = 2.3$ V	-	0.55	-	0.55	V
		$I_O = 12$ mA; $V_{CC(A)} = V_{CC(B)} = 3.0$ V	-	0.7	-	0.7	V
I_I	input leakage current	nDIR, $n\overline{OE}$ input; $V_I = 0$ V or 3.6 V; $V_{CC(A)} = V_{CC(B)} = 0.8$ V to 3.6 V	-	±1	-	±5	µA
I_{BHL}	bus hold LOW current	A or B port [3]					
		$V_I = 0.49$ V; $V_{CC(A)} = V_{CC(B)} = 1.4$ V	15	-	15	-	µA
		$V_I = 0.58$ V; $V_{CC(A)} = V_{CC(B)} = 1.65$ V	25	-	25	-	µA
		$V_I = 0.70$ V; $V_{CC(A)} = V_{CC(B)} = 2.3$ V	45	-	45	-	µA
		$V_I = 0.80$ V; $V_{CC(A)} = V_{CC(B)} = 3.0$ V	100	-	90	-	µA
I_{BHH}	bus hold HIGH current	A or B port [4]					
		$V_I = 0.91$ V; $V_{CC(A)} = V_{CC(B)} = 1.4$ V	−15	-	−15	-	µA
		$V_I = 1.07$ V; $V_{CC(A)} = V_{CC(B)} = 1.65$ V	−25	-	−25	-	µA
		$V_I = 1.60$ V; $V_{CC(A)} = V_{CC(B)} = 2.3$ V	−45	-	−45	-	µA
		$V_I = 2.00$ V; $V_{CC(A)} = V_{CC(B)} = 3.0$ V	−100	-	−100	-	µA
I_{BHLO}	bus hold LOW overdrive current	A or B port [5]					
		$V_{CC(A)} = V_{CC(B)} = 1.6$ V	125	-	125	-	µA
		$V_{CC(A)} = V_{CC(B)} = 1.95$ V	200	-	200	-	µA
		$V_{CC(A)} = V_{CC(B)} = 2.7$ V	300	-	300	-	µA
		$V_{CC(A)} = V_{CC(B)} = 3.6$ V	500	-	500	-	µA
I_{BHHO}	bus hold HIGH overdrive current	A or B port [6]					
		$V_{CC(A)} = V_{CC(B)} = 1.6$ V	−125	-	−125	-	µA
		$V_{CC(A)} = V_{CC(B)} = 1.95$ V	−200	-	−200	-	µA
		$V_{CC(A)} = V_{CC(B)} = 2.7$ V	−300	-	−300	-	µA
		$V_{CC(A)} = V_{CC(B)} = 3.6$ V	−500	-	−500	-	µA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0$ V or V_{CCO}; $V_{CC(A)} = V_{CC(B)} = 3.6$ V [7]	-	±5	-	±30	µA
		suspend mode A port; $V_O = 0$ V or V_{CCO}; $V_{CC(A)} = 3.6$ V; $V_{CC(B)} = 0$ V [7]	-	±5	-	±30	µA
		suspend mode B port; $V_O = 0$ V or V_{CCO}; $V_{CC(A)} = 0$ V; $V_{CC(B)} = 3.6$ V [7]	-	±5	-	±30	µA

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Table 7. **Static characteristics** ...continued[1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V	-	±5	-	±30	μA
I_{CC}	supply current	A port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$\quad V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	30	-	125	μA
		$\quad V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	25	-	100	μA
		$\quad V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	25	-	100	μA
		$\quad V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	−5	-	−20	-	μA
		B port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$\quad V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	30	-	125	μA
		$\quad V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	25	-	100	μA
		$\quad V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	−5	-	−20	-	μA
		$\quad V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	-	25	-	100	μA
		A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	55	-	185	μA
		A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	45	-	150	μA

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL} max.

[4] The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH} min.

[5] An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.

[6] An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.

[7] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. **Typical total supply current ($I_{CC(A)}$ + $I_{CC(B)}$)**

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA

Table 8. **Typical** …*continued* **total supply current (I$_{CC(A)}$ + I$_{CC(B)}$)** …*continued*

V$_{CC(A)}$	V$_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

10. Dynamic characteristics

Table 9. **Typical power dissipation capacitance at V$_{CC(A)}$ = V$_{CC(B)}$ and T$_{amb}$ = 25 °C** [1][2]
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	V$_{CC(A)}$ = V$_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C$_{PD}$	power dissipation capacitance	A port: (direction A to B); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction A to B); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction B to A); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		A port: (direction B to A); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction A to B); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		B port: (direction A to B); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction B to A); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction B to A); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C$_{PD}$ is used to determine the dynamic power dissipation (P$_D$ in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f$_i$ = input frequency in MHz;

f$_o$ = output frequency in MHz;

C$_L$ = load capacitance in pF;

V$_{CC}$ = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f$_i$ = 10 MHz; V$_I$ = GND to V$_{CC}$; t$_r$ = t$_f$ = 1 ns; C$_L$ = 0 pF; R$_L$ = ∞ Ω.

Table 10.   Typical dynamic characteristics at $V_{CC(A)}$ = 0.8 V and T_{amb} = 25 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
t_{dis}	disable time	nOE to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		nOE to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
t_{en}	enable time	nOE to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		nOE to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 11.   Typical dynamic characteristics at $V_{CC(B)}$ = 0.8 V and T_{amb} = 25 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
t_{dis}	disable time	nOE to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		nOE to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
t_{en}	enable time	nOE to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		nOE to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

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16-bit dual supply translating transceiver; 3-state

Table 12. Dynamic characteristics for temperature range −40 °C to +85 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

| Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	nAn to nBn	0.5	9.2	0.5	6.9	0.5	6.0	0.5	5.1	0.5	4.9	ns
		nBn to nAn	0.5	9.2	0.5	8.7	0.5	8.5	0.5	8.2	0.5	8.0	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	ns
		n$\overline{OE}$ to nBn	1.5	12.5	1.5	9.7	1.5	9.5	1.0	8.1	1.0	8.9	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	ns
		n$\overline{OE}$ to nBn	1.1	14.9	1.1	11.0	1.1	9.6	1.0	8.1	1.0	7.7	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	nAn to nBn	0.5	8.7	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.9	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
		n$\overline{OE}$ to nBn	1.5	11.4	1.5	8.7	1.5	7.5	1.0	6.5	1.0	6.3	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	ns
		n$\overline{OE}$ to nBn	1.0	13.5	1.0	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	nAn to nBn	0.5	8.5	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
		nBn to nAn	0.5	6.0	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
		n$\overline{OE}$ to nBn	1.5	11.1	1.5	8.4	1.5	7.1	1.0	5.9	1.0	5.7	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		n$\overline{OE}$ to nBn	1.0	13.0	1.0	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	nAn to nBn	0.5	8.2	0.5	5.6	0.5	4.6	0.5	3.3	0.5	2.8	ns
		nBn to nAn	0.5	5.1	0.5	4.1	0.5	3.7	0.5	3.4	0.5	3.2	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	ns
		n$\overline{OE}$ to nBn	1.0	10.6	1.0	7.9	1.0	6.6	1.0	6.1	1.0	5.2	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		n$\overline{OE}$ to nBn	0.5	12.5	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	nAn to nBn	0.5	8.0	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
		nBn to nAn	0.5	4.9	0.5	3.7	0.5	3.3	0.5	2.9	0.5	2.7	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	ns
		n$\overline{OE}$ to nBn	1.0	10.3	1.0	7.7	1.0	6.5	1.0	5.2	0.5	5.0	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	0.5	4.3	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4.0	ns
		n$\overline{OE}$ to nBn	0.5	12.4	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4.0	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 13. Dynamic characteristics for temperature range −40 °C to +125 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	nAn to nBn	0.5	10.2	0.5	7.6	0.5	6.6	0.5	5.7	0.5	5.4	ns
		nBn to nAn	0.5	10.2	0.5	9.6	0.5	9.4	0.5	9.1	0.5	8.8	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	ns
		n$\overline{OE}$ to nBn	1.5	13.8	1.5	10.7	1.5	10.5	1.0	9.0	1.5	9.8	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	ns
		n$\overline{OE}$ to nBn	1.1	16.4	1.1	12.1	1.1	10.6	1.0	9.0	1.0	8.5	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	nAn to nBn	0.5	9.6	0.5	6.9	0.5	5.8	0.5	4.6	0.5	4.1	ns
		nBn to nAn	0.5	7.6	0.5	6.9	0.5	6.5	0.5	6.2	0.5	6.1	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	ns
		n$\overline{OE}$ to nBn	1.5	12.6	1.5	9.6	1.5	8.3	1.0	7.2	1.0	7.0	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	ns
		n$\overline{OE}$ to nBn	1.0	14.9	1.0	11.2	0.5	9.0	0.5	6.5	0.5	5.8	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	nAn to nBn	0.5	9.4	0.5	6.5	0.5	5.3	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.6	0.5	5.8	0.5	5.3	0.5	5.0	0.5	4.9	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns
		n$\overline{OE}$ to nBn	1.5	12.3	1.5	9.3	1.5	7.9	1.0	6.5	1.0	6.3	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	ns
		n$\overline{OE}$ to nBn	1.0	14.3	1.0	10.2	0.5	8.2	0.5	5.9	0.5	5.0	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	nAn to nBn	0.5	9.1	0.5	6.2	0.5	5.1	0.5	3.7	0.5	3.1	ns
		nBn to nAn	0.5	5.7	0.5	4.6	0.5	4.1	0.5	3.8	0.5	3.6	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		n$\overline{OE}$ to nBn	1.0	11.7	1.0	8.7	1.0	7.3	1.0	6.8	1.0	5.8	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	ns
		n$\overline{OE}$ to nBn	0.5	13.8	0.5	10.4	0.5	8.1	0.5	5.7	0.5	5.0	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	nAn to nBn	0.5	8.8	0.5	6.1	0.5	4.9	0.5	3.6	0.5	3.0	ns
		nBn to nAn	0.5	5.4	0.5	4.1	0.5	3.7	0.5	3.2	0.5	3.0	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	ns
		n$\overline{OE}$ to nBn	1.0	11.4	1.0	8.5	1.0	7.2	1.0	5.8	0.5	5.5	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	0.5	4.8	0.5	4.8	0.5	4.7	0.5	4.6	0.5	4.4	ns
		n$\overline{OE}$ to nBn	0.5	13.7	0.5	10.3	0.5	8.0	0.5	5.4	0.5	4.4	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.
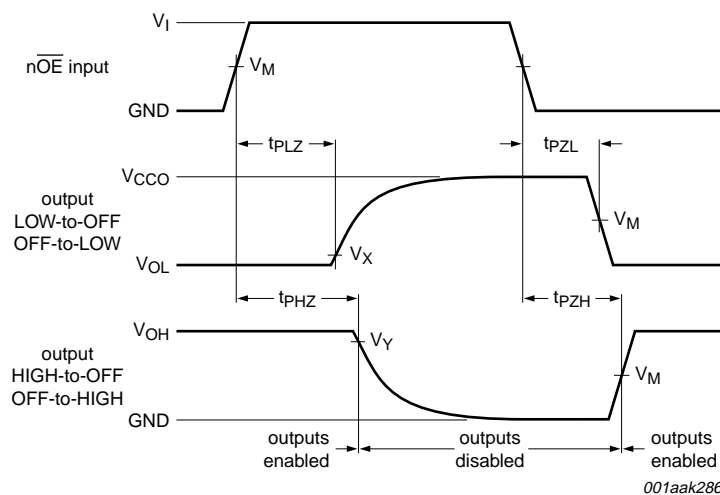
11. Waveforms
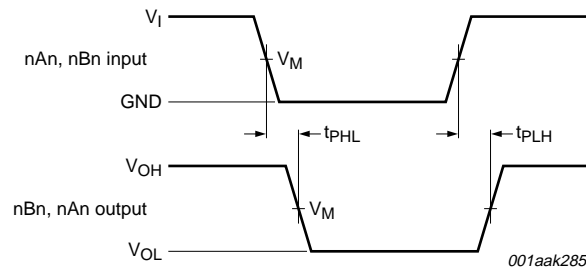
Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. **The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**

Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. **Enable and disable times**

Table 14. **Measurement points**

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} − 0.1 V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

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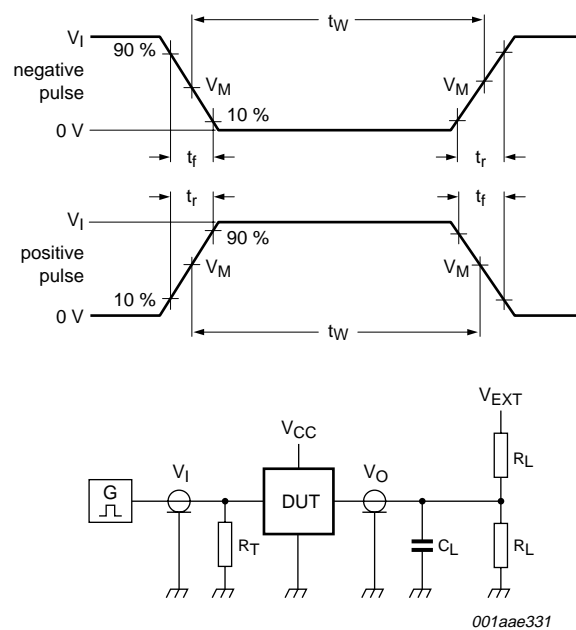
Test data is given in Table 15.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Load circuit for switching times

Table 15. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I[1]	$\Delta t / \Delta V$[2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[3]
0.8 V to 1.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] dV/dt ≥ 1.0 V/ns

[3] V_{CCO} is the supply voltage associated with the output port.

12. Typical propagation delay characteristics
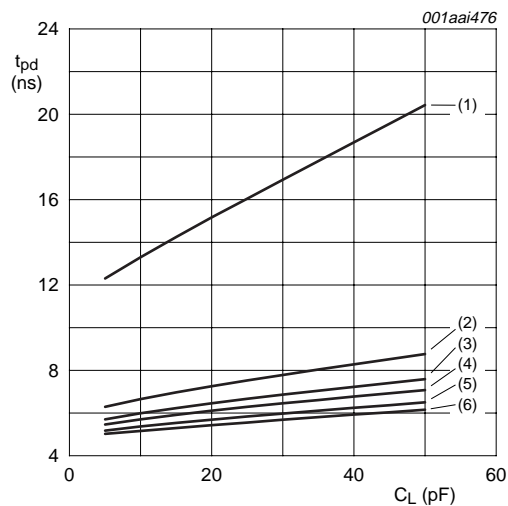
a. Propagation delay (A to B); $V_{CC(A)} = 0.8$ V

(1) $V_{CC(B)} = 0.8$ V.
(2) $V_{CC(B)} = 1.2$ V.
(3) $V_{CC(B)} = 1.5$ V.
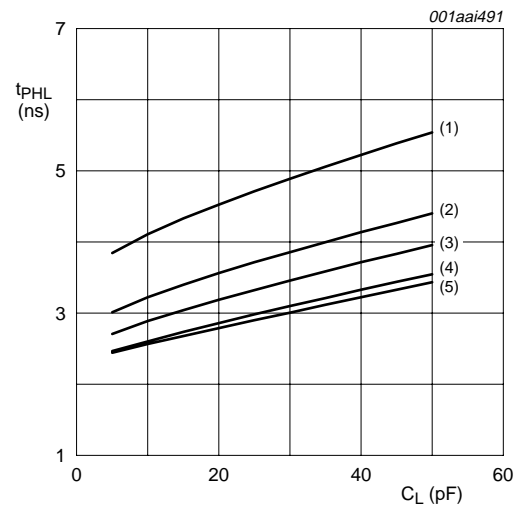(4) $V_{CC(B)} = 1.8$ V.
(5) $V_{CC(B)} = 2.5$ V.
(6) $V_{CC(B)} = 3.3$ V.
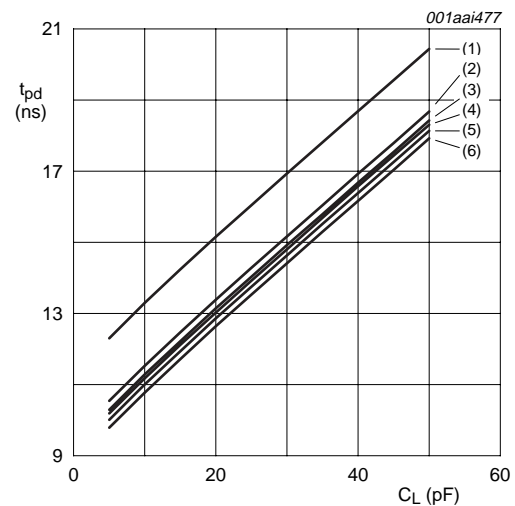
b. Propagation delay (A to B); $V_{CC(B)} = 0.8$ V

(1) $V_{CC(A)} = 0.8$ V.
(2) $V_{CC(A)} = 1.2$ V.
(3) $V_{CC(A)} = 1.5$ V.
(4) $V_{CC(A)} = 1.8$ V.
(5) $V_{CC(A)} = 2.5$ V.
(6) $V_{CC(A)} = 3.3$ V.

Fig 9.   Typical propagation delay vs load capacitance; $T_{amb} = 25$ °C

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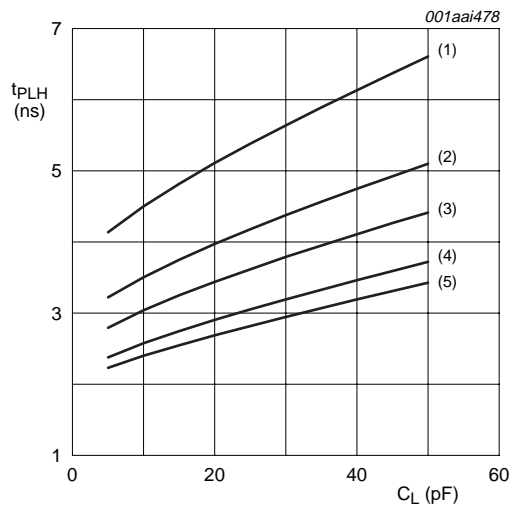
a. LOW to HIGH propagation delay (A to B);
   $V_{CC(A)} = 1.2$ V

b. HIGH to LOW propagation delay (A to B);
   $V_{CC(A)} = 1.2$ V
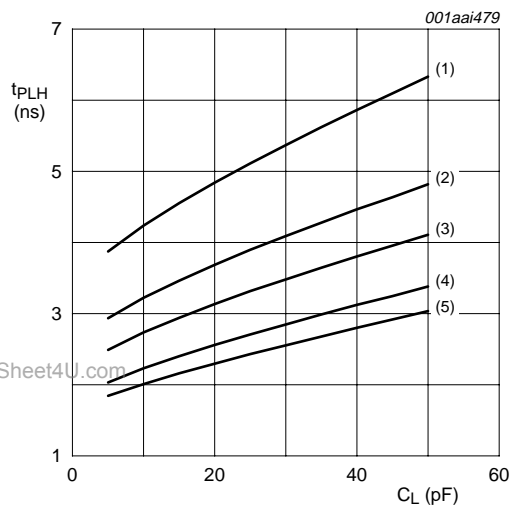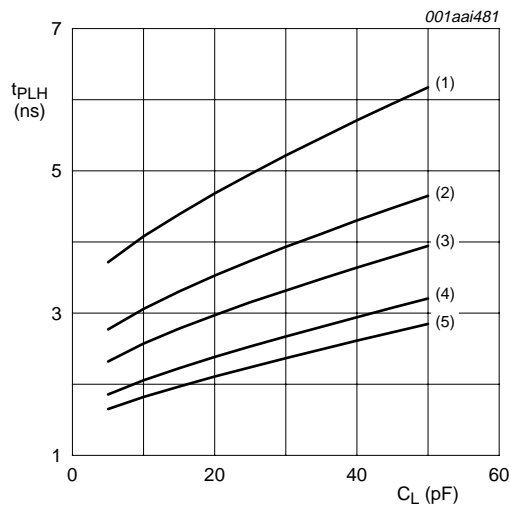
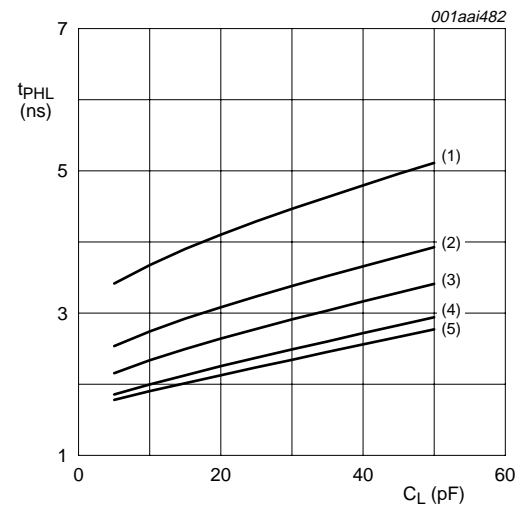c. LOW to HIGH propagation delay (A to B);
   $V_{CC(A)} = 1.5$ V
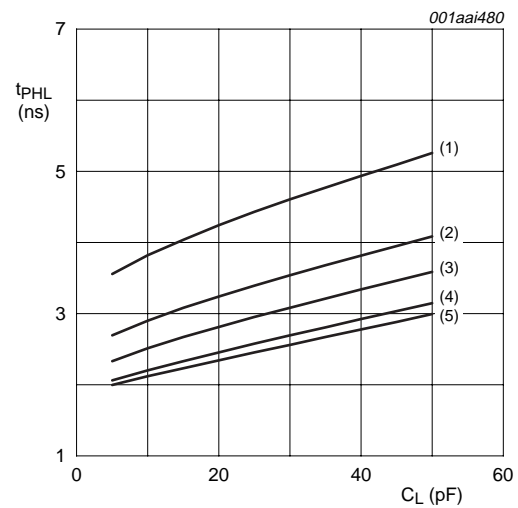
d. HIGH to LOW propagation delay (A to B);
   $V_{CC(A)} = 1.5$ V

(1) $V_{CC(B)} = 1.2$ V.

(2) $V_{CC(B)} = 1.5$ V.

(3) $V_{CC(B)} = 1.8$ V.

(4) $V_{CC(B)} = 2.5$ V.

(5) $V_{CC(B)} = 3.3$ V.

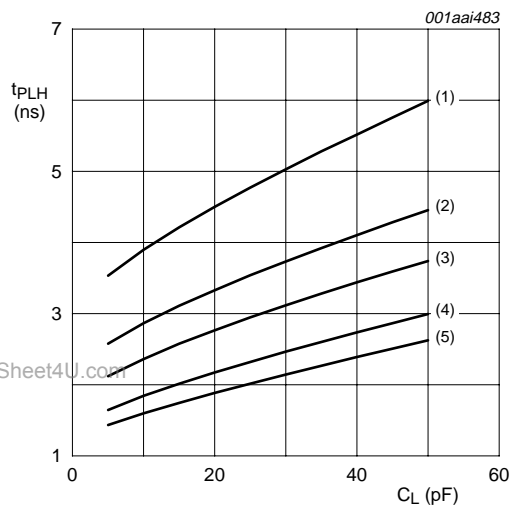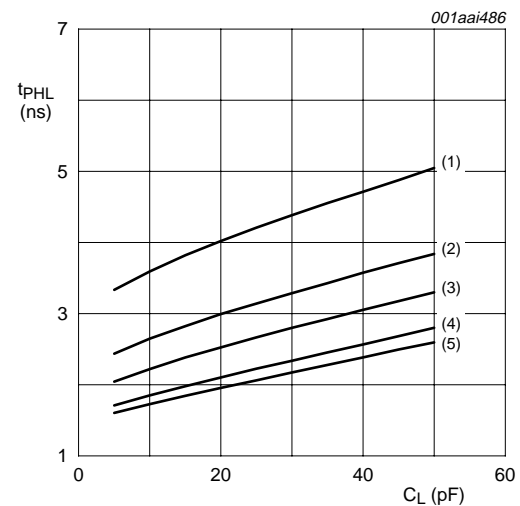**Fig 10. Typical propagation delay vs load capacitance; $T_{amb} = 25$ °C**

a. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 1.8 V

b. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 1.8 V
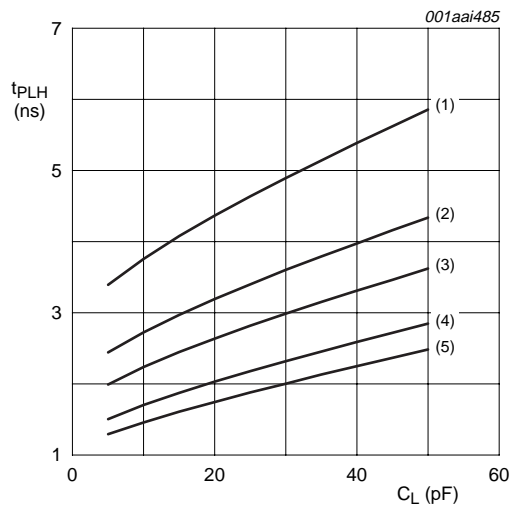
c. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 2.5 V

d. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 2.5 V

(1) $V_{CC(B)}$ = 1.2 V.
(2) $V_{CC(B)}$ = 1.5 V.
(3) $V_{CC(B)}$ = 1.8 V.
(4) $V_{CC(B)}$ = 2.5 V.
(5) $V_{CC(B)}$ = 3.3 V.

Fig 11. Typical propagation delay vs load capacitance; T_{amb} = 25 °C

a. LOW to HIGH propagation delay (A to B);
   $V_{CC(A)} = 3.3$ V

(1) $V_{CC(B)} = 1.2$ V.

(2) $V_{CC(B)} = 1.5$ V.

(3) $V_{CC(B)} = 1.8$ V.

(4) $V_{CC(B)} = 2.5$ V.

(5) $V_{CC(B)} = 3.3$ V.
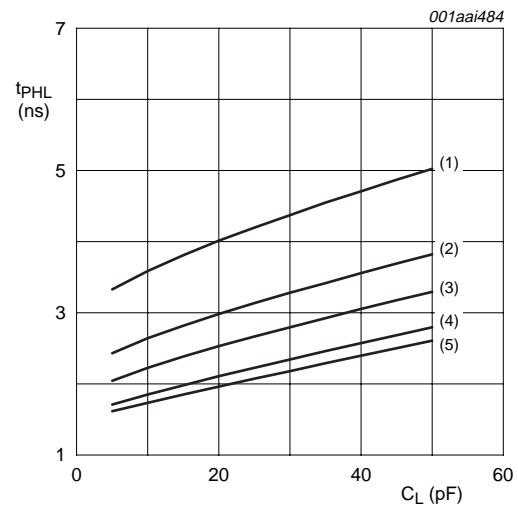
b. HIGH to LOW propagation delay (A to B);
   $V_{CC(A)} = 3.3$ V

Fig 12. Typical propagation delay vs load capacitance; $T_{amb} = 25$ °C

13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm   SOT362-1

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DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(2)	e	H_E	L	Lₚ	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT362-1 (TSSOP48)

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TSSOP48: plastic thin shrink small outline package; 48 leads;
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1

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DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.8 9.6	4.5 4.3	0.4	6.6 6.2	1	0.7 0.5	0.4 0.3	0.2	0.07	0.08	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT480-1		MO-153				99-12-27 03-02-18

Fig 14. Package outline SOT480-1 (TSSOP48)

NXP Semiconductors

74AVCH16T245

16-bit dual supply translating transceiver; 3-state

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm   **SOT702-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	b	D	E	e	e₁	e₂	v	w	y	y₁
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~02-08-08~~ 03-07-01
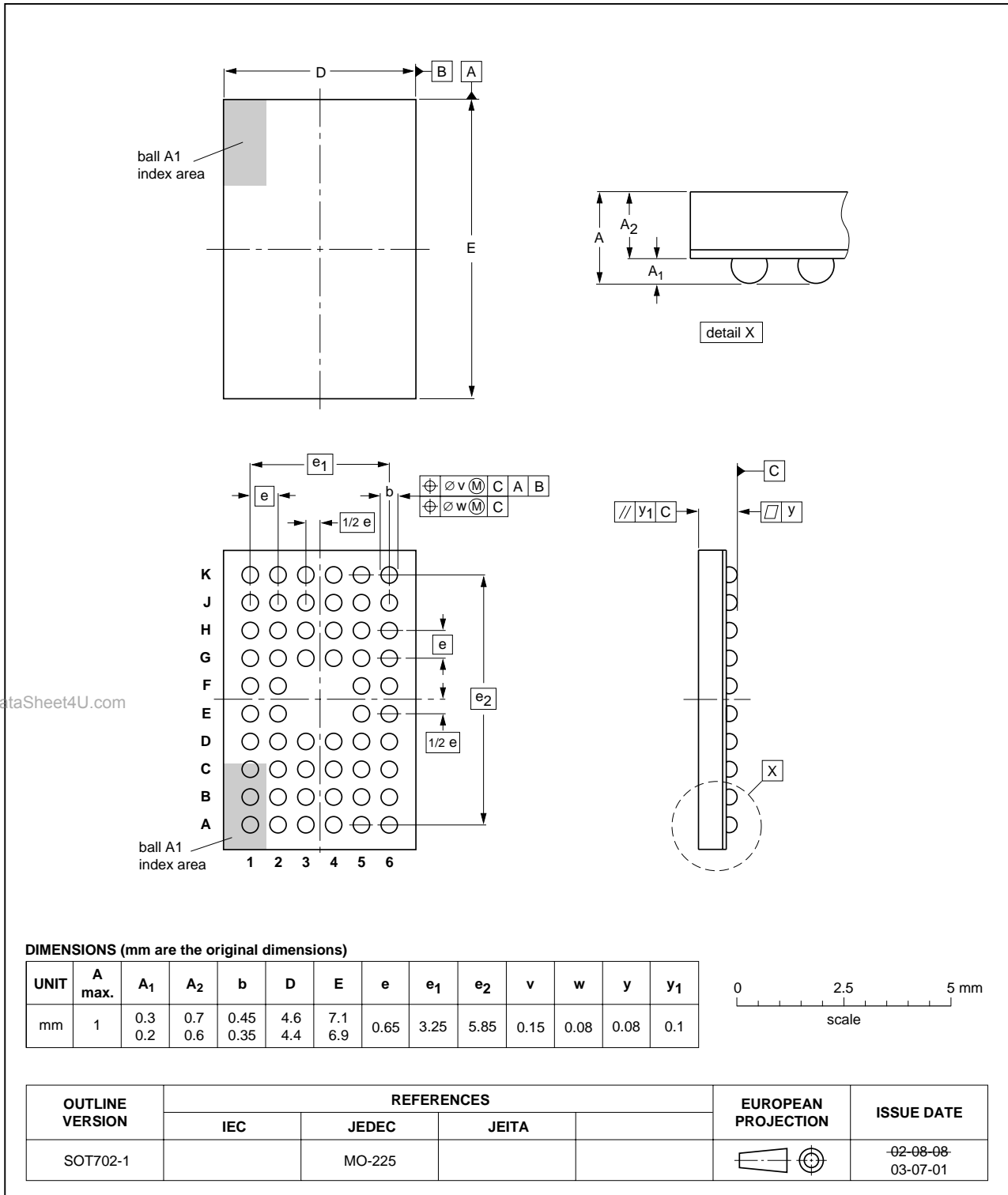
Fig 15. Package outline SOT702-1 (VFBGA56)

HUQFN60U: plastic thermal enhanced ultra thin quad flat package; no leads
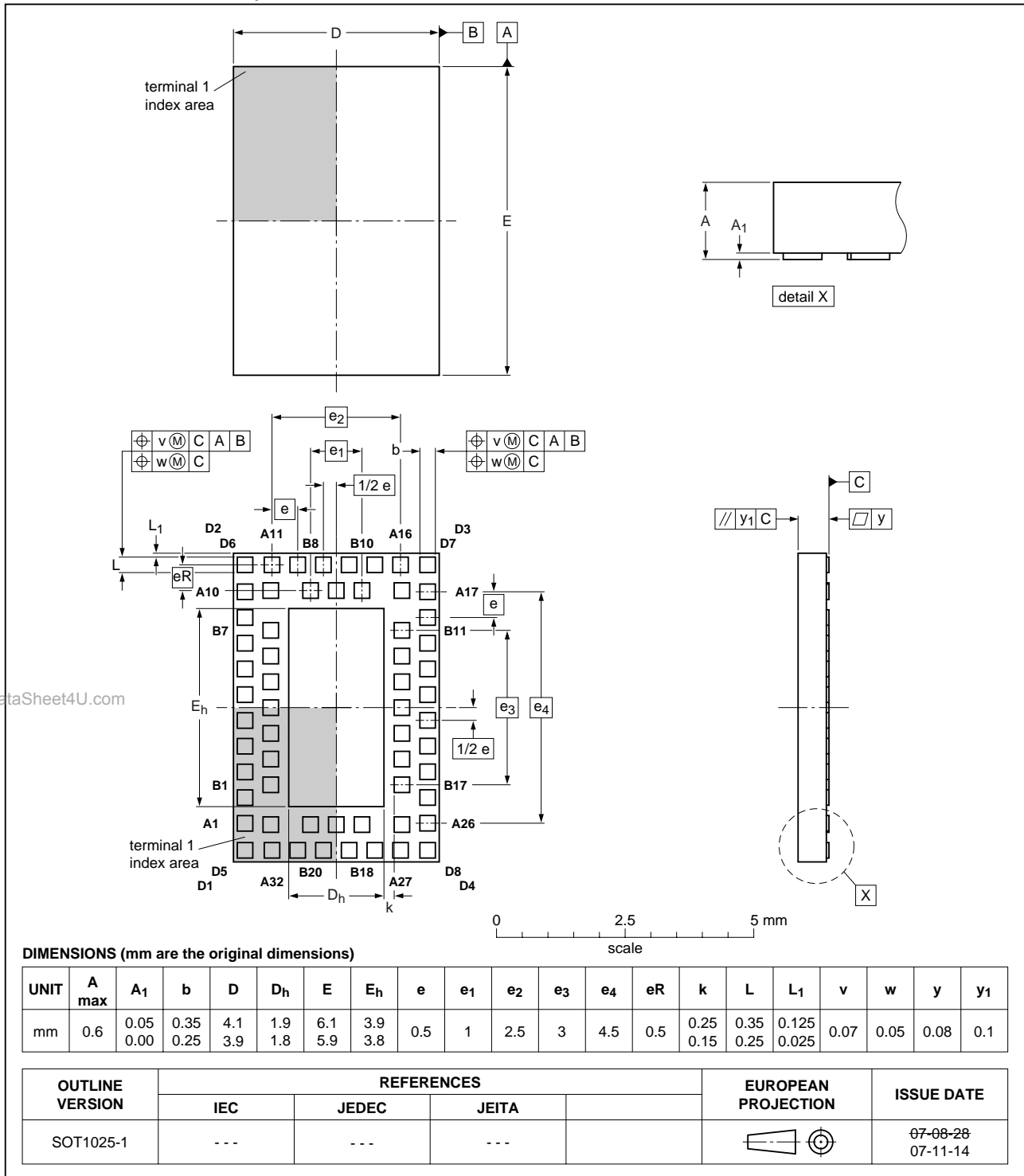**60 terminals; UTLP based; body 4 x 6 x 0.55 mm**

SOT1025-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	eR	k	L	L_1	v	w	y	y_1
mm	0.6	0.05 0.00	0.35 0.25	4.1 3.9	1.9 1.8	6.1 5.9	3.9 3.8	0.5	1	2.5	3	4.5	0.5	0.25 0.15	0.35 0.25	0.125 0.025	0.07	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1025-1	- - -	- - -	- - -			07-08-28 07-11-14

Fig 16. Package outline SOT1025-1 (HUQFN60U)

14. Abbreviations

Table 16.   Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 17.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH16T245_1	20091014	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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