

PN7220

NFC controller with NCI interface supporting EMV and NFC Forum applications

Rev. 3.0 — 5 July 2023

Product data sheet

1 General description

This document describes the functionality and electrical specification of the PN7220 high-power NFC controller family with NCI interface.

As an NCI 2.2 compliant NFC controller with high RF output (2 W) and high receiver sensitivity, the NXP PN7220 is a robust solution for payment terminals and all readers that must generate a strong RF field in a difficult environment. Offering full compliance with EMVCo 3.1 L1 analog and digital, the PN7220 simplifies designs while ensuring interoperability with a broad range of smartcards and mobile phones.

In addition to the reader/writer functionality, the device supports the emulation of ISO14443-A cards up to 848 kbit/s.

The PN7221 is based on the PN7220 and supports all features of PN7220 plus "Enhanced Contactless Polling" (ECP) by Apple (see Ref. [12]) - this description is not part of this document. Note, that the ECP feature is available after formal authorization only.

The PN7220 communicates to a connected host by a physical I²C interface using the NCI 2.2 protocol.

The PN7221 communicates to a connected host by a physical I²C interface using the NCI 2.2 protocol and supports Apple ECP.

Planned, but not available yet:

The PN7222 communicates to a connected host by one physical I²C interface using the NCI 2.2 protocol and one dedicated SPI interface.

The PN7223 communicates to a connected host by one physical I²C interface using the NCI 2.2 protocol and one dedicated SPI interface and supports Apple ECP.

The PN7220 product family supports highly innovative and unique features which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveform control (AWC), and fully automatic EMD error handling.

Additional documents supporting a design-in of the are available from NXP, this additional design-in information is not part of this document.

In this document, the term „MIFARE card“ refers to a contactless card with an embedded MIFARE IC.



2 Features and benefits

2.1 RF functionality

2.1.1 ISO/IEC14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC 14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kbit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic Crypto supporting MIFARE Classic en-/decryption is integrated in hardware

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
 - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 6.6 kBd
 - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 26 kBd
 - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 53 kBd
 - TX: "1 of 4" encoding with 10 % modulation (53 kBd)
 - TX: "1 of 4" encoding with 100 % modulation (53 kBd).

2.1.7 NFC Forum compliancy

- NFC Forum compliance for R/W – analog and digital

2.1.8 EMVCo compliancy

- EMVCo 3.1 compliance for R/W – digital
- EMVCo 3.1 compliance for R/W analog can be achieved, but depends on connected antenna geometry and size, matching network and RF settings.

2.1.9 Host interface

The devices PN7220 and PN7221 support one host interface using a single interface connection based on a I²C interface host interface (host interface 1) with data rates up to 3.4 Mbit/s.

The logical interface layer of the host interfaces is based on the NCI 2.0 interface specification, enhanced by NXP proprietary commands.

The devices PN7222 and PN7223 support two host interfaces using one interface connection based on a I²C interface (host interface 2) and one SPI interface (host interface 1).

2.2 Transmitter

- Transmitter with high RF output power of 2.0 W
- Dynamic power control 2.0 (DPC) (dynamic power control without processing load on host MCU)
- Adaptive waveshaping control (AWC)

2.3 Receiver

- Robust receiver: Automatic configuration, advanced insensitivity against TFT display noise for higher RF performance

2.4 Integrated polling loop

- RF polling loop according to NFC Forum
- RF Polling loop according to EMVCo 3.1, integrated EMVCo L1 software stack
- Integrated EMVCo L1 contact stack

2.5 Integrated DC-DC

The PN7220 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 Volts, this simplifies the design of the power supply.

A single supply concept for the RF system, for example, with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage.

The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip.

The usage of the DC-DC is optional.

For applications making use of the low-power card detection, the DC-DC is available.

2.6 RF debugging support

- RF debugging without external probing of test signals possible by sampling debug data into chip-internal memory based on pre-define trigger conditions – ideal debugging solution for PCI-compliant POS terminals
- One digital and one analog debug signal is provided by the chip for connection of an oscilloscope

3 Applications

- Payment terminals following the COTS security requirements with full EMVCo3.1 analog and digital compliancy
- Multi-Application terminals
- Ticket validators for the controlling staff in public transport
- E-Vehicle charging stations
- Vending machines

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	$V_{BAT} \geq V_{DDIO}$	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	PN7220 - supply with VDDPA from internal VDDPALDO with DC-DC	1.5	-	5.7	V
I_{pd}	power down current	$V_{DD(VDDPA)} = V_{DD(VDDIO)} = V_{DD(VDD)} = 3.0$ V; hard power down state; pin VEN set LOW, $T_{amb} = 25$ °C, External supply by VDDIO	-	40	105	µA
I_{stb}	standby current	$T_{amb} = 25$ °C	-	45	110	µA
$I_{DD(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB,	-40	-	+85	°C
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB,	-40	-	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA = 3.6 V	-40	-	+105	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

5 Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
PN7220EV/C1	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray" ; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller	SOT1307-2
PN7220EV/C1J	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller	SOT1307-2
PN7221EV/C1	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray" ; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller and ECP	SOT1307-2
PN7221EV/C1J	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller and ECP	SOT1307-2

6 Block diagram

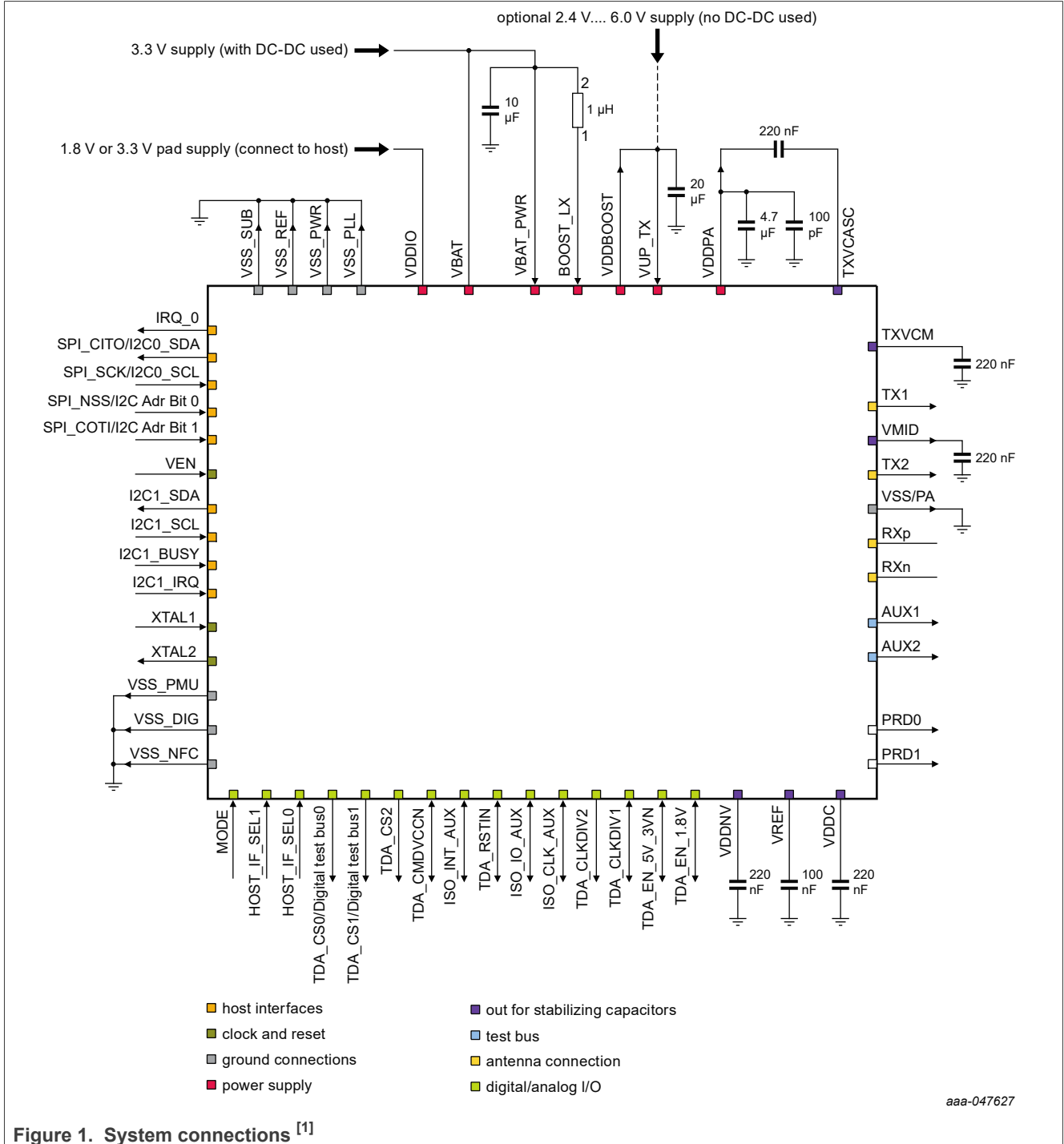


Figure 1. System connections [1]

[1] The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I²C standards organization.

The PN7220 is connected to an application processor / host CPU based on an NCI interface.

The device offers high compatibility to existing solutions which offer an NCI interface (Host IF_1). The physical interface used for the connection is a I2C interface.

Host IF_1 allows I²C data rates up to 3.4 Mbit/s.

I²C address:

The PN7220 host interface 1 supports the 7-bit addressing mode, first 5-bits are fixed and is decimal 40, last two bits are configurable using ADDR0 and ADDR1 pins . This provides maximum flexibility even in cases where the I²C bus is shared with other devices on top of the PN7220.

Default mode after boot:

The system is always booting in mode (EMVCo polling or NFC Forum polling) defined by the level on the pin MODE/GPIO2.

Switching between NFC Forum and EMVCo polling:

Switching to a EMVCo polling loop is done based on a physical signal "MODE/GPIO2" controlled by the application processor / host CPU. All previous data from earlier communications are erased, and the NCI software stack is being reset. The system enters then the new EMVCo polling mode. Switching back to NFC Forum mode again clears all previous data from earlier communication and resets the NCI software stack.

7 Pinning information

7.1 Pin description VFBGA64

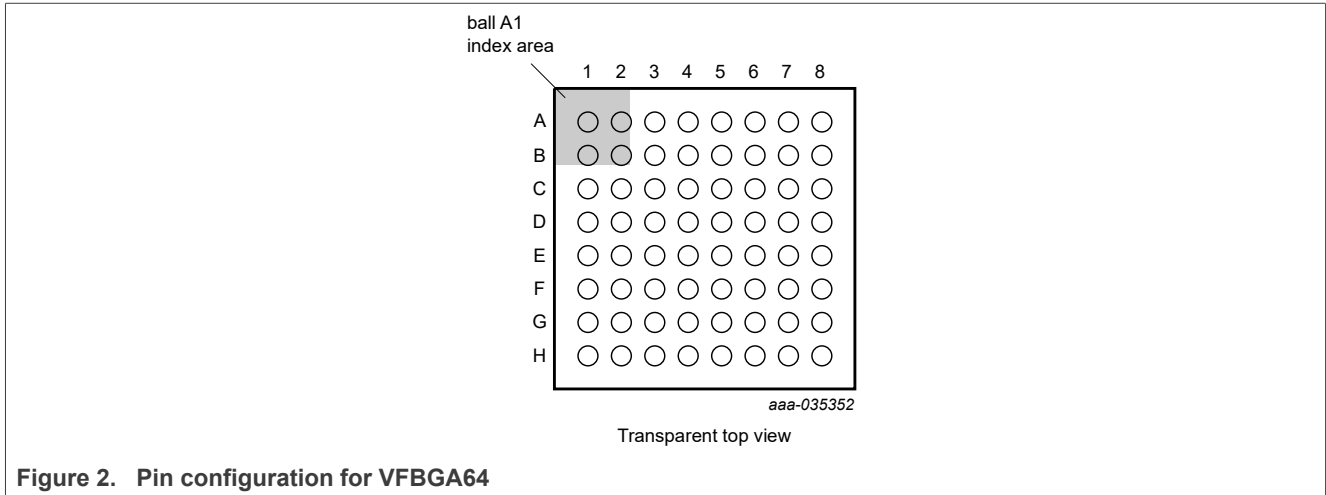


Figure 2. Pin configuration for VFBGA64

Table 3. Pin description VFBGA64

Pin Number	Symbol ^[1]	Type	Description ^[1]
Host Interface 1 (I²C / SPI)			
E6	SPI CITO / I2C1_ SDA	Output	PN7220 / PN7221: I ² C1_ SDA PN7222 / PN7223: SPI CITO
E5	SPI SCK / I2C1_ SCL	Input	PN7220 / PN7221: I ² C1_ SCL PN7222 / PN7223: SPI SCK
D6	SPI NSS / I2C Adr Bit 0	Input	PN7220 / PN7221: I ² C Adr Bit 0 (Address is configured using 5 fixed bits (40d - 028h) and 2 Bits from D5/D6) I ² C interface address can be configured to 0x28 (00), 0x29 (01) , 0x2A (10) , 0x2B (11) based on D6 and D5 Pins PN7222 / PN7223: SPI NSS
D5	SPI COTI / I2C Adr Bit 1	Input	PN7220 / PN7221: I ² C Adr Bit 1 ((Address is configured using 5 fixed bits (40d - 028h) and 2 Bits from D5/D6) I ² C interface address can be configured to 0x28 (00), 0x29 (01) , 0x2A (10) , 0x2B (11) based on D6 and D5 Pins PN7222 / PN7223: SPI COTI
B7	IRQ1	Output	Host communication IF1 / event interrupt signal
Host Interface 2 (I2C)			
A6	I2C2_ SDA	Input/Output	PN7220 / PN7221: n.c. PN7222 / PN7223: I ² C 2 SDA

NFC controller with NCI interface supporting EMV and NFC Forum applications

Table 3. Pin description VFBGA64...continued

Pin Number	Symbol ^[1]	Type	Description ^[1]
B6	I2C2_SCL	Input	PN7220 / PN7221: n.c. PN7222 / PN7223: I ² C 2 SCL
D7	WAKEUP	input	PN7220 / PN7221: n.c. ; Wakeup signal for 2 CPU system PN7222 / PN7223: BUSY host Interface 2
H8	I2C2_IRQ	Output	PN7220 / PN7221: n.c. PN7222 / PN7223: Host communication interface 2 event interrupt signal
Hardware reset			
B3	VEN	Input	Hardware reset, low active (independent from V _{VDDIO})
Host interface and Mode selection			
E7	MODE	Input	Mode selection (EMVCo or NFC Forum polling loop) Input H: EMVCo polling mode Input L: NFC Forum polling mode Input defines always EMVCo or NFC Forum polling loop, but the used host interface is different dependent on configuration of C7: C7= H at boot (1 CPU system): NFC Forum and EMVCo polling loop data transfer is done always using host interface 1 C7 = L at boot (2 CPU system): NFC Forum polling loop is doing data transfer using host interface 2 and EMVCo polling loop is doing data transfer using host interface 1
C6	HOST_IF_SEL1	Input	Shall always be on GND on PN7220
C7	HOST_IF_SEL0	Input	Host interface select 0 - selection of 1 or 2 CPU system 0: Host Interface1 active after boot (I2C Host Interface 2 has no function) 1: Host Interface 2 is always active after boot, SPI Interface 1 is active only after selecting EMVCo mode on E7 - MODE/GPIO2 HIF_SEL0 pin is read by FW after POR or reset via VEN or boot from low-power mode (OFF, standby, LPCD etc.).
XTAL connection			
F8	XTAL1	Input	Crystal / system clock input
G8	XTAL2	Output	Clock output (amplifier-inverted signal output) for crystal
Supply pins			
H2	VSS_PA	Supply GND	Transmitter ground
G3	VSS_PLL	Supply GND	PLL ground (low noise)
A2	VSS_PWR	Supply GND	DC-DC boost ground
D3	VSS_REF	Supply GND	PMU ground
B2, E3	VSS_SUB	Supply GND	Substrate ground
C3	VSS_PMU	Supply GND	PMU ground
F4	VSS_DIG	Supply GND	Digital ground
F3	VSS_NFC	Supply GND	NFC ground

Table 3. Pin description VFBGA64...continued

Pin Number	Symbol ^[1]	Type	Description ^[1]
E1	VBAT	Supply	System supply, used to supply the analog and digital blocks, memory and internal voltage references
A8	VDDIO	Supply	I/O pads power supply
G1	VDDPA	Supply	Transmitter supply
F1	VUP_TX	Supply	Input supply voltage for transmitter LDO
B1	VDDBOOST	Supply	DC-DC boost supply
A1	BOOST_LX	Output	Boost inductance loopback, to be connected to boost inductor
A3	VBATPWR	Supply	To be connected to boost inductor and transmitter power supply
Outputs for stabilizing cap			
A4	VDDNV	Output	Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap
D2	VREF	Output	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap
C1	VDDC	Output	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap
G2	TXVCM	Output	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap
F2	TXVCASC	Output	TX decoupling cap, to be connected to VDDPA
H6	VMID	Output	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap
RF Debug signals			
G7	AUX_1	Output	Test bus 1
F7	AUX_2	Output	Test bus 2
Antenna connections			
H5	RXP	Input	Receiver input "Positive"
H4	RXN	Input	Receiver input "Negative"
H1	TX1	Output	Antenna driver output 1
H3	TX2	Output	Antenna driver output 2
Analog/Digital inputs and outputs			
E8	TDA_CS0 / GPIO0	Output	Digital test bus0 / TDA chip select 0
D8	TDA_CS1 / GPIO1	Output	Digital test bus1 / TDA chip select 1
Security Feature			
B4	PRD1	Input/ Output	Package removal detection, internally connected to PRD2
G4	PRD2	Input/ Output	Package removal detection, internally connected to PRD1

Table 3. Pin description VFBGA64...continued

Pin Number	Symbol ^[1]	Type	Description ^[1]
TDA8035 Interface			
A7	TDA_CS2	Output	TDA chip select 2 (TDA_CS2) Note: Pulldown resistor required. EEPROM configuration to configure as TDA_CS. Default is TDA_CS = disabled.
B5	TDA_CMDVCCN / GPIO5	Input/Output	TDA_CMDVCCN
C4	ISO_INT_AUX	Input/Output	Auxiliary Card Interrupt
C5	TDA_RSTIN / GPIO4	Input/Output	TDA_RSTIN
D4	ISO_IO_AUX	Input/Output	Auxiliary Card I/O
E4	ISO_CLK_AUX	Input	Auxiliary Card Clock
F5	TDA_CLKDIV2 / SPIM_COTI	Input	TDA_CLKDIV2
F6	TDA_CLKDIV1 / SPIM_CITO	Input / Output	TDA_CLKDIV1
G5	SPIM_SCLK / TDA_EN_5V_3V	Input / Output	TDA_EN5V_3V
G6	SPIM_SSN / TDA_EN_1.8V	Input / Output	TDA_EN_1.8V
Pins not to be connected			
A5	PVDD_OUT	Output	Do not connect
B8	SWDIO	Input/Output	Do not connect
C2	TEST	Input/Output	Do not connect.
C8	SWD_CLK	Input	Do not connect
D1	USB_VBUS	Supply	Do not connect
E2	AD1	Input	Do not connect
H7	VTUNE1	Output	Do not connect

[1] The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I2C standards organization.

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

PN7220 is a planned product, the pin allocation is provided for information only.

8 Functional description

PN7220 can be connected on a host controller through the physical Pulldown resistor required. EEPROM configuration to configure as TDA_CS. Default is TDA_CS = disabled. interface. The logical interface toward the host controller is NCI 2.0-compliant Ref. [2] with additional commands for NXP-specific product features.

The device implements an EMVCo3.1 compliant polling loop and allows to be compliant to EMVCo L1 digital.

Enhanced RF debugging and easy configuration are supported by usage of the SPI interface, analog and digital debug outputs (AUX) and the CLIF test station.

8.1 Functional overview

The PN7220 is an NFC controller with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuitry and all the low-level functionality to realize an NFC Forum and EMVCo compliant reader.

Connection to host controller

The PN7220 connects to a host microcontroller with a I2C interface for configuration, NFC data exchange, and a high-level NCI 2.0 protocol implementation extended by proprietary commands.

The processing of the NCI commands had been improved on the PN7220 compared to previous NFC reader generations with NCI interface which eases the meeting of EMVCo timing requirements.

Integrated EMVCo3.1 L1 polling loop

The PN7220 implements an integrated EMVCo3.1 PCD-compliant polling loop. The polling loop can be configured to poll as well for FeliCa compliant cards following the EMVCo specification for “other technologies”. Alternatively, the device can be configured to poll for FeliCa cards exclusively. In addition, the PN7221 allows to configure the ECP. The firmware of the device had been optimized for low latency which helps to achieve the EMVCo timing requirements even with Android-based host systems.

Integrated NFC Forum polling loop

All supported RF technologies can be independently enabled within this PCD polling loop. The sequence of RF technologies within the PCD polling loop cannot be modified.

Selection of dedicated polling loop NFC Forum or EMVCo

The selection of a dedicated polling loop is done based on a hardware input "MODE".

After reset, the polling loop which can be activated depends on the MODE selection. It can be either EMVCo or NFC Forum compliant polling.

Switching the polling loop from one mode to the other is done by changing the level of the MODE input pin. Switching from NFC Forum polling mode to the EMVCo polling mode resets the NCI stack, clears all data in the buffers, performs an RF reset and allows then to activate the polling according to EMVCo 3.1. Switching back to the NFC Forum polling mode, again reset resets the NCI stack, performs an RF reset, clears all data in the buffers and is ready to receive NCI Interface commands to activate NFC Forum polling.

In addition to the selection of the polling loop, the mode activates a dedicated user defined set of RF configuration parameters. With this, a different RF behaviour for EMVCo and NFC Forum can be realized.

This switching of modes based on an external mode pin is working faster than alternative solutions based on loading configuration files, and allows a more secure implementation of the software on the host MCU.

Clock supply

The PN7220 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. Alternatively, an internal PLL allows using an accurate external clock source of either 24 MHz, 32 MHz, and 48 MHz (configured in EEPROM register CLK_INPUT_FREQ, 0012h)). This allows saving the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies.

Integrated DC-DC

The DC-DC is a step-up converter and is able to deliver an output voltage from approx. 2.8 V up to 6.0 V. The targeted output voltage can be configured by software. It allows a single supply voltage (for example, 3.3 V) while delivering maximum RF output power. Dependent on the application target either a direct transmitter supply or a transmitter supply by the integrated DC-DC can be chosen. The DC-DC is controlled by the Dynamic Power Control 2.0 to keep the power dissipation of the chip minimized in antenna loading cases which require a reduction of the RF output power.

Transmitter LDO (TX_LDO)

The Transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the TX_LDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

Low-power card detection

The low-power card detection (LPCD) allows saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the low-power card detection provides a functionality, which allows to power down the reader for a certain amount of time to save energy. After some time, the reader becomes active again to poll for cards. If no card is detected, the reader can go back to the power down state. During the polling time, a host controller can be set to a power-saving mode. An interrupt request from the PN7220 allows waking up the host controller in case an antenna detuning by a card or cell phone had been detected.

Dynamic power control 2.0

The next generation Dynamic Power Control (DPC2.0) with true transmitter current measurement works autonomous without host interaction. Avoiding additional host controller processing load is important for time critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matchings.

Adaptive wave shape control

The Adaptive Wave Shape Control (AWC) helps to keep the waveshapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna matching procedure and does not require any matching compromises to be taken.

Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true Baseband Amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards, and mobile phones.

RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and non-standard compliant cards and mobile phones. An integrated contactless test station allows performing a non-intrusive debugging of receiver signals without the need of connecting additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred by SPI to a host microcontroller and visualized on a PC by the NFC Cockpit

development tool. A virtual comfort interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller. Analog and digital debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system design.

Automatic EMD error handling

An automatic EMD handling performed without host interaction relaxes the timing requirements on the host controller. Automatic EMD error handling according to ISO/IEC14443 and EMVCo 3.0 is supported. In addition, the EMD error handling is widely configurable, which allows adaptations in case of future possible specification changes.

Firmware update

The PN7220 supports a secure update of the implemented firmware. In Secure Firmware update mode, the PN7220 requires no dedicated physical handling of the SPI interface lines. The firmware download does not require any additional hardware pin to be handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN7220 will be in download mode.

EEPROM configuration

Non-Volatile EEPROM memory of the PN7220 is used to store configuration data that must be preserved in case the PN7220 is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory as well as other configuration data which must be preserved during power supply disconnect is stored in this EEPROM memory. Examples for these are settings for receiver sensitivity, DPC, waveshaping, LPCD, and power supply configurations.

RF configuration

The PN7220 allows an automatic RF protocol selection based on the actual polling loop state. Pre-defined user configuration data is stored in non-volatile memory (EEPROM) and is automatically loaded for the modulation scheme currently activated by the polling loop.

Two dedicated configuration sets do exist for the RF configuration: One defining the settings in case the EMVCo polling loop is active, and another one on case the NFC Forum polling loop is active. Activating a dedicated polling loop automatically causes the related RF configuration to be loaded from the non-volatile memory. There is no need to load configuration files like it is required by other products supporting the NCI interface.

The loading of the RF configuration to the non-volatile memory is typically done only once during production.

Note:

Frequent automatic reloading of the RF configuration in the application is not recommended, since the number of possible configuration updates (EEPROM programming cycles) is technically limited.

8.2 NCI interface

The functionality of the NCI interface is described in the user manual and the NCI 2.0 Interface standard.

8.3 Byte and bit order

The byte and bit order describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte-sized data (8 bit) with an array size of 2 is as follows:

Value hex: 0x1234

address x: 12

address x+1: 34

The location of word-sized data (16 bit) is as follows:

Value hex: 0x1234

address x: 34

address x+1: 12

The location of word-sized data (16 bit) in an array size of 2 is as follows:

The placement of the array is large endian, the placement of nibbles of the variable is small endian.

Value hex: 0xAABBCCDD

address x: BB

address x+1: AA

address x+2: DD

address x+3: CC

The location of double word-sized data (32 bit) is as follows:

Value hex: 0xAABBCCDD

address x: DD

address x+1: CC

address x+2: BB

address x+3: AA

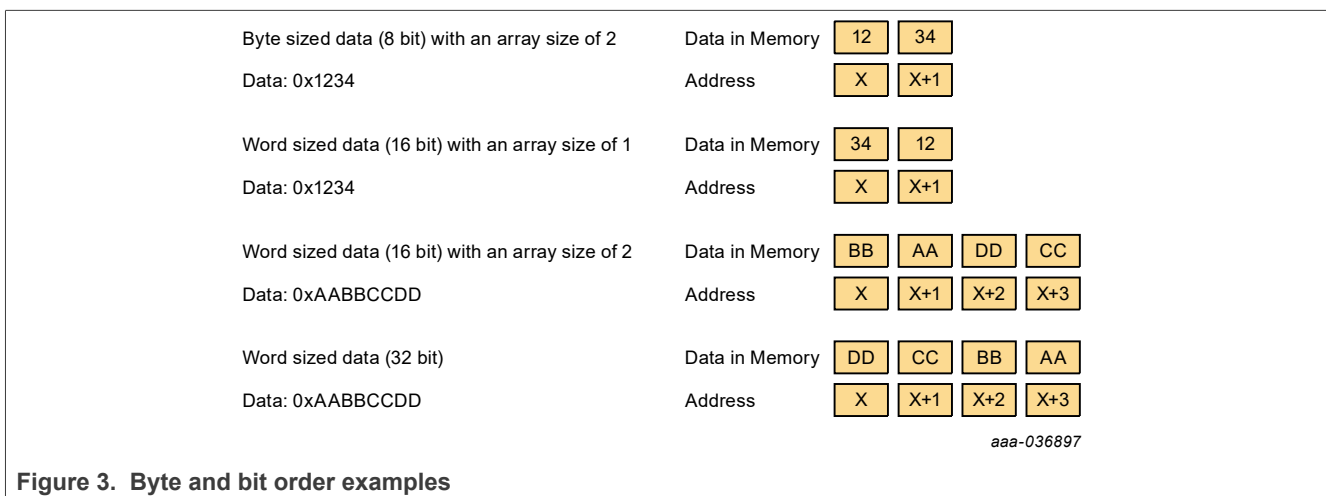


Figure 3. Byte and bit order examples

Data from the EEPROM is read in little-endian format - LSB first. This means that the byte at the lower address is read first.

The PN7220 is a little-endian system. This means that the byte at the lower address is read first.

8.4 Initial calibration

The PN7220 requires a calibration before the RF field is switched on for the first time with unloaded condition.

"Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following:

Write EEPROM CfgNovCal – 0x00

Write REGISTER TX_NOV_CALIBRATE_AND_STORE_VAL - 0x01

Write EEPROM CfgNovCal – 0x02

8.5 System power states

The PN7220 can operate in different power states. The functionality and current consumption is dependent on the actual system power state.

Power states can be changed by the level on the pin VEN and by connecting/disconnecting the power supply of VBAT. Power state change will also be triggered by certain events - VDDIO Loss, overcurrent detection, overtemperature.

In addition, state changes are triggered possible by host commands.

Disconnecting and connecting the power supply on VBAT restarts the PN7220 always in Active State after releasing the pin VEN (transition low to high).

A transition of low to high on pin VEN restarts the PN7220 always in Active State.

The following power states are supported:

Power state	Description	Typical current consumption
Power off	The NFC system (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, I/O pad interface on pin VDDIO). Device is not functional	-
PMU off	The NFC system is disabled by the host via a low signal on pin VEN. No internal clocks of the PN7220 are active. Entry to PMU OFF can also be triggered by power loss on VDDIO. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, VDDIO restore.	5 µA
ULP standby	Not supported	-
Hard power down	The NFC system is disabled by the host system via the reset/enable signal on VEN or by detecting an external condition (for example, battery voltage monitor). The power dissipation is reduced to a minimum. No power dissipation or leakage is expected on the different interfaces. Low-power resources are enabled (VDDC_LP, VHV_LP, LQ_REF, LQ-BIAS). LFO clock is available. PCRM is supplied and is running in low-power state. I/	40 µA

Power state	Description	Typical current consumption
	Os are supplied by VDDC_HP. Wake-up events: Power reset on pin VBAT, VEN rising edge,	
Standby	The NFC system can switch after a specific time of inactivity automatically into a low-power mode to minimize power dissipation. The state of external interfaces is maintained properly. PMU operates in low-power state. Wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, LPDET, wake-up counter, power loss on VDDIO, GPIO, RxPROT, No High Temp on TX and so on.	45 µA
Active	The PN7220 is able to process internal or external events or data. All external power supply sources and the external clock must be available, and all internal clocks are active.	20 mA (system without RF current)

8.6 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations must be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX_LDO. A clean supply voltage without noise is required to achieve a good RF performance. In this configuration the DPC, current measurement and overcurrent protection is not available.

8.6.1 System power supply overview

The PN7220 is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIOs (VDDIO)
2. Supply for the analog and digital blocks (VBAT/VBAT_PWR)
3. Supply of the RF drivers (VDDPA), DC-DC (VBAT_PWR), and TX_LDO (VUP)

The functionality of the GPIOs, host interface and internal analog and digital blocks is independent from the supply of the RF driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBAT_PWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT.

8.6.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors must be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.

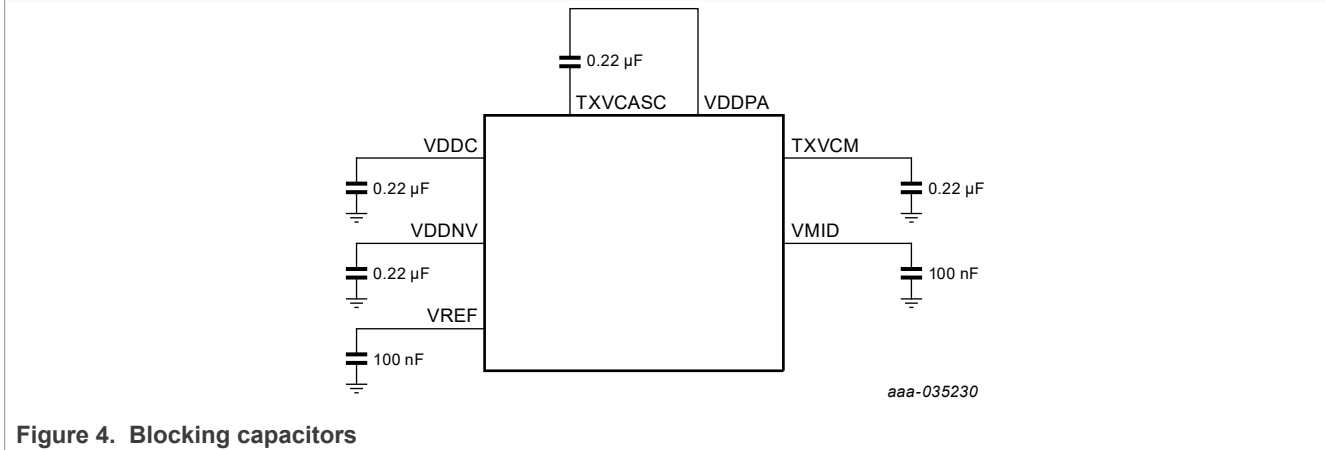


Figure 4. Blocking capacitors

8.6.3 Transmitter power supply

The PN7220 is configured by EEPROM for the different power supply options.

The following EEPROM Addresses are used to configure the power supply of the transmitter:

DCDC_PWR_CONFIG (0000h) - Enables/disables and configures the DC-DC according to the external supply connections.

TX_LDO_CONFIG (address 0002h) - Enables/disables and configures the TX_LDO.

TX_LDO_VDDPA_HIGH (address 0006h) - initial out voltage when DPC is used.

TX_LDO_VDDPA_LOW (address 0007h) - lowest VDDPA when DPC is used.

TX_LDO_VDDPA_MAX_RDR (address 0008h) - maximum voltage to be set in reader mode used by DPC.

TX_LDO_VDDPA_MAX_CARD (address 0009h) - VDDPA maximum voltage to be set in card mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

8.6.3.1 TX_LDO transmitter supply

TX_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.

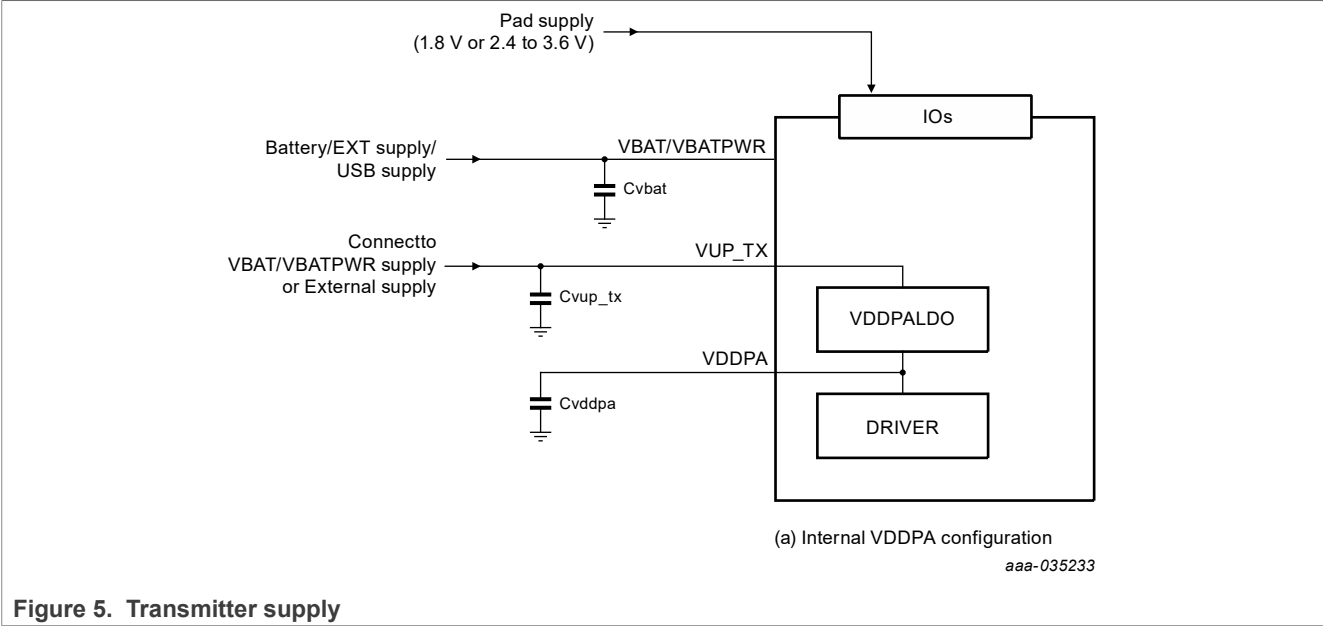


Figure 5. Transmitter supply

8.6.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX_LDO must be configured OFF by SW configuration. VUP_TX and VDDPA connected to VBAT/VBAPWR.

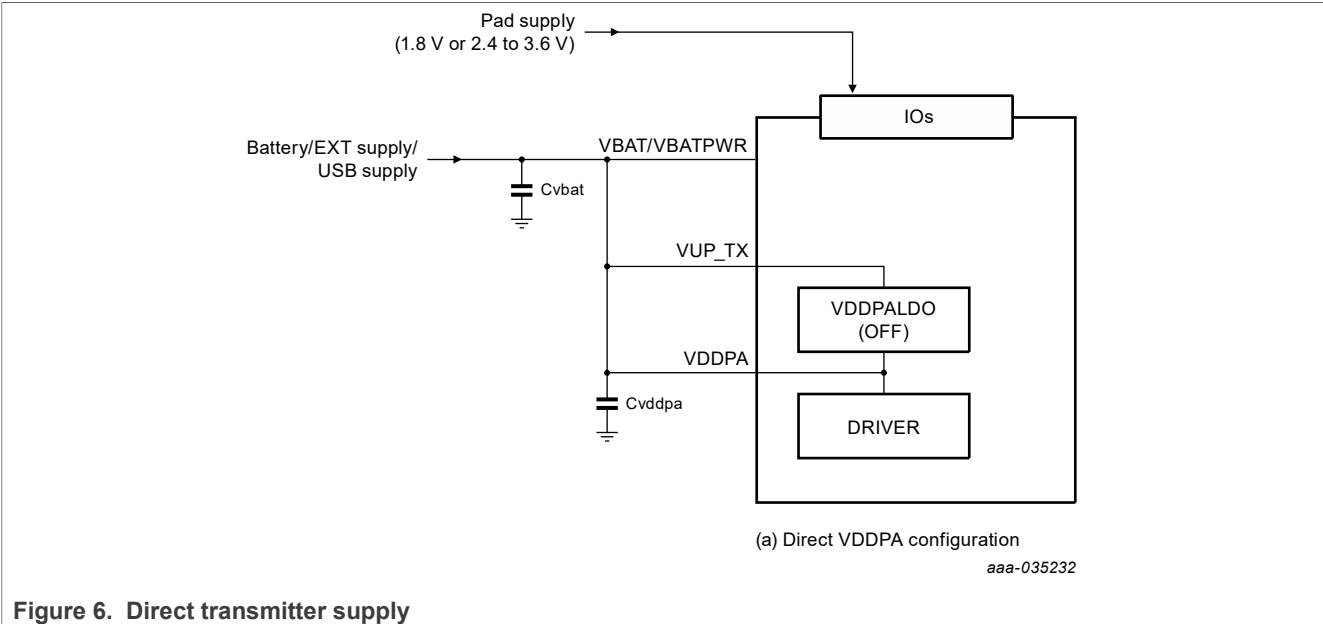


Figure 6. Direct transmitter supply

8.6.3.3 DC-DC (boost) supply

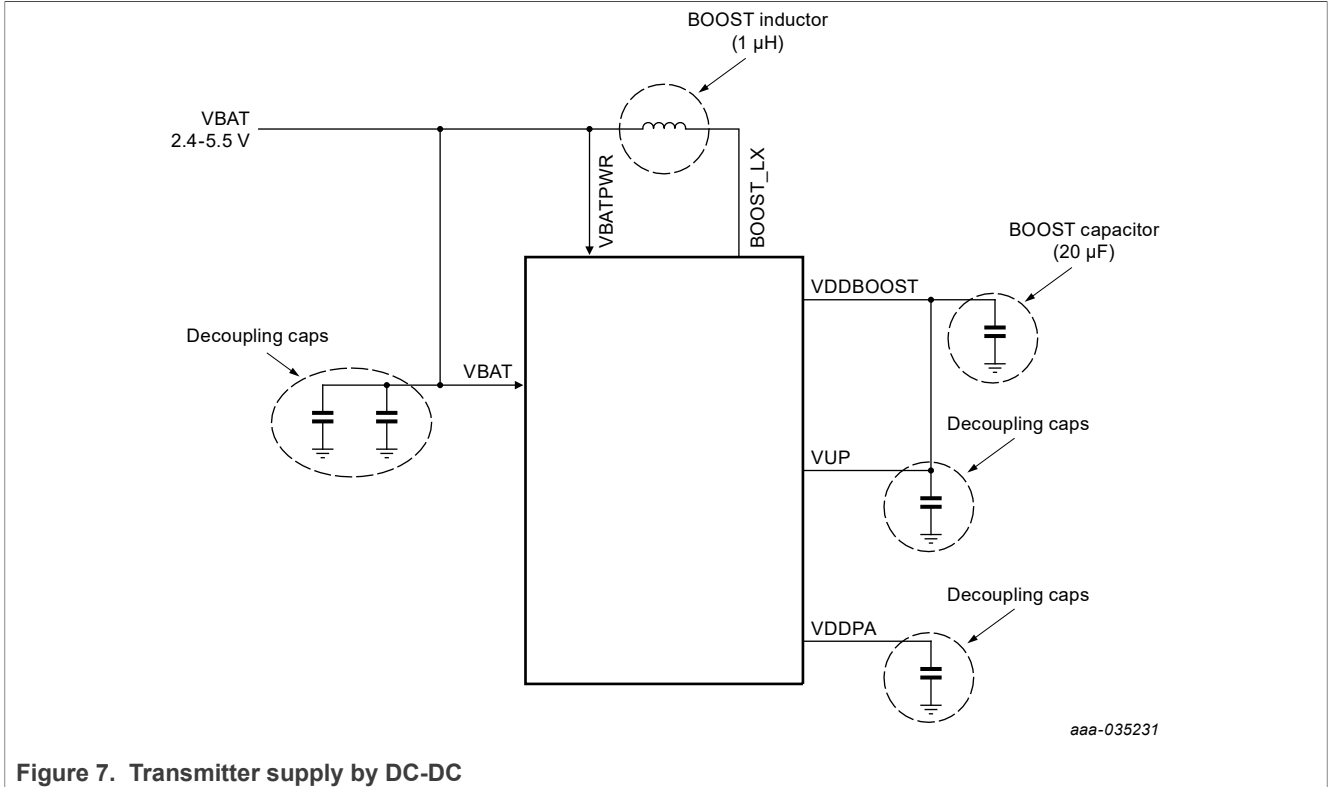


Figure 7. Transmitter supply by DC-DC

8.6.3.4 Configuration example 1: TX_LDO transmitter supply - DC-DC active

VBAT is connected to VBATPWR.

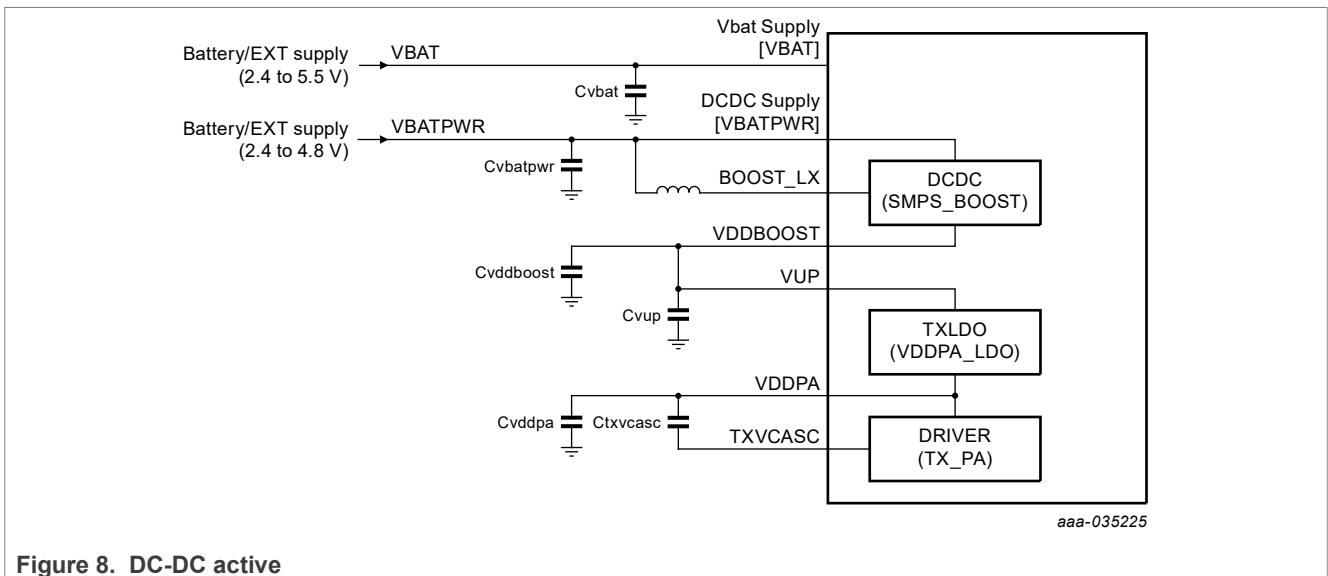


Figure 8. DC-DC active

8.6.3.5 Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed

VBAT is connected to VBATPWR.

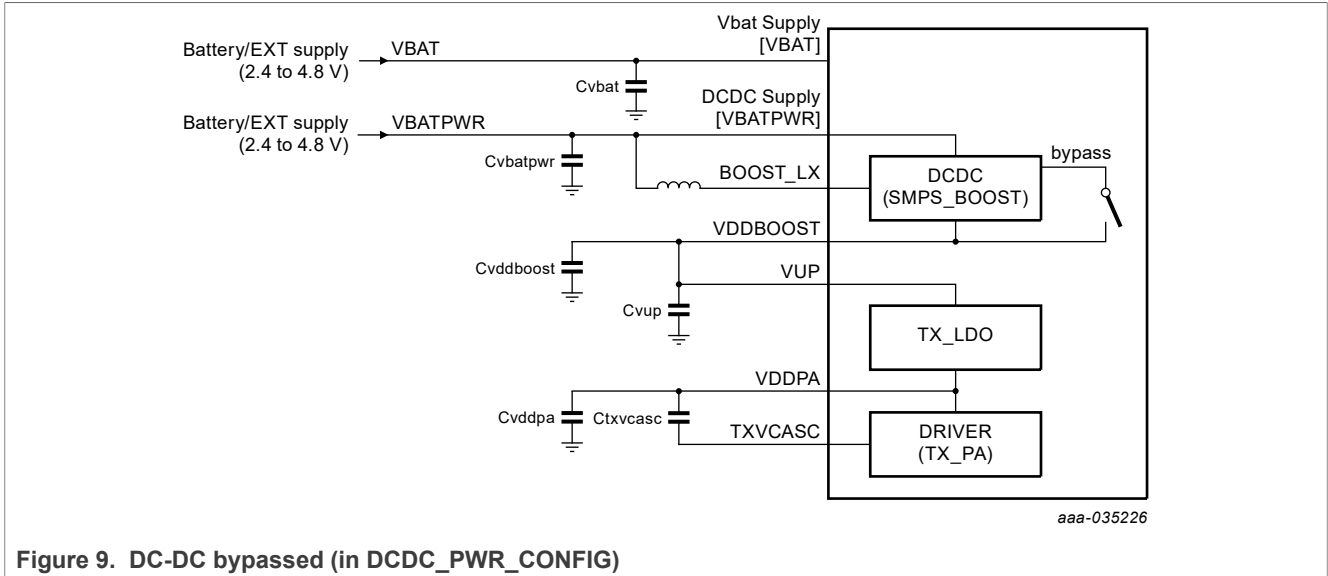


Figure 9. DC-DC bypassed (in DCDC_PWR_CONFIG)

8.6.3.6 Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC

VBAT is connected to VBATPWR.

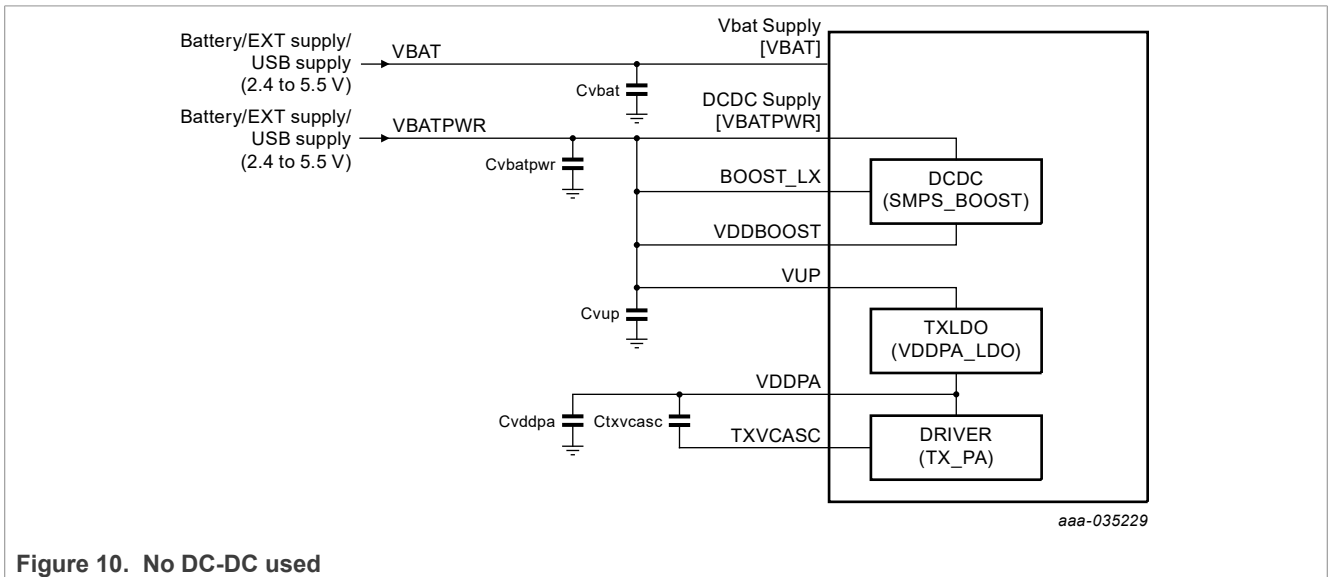


Figure 10. No DC-DC used

8.6.3.7 Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC

VBAT is connected to VBATPWR.

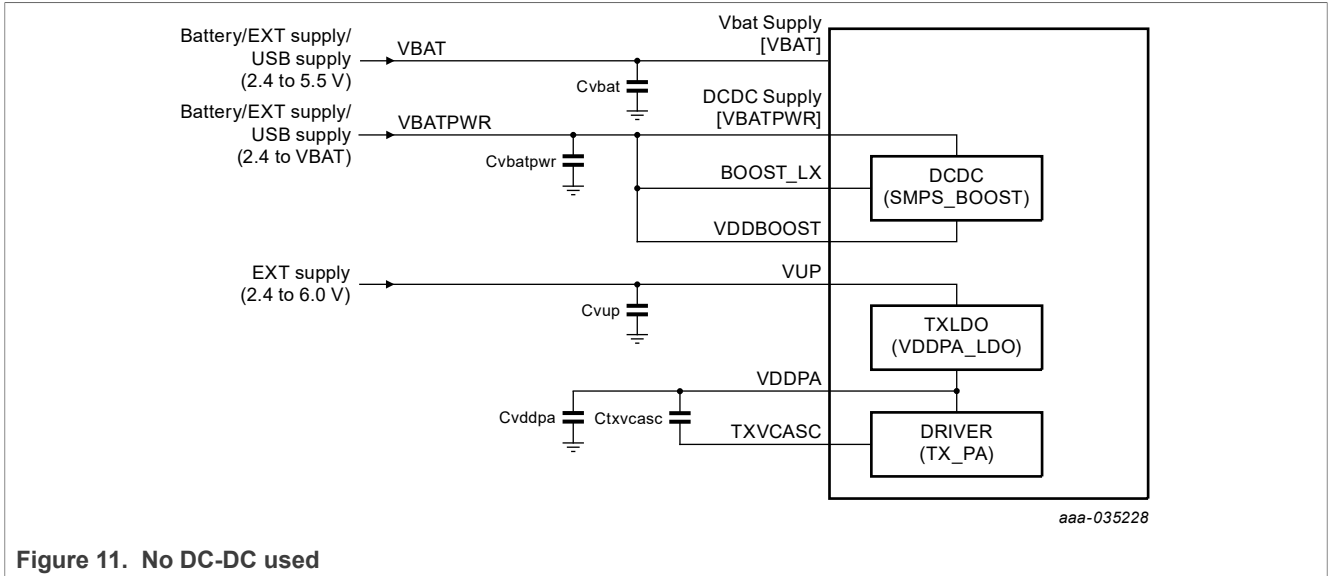


Figure 11. No DC-DC used

8.6.3.8 Configuration example 5: TX_LDO not used - no DC-DC

VBAT is connected to VBATPWR.

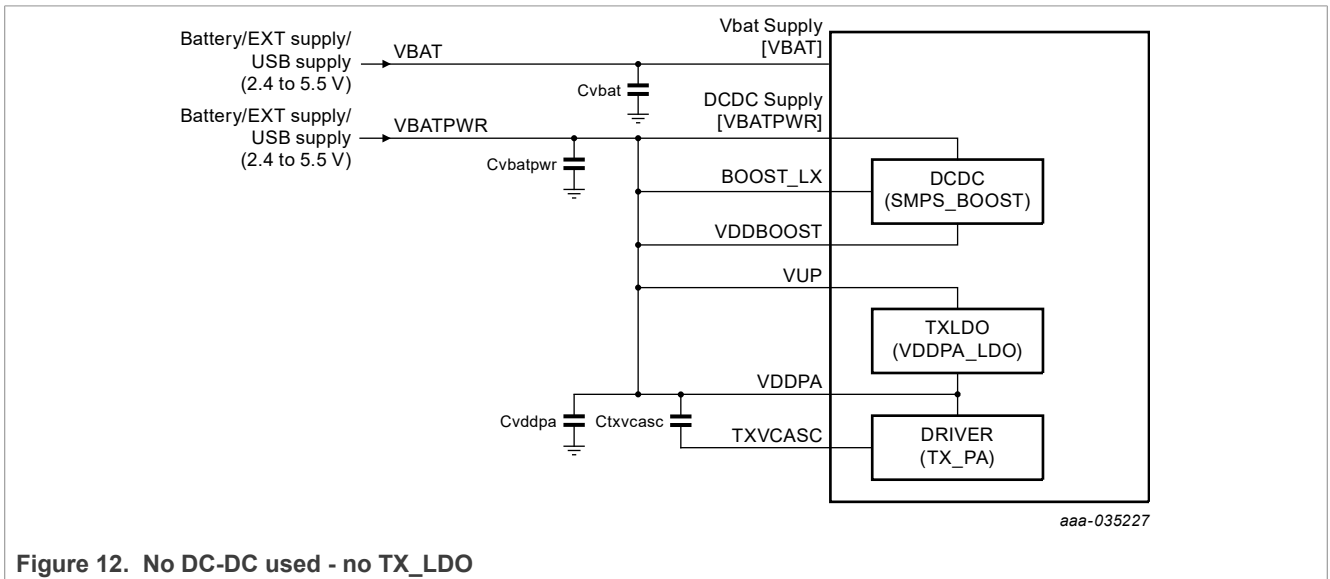


Figure 12. No DC-DC used - no TX_LDO

8.6.3.9 Supply voltage range for transmitter supply configuration examples

Table 4. Supply voltage range configuration

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independent from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (address 0076h)					
DCDC_PWR_CONFIG (address 0000h)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x01	0x01	NA
TXLDO_VDDPA_HIGH (0x06)	0x0 (1.5 V)	0x0(1.5 V)	0x0(1.5 V)	0x0(1.5 V)	NA
TXLDO_VDDPA_MAX_RDR (0008h)	0x2A(5.7 V)	0x2A(5.7 V)	0x2A(5.7 V)	0x2A(5.7 V)	NA
BOOST_DEFAULT_VOLTAGE (000Ah)	0x1D (6 V).	NA	NA	NA	NA
EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (address 0076h)					
DCDC_PWR_CONFIG (address 0000h)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x01	0x01	0x00
TXLDO_VDDPA_HIGH (0x06)	0x0 (1.5 V)	0x0(1.5 V)	0x0(1.5 V)	0x0(1.5 V)	0x0(1.5 V)
TXLDO_VDDPA_MAX_RDR (0008h)	NA	NA	NA	NA	NA
BOOST_DEFAULT_VOLTAGE (000Ah)	0x1D (6 V).	NA	NA	NA	NA

Table 5. Supply voltage range

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independent from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
VBAT	2.8 V ... 4.8 V	2.8 V ... 4.8 V	2.4 V ... 5.5 V	2.4 V ... 5.5 V	2.4 V ... 5.5 V
VBATPWR	2.8 V ... 4.8 V	2.8 V ... 4.8 V	2.4 V ... 5.5 V	2.4 V ... 5.5 V	2.4 V ... 5.5 V
VUP	3.1 V ... 6.0 V	2.8 V ... 6.0 V	2.4 V ... 6.0 V	2.4 V ... 6.0 V	2.4 V ... 5.5 V
VDDPA	VUP-0.3V drop of TX_LDO. max 5.7 V	VBATPWR - 0.5 V voltage drop	internally connected to TX_LDO	internally connected to TX_LDO	2.4 V ... 5.5 V

8.7 Clock generation

The device supports the operation with two clock options, which is configured in EEPROM address CLK_INPUT_FREQ (0012h).

One option is clocking by a crystal (default), the other a clocking by an external clock input frequency.

It is important to consider additional phase noise introduced, for example by clock drivers in the design. Phase noise of the external clock has an impact on the RF performance which can be achieved.

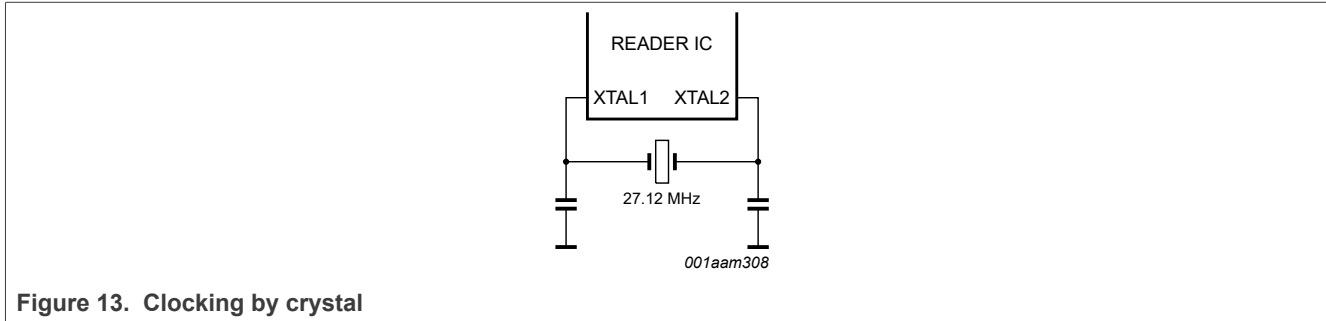


Figure 13. Clocking by crystal

8.8 External interfaces

The PN7220 requires the connection of a power supply, and a clock source like crystal or external clock and a host microcontroller connected to at least one NCI host interface for operation.

Additional connections of the package require the connection of stabilizing capacitors and ground.

The RF interface connects transmitter and receiver to the EMC filter of a connected antenna matching network. Additional connections are available for the GPIOs (on PN7220 only outputs are implemented).

The device supports the connection of up to 3x TDA8035 contact reader ICs which allow to realize ISO/IEC7816 compliant interfaces.

8.9 Transmitter overcurrent and temperature protection

The PN7220 implements different mechanisms to protect the chip against damage.

On the one hand, an overcurrent protection exists which shuts down the transmitter driver if there is a out of spec current. This can be enabled in EEPROM TXLDO_CONFIG (0002h), bit 11: overcurrent enable (0: disable, 1: enable)

An NCI notification is used to indicate the shut-down of the transmitter driver to a connected host.

On the other hand, an internal temperature sensor allows to monitor the temperature of the chip. This is configured in the EEPROM TEMP_WARNING (0648h). Three temperatures can be configured: 114 °C, 2:125 °C, 3:130 °C.

An NCI notification is used to indicate this temperature warning to a connected host.

The actual measured temperature is available in the register TEMP_SENSOR (005Bh). The chip will go into standby immediately.

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

8.10 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong near of the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (e.g. NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

The DPC allows to define two different targets current and maximum VDDPA settings for the two available modes to address EMVCo and NFC-related requirements with the same antenna.

Features of the Dynamic power control (DPC 2.0):

- True current measurement provides maximum information for the regulation loop
- The transmitter current can be limited and additionally reduced according to detected transmitter current condition / antenna detuning condition
- DPC works autonomously without host interaction causing no additional processing load on the host
- Fastest response time of 1 ms for regulation
- Used for adaptive waveshape control (AWC)
- Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode

2. Current limiting + Current reduction mode

The DPC is configured in the EEPROM, this configuration is used after startup. This avoids that the host must configure the chip after each reset or power off.

The following EEPROM registers are most relevant for the DPC configuration:

DPC_Config: Enables/Disables the DPC (enable: 0x39, disable: 0x00)

DPC_TargetCurrent: Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

- The DPC_TargetCurrent is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at. For each of the modes - NFC Forum and EMVCo, one dedicated configuration does exist:

DPC_TargetCurrent_EMVCo

DPC_TargetCurrent_NFC

VDDPA_max_EMVCo

VDDPA_max_NFC

All other DPC-related settings are used for both modes.

DPC_Hysteresis: Absolute difference to current target current in mA that triggers a DPC update event.

- The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC_Hysteresis is e.g. 20 mA.

DPC_Lookup_Table: configures the current reduction

The DPC_LOOKUP_TABLE allows in addition to the limitation of the current, to configure

- an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
- a relative change of modulated amplitude level
- and a relative change of falling and raising edge time constant for ASK10 % and ASK100 % modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC_LOOKUP_TABLE means that no additional function then the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC_LOOKUP_TABLE.

For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC_TargetCurrent or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

0x30 - DGRM_RSSI

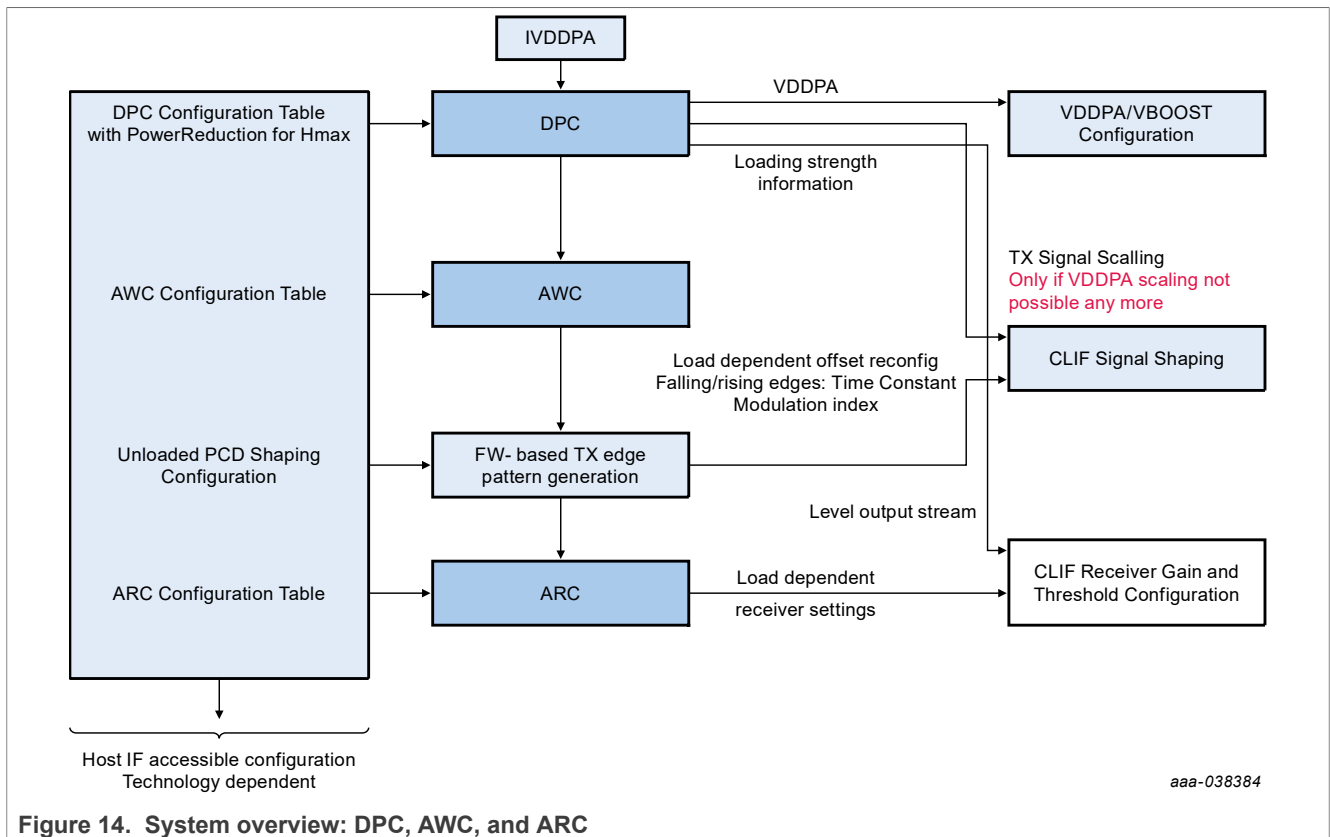


Figure 14. System overview: DPC, AWC, and ARC

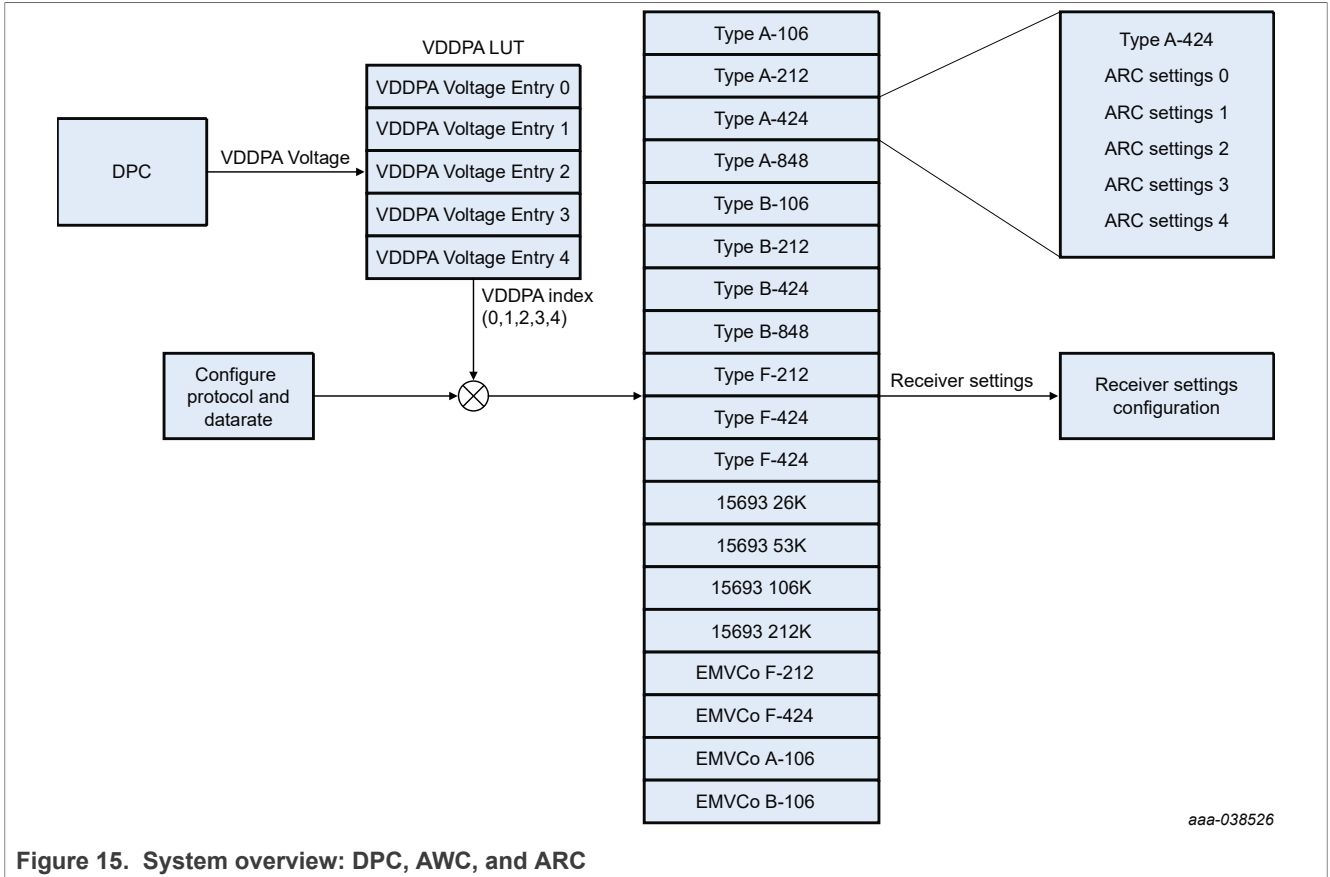


Figure 15. System overview: DPC, AWC, and ARC

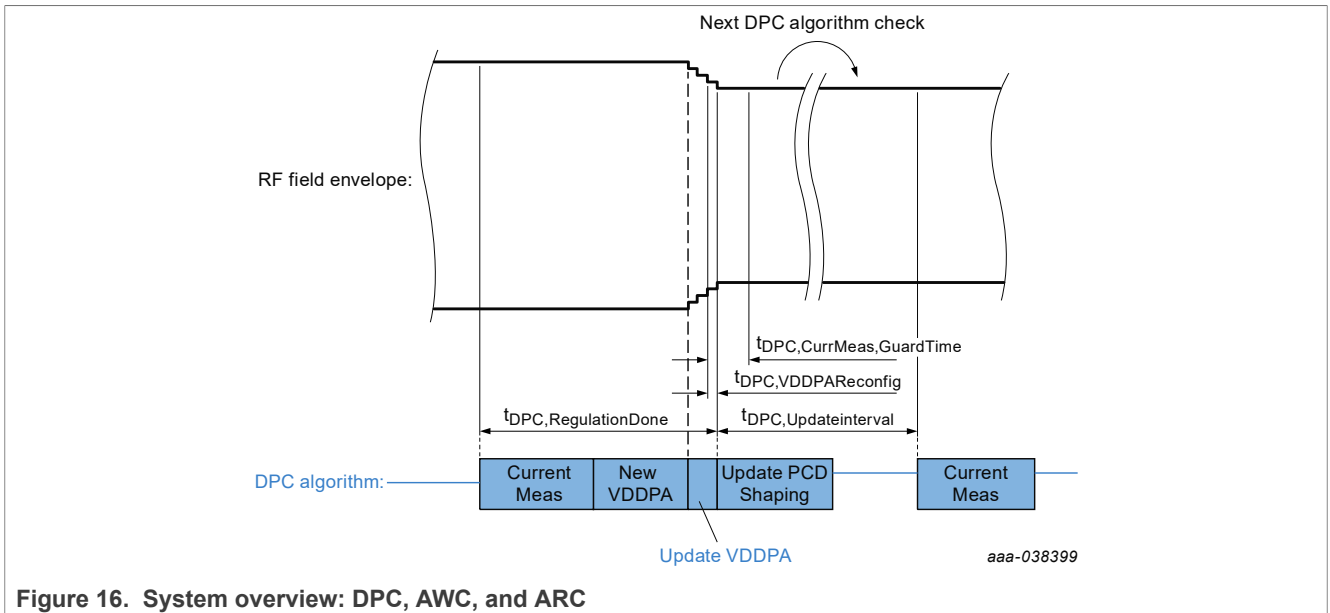


Figure 16. System overview: DPC, AWC, and ARC

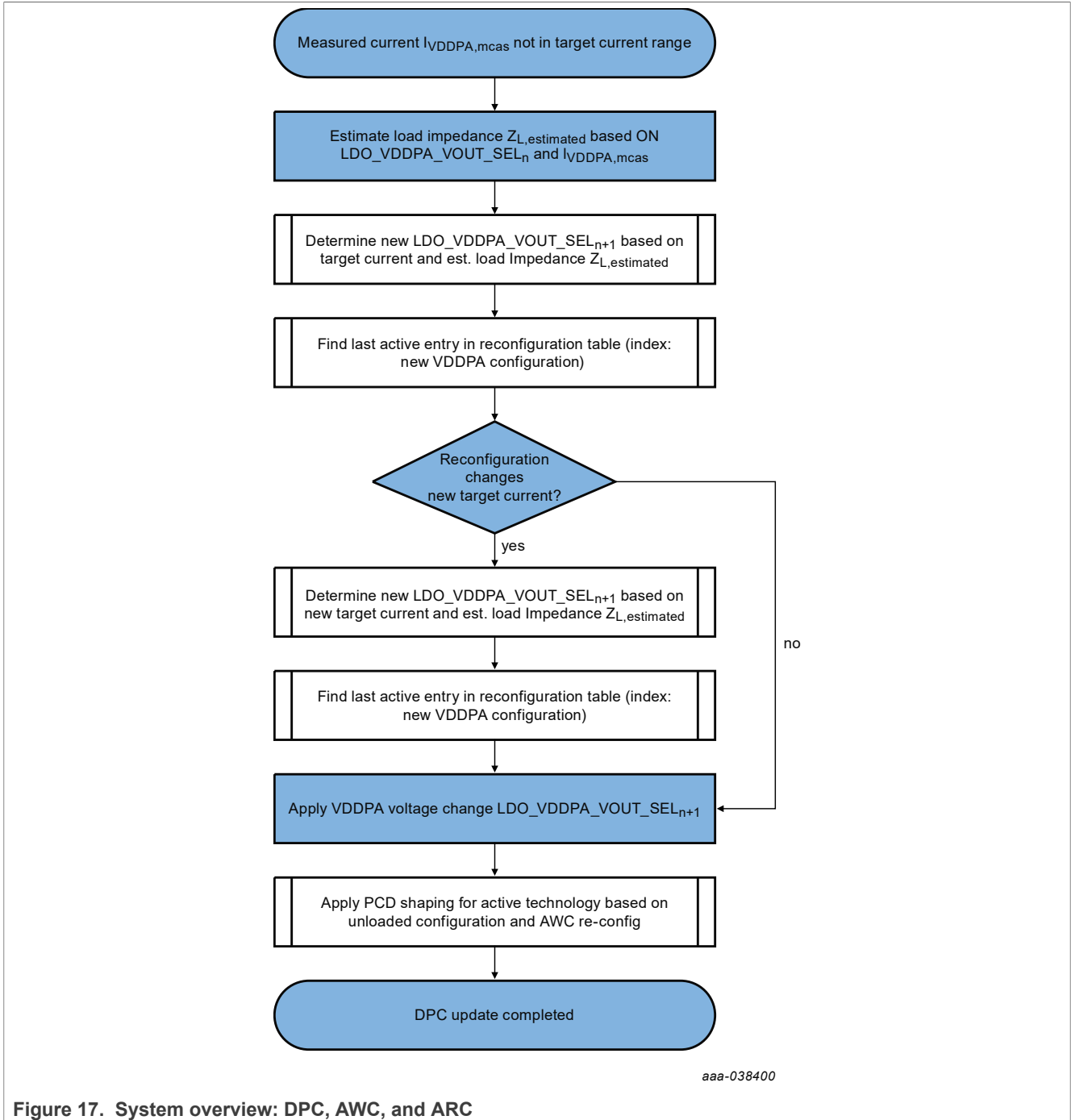


Figure 17. System overview: DPC, AWC, and ARC

8.10.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current

$$\text{VDDPA New (for target current of } I_{\text{target}}) = \text{VDDPA Voltage} / \text{VDDPA current} * I_{\text{target}}$$
3. Update VDDPA: Perform output power update

- 4. Update PCD Shaping: Apply AWC configuration updates for active technology
- 5. Update RX sensitivity parameter only for short duration

Reconfiguration table includes Relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO_VDDPA_VOOUT_SEL=0 (represents 1V5).

EXAMPLE:

Unloaded configuration After Field ON:

VDDPA max set to 42 (5.7 V) ·target current set to 280 mA

Technology B106: amp_mod=200

Falling edge time constant=rising edge time constant=3

Table 6. DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage

Function	Bit	Description
ENTRY 0	31:0	This is the entry for 1.5 V.
Target current reduction	31:23	ENTRY 0 -LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
AWC falling edge time constant for ASK10	7:0	ENTRY 0 -MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)

Loaded configuration After Field ON:

DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.

Target current stays at 280 mA.

Technology B106: amp_mod=205, falling edge time constant=2, rising edge time constant=0

8.11 Adaptive waveshaping control (AWC)

Depending on the level of detected detuning of the antenna, waveshaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. Firmware based shaping (1,2,3)
2. Lookup table based shaping (4,5,6)

The firmware based shaping allows to correct rise times and overshoot with linear transition shapes.

The lookup table based shaping allows maximum flexibility and enables to configure almost any possible correction.

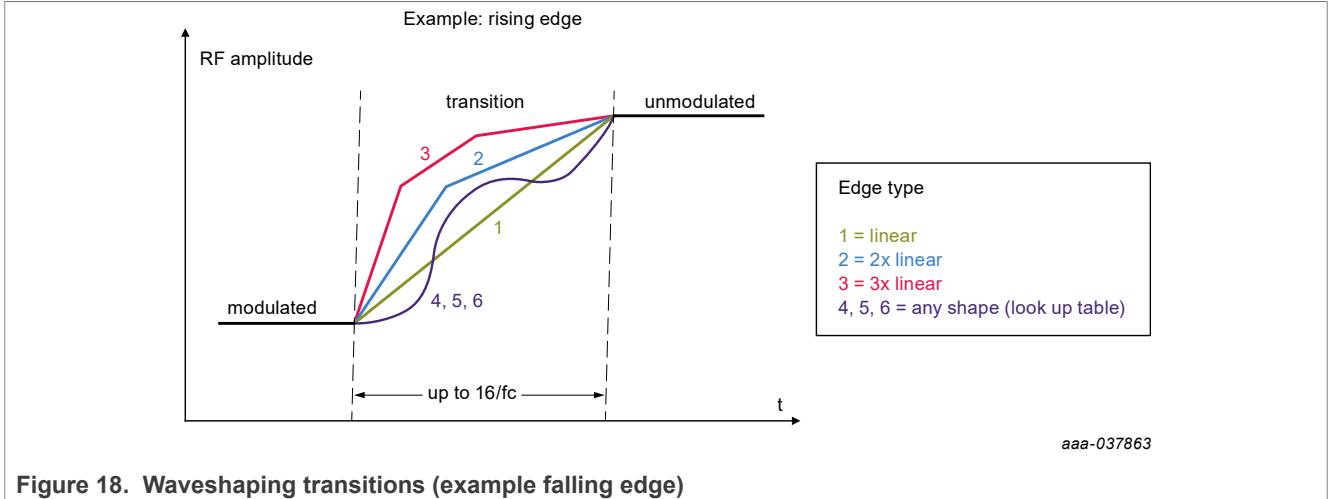


Figure 18. Waveshaping transitions (example falling edge)

The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated waveshaping configuration for the corresponding detuning condition. But allows in addition to configure the waveshaping individually dependent on the actual protocol which is active.

Features of the Adaptive Waveshape Control:

- No external components required
- No need to compromise antenna matching to meet waveshape requirements
- Waveshapes automatically adapted according to detected detuning condition
- RF standards define envelope timing and residual carrier parameters required for compliance and interoperability.

The device supports the design of compliant antennas by allowing to actively shaping the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

1. Linear transition between two amplitude levels
2. Two linear transitions between amplitude levels and
3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers `EDGE_TYPE_(protocol)`. It can be defined independent for each RF protocol and data rate - for both falling and rising edge.

The EEPROM registers `EDGE_STYLE_(protocol)` define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers `EDGE_LENGTH_(protocol)` define the total length of the edge pattern.

The figures below illustrate the edge type for the falling edge.

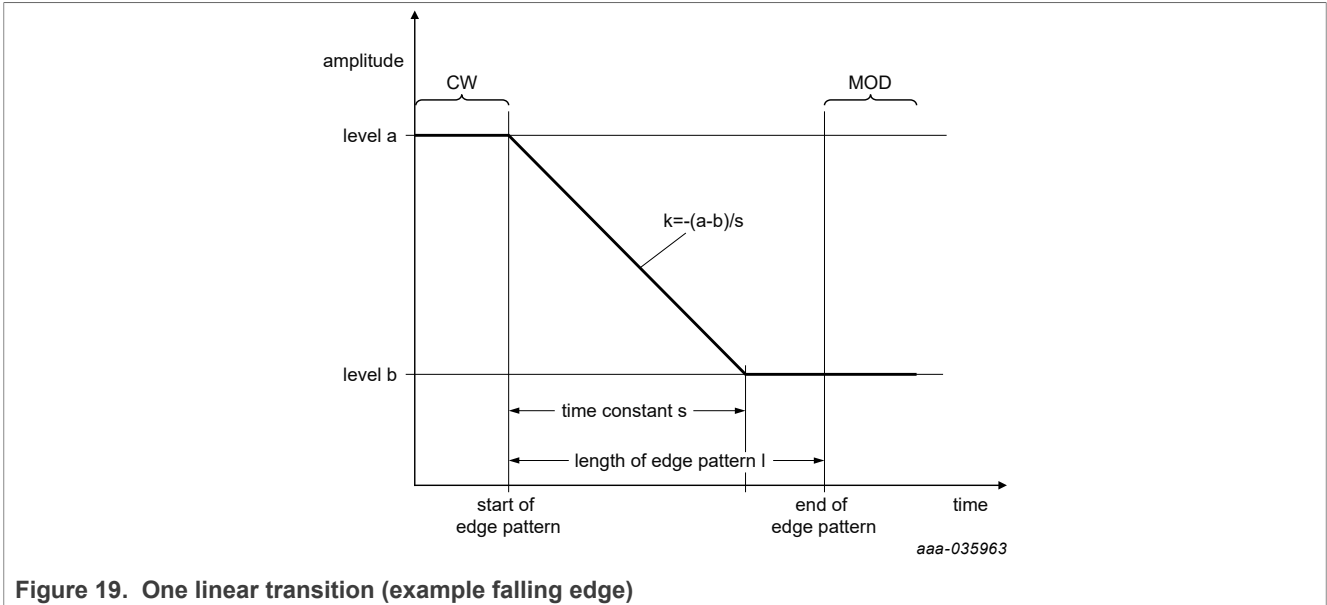


Figure 19. One linear transition (example falling edge)

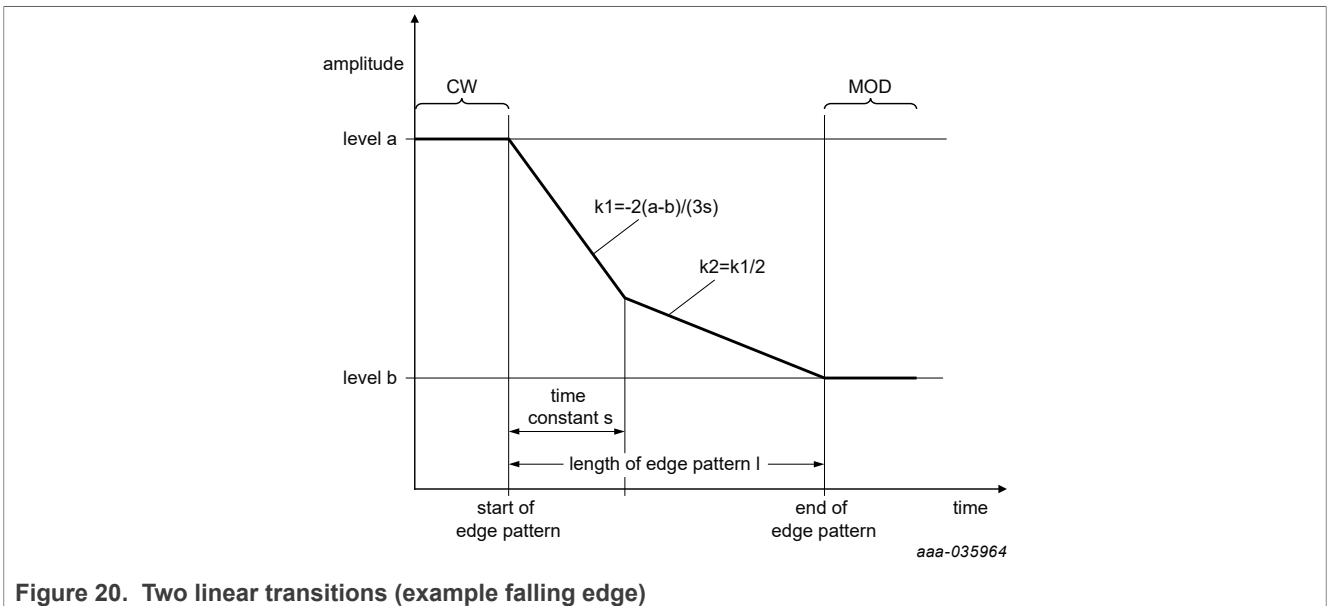


Figure 20. Two linear transitions (example falling edge)

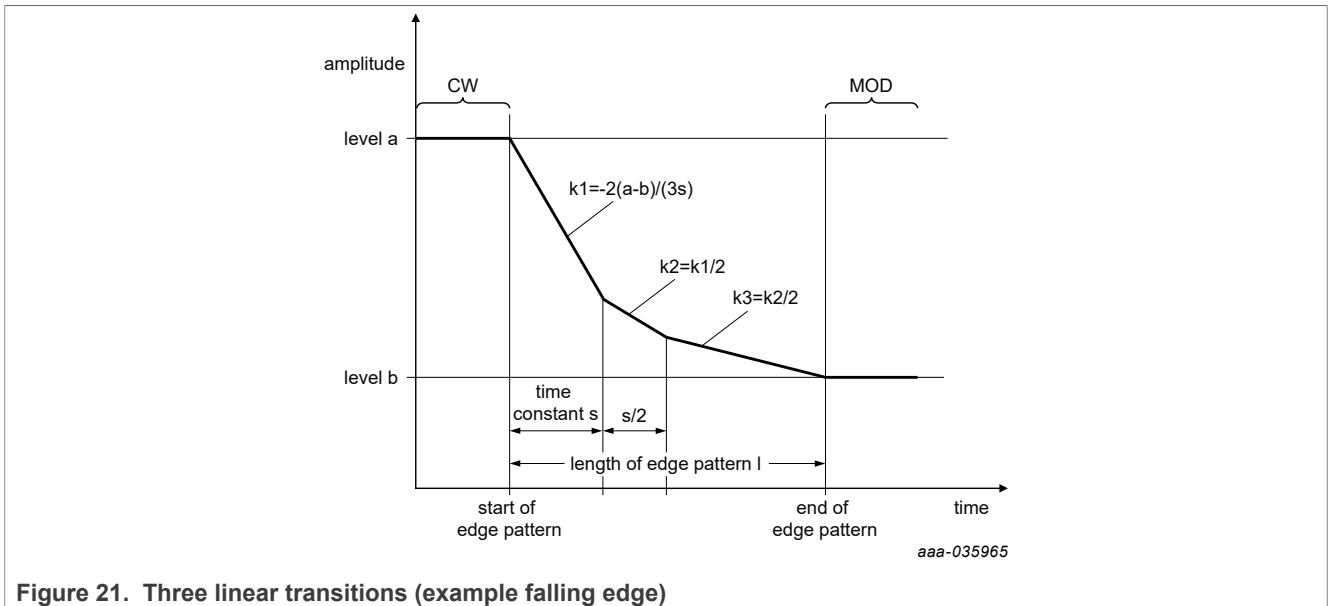


Figure 21. Three linear transitions (example falling edge)

The transition patterns are used as implicit pre-distortion to compensate effects of TX loading circuitry (for example, resonant circuitry parameters) to the emitted RF envelope.

8.12 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM_RSSI_REG (30h) ->DGRM_SIGNAL_DETECT_TH_OVR_VAL

SIGPRO_RM_Tech_REG (22h) ->RM_MF_GAIN,

The adaptive receiver control settings override the default RM_MF_GAIN and DGRM_SIGNAL_DETECT_TH_OVR_VAL settings configured by the command LOAD_RF_CONFIGURATION (0Dh).

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM_MF_GAIN, DGRM_SIGNAL_DETECT_TH_OVR_VAL and IIR_ENABLE are read from EEPROM lookup table and configured in registers.

VDDPA lookup table:

VDDPA lookup table define maximum five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA_range_index (i.e 0,1,2,3,4).

ARC_VDDPA EEPROM configuration bit description

Function	Bit	Description
ARC VDDPA Setting	7:0	Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4
	7:0	Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3

Function	Bit	Description
	7:0	Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2
	7:0	Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1
	7:0	Byte[0] = ARC_VDDPA_0: 1.5 > VDDPA < ARC_VDDPA_0

ARC lookup table:

VDDPA index and **RF protocol/datarates** are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. ARC algorithm select one out of five entries (at current protocol and baud rate) based on VDDPA_range_index.

Following table show ARC settings for Type A-106.

Table 7. ARC_RM_A106 EEPROM configuration bit description

Function	Bit	Description
RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 7. ARC_RM_A106 EEPROM configuration bit description...continued

Function	Bit	Description
		Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Table 8. ARC_RM_A106 EEPROM configuration bit description

Function	Bit	Description
RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter.

Table 8. ARC_RM_A106 EEPROM configuration bit description...continued

Function	Bit	Description
		Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: For ISO14443-A: In case ARC is disabled, it requires DPC_SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))

Note: For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.

8.13 Energy-saving card detection

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7220. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning, the system is woken up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning and the system is woken up from power-saving mode.

There is no trimming for the Low Frequency Timer required.

The NCI configuration is enabled to enter the LPCD mode with a total duration once a RF_DISCOVER_CMD is issued by the DH.

8.13.1 Low-power card detection (LPCD)

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7220. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required. The host microcontroller is woken up from power-saving mode by an IRQ send by the PN7220.

A low frequency oscillator (there is no trimming for the low frequency oscillator required) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short RF pulse. This RF pulse allows to detect a detuning of the antenna by presence of conductive objects in proximity of the antenna (card, cell phone, metal).

In case of a detected antenna detuning, the system wakes up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN7220 from Standby mode. This allows implementation of low-power card detection polling loop at application level.

The host microcontroller can then perform a card polling sequence to verify if the technology of the object causing the antenna detuning is supported by the system.

Before entering the LPCD mode, ADC_I and ADC_Q reference value must be determined. This is done during the so-called calibration.

LPCD calibration phase

- a) An initial calibration measurement is performed to set up the RX chain parameters namely HFATT, DCO_DAC_I_CTRL and DCO_DAC_Q_CTRL values.
- b) The next measurement is done using the RX chain parameters that are set up, to arrive at the ADC_I and ADC_Q values which are used as reference values. All following LPCD measurements are done relative to the LPCD calibration measurement.

The LPCD loop itself works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN7220.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the ADC_I and ADC_Q values are compared to a reference value.

- If the ADC_I and ADC_Q values exceed the reference value, PN7220 will wake-up from standby and shall try to perform Technology detection and if successful RF_INTF_ACTIVATED_NTF shall be sent to Device Host.
- If the ADC_I and ADC_Q values do not exceed the thresholds of the reference value, then PN7220 will enter into standby mode again.

These two phases are executed in a loop until:

- Card / metal is detected (LPCD_IRQ is raised).
- Reset occurs, which resets all the system configurations. The LPCD is also terminated in this case.
- NTS on host interface
- RF Level Detected

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

Table 9. Low-Power Card Detection: relevant EEPROM configuration

Name	Description
LPCD_AVG_SAMPLES	Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.
LPCD_RSSI_TARGET	Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters.

Table 9. Low-Power Card Detection: relevant EEPROM configuration...continued

Name	Description
	This parameter is used to arrive at an optimal target voltage level at RXP.
LPCD_RSSI_HYST	Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters. This is used to avoid oscillations while arriving at the target voltage level at RXP.
LPCD_THRESHOLD	If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.
LPCD_VDDPA	VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO
XTAL_CHECK_DELAY	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). For fastest startup this time, a check is performed at a time slightly higher than the expected startup time of the crystal.

Table 10. Low-Power Card Detection: relevant EEPROM configuration

Name	Description
LPCD_AVG_SAMPLES	Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.
LPCD_RSSI_TARGET	Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters. This parameter is used to arrive at an optimal target voltage level at RXP.
LPCD_RSSI_HYST	Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters. This is used to avoid oscillations while arriving at the target voltage level at RXP.
LPCD_THRESHOLD	If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.
LPCD_VDDPA	VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO
XTAL_CHECK_DELAY	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18,8us). For fastest startup this time, a check is performed at a time slightly higher than the expected startup time of the crystal.

8.14 RF-level detection

The PN7220 implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

The collision avoidance is not enabled for the EMVCo mode, and active for the NFC Forum mode.

RF Level Detector:

During low-power card detection (LPCD), the RF level detector (RFLD) acts as wake-up source from power-saving mode.

The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN7220 from power-saving mode.

NFC Level Detector:

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

8.15 Antenna connection

The PN7220 allows to connect antennas of different topology and matching to the transmitter.

Standard and recommended tuning of the antenna fitting to most applications is a symmetrical matched antenna connected to TX1, TX2 operating in push-pull operation.

VBAT is connected to VBATPWR.

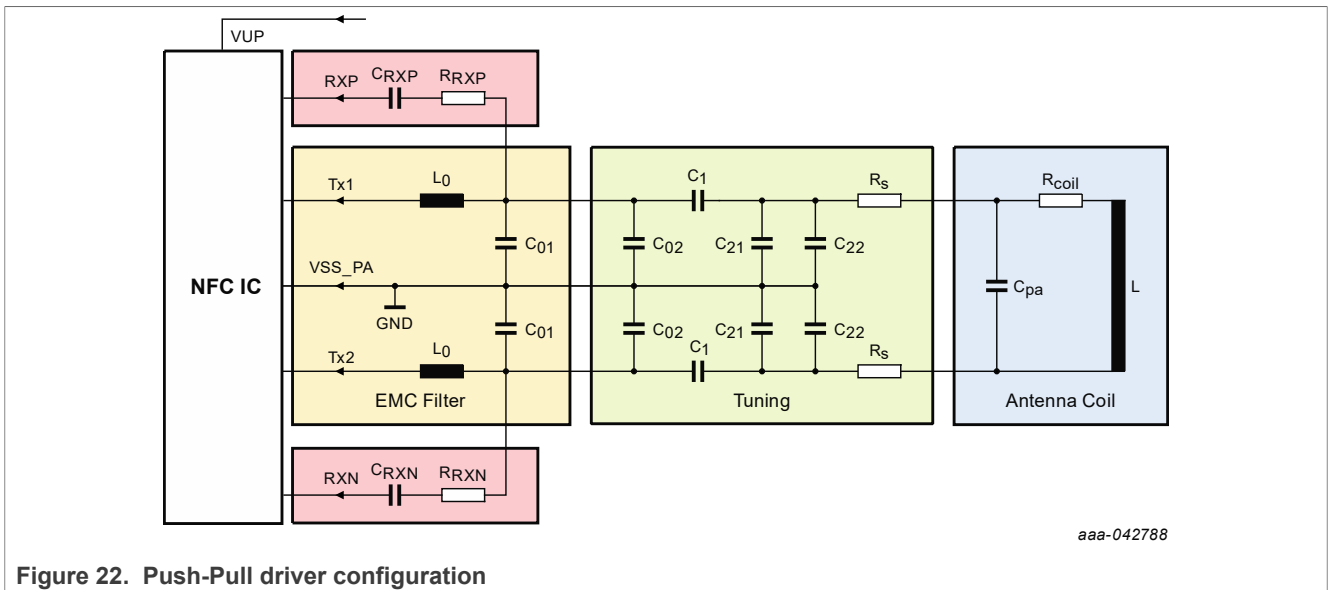


Figure 22. Push-Pull driver configuration

The PN7220 allows to operate the TX1, TX2 in common mode as well, which allows to use a single ended antenna. This configuration saves one EMC filter coil.

Note:

The RSSI target for SE must be calculated as follows and differs from the differential antenna:

$$RSSI\ target = Target\ RX\ Peak\ Voltage * 1024 / (1.8 * 2)$$

Example: For a 1.2 V target: $DGRM_RSSI_TARGET = 1.2 * 1024 / (1.8 * 2) = 341d = 0x155$

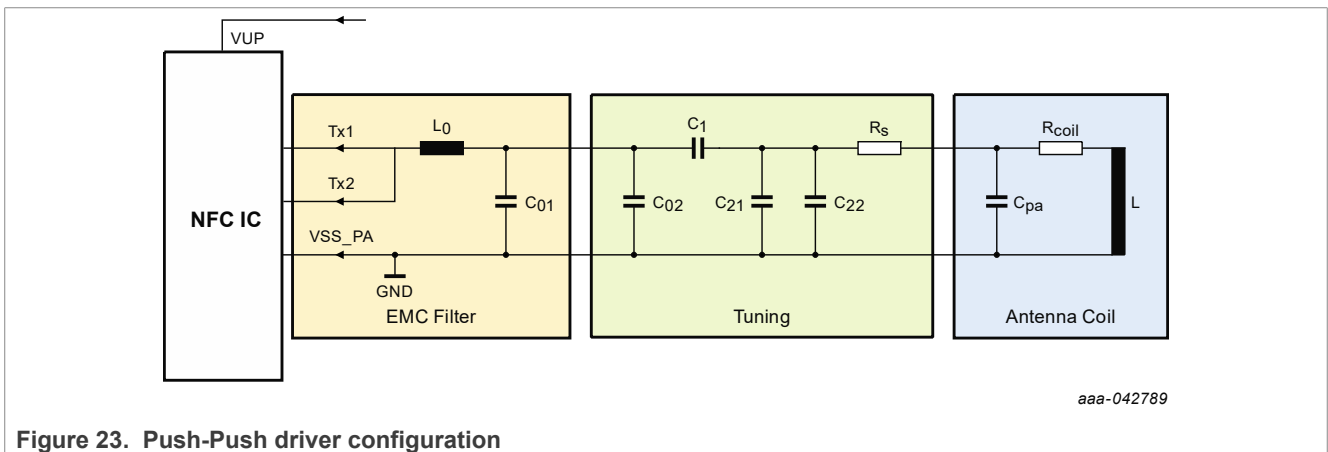


Figure 23. Push-Push driver configuration

Table 11. Antenna register configuration

Register (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2
SS_TX_CFG (0x15)	TX2_USE_TX1_CONF	1b	1b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_TRANS_RM	111b	111b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_MOD_RM	111b	111b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_CW_RM	111b	111b
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_TRANS_RM	do not care	do not care
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_MOD_RM	do not care	do not care
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_CW_RM	do not care	do not care
DGRM_RSSI (0x30)	DGRM_RSSI_TARGET	direct entry	as per calculation for SE (RSSI target = Target RX Peak Voltage*1024/ (1.8*2))
ANA_RX_CTRL (0x43)	RX_MIXER_SE_MODE_EN	0	1
ANACTRL_TX_CONFIG (0x44)	TX_INV_P_RM	10b	00b
ANACTRL_TX_CONFIG (0x44)	TX_PWM_MODE_RM	0b	0b

Table 12. Antenna EEPROM configuration

EEPROM (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2
TX_SHAPING_CONFIG (0x17)	0	0	0

Note:

Recommendation is to use all the settings configured in EEPROM. For CLIF_SS_TX_CFG_REG, the value has to be configured in EEPROM for each technology and baud rate so that the value is loaded after every load protocol.

8.16 RF debug signals

The following signals are available for debugging purposes:

The test signals are selected by sending a command string to the PN7220.

If used, **ADC-Q must be routed always to AUX1, ADC-I must be routed always to AUX2.**

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):

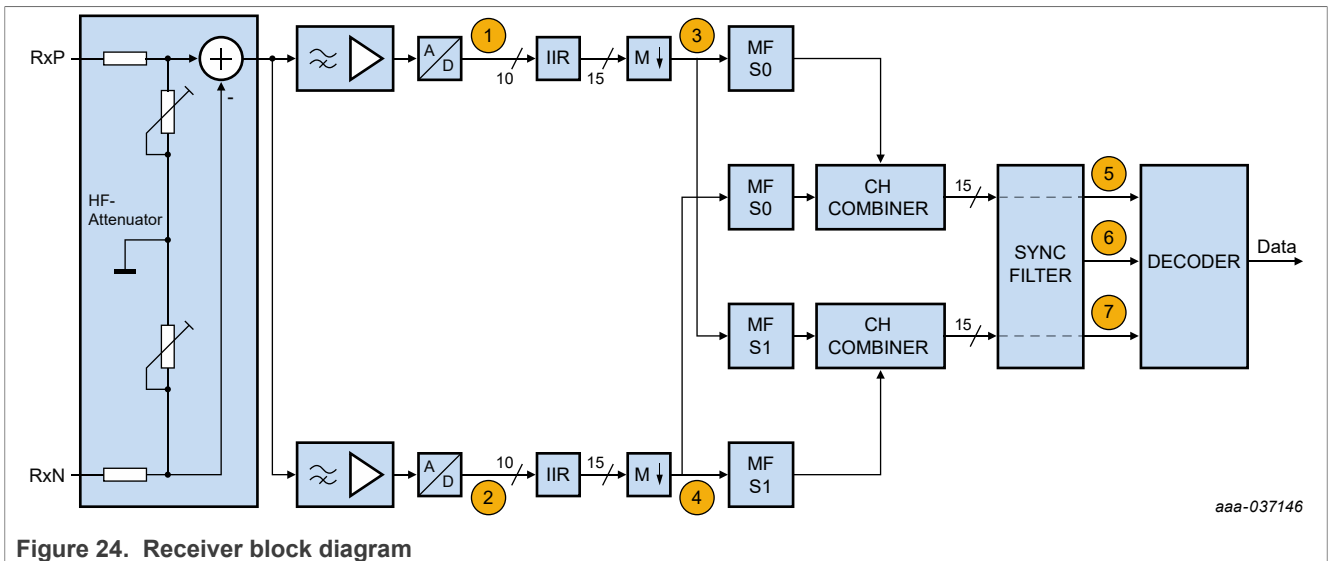


Figure 24. Receiver block diagram

Table 13. DEBUG SIGNALS

Signal	REGISTER	SIGNAL NAME	BITS	Description
ADC Data I Channel (1)	obs_clif_tbcontrol_patchbox0	adc_data_i_i	9:2	Unfiltered I channel signal upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
	obs_clif_tbcontrol_patchbox1		9; 6:0	Unfiltered I channel signal lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
ADC Data Q Channel (2)	obs_clif_tbcontrol_patchbox2	adc_data_q_i	9:2	Unfiltered Q channel signal upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
	obs_clif_tbcontrol_patchbox3		9; 6:0	Unfiltered Q channel signal lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
Preprocessor Out I Channel (3)	obs_clif_sigpro_rm0	rm_cor_adc_i_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm1		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling
Preprocessor Out Q Channel (4)	obs_clif_sigpro_rm2	rm_cor_adc_q_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm3		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling

Table 13. DEBUG SIGNALS ...continued

Signal	REGISTER	SIGNAL NAME	BITS	Description
Output MF S0 (5)	obs_clif_sigpro_rm4	mf_pt_s0_d	14:8	Delayed matched filter S0 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm5		7:0	Delayed matched filter S0 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner
Output MF S1 (6)	obs_clif_sigpro_rm6	mf_pt_s1_d	14:8	Delayed matched filter S1 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106
	obs_clif_sigpro_rm7		7:0	Delayed matched filter S1 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106
Output Synchronization Filter (7)	obs_clif_sigpro_rm8	sync_filt_out	14:8	Synchronization filter output upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm9		7:0	Synchronization filter output lower 8 bit of the 15 bit signed synchronization filter output
clif_status	transceive_state		7:5	
	rx_cl_error		4	
	tx_envelope		3	
	rx_enevelope		2	
	svalid		1	
	sdata		0	
clif_transceive	rx_start_receive		7	
	rx_over_ok		6	
	rx_over_term		5	
	rx_resume		4	
	sgp_msg_busy		3	
	fig_reset_sigpro		2	
	fig_reset_rxdec		1	
	cfg_sw_reset_sigpro		0	

Table 14. TRIGGER SIGNALS

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
TX Active	obs_clif_txenc1	tx_active_o	1	high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission.
RX Enable	obs_clif_sigpro_rm15	rx_enable_o	1	high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception
RX collision detected	obs_clif_sigpro_rm14	rm_scoll_o	1	high-level pulse indicates that the collision is detected during reception

8.17 Polling loop

The polling loop and related configuration are described in the user manual.

8.18 System settings and configuration

The configuration and behavior of the device is controlled at a central place.

EEPROM settings are a collection of all available configuration parameters that are needed for different operation modes. EEPROM settings serve as the source for the register settings.

The following two chapters list down the registers that are available to the user, as well as all available EEPROM configuration options.

This list of registers and EEPROM configuration is copied from PN5190 - it will be updated for the final product. Not all registers /EEPROM might be available on the PN7220.

8.18.1 CLIF Register description

The default setting of a bit within a register is indicated by the "*" or "Reset value". Value indicates the allowed range for the bits of a symbol.

Note, that some registers change its content by the firmware between an RF Exchange followed by an RF Reset command.

The detailed description of the registers is available in the User API documentation.

8.18.1.1 List of CLIF registers

List of CLIF registers and its addresses

Table 15. List of CLIF registers

Register Name	Register address (Hex)	Register address (Decimal)
SYSTEM_CONFIG (0x00)	0x00	0
CLIF_RX_STATUS (0x05)	0x05	5
CLIF_RX_STATUS_ERROR (0x06)	0x06	6
CLIF_STATUS (0x07)	0x07	7
CLIF_CRC_TX_CONFIG (0x12)	0x12	18
CLIF_SS_TX1_RMCFG (0x16)	0x16	22
CLIF_SIGPRO_RM_TECH (0x22)	0x22	34

Table 15. List of CLIF registers...continued

Register Name	Register address (Hex)	Register address (Decimal)
CLIF_SIGPRO_IIR_CONFIG0 (0x2A)	0x2A	42
CLIF_DGRM_BBA (0x2D)	0x2D	45
CLIF_DGRM_DCO (0x2E)	0x2E	46
CLIF_DGRM_RSSI (0x30)	0x30	48
CLIF_CRC_RX_CONFIG (0x31)	0x31	49
CLIF_RX_WAIT (0x32)	0x32	50
CLIF_SS_TX1_CMCFG (0x3B)	0x3B	59
CLIF_TIMER1_CONFIG (0x3F)	0x3F	63
CLIF_TIMER1_RELOAD (0x40)	0x40	64
TXLDO_VDDPA_CONFIG (0x54)	0x54	84
TXLDO_VOUT_CURR (0x56)	0x56	84
CLIF_RXM_FREQ (0x59)	0x59	89
INTERPOLATED_RSSI_REG (0x5C)	0x5C	92
TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D)	0x5D	93
CLIF_SS_TX1_RTRANS0 (0x80)	0x80	128
CLIF_SS_TX1_RTRANS1 (0x81)	0x81	129
CLIF_SS_TX1_RTRANS2 (0x82)	0x82	130
CLIF_SS_TX1_RTRANS3 (0x83)	0x83	131
CLIF_SS_TX2_RTRANS0 (0x84)	0x84	132
CLIF_SS_TX2_RTRANS1 (0x85)	0x85	133
CLIF_SS_TX2_RTRANS2 (0x86)	0x86	134
CLIF_SS_TX2_RTRANS3 (0x87)	0x87	135
CLIF_SS_TX1_FTRANS0 (0x88)	0x88	136
CLIF_SS_TX1_FTRANS1 (0x89)	0x89	137
CLIF_SS_TX1_FTRANS2 (0x8A)	0x8A	138
CLIF_SS_TX1_FTRANS3 (0x8B)	0x8B	139
CLIF_SS_TX2_FTRANS0 (0x8C)	0x8C	140
CLIF_SS_TX2_FTRANS1 (0x8D)	0x8D	141
CLIF_SS_TX2_FTRANS2 (0x8E)	0x8E	142
CLIF_SS_TX2_FTRANS3 (0x8F)	0x8F	143

8.18.1.2 SYSTEM_CONFIG (0x00)

This register provides the system configuration on Autocoll, MFC Crypto bit generation, ISO15693 baud-rate, TXNOV calibration.

Table 16. SYSTEM_CONFIG (0x00) register bit description

Bit	Symbol	Access	Value	Description
[31:9]	RFU	rw		Reserved
[8:8]	TX_NOV_CALIBRATE	rw		One time calibration when the host writes a 1 into this register, a one time calibration will be performed. Note: The calibration is resulting a short RF-on. All the power configurations shall be configured before setting this bit.
[7:7]	RFU	rw		Reserved
[6:5]	15693_CHANGE_DATARATE	rw		15693_changedatarate. By default, the basic data rate of 26 kB/s will be loaded, switching to a different higher data rate requires this config register to be updated. All relevant related registers will be updated automatically.
			0	RFU
			1	Change Data Rate to 53 kB/s
			2	Change Data Rate to 106 kB/s
			3	Change Data Rate to 212 kB/s
[4:2]	RFU	rw		Reserved
[1:1]	MFC_CRYPTON_ON	rw		MIFARE crypto bit generation for MIFARE Classic en/de-cryption
			0	MIFARE - crypto bit is not generated for MIFARE Classic en-/de-cryption
			1	MIFARE - crypto bit is generated for MIFARE Classic en-/de-cryption
[0:0]	AUTOCOLL_STATE_A	rw		Autocoll state for Type A
			0	TypeA Card mode: Autocoll entry with IDLE state of the card
			1	TypeA Card mode: Autocoll entry with HALT state of the card

8.18.1.3 CLIF_RX_STATUS (0x05)

This register provides the CLIF RX status.

Table 17. CLIF_RX_STATUS (0x05) register bit description

Bit	Symbol	Access	Value	Description
[31:27]	RESERVED	r-	0x0	Reserved
[26:20]	RX_COLL_POS	r-	0x0	Status indicating the bit position of the first collision detected in the data bit. The value is valid only when RX_COLLISION_DETECTED==1. The value of the RX_BIT_ALIGN is also taken into account (RX_COLL_POS = physical bit position in the flow + RX_BIT_ALIGN value). Indicates the collision position in the first 8 bytes only. Can be used during the Type A/ICODE/EPC anticollision procedure. 0x00 - 1st bit 0x01 - 2nd bit...0x7F - 128th bit. The status register is

Table 17. CLIF_RX_STATUS (0x05) register bit description...continued

Bit	Symbol	Access	Value	Description
				not updated by the collision detected on stop or parity bit.
[19:17]	RX_NUM_LAST_BITS	r-	0x0	Indicating the number of valid bits in the last byte received. This is generally used during ISO/IEC14443 type A anti-collision
			0	0: all bits are valid
			1	1: 1 bit is valid
			2	2: 2 bits are valid
			3	3: 3 bits are valid
			4	4: 4 bits are valid
			5	5: 5 bits are valid
			6	6: 6 bits are valid
			7	7: 7 bits are valid
[16:13]	RX_NUM_FRAMES_RECEIVED	r-	0x0	Indicates the number of frames received. The value is updated after every normal frame reception in RX_MULTIPLE mode. The value is valid only if the bit RX_MULTIPLE_ENABLE==1.
[12:0]	RX_NUM_BYTES_RECEIVED	r-	0x0	Number of bytes received on the RF interface. This field is not relevant when RX_MULTIPLE_ENABLE=='1'.

8.18.1.4 CLIF_RX_STATUS_ERROR (0x06)

This register provides the CLIF_RX_ERROR status.

Table 18. CLIF_RX_STATUS_ERROR (0x06) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x0	Reserved
[29:29]	EMD_DETECTED_IN_RXDEC	r-	0x0	The high level indicates that the EMD was detected (in the SigPro or in the RxDecoder or in both) during the reception.
[28:28]	EMD_DETECTED_IN_SIGPRO	r-	0x0	The high level indicates that the EMD was detected on the Physical layer (in the SigPro) during the reception.
[27:27]	EXT_RFOFF_DETECTED	r-	0x0	The high level indicates that the received frame length violated the configured minimum limit.
[26:26]	RX_FRAME_MAXLEN_VIOL	r-	0x0	The high level indicates that the received frame length is less or equal to the expected CRC field length
[25:25]	RX_FRAME_MINLEN_VIOL	r-	0x0	The high level indicates that the last received character in the frame has less than 8 bits.
[24:24]	RX_FRAME_LE_CRC	r-	0x0	The high level indicates that the last received character in the frame has 8 data bits but the expected parity bit is absent.

Table 18. CLIF_RX_STATUS_ERROR (0x06) register bit description...continued

Bit	Symbol	Access	Value	Description
[23:23]	RX_NOT_FULL_BYTE	r-	0x0	The high level indicates that the last received character in the frame has 8 data bits but the expected stop bit is absent.
[22:22]	RX_MISSING_PARBIT_DETECTED	r-	0x0	The high level indicates that the collision was detected on the parity bit position.
[21:21]	RX_MISSING_STOPBIT_DETECTED	r-	0x0	The high level indicates that the collision was detected on the stop bit position.
[18:18]	RX_COLLISION_DETECTED	r-	0x0	The high level indicates that the collision was detected during the frame reception.
[17:17]	RX_STOP_ON_RXOVER	r-	0x0	The high level indicates that the frame reception was stopped by SGP_MSG_RXOVER_* message reception.
[16:16]	RX_STOP_ON_RFOFF	r-	0x0	The high level indicates that the frame reception was interrupted by external RF-field vanishing event.
[15:15]	RX_STOP_ON_ERR	r-	0x0	The high level indicates that the frame reception was stopped by detected communication error event.
[14:14]	RX_STOP_ON_LEN	r-	0x0	The high level indicates that the frame reception was normally stopped by byte counter expiration event. Relates to the protocols where the LEN field is used in the frame format (Felica RM/CM, FWEC RM/CM).
[13:13]	RX_STOP_ON_INVPAR	r-	0x0	The high level indicates that the frame reception was normally stopped by the inverted parity detection event. Relates to the TypeA RM 212 kbit/s - 848 kbit/s modes. 12 RX_STOP_ON_PATTERN R 0h The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes.
[12:12]	RX_STOP_ON_PATTERN	r-	0x0	The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes.
[11:11]	RX_STOP_ON_ANTICOLL	r-	0x0	The high level indicates that the frame reception was normally stopped by collision detected on data bit position. Relates to the bit-oriented frame reception in TypeA RM 106 kbit/s mode during the anticollision procedure.
[10:10]	RX_CRC_ERROR	r-	0x0	The high level indicates that the CRC error is detected in the received frame.
[9:9]	RX_LEN_ERROR	r-	0x0	The high level is set if the received frame is shorter than the length stated in the received frame LEN field OR if the LEN parameter in the received frame violates the configured [RX_FRAME_MINLEN:RX_FRAME_MAX LEN] limits. Can assert only in the mode where the LEN field is used in the frame format (Felica RM/CM, FWEC RM/CM).
[8:8]	RX_SIGPRO_ERROR	r-	0x0	The high level indicates that the communication error/errors were detected during the frame reception on physical layer(in the SigPro).

Table 18. CLIF_RX_STATUS_ERROR (0x06) register bit description...continued

Bit	Symbol	Access	Value	Description
[7:7]	RX_PARITY_ERROR	r-	0x0	The high level indicates that the parity error was detected during the frame reception.
[6:6]	RX_STOPBIT_ERROR	r-	0x0	The high level indicates that the stop bit error (0 level instead of 1 on the stop bit position) was detected during the frame reception.
[5:5]	RX_WRITE_ERROR	r-	0x0	The high level indicates that the error acknowledge status was received on the CLIF-system interface during the received frame transmission to the System RAM.
[4:4]	RX_BUFFER_OVFL_ERROR	r-	0x0	The high level indicates that the data payload length in the received frame exceeds the 28 bytes limit. Relates to the PollReq procedure in the Felica RM mode only.
[3:3]	RX_LATENCY_ERROR	r-	0x0	The high level indicates that the write request flow was corrupted due to traffic congestion on the system interface during the received frame transmission to the System RAM.
[2:2]	RX_DATA_INTEGRITY_ERROR	r-	0x0	The high level indicates that the data integrity corruption (parity/CRC/etc error) was detected in the received frame.
[1:1]	RX_PROTOCOL_ERROR	r-	0x0	The high level indicates that the protocol requirements violation (stop bit error, missing parity bit, not full byte received, etc) was detected in the received frame.
[0:0]	RX_CL_ERROR	r-	0x0	The high level indicates that some protocol/data integrity error/errors were detected during the frame reception

8.18.1.5 CLIF_STATUS (0x07)

This register provides the CLIF status.

Table 19. CLIF_STATUS (0x07) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RESERVED	r-	0x0	Reserved
[29:29]	CRC_OK	r-	0x1	This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct. meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only be evaluated at the end of a communication
[28:28]	RX_SC_DETECTED	r-	0x0	Status signal indicating that a sub-carrier is detected.
[27:27]	RX_SOF_DETECTED	r-	0x0	Status signal indicating that a SOF has been detected.
[26:26]	TX_RF_STATUS	r-	0x0	If set to 1 this bit indicates that the drivers are turned on. meaning an RF-Field is created by the device itself.
[25:25]	RF_DET_STATUS	r-	0x0	If set to 1 this bit indicates that an external RF-Field is detected by the rf level detectors (after digital filtering)

Table 19. CLIF_STATUS (0x07) register bit description...continued

Bit	Symbol	Access	Value	Description
[24:24]	ADC_Q_CLIPPING	r-	0x0	Indicates that the Q-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
[23:23]	ADC_I_CLIPPING	r-	0x0	Indicates that the I-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).
[22:22]	DPLL_SATURATED_LIMIT	r-	0x0	Status signal indicating that the DPLL has reached its locking limits (integrator is at 0 or maximum)
[21:21]	DPLL_SATURATED_LOCK_RANGE	r-	0x0	Status signal indicating that the DPLL has reached its locking limits. (Saturation range configured via DPLL_SATURATION_VAL)
[20:20]	DPLL_FREQ_LOCK_SUPER_FINE	r-	0x0	Status signal indicating that the DPLL has reached frequency-lock with ~1.4Hz accuracy
[19:19]	DPLL_FREQ_LOCK_FINE	r-	0x0	Status signal indicating that the DPLL has reached frequency-lock with ~5Hz accuracy
[18:18]	DPLL_FREQ_LOCK_COARSE	r-	0x0	Status signal indicating that the DPLL has reached frequency-lock with ~50Hz accuracy
[17:17]	DPLL_PHASE_LOCK	r-	0x0	Status signal indicating that the DPLL has reached phase-lock (typically happens before DPLL_FREQUENCY_LOCK_COARSE is set).
[16:16]	DPLL_ENABLE	r-	0x0	This bit indicates that the DPLL Controller has enabled the DPLL (RF on RF frequency ok PLL locked)
[15:15]	RESERVED	r-	0x0	Reserved
[14:14]	BMA_TRANSFER_ONGOING	r-	0x0	Status signal from Buffer Manager to indicate that a transfer is actually ongoing.
[13:13]	TX_READ_ERROR	r-	0x0	This error flag is set to 1 if for an ongoing transmission data is not copied from RAM in time (BMA encountered read error) and therefor the transmission is aborted. Note: This case should not happen in normal operation
[12:12]	TX_LATENCY_ERROR	r-	0x0	This error flag is set to 1. if for an ongoing transmission data is not available in time (BMA latency to big) and therefor the transmission is aborted. Note: This case should not happen in normal operation
[11:11]	TX_NO_DATA_ERROR	r-	0x0	This error flag is set to 1. in case a transmission is started but no data is available (register NumBytesTo Send == 0).
[10:8]	RF_ACTIVE_ERROR_CAUSE	r-	0x00	This status flag indicates the cause of an NFC-Active error. Note: This bits are only valid when the RF_ACTIVE_ERROR_IRQ is raised and will be cleared as soon as the bit TX_RF_ENABLE is set to 1.
			0x00	reset value

Table 19. CLIF_STATUS (0x07) register bit description...continued

Bit	Symbol	Access	Value	Description
			0x01	External field was detected on within TIDT timing
			0x02	External field was detected on within TADT timing
			0x03	No external field was detected within TADT timings
			0x04	Peer did switch off RFField without but no Rx event was raised (no data received)
			0x05-0x07	Reserved.
[7:6]	RESERVED	r-	0x0	Reserved
[5:5]	RX_ENABLE	r-	0x0	This bit indicates if the RxDecoder is enabled. If 1 the RxDecoder was enabled by the Transceive Unit and is now ready for data reception
[4:4]	TX_ACTIVE	r-	0x0	This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing otherwise the TxEncoder is in idle state.
[3:3]	RX_ACTIVE	r-	0x0	This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing. otherwise the RxDecoder is in idle state.
[2:0]	TRANSCEIVE_STATE	r-	0x0	This registers hold the command bits
			0	0: IDLE state
			1	1: WaitTransmit state
			2	2: Transmitting state
			3	3: WaitReceive state
			4	4: WaitForData state
			5	5: Receiving state
			6	6: LoopBack state
			7	7: reserved

8.18.1.6 CLIF_CRC_TX_CONFIG (0x12)

This register provides the settings for CLIF_CRC_TX_CONFIG

Table 20. CLIF_CRC_TX_CONFIG (0x12) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	TX_CRC_PRESET_VALUE	rw	0x0	Arbitrary preset value for the Tx-Encoder CRC calculation.
[15:7]	RESERVED	r-	0x0	Reserved
[6:6]	TX_CRC_BYTE2_ENABLE	rw	0x0	If set. the CRC is calculated from the 2nd byte onwards (intended for HID). Note that this option is used in the Tx-Encoder.
[5:3]	TX_CRC_PRESET_SEL	rw	0x000	Preset value of the CRC register for the Tx-Encoder. For a CRC calculation using 5 bits, only the LSByte is used.
			000b	000b -> 0000h reset value

Table 20. CLIF_CRC_TX_CONFIG (0x12) register bit description...continued

Bit	Symbol	Access	Value	Description
			001b	001b -> 6363h
			010b	010b -> A671h
			011b	011b -> FFFFh
			100b	100b -> 0012h
			101b	101b -> E012h
			110b	110b -> RFU
			111b	111b -> Use arbitrary preset value TX_CRC_PRESET_VALUE
[2:2]	TX_CRC_TYPE	rw	0x0	Controls the type of CRC calculation for the Tx-Encoder 0* 16-bit CRC calculation. reset value 1 5-bit CRC calculation
[1:1]	TX_CRC_INV	rw	0x0	Controls the sending of an inverted CRC value by the Tx-Encoder 0* Not inverted CRC checksum. reset value 1 Inverted CRC checksum
[0:0]	TX_CRC_ENABLE	rw	0x0	If set to one. the Tx-Encoder will compute and transmit a CRC.

8.18.1.7 CLIF_SS_TX1_RMCFG (0x16)

This register provides the settings for CLIF_SS_TX1_RMCFG

Table 21. CLIF_SS_TX1_RMCFG (0x16) register bit description

Bit	Symbol	Access	Value	Description
[31:25]	RESERVED	r-	0x00	Reserved
[24:22]	TX1_CLK_MODE_TRANS_RM	rw	0x00	TX1 clock mode in RM during transition
[21:19]	TX1_CLK_MODE_MOD_RM	rw	0x00	TX1 clock mode of modulated wave in RM
[18:16]	TX1_CLK_MODE_CW_RM	rw	0x00	TX1 clock mode of unmodulated wave in RM
[15:8]	TX1_AMP_MOD_RM	rw	0x00	TX1 amplitude of modulated wave in RM (0x00 = 0 %modulaton, 0xFF: 100 % modulation)
[7:0]	TX1_AMP_CW_RM	rw	0xFF	TX1 amplitude of unmodulated wave in RM (0x00 = 0 % signal, 0xFF: 100 % signal)

8.18.1.8 CLIF_SIGPRO_RM_TECH (0x22)

This register provides the settings for CLIF_SIGPRO_RM_TECH

Table 22. CLIF_SIGPRO_RM_TECH (0x22) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	RM_NCO_PERIOD_SEL	rw	0x0	Defines the reset value for the NCO counter
[29:27]	RM_WAIT_RES_PERIOD_SEL	rw	0x0	Defines the reset value for the Delay counter
[26:26]	RM_EGT_WINDOW_TH_SEL	rw	0x0	Defines the EGT window threshold for Type B
[25:25]	RM_DC_REMOVAL_ENABLE	rw	0x0	Reserved
[24:23]	RM_DOWNSAMPLE_RATE_SEL	rw	0x0	Defines the down sample rate for the reader demod.

Table 22. CLIF_SIGPRO_RM_TECH (0x22) register bit description...continued

Bit	Symbol	Access	Value	Description
[22:20]	RM_SOF_NUM_CYCLES_SEL	rw	0x0	Defines the number of samples in I-Code SOF.
[19:17]	RM_MF_SEL	rw	0x0	Defines the selection for the Matched-Filters
[16:15]	RM_MF_GAIN	rw	0x0	Defines the gain of the Matched-Filters
[14:13]	RM_MRC_WEIGHT_SEL	rw	0x0	Defines the channel combiner weight on the lower channel
[12:12]	RM_AVG_FILT_GAIN	rw	0x0	Defines the averaging filter gain
[11:10]	RM_AVG_FILT_SEL	rw	0x0	Defines the averaging filter selection
[9:8]	RM_SYNC_FILT_IN_SEL	rw	0x0	Defines the input selection for the sync filter.
[7:6]	RM_SYNC_FILT_SEL	rw	0x0	Defines the synchronization filter selection
[5:3]	RM_WATCH_DOG_PERIOD_SEL	rw	0x0	Defines the reset value for the watch-dog counter
[2:2]	RM_EST_RESTART_ENABLE	rw	0x0	Reserved
[1:0]	RM_OOK_STAT_LEN	rw	0x3	Defines the number of samples used to check for invalid at the beginning of a reception in A106 and Icode. Value 0x0 = 2 samples, value 0x1 = 4 samples, value 0x2 = 8 samples, value 0x3 = 16 samples

8.18.1.9 CLIF_SIGPRO_IIR_CONFIG0 (0x2A)

This register provides the settings for CLIF_SIGPRO_IIR_CONFIG0

Table 23. CLIF_SIGPRO_IIR_CONFIG0 (0x2A) register bit description

Bit	Symbol	Access	Value	Description
[31:20]	RESERVED	r-	0x0	Reserved
[19:19]	IIR_SIGN_A2	rw	0x0	IIR A1 sign
[18:12]	IIR_COEF_A2	rw	0x0	IIR A1 coef (unsigned, MSB unused) Value is coded value/64
[11:11]	IIR_SIGN_A1	rw	0x0	IIR A0 sign
[10:4]	IIR_COEF_A1	rw	0x0	IIR A0 coef (unsigned, MSB unused) Value is coded value/64
[3:1]	IIR_GAIN	rw	0x0	IIR filter gain
[0:0]	IIR_ENABLE	rw	0x0	Enable the IIR filter

8.18.1.10 CLIF_DGRM_BBA (0x2D)

This register provides the settings for CLIF_DGRM_BBA

Table 24. CLIF_DGRM_BBA (0x2D) register bit description

Bit	Symbol	Access	Value	Description
[31:30]	DGRM_FALSE_ALARM_WAIT	rw	0x0	False alarm wait in multiples of 256 cycles
[29:29]	DGRM_BBA_FAST_MODE_ENABLE	rw	0x0	Enables the BBA fast mode

Table 24. CLIF_DGRM_BBA (0x2D) register bit description...continued

Bit	Symbol	Access	Value	Description
[28:26]	DGRM_GAIN_SHIFT_DELAY	rw	0x0	Defines the delay for digital gain compensation to match the latency from BBA gain
[25:24]	DGRM_BBA_TH_SEL	rw	0x0	Defines the threshold for the max absolute ADC value
[23:22]	DGRM_MAX_SWING_TH_SEL	rw	0x0	Defines the maximum swing threshold for decreasing BBA gain
[21:20]	DGRM_MIN_SWING_TH_SEL	rw	0x0	Defines the minimum swing threshold for increasing BBA gain
[19:18]	DGRM_WATER_LEVEL_TH_SEL	rw	0x0	Defines the water level threshold
[17:17]	RESERVED	rw	0x0	RESERVED
[16:14]	DGRM_BBA_MIN_VAL	rw	0x0	Defines the minimum value of BBA gain.
[13:11]	DGRM_BBA_MAX_VAL	rw	0x0	Defines the maximum value of BBA gain.
[10:8]	DGRM_BBA_INIT_VAL	rw	0x0	Defines initial value of BBA gain. If BBA fast and slow modes are disabled, this value defines the forced value.
[7:7]	DGRM_GUESS_BBA_GAIN_ENABLE	rw	0x0	Enables the initial guess of BBA gain based on noise power estimate
[5:5]	DGRM_NOISE_POWER_EST_ENABLE	rw	0x0	Enables the noise power estimator in free running mode
[4:2]	DGRM_NOISE_POWER_SHIFT_VAL	rw	0x0	Defines the number of bits to shift right in order to scale the noise power. This is in addition to the scaling due to accumulation
[1:0]	RESERVED	r-	0x0	Reserved

8.18.1.11 CLIF_DGRM_RSSI (0x30)

This register provides the settings for CLIF_DGRM_RSSI

Table 25. CLIF_DGRM_RSSI (0x30) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	DGRM_DEMOD_EN_FORCE	rw	0x0	When set, forces demod_enable high
[30:30]	DGRM_NUM_GAIN_UPDT_FORCE	rw	0x0	When set, forces dgrm_num_gain_updt to be zero
[29:29]	DGRM_SIGNAL_DETECT_TH_OVR	rw	0x0	Enables the override of signal detect threshold. Override value is set based on DGRM_SIGNAL_DETECT_TH_OVR_VAL.
[28:27]	DGRM_RSSI_TRACK_AVG_LEN_SEL	rw	0x0	Defines the number of RSSI samples to average during track mode
[26:25]	DGRM_RSSI_INIT_AVG_LEN_SEL	rw	0x0	Defines the number of RSSI samples to average during INIT mode
[24:23]	DGRM_RSSI_WAIT_PERIOD	rw	0x0	Defines the number of RSSI samples to discard before averaging
[22:17]	DGRM_RSSI_HYST	rw	0x0	Hysteresis value for RSSI target

Table 25. CLIF_DGRM_RSSI (0x30) register bit description...continued

Bit	Symbol	Access	Value	Description
[16:7]	DGRM_RSSI_TARGET	rw	0x0	RSSI target value
[6:0]	DGRM_SIGNAL_DETECT_TH_OVR_VAL	rw	0x0	Defines the override value for signal detect threshold. when DGRM_SIGNAL_DETECT_TH_OVR is set. These bits are modified dynamically by the ARC algorithm based on the DPC voltage. Only if the ARC is disabled, the value written during LOAD_RF_CONFIGURATION(0x0D) is retained throughout the RF Field session

8.18.1.12 CLIF_CRC_RX_CONFIG (0x31)

This register provides the settings for CLIF_CRC_RX_CONFIG

Table 26. CLIF_CRC_RX_CONFIG (0x31) register bit description

Bit	Symbol	Access	Value	Description
[31:16]	RX_CRC_PRESET_VALUE	rw	0x0	Arbitrary preset value for the Rx-Decoder CRC calculation.
[15:8]	RESERVED	r-	0x0	Reserved
[7:7]	RX_FORCE_CRC_WRITE	rw	0x0	If set. the Rx-Decoder will send to the RAM the CRC bits as well.
[6:6]	RX_CRC_ALLOW_BITS	rw	0x0	If activated the frame with length less than or equal CRC_length will be always sent to the System RAM as is, without CRC bits removal.
[5:3]	RX_CRC_PRESET_SEL	rw	0x000	Preset value of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits only the LSB byte is used.
			000b	000b -> 0000h reset value Note that this configuration is set by the Mode detector for FeliCa.
			001b	001b -> 6363h Note that this configuration is set by the Mode detector for ISO14443 type A.
			010b	010b -> A671h
			011b	011b -> FFFFh Note that this configuration is set by the Mode detector for ISO14443 type B
			100b	100b -> 0012h
			101b	101b -> E012h
			110b	110b -> RFU
			111b	111b -> Use arbitrary preset value RX_CRC_PRESET_VALUE
[2:2]	RX_CRC_TYPE	rw	0x0	Controls the type of CRC calculation for the Rx Decoder 0* 16-bit CRC calc
[1:1]	RX_CRC_INV	rw	0x0	Controls the comparison of the CRC checksum for the Rx-Decoder 0* Not inverted CRC value: 0000h reset value Note that this bit is cleared by the Mode detector for ISO14443 type A and FeliCa. 1 Inverted CRC value: F0B8h Note that this bit is set by the Mode detector for ISO14443 type B.

Table 26. CLIF_CRC_RX_CONFIG (0x31) register bit description...continued

Bit	Symbol	Access	Value	Description
[0:0]	RX_CRC_ENABLE	rw	0x0	If set, the Rx-Decoder will check the CRC for correctness. Note that this bit is set by the Mode Detector when ISO14443 type B, or FeliCa (212 kBd or 424 kBd) is detected.

8.18.1.13 CLIF_RX_WAIT (0x32)

This register provides the settings for CLIF_RX_WAIT

Table 27. CLIF_RX_WAIT (0x32) register bit description

Bit	Symbol	Access	Value	Description
[31:28]	RESERVED	r-	0x0	Reserved
[27:8]	RX_WAIT_VALUE	rw	0x0	Defines the rx_wait timer reload value. Note: If set to 00000h the rx_wait guard time is disabled
[7:0]	RX_WAIT_PRESCALER	rw	0x0	Defines the prescaler reload value for the rx_wait timer.

8.18.1.14 CLIF_SS_TX1_CMCFG (0x3B)

This register provides the settings for CLIF_SS_TX1_CMCFG

Table 28. CLIF_SS_TX1_CMCFG (0x3B) register bit description

Bit	Symbol	Access	Value	Description
[31:22]	RESERVED	r-	0x00	Reserved
[21:19]	TX1_CLK_MODE_MOD_CM	rw	0x00	TX1 clock mode of modulated wave in CM
[18:16]	TX1_CLK_MODE_CW_CM	rw	0x00	TX1 clock mode of unmodulated wave in CM
[15:8]	TX1_AMP_MOD_CM	rw	0x00	TX1 amplitude of modulated wave in CM
[7:0]	TX1_AMP_CW_CM	rw	0xFF	TX1 amplitude of unmodulated wave in CM

8.18.1.15 CLIF_TIMER1_CONFIG (0x3F)

This register provides the settings for CLIF_TIMER1_CONFIG

Table 29. CLIF_TIMER1_CONFIG (0x3F) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RESERVED	r-	0x0	Reserved
[30:30]	T1_STOP_ON_RX_STARTED	rw	0x0	T1_STOP_EVENT: If set, the timer T1 is stopped when a data reception begins (1 st bit is received).
[29:29]	T1_STOP_ON_TX_STARTED	rw	0x0	T1_STOP_EVENT: If set, the timer T1 is stopped when a data transmission begins.
[28:28]	T1_STOP_ON_RF_ON_EXT	rw	0x0	T1_STOP_EVENT: If set, the timer T1 is stopped when the external RF field is detected.
[27:27]	T1_STOP_ON_RF_OFF_EXT	rw	0x0	T1_STOP_EVENT: If set, the timer T1 is stopped when the external RF field vanishes.

Table 29. CLIF_TIMER1_CONFIG (0x3F) register bit description...continued

Bit	Symbol	Access	Value	Description
[26:26]	T1_STOP_ON_RF_ON_INT	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned on.
[25:25]	T1_STOP_ON_RF_OFF_INT	rw	0x0	T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned off.
[24:24]	T1_STOP_ON_RX_ENDED	rw	0x0	T1_STOP_EVENT: If set the timer T1 is stopped when an activity on RX is detected.
[23:18]	RESERVED	r-	0x0	Reserved
[17:17]	T1_START_ON_RX_STARTED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data reception begins (1st bit is received).
[16:16]	T1_START_ON_RX_ENDED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data reception ends.
[15:15]	T1_START_ON_TX_STARTED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data transmission begins.
[14:14]	T1_START_ON_TX_ENDED	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when a data transmission ends.
[13:13]	T1_START_ON_RF_ON_EXT	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when the external RF field is detected.
[12:12]	T1_START_ON_RF_OFF_EXT	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when the external RF field is not detected any more.
[11:11]	T1_START_ON_RF_ON_INT	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned on.
[10:10]	T1_START_ON_RF_OFF_INT	rw	0x0	T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned off.
[8:8]	T1_START_NOW	rw	0x0	T1_START_EVENT: If set. the timer T1 is started immediately.
[7:7]	RESERVED	r-	0x0	Reserved
[6:6]	T1_ONE_SHOT_MODE	rw	0x00	When set to 1 the counter value does not reload again until the counter value has reached zero
[5:3]	T1_PRESCALE_SEL	rw	0x00	Controls input frequency/period of the timer T0 when the prescaler is activated in T1_MODE_SEL.
			000b	000b -> 6.78 MHz counter
			001b	001b -> 3.39 MHz counter
			010b	010b -> 1.70 MHz counter
			011b	011b -> 848 kHz counter
			100b	100b -> 424 kHz counter
			101b	101b -> 212 kHz counter
			110b	110b -> 106 kHz counter
			111b	111b -> 53 kHz counter
[2:2]	T1_MODE_SEL	rw	0x00*	Configuration of the timer T1 clock.
			0b	Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56MHz).

Table 29. CLIF_TIMER1_CONFIG (0x3F) register bit description...continued

Bit	Symbol	Access	Value	Description
			1b	Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T1_PRESCALE_SEL).
[1:1]	T1_RELOAD_ENABLE	rw	0x00*	If set to 0.the timer T1 will stop on expiration.
			0b	After expiration the timer T1 will stop counting. i.e.. remain zero. reset value.
			1b	After expiration the timer T1 will reload its preset value and continue counting down.
[0:0]	T1_ENABLE	rw	0x0	Enables the timer T1

8.18.1.16 CLIF_TIMER1_RELOAD (0x40)

This register provides the settings for CLIF_TIMER1_RELOAD

Table 30. CLIF_TIMER1_RELOAD (0x40) register bit description

Bit	Symbol	Access	Value	Description
[31:20]	RESERVED	r-	0x0	Reserved
[19:0]	T1_RELOAD_VALUE	rw	0x0000	Reload value of the timer T1.

8.18.1.17 TXLDO_VDDPA_CONFIG (0x54)

This register provides the settings for TXLDO_VDDPA_CONFIG

Table 31. TXLDO_VDDPA_CONFIG (0x54) register bit description

Bit	Symbol	Access	Value	Description
[31:8]	RESERVED	rw		Reserved
[7:0]	VDDPA_CONFIG	rw		VDDPALDO output voltage VDDPA_1V50

8.18.1.18 TXLDO_VOUT_CURR (0x56)

This register provides the settings for TXLDO_VOUT_CURR

Table 32. TXLDO_VOUT_CURR (0x56) register bit description

Bit	Symbol	Access	Value	Description
[23:8]	TXLDO_CURRENT	r-		Indicates the TXLDO Current, measured value is indicated in mA (1 bit = 1 mA)
[7:0]	VDDPA_VOUT	r-		VDDPALDO output voltage VDDPA_1V50

8.18.1.19 CLIF_RXM_FREQ (0x59)

This register provides the settings for CLIF_RXM_FREQ

Table 33. CLIF_RXM_FREQ (0x59) register bit description

Bit	Symbol	Access	Value	Description
[31:31]	RXM_FREQ_VALID	r-	0x00	CLIF_RXM_FREQ_REG fields are valid
[30:25]	RESERVED	r-	0x00	Reserved

Table 33. CLIF_RXM_FREQ (0x59) register bit description...continued

Bit	Symbol	Access	Value	Description
[24:16]	RXM_FREQ	r-	0x00	frequency difference between the last two consecutive measures at 1.7 MHz (multiple of 13.56 MHz/4096). Signed. 2-Complement coded.
[15:9]	RESERVED	r-	0x00	Reserved
[8:0]	RXM_PHASE	r-	0x00	phase value

8.18.1.20 INTERPOLATED_RSSI_REG (0x5C)

This register provides the settings for INTERPOLATED_RSSI_REG

Table 34. INTERPOLATED_RSSI_REG (0x5C) register bit description

Bit	Symbol	Access	Value	Description
[31:0]	INTERPOLATED_RSSI	r-		Calculated Interpolated RSSI

8.18.1.21 TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D)

This register provides the settings for TX_NOV_CALIBRATE_AND_STORE_VAL_REG

Table 35. TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D) register bit description

Bit	Symbol	Access	Value	Description
[31:2]	RFU	rw		Reserved
[1:0]	TX_NOV_CALIBRATE_STORE	rw		Perform TX_NOV Calibration and store in User Area

8.18.1.22 CLIF_SS_TX1_RTRANS0 (0x80)

This register provides the settings for CLIF_SS_TX1_RTRANS0

Table 36. CLIF_SS_TX1_RTRANS0 (0x80) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS3	rw	0x00	TX1 rising transition value 3
[23:16]	TX1_SS_RTRANS2	rw	0x00	TX1 rising transition value 2
[15:8]	TX1_SS_RTRANS1	rw	0x00	TX1 rising transition value 1
[7:0]	TX1_SS_RTRANS0	rw	0x00	TX1 rising transition value 0

8.18.1.23 CLIF_SS_TX1_RTRANS1 (0x81)

This register provides the settings for CLIF_SS_TX1_RTRANS1

Table 37. CLIF_SS_TX1_RTRANS1 (0x81) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS7	rw	0x00	TX1 rising transition value 7
[23:16]	TX1_SS_RTRANS6	rw	0x00	TX1 rising transition value 6
[15:8]	TX1_SS_RTRANS5	rw	0x00	TX1 rising transition value 5
[7:0]	TX1_SS_RTRANS4	rw	0x00	TX1 rising transition value 4

8.18.1.24 CLIF_SS_TX1_RTRANS2 (0x82)

This register provides the settings for CLIF_SS_TX1_RTRANS2

Table 38. CLIF_SS_TX1_RTRANS2 (0x82) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS11	rw	0x00	TX1 rising transition value 11
[23:16]	TX1_SS_RTRANS10	rw	0x00	TX1 rising transition value 10
[15:8]	TX1_SS_RTRANS9	rw	0x00	TX1 rising transition value 9
[7:0]	TX1_SS_RTRANS8	rw	0x00	TX1 rising transition value 8

8.18.1.25 CLIF_SS_TX1_RTRANS3 (0x83)

This register provides the settings for CLIF_SS_TX1_RTRANS3

Table 39. CLIF_SS_TX1_RTRANS3 (0x83) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_RTRANS15	rw	0x00	TX1 rising transition value 15
[23:16]	TX1_SS_RTRANS14	rw	0x00	TX1 rising transition value 14
[15:8]	TX1_SS_RTRANS13	rw	0x00	TX1 rising transition value 13
[7:0]	TX1_SS_RTRANS12	rw	0x00	TX1 rising transition value 12

8.18.1.26 CLIF_SS_TX2_RTRANS0 (0x84)

This register provides the settings for CLIF_SS_TX2_RTRANS0

Table 40. CLIF_SS_TX2_RTRANS0 (0x84) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS3	rw	0x00	TX2 rising transition value 3
[23:16]	TX2_SS_RTRANS2	rw	0x00	TX2 rising transition value 2
[15:8]	TX2_SS_RTRANS1	rw	0x00	TX2 rising transition value 1
[7:0]	TX2_SS_RTRANS0	rw	0x00	TX2 rising transition value 0

8.18.1.27 CLIF_SS_TX2_RTRANS1 (0x85)

This register provides the settings for CLIF_SS_TX2_RTRANS1

Table 41. CLIF_SS_TX2_RTRANS1 (0x85) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS7	rw	0x00	TX2 rising transition value 7
[23:16]	TX2_SS_RTRANS6	rw	0x00	TX2 rising transition value 6
[15:8]	TX2_SS_RTRANS5	rw	0x00	TX2 rising transition value 5
[7:0]	TX2_SS_RTRANS4	rw	0x00	TX2 rising transition value 4

8.18.1.28 CLIF_SS_TX2_RTRANS2 (0x86)

This register provides the settings for CLIF_SS_TX2_RTRANS2

Table 42. CLIF_SS_TX2_RTRANS2 (0x86) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS11	rw	0x00	TX2 rising transition value 11
[23:16]	TX2_SS_RTRANS10	rw	0x00	TX2 rising transition value 10
[15:8]	TX2_SS_RTRANS9	rw	0x00	TX2 rising transition value 9
[7:0]	TX2_SS_RTRANS8	rw	0x00	TX2 rising transition value 8

8.18.1.29 CLIF_SS_TX2_RTRANS3 (0x87)

This register provides the settings for CLIF_SS_TX2_RTRANS3

Table 43. CLIF_SS_TX2_RTRANS3 (0x87) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_RTRANS15	rw	0x00	TX2 rising transition value 15
[23:16]	TX2_SS_RTRANS14	rw	0x00	TX2 rising transition value 14
[15:8]	TX2_SS_RTRANS13	rw	0x00	TX2 rising transition value 13
[7:0]	TX2_SS_RTRANS12	rw	0x00	TX2 rising transition value 12

8.18.1.30 CLIF_SS_TX1_FTRANS0 (0x88)

This register provides the settings for CLIF_SS_TX1_FTRANS0

Table 44. CLIF_SS_TX1_FTRANS0 (0x88) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS3	rw	0x00	TX1 falling transition value 3
[23:16]	TX1_SS_FTRANS2	rw	0x00	TX1 falling transition value 2
[15:8]	TX1_SS_FTRANS1	rw	0x00	TX1 falling transition value 1
[7:0]	TX1_SS_FTRANS0	rw	0x00	TX1 falling transition value 0

8.18.1.31 CLIF_SS_TX1_FTRANS1 (0x89)

This register provides the settings for CLIF_SS_TX1_FTRANS1

Table 45. CLIF_SS_TX1_FTRANS1 (0x89) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS7	rw	0x00	TX1 falling transition value 7
[23:16]	TX1_SS_FTRANS6	rw	0x00	TX1 falling transition value 6
[15:8]	TX1_SS_FTRANS5	rw	0x00	TX1 falling transition value 5
[7:0]	TX1_SS_FTRANS4	rw	0x00	TX1 falling transition value 4

8.18.1.32 CLIF_SS_TX1_FTRANS2 (0x8A)

This register provides the settings for CLIF_SS_TX1_FTRANS2

Table 46. CLIF_SS_TX1_FTRANS2 (0x8A) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS11	rw	0x00	TX1 falling transition value 11
[23:16]	TX1_SS_FTRANS10	rw	0x00	TX1 falling transition value 10
[15:8]	TX1_SS_FTRANS9	rw	0x00	TX1 falling transition value 9
[7:0]	TX1_SS_FTRANS8	rw	0x00	TX1 falling transition value 8

8.18.1.33 CLIF_SS_TX1_FTRANS3 (0x8B)

This register provides the settings for CLIF_SS_TX1_FTRANS3

Table 47. CLIF_SS_TX1_FTRANS3 (0x8B) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX1_SS_FTRANS15	rw	0x00	TX1 falling transition value 15
[23:16]	TX1_SS_FTRANS14	rw	0x00	TX1 falling transition value 14
[15:8]	TX1_SS_FTRANS13	rw	0x00	TX1 falling transition value 13
[7:0]	TX1_SS_FTRANS12	rw	0x00	TX1 falling transition value 12

8.18.1.34 CLIF_SS_TX2_FTRANS0 (0x8C)

This register provides the settings for CLIF_SS_TX2_FTRANS0

Table 48. CLIF_SS_TX2_FTRANS0 (0x8C) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS3	rw	0x00	TX2 falling transition value 3
[23:16]	TX2_SS_FTRANS2	rw	0x00	TX2 falling transition value 2
[15:8]	TX2_SS_FTRANS1	rw	0x00	TX2 falling transition value 1
[7:0]	TX2_SS_FTRANS0	rw	0x00	TX2 falling transition value 0

8.18.1.35 CLIF_SS_TX2_FTRANS1 (0x8D)

This register provides the settings for CLIF_SS_TX2_FTRANS1

Table 49. CLIF_SS_TX2_FTRANS1 (0x8D) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS7	rw	0x00	TX2 falling transition value 7
[23:16]	TX2_SS_FTRANS6	rw	0x00	TX2 falling transition value 6
[15:8]	TX2_SS_FTRANS5	rw	0x00	TX2 falling transition value 5
[7:0]	TX2_SS_FTRANS4	rw	0x00	TX2 falling transition value 4

8.18.1.36 CLIF_SS_TX2_FTRANS2 (0x8E)

This register provides the settings for CLIF_SS_TX2_FTRANS2

Table 50. CLIF_SS_TX2_FTRANS2 (0x8E) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS11	rw	0x00	TX2 falling transition value 11
[23:16]	TX2_SS_FTRANS10	rw	0x00	TX2 falling transition value 10
[15:8]	TX2_SS_FTRANS9	rw	0x00	TX2 falling transition value 9
[7:0]	TX2_SS_FTRANS8	rw	0x00	TX2 falling transition value 8

8.18.1.37 CLIF_SS_TX2_FTRANS3 (0x8F)

This register provides the settings for CLIF_SS_TX2_FTRANS3

Table 51. CLIF_SS_TX2_FTRANS3 (0x8F) register bit description

Bit	Symbol	Access	Value	Description
[31:24]	TX2_SS_FTRANS15	rw	0x00	TX2 falling transition value 15
[23:16]	TX2_SS_FTRANS14	rw	0x00	TX2 falling transition value 14
[15:8]	TX2_SS_FTRANS13	rw	0x00	TX2 falling transition value 13
[7:0]	TX2_SS_FTRANS12	rw	0x00	TX2 falling transition value 12

8.18.2 EEPROM configuration description

The settings done in EEPROM are used for basic configuration which does not change frequently. Typically it is performed once during trimming or configuration of a product. The EEPROM has a limited number of erase/write cycles that can be performed. This means, that configurations that change frequently must be performed in standard registers which do not keep their value during reset and power off.

This section describes the EEPROM configuration of the PN7220.

Writing to the EEPROM has to be performed with Read-Modify-Write for all memory addresses which contain RFU bits.

8.18.2.1 EEPROM configuration for power, TXLDO, XTAL and Clocks

This section provides the configuration of different EEPROM parameters for the system.

8.18.2.1.1 List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks

Table 52. List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
DCDC_PWR_CONFIG (0x0000)	PN76_USER_PMU->PwrConfig	0x0000	0	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
DCDC_CONFIG (0x0001)	PN76_USER_PMU->Dcdc Config	0x0001	1	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

Table 52. List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks...continued

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
TXLDO_CONFIG (0x0002)	PN76_USER_PMU->TxLdo Config	0x0002	2	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
TXLDO_VDDPA_CONFIG (0x0006)	PN76_USER_PMU->TxLdoStart Vddpa	0x0006	6	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TXLDO_VDDPA_MAX_RDR (0x0007)	PN76_USER_PMU->TxLdo VddpaMaxRdr	0x0007	7	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TXLDO_VDDPA_MAX_CARD (0x0008)	PN76_USER_PMU->TxLdo VddpaMaxCard	0x0008	8	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
BOOST_DEFAULT_VOLTAGE (0x0009)	PN76_USER_PMU->Boost DefaultVoltage	0x0009	9	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
XTAL_CONFIG (0x000F)	PN76_CLKGEN->bXtalConfig	0x000F	15	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
XTAL_TIMEOUT (0x0010)	PN76_CLKGEN->bXtalTimeOut	0x0010	16	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
CLK_INPUT_FREQ (0x0011)	PN76_RF_CLOCK_CFG->b PLLClkInputFrq	0x0011	17	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
XTAL_CHECK_DELAY (0x0012)	PN76_RF_CLOCK_CFG->bXtal CheckDelay	0x0012	18	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.1.2 DCDC_PWR_CONFIG (0x0000)

Configuration for power.

Table 53. DCDC_PWR_CONFIG (0x0000)

Function	bit	Values	Description
DC-DC usage in card mode	[7]	0x00	DC-DC is not powered and set to bypass
		0x01	DC-DC is powered and not bypassed
DC-DC usage in reader mode	[6]	0x00	DC-DC is not powered and set to bypass
		0x01	DC-DC is powered and not bypassed
RFU	[5]		Do not touch. Default value is 0x01
VUP input voltage	[4:0]	0x00	Not connected or 0 V
		0x01	No DC-DC and internal VDDPA_LDO: VUP supplied by VBAT / VBATPWR (pin VUP_TX connected to VBAT/VBATPWR)
		0x02	Internal DC-DC: with auto by pass and variable boost w.r.t VDDPA (internal DPC controls VDDBOOST): DC-DC goes into pass through mode when the VDDPA goes below 3.3 V. When VDDPA is greater than 3.3 V, the DC-DC is configured to boost voltage in range of 3.3 V to 6 V. Internal DC-DC: with fixed VDDBOOST
		0x05 - 0x09	RFU
		0x10	No DC-DC and internal VDDPA_LDO: VUP supplied by external LDO (not connected to VBAT)

8.18.2.1.3 DCDC_CONFIG (0x0001)

DCDC Configuration

Table 54. DCDC_CONFIG (0x0001)

Function	bit	Values	Description
RFU	[7:5]		Reserved
DC-DC pass through feature	[4]	0x00	DC-DC pass through feature is not supported ($V_{out} = 0\text{ V}$ or 5 V)
		0x01	DC-DC pass through feature is supported ($V_{out} = 0\text{ V}$ or 5 V)
DC-DC for LPCD (Not ULPCD)	[3]	0x00	Use of DC-DC for LPCD disabled (Not ULPCD)
		0x01	Use of DC-DC for LPCD enabled (Not ULPCD)
RFU	[2:0]		Reserved

8.18.2.1.4 TXLDO_CONFIG (0x0002)

Table 55. TXLDO_CONFIG (0x0002)

Function	bit	Values	Description
RFU	[31:2]		Reserved
Overcurrent protection	[1]	0x00	Overcurrent protection feature disabled
		0x01	Overcurrent protection feature enabled
Enable Tx-LDO	[0]	0x00	TxLDO is disabled. No voltage output of the TxLDO
		0x01	TxLDO is enabled. Regulated voltage output of the TxLDO
RFU	[2:0]		Reserved

8.18.2.1.5 TXLDO_VDDPA_CONFIG (0x0006)

Table 56. TXLDO_VDDPA_CONFIG (0x0006)

Function	bit	Values	Description
VDDPA voltage level	[7:0]	0x00 - 0x2A	Value 0 indicates 1.5 V. Further VDDPA voltage would be $1.5\text{ V} + 0.1\text{ V} \times$ this parameter value. Maximum value of 0x2A indicates for 5.7 V

8.18.2.1.6 TXLDO_VDDPA_MAX_RDR (0x0007)

Table 57. TXLDO_VDDPA_MAX_RDR (0x0007)

Function	bit	Values	Description
VDDPA max voltage level	[7:0]	0x00 - 0x2A	Value 0 indicates 1.5 V. Further VDDPA voltage would be $1.5 + 0.1\text{ V} \times$ this parameter value. Maximum value of 0x2A indicates for 5.7 V

8.18.2.1.7 TXLDO_VDDPA_MAX_CARD (0x0008)

Table 58. TXLDO_VDDPA_MAX_CARD (0x0008)

Function	bit	Values	Description
VDDPA max voltage level	[7:0]	0x00 - 0x2A	Value 0 indicates 1.5 V. Further VDDPA voltage would be 1.5 + 0.1 V × this parameter value. Maximum value of 0x2A indicates for 5.7 V

8.18.2.1.8 BOOST_DEFAULT_VOLTAGE (0x0009)

Table 59. BOOST_DEFAULT_VOLTAGE (0x0009)

Function	bit	Values	Description
VDDBOOST output voltage	[7:0]	0x00 - 0x1D	Value 0 indicates 3.1 V. Further VDDBOOST voltage would be 3.1 V + 0.1 V × this parameter value. Maximum value of 0x1D indicates for 6 V
		Other values	RFU

8.18.2.1.9 XTAL_CONFIG (0x000F)

Configuration for the XTAL startup procedure

Table 60. XTAL_CONFIG (0x000F)

Function	bit	Values	Description
RFU	[7:1]		RFU
XTAL startup procedure	[0]	0x00	disable Crystal recalibration start after wake-up
		0x01	enable Crystal recalibration start after wake-up

8.18.2.1.10 XTAL_TIMEOUT (0x0010)

Timeout for XTAL to be ready

Table 61. XTAL_TIMEOUT (0x0010)

Function	bit	Values	Description
Configuration for XTAL startup procedure	[7:0]		Timeout for XTAL to be ready (in *128 μs). This configuration does not speed up the boot time.

8.18.2.1.11 CLK_INPUT_FREQ (0x0011)

Configuration for the PLL input clock frequency

Table 62. CLK_INPUT_FREQ (0x0011)

Function	bit	Values	Description
RFU	[7:4]		RFU
PLL clock configuration	[3:0]	0x00	8 MHz
		0x01	12 MHz
		0x02	16 MHz
		0x03	24 MHz

Table 62. CLK_INPUT_FREQ (0x0011)...continued

Function	bit	Values	Description
		0x04	32 MHz
		0x05	48 MHz
		0x06	RFU
		0x07	22.5 MHz HFO
		0x08	XTAL 27.12 MHz
		others	RFU

8.18.2.1.12 XTAL_CHECK_DELAY (0x0012)

Table 63. XTAL_CHECK_DELAY (0x0012)

Function	bit	Values	Description
RFRetry_numberU	[7:5]		Max Number of retries before a clock error is raised
Interval	[4:0]		Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 μs). This is the time to try to lock the PLL, a stable crystal clock is required for locking. If the PLL is not locked, a next retry to lock the PLL will be done after this interval. This value can be used to optimize the startup time dependent on the crystal characteristics. This is important, e.g., for optimization of the LPCD and ULPCD.

8.18.2.1.13 VDDPA_DISCHARGE (0x050D)

enable/disable fast VDDPA Discharge

Table 64. VDDPA_DISCHARGE (0x050D)

Function	bits	Values	Description
RFU	[7:1]		Reserved
EnableFast VDDPADischarge	[0]	0x00	Disables fast discharge of VDDPA by setting VDDPA = 5.7 V and then to 1.5 V, during RF OFF
		0x01	Enables fast discharge of VDDPA by setting VDDPA = 5.7 V and then to 1.5 V, during RF OFF (default)

8.18.2.2 RM_TX_SHAPING - TX wave shaping for passive reader mode

This section provides the TX shaping for different type of cards in passive reader mode.

8.18.2.2.1 TX wave shaping for TypeA passive reader mode for all baud-rates.

This section provides the TX shaping for TypeA passive reader mode.

8.18.2.2.1.1 RESIDUAL_AMPL_LEVEL_A106 (0x0014)

Residual amplitude level for A106

Table 65. RESIDUAL_AMPL_LEVEL_A106 (0x0014)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.1.2 EDGE_TYPE_A106 (0x0015)

Edge type for A106

Table 66. EDGE_TYPE_A106 (0x0015)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05		lookup table-based transition, automatic adaptation based on VDDPA including Correction	
	0x06		lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
	Others	RFU		

8.18.2.2.1.3 EDGE_STYLE_A106 (0x0016)

Time constant Edge style configuration for A106

Table 67. EDGE_STYLE_A106 (0x0016)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.1.4 EDGE_LENGTH_A106 (0x0017)

Edge length for A106

Table 68. EDGE_LENGTH_A106 (0x0017)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.1.5 RESIDUAL_AMPL_LEVEL_A212 (0x0018)

Table 69. RESIDUAL_AMPL_LEVEL_A212 (0x0018)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.1.6 EDGE_TYPE_A212 (0x0019)

Table 70. EDGE_TYPE_A212 (0x0019)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05		lookup table-based transition, automatic adaptation based on VDDPA including Correction	
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.2.1.7 EDGE_STYLE_A212 (0x001A)

Table 71. EDGE_STYLE_A212 (0x001A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]		Defines edge style configuration

Table 71. EDGE_STYLE_A212 (0x001A)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_A212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.1.8 EDGE_LENGTH_A212 (0x001B)

Table 72. EDGE_LENGTH_A212 (0x001B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.1.9 RESIDUAL_AMPL_LEVEL_A424 (0x001C)

Table 73. RESIDUAL_AMPL_LEVEL_A424 (0x001C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.1.10 EDGE_TYPE_A424 (0x001D)

Table 74. EDGE_TYPE_A424 (0x001D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels

Table 74. EDGE_TYPE_A424 (0x001D)...continued

Function	bit	Values	Description	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
	Others	RFU		
	Lookup table based shaping			
	0x04	lookup table-based transition, no automatic adaptation based on VDDPA		
	0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction		
	0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction		
	Others	RFU		

8.18.2.2.1.11 EDGE_STYLE_A424 (0x001E)

Table 75. EDGE_STYLE_A424 (0x001E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]		Defines edge style configuration

Table 75. EDGE_STYLE_A424 (0x001E)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_A424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.1.12 EDGE_LENGTH_A424 (0x001F)

Table 76. EDGE_LENGTH_A424 (0x001F)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.1.13 RESIDUAL_AMPL_LEVEL_A848 (0x0020)

Table 77. RESIDUAL_AMPL_LEVEL_A848 (0x0020)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.1.14 EDGE_TYPE_A848 (0x0021)

Table 78. EDGE_TYPE_A848 (0x0021)

Function	bit	Values	Description
Edge transition style	[7:4]		Defines style of edge transition of falling edge, Defines style of edge transition:
			Firmware based shaping
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
			Lookup table based shaping
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction		

Table 78. EDGE_TYPE_A848 (0x0021)...continued

Function	bit	Values	Description	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
	Others	RFU		

8.18.2.2.1.15 EDGE_STYLE_A848 (0x0022)

Table 79. EDGE_STYLE_A848 (0x0022)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A848 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A848 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_A848 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A848 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.1.16 EDGE_LENGTH_A848 (0x0023)

Table 80. EDGE_LENGTH_A848 (0x0023)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.2 TX wave shaping for Type B passive reader mode for all baud-rates.

This section provides the TX shaping for Type B passive reader mode.

8.18.2.2.2.1 RESIDUAL_AMPL_LEVEL_B106 (0x0024)

Table 81. RESIDUAL_AMPL_LEVEL_B106 (0x0024)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.2.2 EDGE_TYPE_B106 (0x0025)

Table 82. EDGE_TYPE_B106 (0x0025)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:

Table 82. EDGE_TYPE_B106 (0x0025)...continued

Function	bit	Values	Description
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

8.18.2.2.2.3 EDGE_STYLE_B106 (0x0026)

Table 83. EDGE_STYLE_B106 (0x0026)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.2.4 EDGE_LENGTH_B106 (0x0027)

Table 84. EDGE_LENGTH_B106 (0x0027)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)

Table 84. EDGE_LENGTH_B106 (0x0027)...continued

Function	bit	Values	Description
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.2.5 RESIDUAL_AMPL_LEVEL_B212 (0x0028)

Table 85. RESIDUAL_AMPL_LEVEL_B212 (0x0028)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.2.6 EDGE_TYPE_B212 (0x0029)

Table 86. EDGE_TYPE_B212 (0x0029)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
			0x02	two linear transitions between amplitude levels
	0x03		three linear transitions between amplitude levels	
Others	RFU			
Lookup table based shaping				
0x04	lookup table-based transition, no automatic adaptation based on VDDPA			

Table 86. EDGE_TYPE_B212 (0x0029)...continued

Function	bit	Values	Description
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

8.18.2.2.2.7 EDGE_STYLE_B212 (0x002A)

Table 87. EDGE_STYLE_B212 (0x002A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_B212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.2.8 EDGE_LENGTH_B212 (0x002B)

Table 88. EDGE_LENGTH_B212 (0x002B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.2.9 RESIDUAL_AMPL_LEVEL_B424 (0x002C)

Table 89. RESIDUAL_AMPL_LEVEL_B424 (0x002C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.2.10 EDGE_TYPE_B424 (0x002D)

Table 90. EDGE_TYPE_B424 (0x002D)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction		
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.2.2.11 EDGE_STYLE_B424 (0x002E)

Table 91. EDGE_STYLE_B424 (0x002E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_B424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_B424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.2.12 EDGE_LENGTH_B424 (0x002F)

Table 92. EDGE_LENGTH_B424 (0x002F)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.2.13 RESIDUAL_AMPL_LEVEL_B848 (0x0030)

Table 93. RESIDUAL_AMPL_LEVEL_B848 (0x0030)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.2.14 EDGE_TYPE_B848 (0x0031)

Table 94. EDGE_TYPE_B848 (0x0031)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05		lookup table-based transition, automatic adaptation based on VDDPA including Correction	
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.2.2.15 EDGE_STYLE_B848 (0x0032)

Table 95. EDGE_STYLE_B848 (0x0032)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	

Table 95. EDGE_STYLE_B848 (0x0032)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_B848 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B848 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_B848 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B848 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.2.16 EDGE_LENGTH_B848 (0x0033)

Table 96. EDGE_LENGTH_B848 (0x0033)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.3 TX wave shaping for Type F passive reader mode for all baud-rates.

This section provides the TX shaping for Type F passive reader mode.

8.18.2.2.3.1 RESIDUAL_AMPL_LEVEL_F212 (0x0034)

Table 97. RESIDUAL_AMPL_LEVEL_F212 (0x0034)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.3.2 EDGE_TYPE_F212 (0x0035)

Table 98. EDGE_TYPE_F212 (0x0035)

Function	bit	Values	Description
Edge transition style	[7:4]		Defines style of edge transition of falling edge, Defines style of edge transition:

Table 98. EDGE_TYPE_F212 (0x0035)...continued

Function	bit	Values	Description	
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:		
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
			0x02	two linear transitions between amplitude levels
			0x03	three linear transitions between amplitude levels
Others			RFU	
Lookup table based shaping				
0x04			lookup table-based transition, no automatic adaptation based on VDDPA	
0x05			lookup table-based transition, automatic adaptation based on VDDPA including Correction	
0x06			lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
Others	RFU			

8.18.2.2.3.3 EDGE_STYLE_F212 (0x0036)

Table 99. EDGE_STYLE_F212 (0x0036)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)

Table 99. EDGE_STYLE_F212 (0x0036)...continued

Function	bit	Values	Description
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.3.4 EDGE_LENGTH_F212 (0x0037)

Table 100. EDGE_LENGTH_F212 (0x0037)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.3.5 RESIDUAL_AMPL_LEVEL_F424 (0x0038)

Table 101. RESIDUAL_AMPL_LEVEL_F424 (0x0038)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.3.6 EDGE_TYPE_F424 (0x0039)

Table 102. EDGE_TYPE_F424 (0x0039)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA

Table 102. EDGE_TYPE_F424 (0x0039)...continued

Function	bit	Values	Description	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	

8.18.2.2.3.7 EDGE_STYLE_F424 (0x003A)

Table 103. EDGE_STYLE_F424 (0x003A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.3.8 EDGE_LENGTH_F424 (0x003B)

Table 104. EDGE_LENGTH_F424 (0x003B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4 TX wave shaping for Type V (ISO15693) passive reader mode for all baud-rates.

This section provides the TX shaping for Type V (ISO15693) passive reader mode.

8.18.2.2.4.1 RESIDUAL_AMPL_LEVEL_V10_26 (0x004C)

Table 105. RESIDUAL_AMPL_LEVEL_V10_26 (0x004C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.2 EDGE_TYPE_V10_26 (0x004D)

Table 106. EDGE_TYPE_V10_26 (0x004D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:

Table 106. EDGE_TYPE_V10_26 (0x004D)...continued

Function	bit	Values	Description
			Firmware based shaping
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
			Lookup table based shaping
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

8.18.2.2.4.3 EDGE_STYLE_V10_26 (0x004E)

Table 107. EDGE_STYLE_V10_26 (0x004E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_V10_26 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_26 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_V10_26 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_26 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.4 EDGE_LENGTH_V10_26 (0x004F)

Table 108. EDGE_LENGTH_V10_26 (0x004F)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)

Table 108. EDGE_LENGTH_V10_26 (0x004F)...continued

Function	bit	Values	Description
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4.5 RESIDUAL_AMPL_LEVEL_V10_53 (0x0050)

Table 109. RESIDUAL_AMPL_LEVEL_V10_53 (0x0050)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.6 EDGE_TYPE_V10_53 (0x0051)

Table 110. EDGE_TYPE_V10_53 (0x0051)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:
	Firmware based shaping		
	0x01		linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels
	0x03		three linear transitions between amplitude levels
Others	RFU		
Lookup table based shaping			
0x04	lookup table-based transition, no automatic adaptation based on VDDPA		

Table 110. EDGE_TYPE_V10_53 (0x0051)...continued

Function	bit	Values	Description
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

8.18.2.2.4.7 EDGE_STYLE_V10_53 (0x0052)

Table 111. EDGE_STYLE_V10_53 (0x0052)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_53 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_53 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_53 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_53 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.8 EDGE_LENGTH_V10_53 (0x0053)

Table 112. EDGE_LENGTH_V10_53 (0x0053)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4.9 RESIDUAL_AMPL_LEVEL_V10_106 (0x0054)

Table 113. RESIDUAL_AMPL_LEVEL_V10_106 (0x0054)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.10 EDGE_TYPE_V10_106 (0x0055)

Table 114. EDGE_TYPE_V10_106 (0x0055)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04	lookup table-based transition, no automatic adaptation based on VDDPA		
	0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction		
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.2.4.11 EDGE_STYLE_V10_106 (0x0056)

Table 115. EDGE_STYLE_V10_106 (0x0056)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.12 EDGE_LENGTH_V10_106 (0x0057)

Table 116. EDGE_LENGTH_V10_106 (0x0057)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4.13 RESIDUAL_AMPL_LEVEL_V10_212 (0x0058)

Table 117. RESIDUAL_AMPL_LEVEL_V10_212 (0x0058)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.14 EDGE_TYPE_V10_212 (0x0059)

Table 118. EDGE_TYPE_V10_212 (0x0059)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05		lookup table-based transition, automatic adaptation based on VDDPA including Correction	
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.2.4.15 EDGE_STYLE_V10_212 (0x005A)

Table 119. EDGE_STYLE_V10_212 (0x005A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	

Table 119. EDGE_STYLE_V10_212 (0x005A)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_V10_212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V10_212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V10_212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.16 EDGE_LENGTH_V10_212 (0x005B)

Table 120. EDGE_LENGTH_V10_212 (0x005B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4.17 RESIDUAL_AMPL_LEVEL_V100_26 (0x003C)

Table 121. RESIDUAL_AMPL_LEVEL_V100_26 (0x003C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.18 EDGE_TYPE_V100_26 (0x003D)

Table 122. EDGE_TYPE_V100_26 (0x003D)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels

Table 122. EDGE_TYPE_V100_26 (0x003D)...continued

Function	bit	Values	Description
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
	Firmware based shaping		
	0x01	linear transition between two amplitude levels	
	0x02	two linear transitions between amplitude levels	
	0x03	three linear transitions between amplitude levels	
	Others	RFU	
	Lookup table based shaping		
	0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
	0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
Others	RFU		

8.18.2.2.4.19 EDGE_STYLE_V100_26 (0x003E)

Table 123. EDGE_STYLE_V100_26 (0x003E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_26 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_26 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]	Defines edge style configuration	

Table 123. EDGE_STYLE_V100_26 (0x003E)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_V100_26 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_26 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.20 EDGE_LENGTH_V100_26 (0x003F)

Table 124. EDGE_LENGTH_V100_26 (0x003F)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4.21 RESIDUAL_AMPL_LEVEL_V100_53 (0x0040)

Table 125. RESIDUAL_AMPL_LEVEL_V100_53 (0x0040)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.22 EDGE_TYPE_V100_53 (0x0041)

Table 126. EDGE_TYPE_V100_53 (0x0041)

Function	bit	Values	Description
Edge transition style	[7:4]		Defines style of edge transition of falling edge, Defines style of edge transition:
			Firmware based shaping
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
			Lookup table based shaping
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction		

Table 126. EDGE_TYPE_V100_53 (0x0041)...continued

Function	bit	Values	Description	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	

8.18.2.2.4.23 EDGE_STYLE_V100_53 (0x0042)

Table 127. EDGE_STYLE_V100_53 (0x0042)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_53 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_53 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_53 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_53 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.24 EDGE_LENGTH_V100_53 (0x0043)

Table 128. EDGE_LENGTH_V100_53 (0x0043)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4.25 RESIDUAL_AMPL_LEVEL_V100_106 (0x0044)

Table 129. RESIDUAL_AMPL_LEVEL_V100_106 (0x0044)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.26 EDGE_TYPE_V100_106 (0x0045)

Table 130. EDGE_TYPE_V100_106 (0x0045)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
			[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:
	Firmware based shaping			
0x01	linear transition between two amplitude levels			
0x02	two linear transitions between amplitude levels			

Table 130. EDGE_TYPE_V100_106 (0x0045)...continued

Function	bit	Values	Description
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

8.18.2.2.4.27 EDGE_STYLE_V100_106 (0x0046)

Table 131. EDGE_STYLE_V100_106 (0x0046)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.28 EDGE_LENGTH_V100_106 (0x0047)

Table 132. EDGE_LENGTH_V100_106 (0x0047)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]	RFU	

Table 132. EDGE_LENGTH_V100_106 (0x0047)...continued

Function	bit	Values	Description
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.4.29 RESIDUAL_AMPL_LEVEL_V100_212 (0x0048)

Table 133. RESIDUAL_AMPL_LEVEL_V100_212 (0x0048)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.4.30 EDGE_TYPE_V100_212 (0x0049)

Table 134. EDGE_TYPE_V100_212 (0x0049)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04	lookup table-based transition, no automatic adaptation based on VDDPA		
	0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction		

Table 134. EDGE_TYPE_V100_212 (0x0049)...continued

Function	bit	Values	Description
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
		Others	RFU

8.18.2.2.4.31 EDGE_STYLE_V100_212 (0x004A)

Table 135. EDGE_STYLE_V100_212 (0x004A)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_V100_212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_V100_212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.4.32 EDGE_LENGTH_V100_212 (0x004B)

Table 136. EDGE_LENGTH_V100_212 (0x004B)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.5 TX wave shaping for ISO18000 p3m3 passive reader mode for all baud-rates.

This section provides the TX shaping for ISO18000 p3m3 passive reader mode.

8.18.2.2.5.1 RESIDUAL_AMPL_LEVEL_180003M3_TARI9P44 (0x0060)

Table 137. RESIDUAL_AMPL_LEVEL_180003M3_TARI9P44 (0x0060)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.5.2 EDGE_TYPE_180003M3_TARI9P44 (0x0061)

Table 138. EDGE_TYPE_180003M3_TARI9P44 (0x0061)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
	Others	RFU	
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
0x06		lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
Others	RFU		

8.18.2.2.5.3 EDGE_STYLE_180003M3_TARI9P44 (0x0062)

Table 139. EDGE_STYLE_180003M3_TARI9P44 (0x0062)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_180003M3_TARI9P44 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_180003M3_TARI9P44 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_180003M3_TARI9P44 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_180003M3_TARI9P44 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.5.4 EDGE_LENGTH_180003M3_TARI9P44 (0x0063)

Table 140. EDGE_LENGTH_180003M3_TARI9P44 (0x0063)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.5.5 RESIDUAL_AMPL_LEVEL_180003M3_TARI18P88 (0x005C)

Table 141. RESIDUAL_AMPL_LEVEL_180003M3_TARI18P88 (0x005C)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.5.6 EDGE_TYPE_180003M3_TARI18P88 (0x005D)

Table 142. EDGE_TYPE_180003M3_TARI18P88 (0x005D)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
	0x01		linear transition between two amplitude levels	
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction			
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.2.5.7 EDGE_STYLE_180003M3_TARI18P88 (0x005E)

Table 143. EDGE_STYLE_180003M3_TARI18P88 (0x005E)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_180003M3_TARI18P8 is 1, 2, or 3: time constant

Table 143. EDGE_STYLE_180003M3_TARI18P88 (0x005E)...continued

Function	bit	Values	Description
			configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_180003M3_TARI18P8 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_180003M3_TARI18P8 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_180003M3_TARI18P8 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.5.8 EDGE_LENGTH_180003M3_TARI18P88 (0x005F)

Table 144. EDGE_LENGTH_180003M3_TARI18P88 (0x005F)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.2.6 TX wave shaping for B-Prime passive reader mode for all baud-rates.

This section provides the TX shaping for B-Prime passive reader mode.

8.18.2.2.6.1 RESIDUAL_AMPL_LEVEL_B_PRIME106 (0x0064)

Table 145. RESIDUAL_AMPL_LEVEL_B_PRIME106 (0x0064)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.2.6.2 EDGE_TYPE_B_PRIME106 (0x0065)

Table 146. EDGE_TYPE_B_PRIME106 (0x0065)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05		lookup table-based transition, automatic adaptation based on VDDPA including Correction	
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.2.6.3 EDGE_STYLE_B_PRIME106 (0x0066)

Table 147. EDGE_STYLE_B_PRIME106 (0x0066)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]		Defines edge style configuration

Table 147. EDGE_STYLE_B_PRIME106 (0x0066)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_B_PRIME106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B_PRIME106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_B_PRIME106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_B_PRIME106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.2.6.4 EDGE_LENGTH_B_PRIME106 (0x0067)

Table 148. EDGE_LENGTH_B_PRIME106 (0x0067)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.3 DPC Settings

This section provides the settings related to DPC configuration

8.18.2.3.1 DPC_CONFIG (0x0068)

DPC configuration

Table 149. DPC_CONFIG (0x0068)

Function	bit	Values	Description
RFU	[7:3]		RFU
DPC in Active target mode	[2]		DPC configuration in active target mode
		0x00	disabled
		0x01	enabled
DPC in Active initiator mode	[1]		DPC configuration in active initiator mode
		0x00	disabled

Table 149. DPC_CONFIG (0x0068)...continued

Function	bit	Values	Description
		0x01	enabled
DPC in Reader/Passive Initiator mode	[0]		DPC configuration in Reader/ Passive Initiator mode
		0x00	disabled
		0x01	enabled

8.18.2.3.2 DPC_TARGET_CURRENT (0x0069)

DPC configuration unloaded VDDPA target current in mA

Table 150. DPC_TARGET_CURRENT (0x0069)

Function	bit	Values	Description
DPC in Active target mode	[15:0]		VDDPA target current in mA. The target current +/- hysteresis defines the limiting maximum current for the DPC.

Note: This configuration shall not exceed 350 mA - hysteresis.

Note: The resulting current that is driven by the transmitter can be further reduced based on the current reduction lookup table entries.

8.18.2.3.3 DPC_HYSTERESIS_LOADING (0x006B)

The hysteresis (**bHysteresis** and **bHysteresis_Unloading**) together with the target current (**wTargetCurrent**) defines the current limit, at which the DPC automatically decreases or raises the VDDPA. The VDDPA is automatically reduced, as soon as the current exceeds the **wTargetCurrent + bHysteresis**, and the VDDPA is automatically increased again, as soon as the current is below **wTargetCurrent # bHysteresis_Unloading**.

Table 151. DPC_HYSTERESIS_LOADING (0x006B)

Function	bit	Values	Description
DPC hysteresis loading	[7:0]		Absolute difference to current Target Current in mA that triggers a DPC update event during loading.

Note: If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.

Note: In most application, the default values work well and do not need to be modified.

8.18.2.3.4 DPC_ALGO_INTERVAL (0x006C)

Table 152. DPC_ALGO_INTERVAL (0x006C)

Function	bit	Values	Description
algotinterval	[15:0]	1 ms	DPC algorithm time interval between two consecutive current checks, unit = 128 MHz/13,56 MHz (~9.44 μs) Default = 1 ms

8.18.2.3.5 DPC_HYSTERESIS_UNLOADING (0x006E)

Table 153. DPC_HYSTERESIS_UNLOADING (0x006E)

Function	bit	Values	Description
DPC hysteresis unloading	[7:0]		Absolute difference to current Target Current in mA that triggers a DPC update event during unloading.

8.18.2.3.6 DPC_TXLDOVDDPALow (0x006F)

Table 154. DPC_TXLDOVDDPALow (0x006F)

Function	bit	Values	Description
TXLDOVDDPALow	[7:0]		VDDPA Low Limit for RDON

8.18.2.3.7 DPC_TXGSN (0x0070)

TXGSN configuration.

Table 155. DPC_TXGSN (0x0070)

Function	bit	Values	Description
DPC hysteresis loading	[7:0]	Less than 20	resistance = $10 \Omega / (tx1_gsn + 1)$
		more than or equal 20	20: resistance = 0.5Ω

8.18.2.3.8 DPC_RDON_CONTROL (0x0071)

Table 156. DPC_RDON_CONTROL (0x0071)

Function	bit	Values	Description
VDDPA low limit control	[7:0]	0x00	Disabled
		0x01	RdON Control
		0x02	PWM control
		Others	RFU

8.18.2.3.9 DPC_InitialRDOn_RFOn (0x0072)

Table 157. DPC_InitialRDOn_RFOn (0x0072)

Function	bit	Values	Description
DPC_InitialRDOn_RFOn	[7:0]		Initial GSP TX1/TX2 value during FieldON

8.18.2.3.10 DPC_TXLDO_MAX_DROPOUT (0x0073)

Table 158. DPC_TXLDO_MAX_DROPOUT (0x0073)

Function	bit	Values	Description
DPC_TXLDO_MAX_DROPOUT	[15:0]		At DPC start (on initial RF ON), if TXLDO drop out is higher to this value then VDDPA is reduced to: e VddpaSafe if no boost bypass on going else Vddpa is stopped. Unit is mV. Default = E10h = 3600 mV.

8.18.2.3.11 DPC_GUARD_TIME (0x0079)

Table 159. DPC_GUARD_TIME (0x0079)

Function	bit	Values	Description
algointerval	[7:0]		DPC guard time configuration. Guard time before tx. 1 unit = 1 μ s.

The DPC regulation is done once before TX and once after RX.

The guard time parameter is the time between DPC regulation completion and TX start.

The guard time parameter is the time between RX stop and DPC regulation start.

The guard time is always enabled for TX

Note: Recommendation is not to modify the default value.

8.18.2.3.12 DPC_ENABLE_DURING_FDT (0x007A)

DPC regulation enable during FDT.

Table 160. DPC_ENABLE_DURING_FDT (0x007A)

Function	bit	Values	Description
Disable DPC during FDT	[7:0]	0x00	DPC disabled during FDT (debug purpose only)
		0x01	DPC enabled during FDT (recommendation)
		others	RFU

8.18.2.3.13 DPC_GUARD_TIME_AFTER_RX (0x007B)

Enable DPC with guard time after RX

Table 161. DPC_GUARD_TIME_AFTER_RX (0x007B)

Function	bit	Values	Description
Enable DPC guard time after RX	[7:0]	0x00	DPC disabled after RX (debug purpose only)
		0x01	DPC enabled after RX (recommendation)
		others	RFU

8.18.2.3.14 DPC Lookup table entries

Table 162. DPC lookup table entries

Entry	Address	Function	bit	Values	Description
ENTRY 0 for 1V5	0x7D	This below details are for entry 0. Similar is for all other entries.			
		Target current reduction	[31:24]	-	Byte 0. Target current reduction in mA (unsigned)
		AWC amp mod change	[23:16]	-	Byte 1. Relative change of modulated amplitude level (signed)
		AWC edge time constant for ASK100	[15:8]	-	Byte 2. Target current reduction in mA (unsigned)
[15:12]	-		ASK100, Relative change of rising edge time constant (signed)		

Table 162. DPC lookup table entries...continued

Entry	Address	Function	bit	Values	Description
			[11:8]	-	ASK100, Relative change of falling edge time constant (signed)
		AWC edge time constant for ASK100	[7:0]	-	Byte 2. Target current reduction in mA (unsigned)
			[7:4]	-	ASK10, Relative change of rising edge time constant (signed)
			[3:0]	-	ASK10, Relative change of falling edge time constant (signed)
ENTRY_01 for 1.60V	0x0081	Byte and bit-fields description, refer to Table 162			
ENTRY_02 for 1.70V	0x0085	Byte and bit-fields description, refer to Table 162			
ENTRY_03 for 1.80V	0x0089	Byte and bit-fields description, refer to Table 162			
ENTRY_04 for 1.90V	0x008D	Byte and bit-fields description, refer to Table 162			
ENTRY_05 for 2.00V	0x0091	Byte and bit-fields description, refer to Table 162			
ENTRY_06 for 2.10V	0x0095	Byte and bit-fields description, refer to Table 162			
ENTRY_07 for 2.20V	0x0099	Byte and bit-fields description, refer to Table 162			
ENTRY_08 for 2.30V	0x009D	Byte and bit-fields description, refer to Table 162			
ENTRY_09 for 2.40V	0x00A1	Byte and bit-fields description, refer to Table 162			
ENTRY_10 for 2.50V	0x00A5	Byte and bit-fields description, refer to Table 162			
ENTRY_11 for 2.60V	0x00A9	Byte and bit-fields description, refer to Table 162			
ENTRY_12 for 2.70V	0x00AD	Byte and bit-fields description, refer to Table 162			
ENTRY_13 for 2.80V	0x00B1	Byte and bit-fields description, refer to Table 162			
ENTRY_14 for 2.90V	0x00B5	Byte and bit-fields description, refer to Table 162			
ENTRY_15 for 3.00V	0x00B9	Byte and bit-fields description, refer to Table 162			
ENTRY_16 for 3.10V	0x00BD	Byte and bit-fields description, refer to Table 162			
ENTRY_17 for 3.20V	0x00C1	Byte and bit-fields description, refer to Table 162			
ENTRY_18 for 3.30V	0x00C5	Byte and bit-fields description, refer to Table 162			
ENTRY_19 for 3.40V	0x00C9	Byte and bit-fields description, refer to Table 162			
ENTRY_20 for 3.50V	0x00CD	Byte and bit-fields description, refer to Table 162			
ENTRY_21 for 3.60V	0x00D1	Byte and bit-fields description, refer to Table 162			
ENTRY_22 for 3.70V	0x00D5	Byte and bit-fields description, refer to Table 162			
ENTRY_23 for 3.80V	0x00D9	Byte and bit-fields description, refer to Table 162			
ENTRY_24 for 3.90V	0x00DD	Byte and bit-fields description, refer to Table 162			
ENTRY_25 for 4.00V	0x00E1	Byte and bit-fields description, refer to Table 162			
ENTRY_26 for 4.10V	0x00E5	Byte and bit-fields description, refer to Table 162			
ENTRY_27 for 4.20V	0x00E9	Byte and bit-fields description, refer to Table 162			
ENTRY_28 for 4.30V	0x00ED	Byte and bit-fields description, refer to Table 162			
ENTRY_29 for 4.40V	0x00F1	Byte and bit-fields description, refer to Table 162			
ENTRY_30 for 4.50V	0x00F5	Byte and bit-fields description, refer to Table 162			

Table 162. DPC lookup table entries...continued

Entry	Address	Function	bit	Values	Description
ENTRY_31 for 4.60V	0x00F9	Byte and bit-fields description, refer to Table 162			
ENTRY_32 for 4.70V	0x00FD	Byte and bit-fields description, refer to Table 162			
ENTRY_33 for 4.80V	0x0101	Byte and bit-fields description, refer to Table 162			
ENTRY_34 for 4.90V	0x0105	Byte and bit-fields description, refer to Table 162			
ENTRY_35 for 5.00V	0x0109	Byte and bit-fields description, refer to Table 162			
ENTRY_36 for 5.10V	0x010D	Byte and bit-fields description, refer to Table 162			
ENTRY_37 for 5.20V	0x0111	Byte and bit-fields description, refer to Table 162			
ENTRY_38 for 5.30V	0x0115	Byte and bit-fields description, refer to Table 162			
ENTRY_39 for 5.40V	0x0119	Byte and bit-fields description, refer to Table 162			
ENTRY_40 for 5.50V	0x011D	Byte and bit-fields description, refer to Table 162			
ENTRY_41 for 5.60V	0x0121	Byte and bit-fields description, refer to Table 162			
ENTRY_42 for 5.70V	0x0125	Byte and bit-fields description, refer to Table 162			

8.18.2.4 ARC Settings for passive reader modes

This section provides the ARC settings for Reader Mode TX wave shaping configuration

8.18.2.4.1 ARC_SETTINGS_BARCCONFIG (0x0129)

ARC settings configuration.

Table 163. ARC_SETTINGS_BARCCONFIG (0x0129)

Function	bit	Values	Description	
ARC settings configuration	[7]	0x00	ARC algorithm is disabled.	
		0x01	ARC algorithm is enabled.	
	[6:3]		RFU	
	[2:0]			Number of entries in ARC table
		0x00		one entry
		0x01		two entries
		0x02		three entries
		0x03		four entries
		0x04		five entries
		others		RFU

8.18.2.4.2 ARC_SETTINGS_WARCVDDPA (0x012B)

VDDPA settings.

Table 164. ARC_SETTINGS_WARCVDDPA (0x012B)

Function	byte	Values	Description
VDDPA settings	[4]	See below note	VDDPA_range_index 4: if VDDPA voltage between VDDPA_3 to ARC_VDDPA_4
	[3]		VDDPA_range_index 3: if VDDPA voltage between VDDPA_2 to ARC_VDDPA_3 - 0.1
	[2]		VDDPA_range_index 2: if VDDPA voltage between VDDPA_1 to ARC_VDDPA_2 - 0.1
	[1]		VDDPA_range_index 1: if VDDPA voltage between VDDPA_0 to (ARC_VDDPA_1 - 0.1)
	[0]		VDDPA_range_index 0: if VDDPA voltage between 1.5 to (VDDPA_0 - 0.1)

Note: For above settings, value of 0x00 indicates for 1V50, 0x01 indicates for 1V60. Further increase with 100 mV and value of 0x2A corresponds to 5V70.

8.18.2.4.3 ARC_SETTINGS_WRMARCA_106 (0x0130)

ARC table settings for reader mode Type A 106kbps

Table 165. ARC_SETTINGS_WRMARCA_106 (0x0130)

Function	byte	bits	Values	Description
RM_RX_ARC_0	[9:8]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		ARC enable/disable
			0x00	ARC disabled for this technology and baudrate
			0x01	ARC enabled for this technology and baudrate
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_1	[7:6]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.

Table 165. ARC_SETTINGS_WRMARCA_106 (0x0130)...continued

Function	byte	bits	Values	Description
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		RFU
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_2	[5:4]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		RFU
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_3	[3:2]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.
		[14]		RFU
		[13:10]		RFU
		[9]		Enable the IIR filter
		[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)

Table 165. ARC_SETTINGS_WRMARCA_106 (0x0130)...continued

Function	byte	bits	Values	Description	
		[6:0]		DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)	
RM_RX_ARC_4	[1:0]	[15]		ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'.	
			0x00	ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used.	
			0x01	ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used.	
			[14]		RFU
			[13:10]		RFU
			[9]		Enable the IIR filter
			[8:7]		MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)
		[6:0]		DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)	

8.18.2.4.4 ARC_SETTINGS_TABLE for other technologies

Table 166. ARC_SETTINGS_TABLE for other technologies

Technology	Address	Function	Byte	Description
ARC_SETTINGS_A_212	0x13A-0x143	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_A_424	0x144-0x14D	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_A_848	0x14E-0x157	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_B_106	0x158-0x161	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3

Table 166. ARC_SETTINGS_TABLE for other technologies...continued

Technology	Address	Function	Byte	Description
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_B_212	0x162-0x16B	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_B_424	0x16C-0x175	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_B_848	0x176-0x17F	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_F_424	0x180-0x189	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_F_424	0x18A-0x193	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_V_6P6	0x19E-0x1A7	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_V_26	0x19E-0x1A7	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3

Table 166. ARC_SETTINGS_TABLE for other technologies...continued

Technology	Address	Function	Byte	Description
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_V_53	0x1A8-0x1B1	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_V_106	0x1B2-0x1BB	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_V_212	0x1BC-0x1C5	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_180003M3_SC424_4MAN	0x1C6-1CF	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_180003M3_SC424_2MAN	0x1D0-1D9	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_180003M3_SC848_4MAN	0x1DA-0x1E3	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_180003M3_SC848_2MAN	0x1E4-0x1ED	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3

Table 166. ARC_SETTINGS_TABLE for other technologies...continued

Technology	Address	Function	Byte	Description
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_AI_106	0x1EE-0x1F7	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_AI_212	0x1F8-0x201	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3
ARC_SETTINGS_AI_424	0x202-0x20B	RM_RX_ARC_0	[9:8]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_1	[7:6]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_2	[5:4]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_3	[3:2]	Refer to Section 8.18.2.4.3
		RM_RX_ARC_4	[1:0]	Refer to Section 8.18.2.4.3

8.18.2.4.5 ARC_RM_A106_FDT (0x051B)

Table 167. ARC_RM_A106_FDT (0x051B)

Function	Address	Bytesn	Bits	Value	Description
RM_RX_ARC_FDT_0	0x51B	[1:0]	Settings for RM_RX_ARC_FDT_0		
			[15]	0x00	ARC settings apply always
				0x01	ARC settings applicable during FDT
			[14]	0x00	ARC Disabled for this Tech and Baudrate
				0x01	ARC Enabled for this Tech and Baudrate
				NOTE	This bit is RFU for RM_RX_ARC_FDT_1, RM_RX_ARC_FDT_2, RM_RX_ARC_FDT_3, RM_RX_ARC_FDT_4.
			[13:10]	-	RFU. Reserved.
			[9]	-	Enable the IIR filter.
[8:7]	-	MF_GAIN (ths value will be applied to the SIGPR_RM_Tech register, applies as soon as the ARC is enabled)			

Table 167. ARC_RM_A106_FDT (0x051B)...continued

Function	Address	Bytesn	Bits	Value	Description
			[6:0]	-	DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_FDT_1	0x51D	[3:2]			Settings for RM_RX_ARC_FDT_1. Bit definitions is same as that of RM_RX_ARC_FDT_0
RM_RX_ARC_FDT_2	0x51F	[5:4]			Settings for RM_RX_ARC_FDT_2. Bit definitions is same as that of RM_RX_ARC_FDT_0
RM_RX_ARC_FDT_3	0x521	[7:6]			Settings for RM_RX_ARC_FDT_3. Bit definitions is same as that of RM_RX_ARC_FDT_0
RM_RX_ARC_FDT_4	0x523	[9:8]			Settings for RM_RX_ARC_FDT_4. Bit definitions is same as that of RM_RX_ARC_FDT_0

8.18.2.5 RSSI configuration parameters (applicable for card emulation)

8.18.2.5.1 EEPROM_APC_RSSI_LIST

List of RSSI settings for card emulation only

Table 168. List of RSSI settings for card emulation only

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
RSSI_TIMER (0x020C)	PN76_APC_RSSI->bRssiTimer	0x020C	524	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_TIMER_FIRST_PERIOD (0x020E)	PN76_APC_RSSI->bRssiTimerFirstPeriod	0x020E	526	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_CTRL_00_AB (0x0210)	PN76_APC_RSSI->bRssiCtrl_00_AB	0x0210	528	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_NB_ENTRIES_AB (0x0211)	PN76_APC_RSSI->bRssiNbEntriesAB	0x0211	529	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_THRESHOLD_AB entries table	PN76_APC_RSSI->wRssiThresholdAB_01	0x0212-0x271	530	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_CTRL_00_F (0x0272)	PN76_APC_RSSI->bRssiCtrl_00_F	0x0272	626	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_NB_ENTRIES_F (0x0273)	PN76_APC_RSSI->bRssiNbEntriesF	0x0273	627	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
RSSI_THRESHOLD_F entries table	PN76_APC_RSSI->wRssiThresholdF_01	0x0274-0x2D3	628	2	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.5.2 RSSI_TIMER (0x020C)

RSSI timer

Table 169. RSSI_TIMER (0x020C)

Function	bits	Values	Description
RSSI_TIMER	[15:0]		RSSI timer. Default: 423d.

8.18.2.5.3 RSSI_TIMER_FIRST_PERIOD (0x020E)

First period duration after Rf field ON.

Table 170. RSSI_TIMER_FIRST_PERIOD (0x020E)

Function	bits	Values	Description
RSSI	[15:0]		First period duration after Rffield ON. Unit is 128/ fc (106 kHz) if set to 0 it means feature is not used 0D2 => ~2 ms

8.18.2.5.4 RSSI_CTRL_00_AB (0x0210)

RSSI control.

Table 171. RSSI_CTRL_00_AB (0x0210)

Function	bits	Values	Description
RSSI	[7:6]	-	Reserved
	[5:0]	-	(APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type AB)

8.18.2.5.5 RSSI_NB_ENTRIES_AB (0x0211)

For Initial RF ON, CEA and CEB.

Table 172. RSSI_NB_ENTRIES_AB (0x0211)

Function	bits	Values	Description
RSSI	[7:5]		Reserved
	[4:0]		Number of entries in RSSI look up table (it refers to RSSI_ENTRY_AB_01 to RSSI_ENTRY_AB_18);

8.18.2.5.6 RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B

Table 173. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B

Entry	Address	Function	bit	Values	Description
RSSI_THRESHOLD_AB_01	0x212	RSSI	Threshold value for APC algorithm for TypeA and TypeB Note: <i>dwRssiEntryAB_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)</i>		
			[15:13]	-	Reserved
			[12:0]	-	RSSI Value
RSSI_PHASE_AB_01	0x214	RSSI	[15:0]	-	Phase compensation value for APC algorithm for TypeA and TypeB. Signed phase compensation with 1/4 degree resolution:16 bits signed value (using complement of 2)

Table 173. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B...continued

Entry	Address	Function	bit	Values	Description
RSSITHRESHOLDAB_02	0x0216	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_02	0x0218	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_03	0x021A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_03	0x021C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_04	0x021E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_04	0x0220	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_05	0x0222	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_05	0x0224	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_06	0x0226	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_06	0x0228	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_07	0x022A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_07	0x022C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_08	0x022E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_08	0x0230	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_09	0x0232	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_09	0x0234	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_0A	0x0236	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_0A	0x0238	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_0B	0x023A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_0B	0x023C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_0C	0x023E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_0C	0x0240	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_0D	0x0242	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_0D	0x0244	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_0E	0x0246	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_0E	0x0248	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_0F	0x024A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_0F	0x024C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_10	0x024E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_10	0x0250	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_11	0x0252	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_11	0x0254	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_12	0x0256	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_12	0x0258	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_13	0x025A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_13	0x025C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			

Table 173. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B...continued

Entry	Address	Function	bit	Values	Description
RSSITHRESHOLDAB_14	0x025E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_14	0x0260	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_15	0x0262	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_15	0x0264	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_16	0x0266	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_16	0x0268	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_17	0x026A	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_17	0x026C	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			
RSSITHRESHOLDAB_18	0x026E	Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description.			
ARBPHASEAB_18	0x0270	Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description.			

8.18.2.5.7 RSSI_CTRL_00_F (0x0272)

Table 174. RSSI_CTRL_00_F (0x0272)

Function	bits	Values	Description
RSSI	[7:6]		Reserved
	[5:0]		(APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type F)

8.18.2.5.8 RSSI_NB_ENTRIES_F (0x0273)

Table 175. RSSI_NB_ENTRIES_F (0x0273)

Function	bits	Values	Description
RSSI	[7:5]		Reserved
	[4:0]		Number of entries in RSSI look up table (it refers to RSSI_ENTRY_F_01 to RSSI_ENTRY_F_18);

8.18.2.5.9 RSSI_THRESHOLD_PHASE_TABLE for Type-F

Table 176. RSSI_THRESHOLD_PHASE_TABLE for Type-F

Entry	Address	Function	bit	Values	Description
RSSI_THRESHOLD_F_01	0x276	RSSI	Threshold value for APC algorithm for TypeF Note: <i>dwRssiEntryF_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)</i>		
			[15:13]	-	Reserved
			[12:0]	-	RSSI Value
RSSI_PHASE_F_01	0x276	RSSI	[15:0]	-	Phase compensation value for APC algorithm for TypeF. Signed phase compensation with 1/4 degree resolution:16 bits signed value (using complement of 2)
RSSITHRESHOLDF_02	0x0278	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			

Table 176. RSSI_THRESHOLD_PHASE_TABLE for Type-F...continued

Entry	Address	Function	bit	Values	Description
ARBPHASEF_02	0x027A	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_03	0x027C	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_03	0x027E	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_04	0x0280	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_04	0x0282	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_05	0x0284	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_05	0x0286	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_06	0x0288	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_06	0x028A	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_07	0x028C	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_07	0x028E	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_08	0x0290	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_08	0x0292	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_09	0x0294	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_09	0x0296	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_0A	0x0298	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_0A	0x029A	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_0B	0x029C	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_0B	0x029E	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_0C	0x02A0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_0C	0x02A2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_0D	0x02A4	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_0D	0x02A6	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_0E	0x02A8	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_0E	0x02AA	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_0F	0x02AC	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_0F	0x02AE	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_10	0x02B0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_10	0x02B2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_11	0x02B4	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_11	0x02B6	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_12	0x02B8	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_12	0x02BA	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_13	0x02BC	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_13	0x02BE	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_14	0x02C0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			

Table 176. RSSI_THRESHOLD_PHASE_TABLE for Type-F...continued

Entry	Address	Function	bit	Values	Description
ARBPHASEF_14	0x02C2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_15	0x02C4	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_15	0x02C6	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_16	0x02C8	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_16	0x02CA	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_17	0x02CC	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_17	0x02CE	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			
RSSITHRESHOLDF_18	0x02D0	Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description.			
ARBPHASEF_18	0x02D2	Refer to the entry RSSI_PHASE_F_01 for bit-fields and description.			

8.18.2.6 RSSI APC algorithm table output settings TX_PARAM_ENTRY_TABLE. Applicable only for card emulation.

APC TX_PARAM_ENTRY for ID.

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)

Entry ID	Address	Function	bits	Values	Description
ENTRY_00_ID	0x2D4	Driver count	[7]	-	Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):
				0x00	Dual driver
				0x01	Single driver
		BPSK mode	[6]	-	BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):
				0x00	Dual driver
				0x01	Single driver
ID	[5:0]	-	ID		
ENTRY_00_Tx1	0x2D5	RFU	[7:6]	-	Reserved
		PMU VDDPA setting	[5:0]	-	$VDDPA(V) = (val \times 10) + 1,5 V$ 0x00 = 1.50 V ... 0x2Ah = 5.70 V
ENTRY_00_Tx2	0x2D6	Scaling factor	[7:0]	-	Scaling factor for TX1 and TX2
ENTRY_01_ID	0x02D7	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_01_TX1	0x02D8	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_01_TX2	0x02D9	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_02_ID	0x02DA	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_02_TX1	0x02DB	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_02_TX2	0x02DC	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_03_ID	0x02DD	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_03_TX1	0x02DE	For bit-field values, refer to ENTRY_00_TX1 above			

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)...continued

Entry ID	Address	Function	bits	Values	Description
ENTRY_03_TX2	0x02DF	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_04_ID	0x02E0	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_04_TX1	0x02E1	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_04_TX2	0x02E2	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_05_ID	0x02E3	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_05_TX1	0x02E4	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_05_TX2	0x02E5	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_06_ID	0x02E6	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_06_TX1	0x02E7	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_06_TX2	0x02E8	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_07_ID	0x02E9	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_07_TX1	0x02EA	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_07_TX2	0x02EB	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_08_ID	0x02EC	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_08_TX1	0x02ED	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_08_TX2	0x02EE	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_09_ID	0x02EF	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_09_TX1	0x02F0	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_09_TX2	0x02F1	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0A_ID	0x02F2	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0A_TX1	0x02F3	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0A_TX2	0x02F4	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0B_ID	0x02F5	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0B_TX1	0x02F6	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0B_TX2	0x02F7	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0C_ID	0x02F8	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0C_TX1	0x02F9	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0C_TX2	0x02FA	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0D_ID	0x02FB	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0D_TX1	0x02FC	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0D_TX2	0x02FD	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0E_ID	0x02FE	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0E_TX1	0x02FF	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_0E_TX2	0x0300	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_0F_ID	0x0301	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_0F_TX1	0x0302	For bit-field values, refer to ENTRY_00_TX1 above			

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)...continued

Entry ID	Address	Function	bits	Values	Description
ENTRY_0F_TX2	0x0303	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_10_ID	0x0304	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_10_TX1	0x0305	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_10_TX2	0x0306	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_11_ID	0x0307	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_11_TX1	0x0308	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_11_TX2	0x0309	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_12_ID	0x030A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_12_TX1	0x030B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_12_TX2	0x030C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_13_ID	0x030D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_13_TX1	0x030E	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_13_TX2	0x030F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_14_ID	0x0310	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_14_TX1	0x0311	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_14_TX2	0x0312	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_15_ID	0x0313	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_15_TX1	0x0314	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_15_TX2	0x0315	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_16_ID	0x0316	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_16_TX1	0x0317	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_16_TX2	0x0318	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_17_ID	0x0319	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_17_TX1	0x031A	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_17_TX2	0x031B	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_18_ID	0x031C	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_18_TX1	0x031D	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_18_TX2	0x031E	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_19_ID	0x031F	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_19_TX1	0x0320	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_19_TX2	0x0321	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1A_ID	0x0322	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1A_TX1	0x0323	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1A_TX2	0x0324	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1B_ID	0x0325	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1B_TX1	0x0326	For bit-field values, refer to ENTRY_00_TX1 above			

NFC controller with NCI interface supporting EMV and NFC Forum applications

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)...continued

Entry ID	Address	Function	bits	Values	Description
ENTRY_1B_TX2	0x0327	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1C_ID	0x0328	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1C_TX1	0x0329	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1C_TX2	0x032A	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1D_ID	0x032B	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1D_TX1	0x032C	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1D_TX2	0x032D	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1E_ID	0x032E	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1E_TX1	0x032F	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1E_TX2	0x0330	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_1F_ID	0x0331	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_1F_TX1	0x0332	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_1F_TX2	0x0333	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_20_ID	0x0334	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_20_TX1	0x0335	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_20_TX2	0x0336	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_21_ID	0x0337	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_21_TX1	0x0338	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_21_TX2	0x0339	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_22_ID	0x033A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_22_TX1	0x033B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_22_TX2	0x033C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_23_ID	0x033D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_23_TX1	0x033E	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_23_TX2	0x033F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_24_ID	0x0340	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_24_TX1	0x0341	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_24_TX2	0x0342	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_25_ID	0x0343	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_25_TX1	0x0344	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_25_TX2	0x0345	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_26_ID	0x0346	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_26_TX1	0x0347	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_26_TX2	0x0348	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_27_ID	0x0349	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_27_TX1	0x034A	For bit-field values, refer to ENTRY_00_TX1 above			

NFC controller with NCI interface supporting EMV and NFC Forum applications

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)...continued

Entry ID	Address	Function	bits	Values	Description
ENTRY_27_TX2	0x034B	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_28_ID	0x034C	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_28_TX1	0x034D	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_28_TX2	0x034E	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_29_ID	0x034F	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_29_TX1	0x0350	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_29_TX2	0x0351	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2A_ID	0x0352	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2A_TX1	0x0353	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2A_TX2	0x0354	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2B_ID	0x0355	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2B_TX1	0x0356	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2B_TX2	0x0357	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2C_ID	0x0358	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2C_TX1	0x0359	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2C_TX2	0x035A	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2D_ID	0x035B	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2D_TX1	0x035C	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2D_TX2	0x035D	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2E_ID	0x035E	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2E_TX1	0x035F	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2E_TX2	0x0360	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_2F_ID	0x0361	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_2F_TX1	0x0362	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_2F_TX2	0x0363	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_30_ID	0x0364	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_30_TX1	0x0365	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_30_TX2	0x0366	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_31_ID	0x0367	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_31_TX1	0x0368	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_31_TX2	0x0369	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_32_ID	0x036A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_32_TX1	0x036B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_32_TX2	0x036C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_33_ID	0x036D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_33_TX1	0x036E	For bit-field values, refer to ENTRY_00_TX1 above			

NFC controller with NCI interface supporting EMV and NFC Forum applications

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)...continued

Entry ID	Address	Function	bits	Values	Description
ENTRY_33_TX2	0x036F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_34_ID	0x0370	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_34_TX1	0x0371	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_34_TX2	0x0372	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_35_ID	0x0373	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_35_TX1	0x0374	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_35_TX2	0x0375	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_36_ID	0x0376	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_36_TX1	0x0377	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_36_TX2	0x0378	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_37_ID	0x0379	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_37_TX1	0x037A	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_37_TX2	0x037B	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_38_ID	0x037C	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_38_TX1	0x037D	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_38_TX2	0x037E	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_39_ID	0x037F	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_39_TX1	0x0380	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_39_TX2	0x0381	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3A_ID	0x0382	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3A_TX1	0x0383	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3A_TX2	0x0384	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3B_ID	0x0385	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3B_TX1	0x0386	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3B_TX2	0x0387	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3C_ID	0x0388	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3C_TX1	0x0389	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3C_TX2	0x038A	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3D_ID	0x038B	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3D_TX1	0x038C	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3D_TX2	0x038D	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3E_ID	0x038E	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3E_TX1	0x038F	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_3E_TX2	0x0390	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_3F_ID	0x0391	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_3F_TX1	0x0392	For bit-field values, refer to ENTRY_00_TX1 above			

NFC controller with NCI interface supporting EMV and NFC Forum applications

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)...continued

Entry ID	Address	Function	bits	Values	Description
ENTRY_3F_TX2	0x0393	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_40_ID	0x0394	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_40_TX1	0x0395	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_40_TX2	0x0396	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_41_ID	0x0397	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_41_TX1	0x0398	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_41_TX2	0x0399	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_42_ID	0x039A	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_42_TX1	0x039B	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_42_TX2	0x039C	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_43_ID	0x039D	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_43_TX1	0x039E	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_43_TX2	0x039F	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_44_ID	0x03A0	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_44_TX1	0x03A1	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_44_TX2	0x03A2	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_45_ID	0x03A3	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_45_TX1	0x03A4	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_45_TX2	0x03A5	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_46_ID	0x03A6	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_46_TX1	0x03A7	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_46_TX2	0x03A8	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_47_ID	0x03A9	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_47_TX1	0x03AA	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_47_TX2	0x03AB	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_48_ID	0x03AC	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_48_TX1	0x03AD	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_48_TX2	0x03AE	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_49_ID	0x03AF	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_49_TX1	0x03B0	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_49_TX2	0x03B1	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4A_ID	0x03B2	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4A_TX1	0x03B3	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4A_TX2	0x03B4	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4B_ID	0x03B5	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4B_TX1	0x03B6	For bit-field values, refer to ENTRY_00_TX1 above			

Table 177. TX_PARAM_ENTRY_00_ID (0x02D4)...continued

Entry ID	Address	Function	bits	Values	Description
ENTRY_4B_TX2	0x03B7	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4C_ID	0x03B8	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4C_TX1	0x03B9	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4C_TX2	0x03BA	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4D_ID	0x03BB	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4D_TX1	0x03BC	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4D_TX2	0x03BD	For bit-field values, refer to ENTRY_00_TX2 above			
ENTRY_4E_ID	0x03BE	For bit-field values, refer to ENTRY_00_ID above			
ENTRY_4E_TX1	0x03BF	For bit-field values, refer to ENTRY_00_TX1 above			
ENTRY_4E_TX2	0x03C0	For bit-field values, refer to ENTRY_00_TX2 above			

8.18.2.7 Autocol configuration settings.

Autocol configuration settings.

8.18.2.7.1 List of Autocoll configuration settings

List of Autocoll configuration settings

Table 178. List of Autocoll configuration settings

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
RF_DEBOUNCE_TIMEOUT (0x03C4)	PN76_AUTOCOLL_CFG->bRf DebounceTimeout	0x03C4	964	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
SENSE_RES (0x03C5)	PN76_AUTOCOLL_CFG->bSensRes	0x03C5	965	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFC_ID1 (0x03C7)	PN76_AUTOCOLL_CFG->bNfc ID1	0x03C7	967	3	E_PN76_EEPROM_SECURE_LIB_CONFIG
SEL_RES (0x03CA)	PN76_AUTOCOLL_CFG->bSel Res	0x03CA	970	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
FELICA_POLLRES (0x03CB)	PN76_AUTOCOLL_CFG->bPoll Res	0x03CB	971	18	E_PN76_EEPROM_SECURE_LIB_CONFIG
RANDOM_UID_ENABLE (0x03DD)	PN76_AUTOCOLL_CFG->bRandomUIDEnable	0x03DD	989	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.7.2 RF_DEBOUNCE_TIMEOUT (0x03C4)

Debounce timeout

Table 179. RF_DEBOUNCE_TIMEOUT (0x03C4)

Function	bits	Values	Description
DEBOUNCE_TIMEOUT	[7:0]	-	Timeout used after the RF detection during the AUTOCOLL to detect if there is a glitch or continuous RF. Value is entered in 1 µs.

8.18.2.7.3 SENSE_RES (0x03C5)

Response to ReqA / ATQA in order byte 0, byte 1.

Table 180. SENSE_RES (0x03C5)

Function	bits	Values	Description
Response to ReqA / ATQA	[15:0]		ATQA in order byte 0, byte 1
	[15:8]		Byte1 value
	[7:0]		Byte0 value

8.18.2.7.4 NFC_ID1 (0x03C7)

Response to ReqA / ATQA in order byte 0, byte 1

Table 181. NFC_ID1 (0x03C7)

Function	bits	Values	Description
UID address generation	[31:0]		If Random UID is disabled (EEPROM address 0x2CB), the content of these addresses is used to generate a Fixed UID. The order is byte 0, Byte 1, Byte 2; Byte3 - which is the first NFCID1 byte - is fixed to 08h, the check byte is calculated automatically.
	[31:24]	0x08	Byte3 value
	[23:16]		Byte2 value
	[15:8]		Byte1 value
	[7:0]		Byte0 value

8.18.2.7.5 SEL_RES (0x03CA)

Response to Select : SAK.

Table 182. SEL_RES (0x03CA)

Function	bits	Values	Description
Response to Select	[7:0]		Response to Select : SAK

8.18.2.7.6 FELICA_POLLRES (0x03CB)

Response to Select : SAK

Table 183. FELICA_POLLRES (0x03CB)

Function	byte	bits	Values	Description
Felica Poll response	[1:0]	[15:0]	0x01FE	FeliCa polling response. Shall be the same value.
	[7:2]	[47:0]		FeliCa polling response. NFCID2 (6 bytes).
	[15:8]	[63:0]		FeliCa polling response. PAD (8 bytes).
	[17:16]	[15:0]		FeliCa polling response. System code (2 bytes).

8.18.2.7.7 RANDOM_UID_ENABLE (0x03DD)

Random UID enable

Table 184. RANDOM_UID_ENABLE (0x03DD)

Function	bits	Values	Description
Random UID enable	[7:1]		Reserved
	[0]	0x00	Use UID stored in EEPROM
		0x01	Randomly generate the UID in which the first byte is fixed and the remaining 3 bytes are random A new random number is generated after each RF-OFF to RF-ON.

8.18.2.8 LPCD related configuration parameters

8.18.2.8.1 EEPROM_LPCD_SETTINGS_LIST

List of LPCD related configuration settings

Table 185. List of LPCD related configuration settings

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
EEPROM_LPCD_SETTINGS_AVG_SAMPLES	PN76_LPCD_SETTINGS->avg_samples	0x03DE	990	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_RSSI_TARGET (0x03E0)	PN76_LPCD_SETTINGS->lpcd_rssi_target	0x03E0	992	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_RSSI_HYST (0x03E2)	PN76_LPCD_SETTINGS->lpcd_rssi_hyst	0x03E2	994	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_CONFIG (0x03E3)	PN76_LPCD_SETTINGS->w Config	0x03E3	995	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_THRESHOLD (0x03E6)	PN76_LPCD_SETTINGS->lpcd_threshold_coarse	0x03E6	998	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_WAIT_RX_SETTLE (0x03F7)	PN76_LPCD_SETTINGS->w WaitRxSettle	0x03F7	1015	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_VDDPA (0x03FB)	PN76_LPCD_SETTINGS->bTx LdoVddpa	0x03FB	1019	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPCD_CHECK_PERIOD (0x03FC)	PN76_LPCD_SETTINGS->w CheckPeriod	0x03FC	1020	2	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.8.2 LPCD_AVG_SAMPLES (0x03DE)

Number of samples used for averaging

Table 186. LPCD_AVG_SAMPLES (0x03DE)

Function	bits	Values	Description
Random UID enable	[7:3]		Reserved

Table 186. LPCD_AVG_SAMPLES (0x03DE)...continued

Function	bits	Values	Description
LPCD_AVG_SAMPLES	[2:0]		Defines how many samples of the I and Q values are used for the averaging. Average samples in power of 2.
		0x00	1 sample
		0x01	2 samples
		0x02	4 samples
		0x03	8 samples
		0x04	16 samples
		0x05	32 samples
		0x06	64 samples
		0x07	RFU

8.18.2.8.3 LPCD_RSSI_TARGET (0x03E0)

Table 187. LPCD_RSSI_TARGET (0x03E0)

Function	bits	Values	Description
LPCD_RSSI_TARGET	[15:0]		Value to be set in register DGRM_RSSI_REG_DGRM_RSSI_TARGET. Typically the same values from the Type A106 LOAD_RF_CONFIGURATION API (DGRM_RSSI register) are used.

8.18.2.8.4 LPCD_RSSI_HYST (0x03E2)

Table 188. LPCD_RSSI_HYST (0x03E2)

Function	bits	Values	Description
LPCD_RSSI_HYST	[7:0]		Value to be set in CLIF_DGRM_RSSI_REG_DGRM_RSSI_HYST. Typically the same values from the Type A106 LOAD_RF_CONFIGURATION API (DGRM_RSSI register) are used.

8.18.2.8.5 LPCD_CONFIG (0x03E3)

Number of samples used for averaging

Table 189. LPCD_CONFIG (0x03E3)

Function	bits	Values	Description
RFU	[15:6]		Reserved
LPCD_CONFIG	[5]	0x00	Disables feature Immediate RF OFF before TXLDO shutdown to save power
		0x01	Enables feature Immediate RF OFF before TXLDO shutdown to save power. For this feature, Enable VDDPA fast discharge must be enabled.
	[4]	0x00	Disables VDDPA fast discharge.
		0x01	Enable VDDPA fast discharge.

Table 189. LPCD_CONFIG (0x03E3)...continued

Function	bits	Values	Description
	[3]	0x00	Enable single driver
		0x01	Enable both drivers
	[2:0]		Acquisition channels
		0x00-0x01	RFU
		0x02	Magnitude
		0x03	I and Q
		0x04	M, I and Q
		0x05-0x07	RFU

8.18.2.8.6 LPCD_THRESHOLD (0x03E6)

LPCD threshold type depends upon the LPCD_CONFIG[2:0] value in [Table 189](#)

For 'I and Q' mode: 1st threshold = I ch; 2nd threshold = Q ch.

Table 190. LPCD_THRESHOLD (0x03E6)

Function	bits	Values	Description
LPCD Q channel threshold	[31:16]		ADC LSB granularity of threshold depends of avg_samples_meas value:
		0x00	unit 1
		0x01	unit 1/2
		0x02	unit 1/4
		0x03	unit 1/8
		0x04	unit 1/16
		0x05	unit 1/32
		Other	Reserved
LPCD I channel threshold	[15:0]	-	ADC LSB granularity of threshold depends of avg_samples_meas value:
		0x00	unit 1
		0x01	unit 1/2
		0x02	unit 1/4
		0x03	unit 1/8
		0x04	unit 1/16
		0x05	unit 1/32
		Other	Reserved

Note: If the difference between the measured value and the reference is greater than the threshold on either channels, then a card is detected.

8.18.2.8.7 LPCD_WAIT_RX_SETTLE (0x03F7)

Delay between FieldOn and starting ADC data averaging.

Table 191. LPCD_WAIT_RX_SETTLE (0x03F7)

Function	bits	Values	Description
LPCD DELAY	[15:0]		Delay between FieldOn and starting ADC data averaging. Value in us, default 14h = 20 μs

8.18.2.8.8 LPCD_VDDPA (0x03FB)

VDDPA voltage when DCDC (internal or external) or external power source is used to feed TXLDO.

Table 192. LPCD_VDDPA (0x03FB)

Function	bits	Values	Description
VDDPA voltage LPCD DELAY	[7:0]		TXLDO output voltage.
		0x00-0x2A	resultant voltage would be: 1V50 + this value × 0.1 V)
		Others	Reserved

8.18.2.8.9 LPCD_CHECK_PERIOD (0x03FC)

Timer value defining standby duration before calibration and reference measurement in LPCD single mode(Mode 4)

Table 193. LPCD_CHECK_PERIOD (0x03FC)

Function	bits	Values	Description
LPCD DELAY	[15:0]	-	2.63ms resolution, default 0x26 = ~100 ms

8.18.2.9 CORRECTION_ENTRY_TABLE TX wave shaping for proprietary correction configuration

Table 194. CORRECTION_ENTRY_TABLE

Entry	Address	Function	bit	Values	Description
CORRECTION_ENTRY 0 for 1V5	0x042B	PROP_CORRECTION_ENTRY	[15:8]		Correction applied for ASK10 Range would be -128 to +127.
			[7:0]		Correction applied for ASK100. Range would be -128 to +127.
CORRECTION_ENTRY1 for 1.60V	0x042D	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY2 for 1.70V	0x042F	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY3 for 1.80V	0x0431	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY4 for 1.90V	0x0433	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY5 for 2.00V	0x0435	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY6 for 2.10V	0x0437	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			

Table 194. CORRECTION_ENTRY_TABLE...continued

Entry	Address	Function	bit	Values	Description
CORRECTION_ENTRY7 for 2.20V	0x0439	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY8 for 2.30V	0x043B	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY9 for 2.40V	0x043D	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY10 for 2.50V	0x043F	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY11 for 2.60V	0x0441	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY12 for 2.70V	0x0443	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY13 for 2.80V	0x0445	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY14 for 2.90V	0x0447	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY15 for 3.00V	0x0449	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY16 for 3.10V	0x044B	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY17 for 3.20V	0x044D	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY18 for 3.30V	0x044F	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY19 for 3.40V	0x0451	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY20 for 3.50V	0x0453	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY21 for 3.60V	0x0455	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY22 for 3.70V	0x0457	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY23 for 3.80V	0x0459	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY24 for 3.90V	0x045B	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY25 for 4.00V	0x045D	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY26 for 4.10V	0x045F	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY27 for 4.20V	0x0461	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY28 for 4.30V	0x0463	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			

Table 194. CORRECTION_ENTRY_TABLE...continued

Entry	Address	Function	bit	Values	Description
CORRECTION_ENTRY29 for 4.40V	0x0465	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY30 for 4.50V	0x0467	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY31 for 4.60V	0x0469	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY32 for 4.70V	0x046B	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY33 for 4.80V	0x046D	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY34 for 4.90V	0x046F	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY35 for 5.00V	0x0471	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY36 for 5.10V	0x0473	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY37 for 5.20V	0x0475	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY38 for 5.30V	0x0477	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY39 for 5.40V	0x0479	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY40 for 5.50V	0x047B	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY41 for 5.60V	0x047D	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			
CORRECTION_ENTRY42 for 5.70V	0x047F	Byte and bit-fields description, refer to CORRECTION_ENTRY 0			

8.18.2.10 TX_SHAPING_RTRANS_FTRANS_TABLE TX wave shaping for proprietary correction configuration for rising edge and falling edges. (0x0481)

8.18.2.10.1 TX_SHAPING_RTRANS_FTRANS_1 (0x0481)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 195. TX_SHAPING_RTRANS_FTRANS_1 (0x0481)

Function	Address	Bytes	Bits	Description
RTRANS0	0x0481	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x0485	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS2	0x0489	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge

Table 195. TX_SHAPING_RTRANS_FTRANS_1 (0x0481)...continued

Function	Address	Bytes	Bits	Description
RTRANS3	0x048D	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x0491	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS1	0x0495	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS2	0x0499	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x049D	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

8.18.2.10.2 TX_SHAPING_RTRANS_FTRANS_2 (0x4A1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 196. TX_SHAPING_RTRANS_FTRANS_2 (0x4A1)

Function	Address	Bytes	Bits	Description
RTRANS0	0x4A1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x04A5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS2	0x04A9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS3	0x04AD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x04B1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS1	0x04B5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS2	0x04B9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x04BD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

8.18.2.10.3 TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 197. TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)

Function	Address	Bytes	Bits	Description
RTRANS0	0x04C1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x04C5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge

Table 197. TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)...continued

Function	Address	Bytes	Bits	Description
RTRANS2	0x04C9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS3	0x04CD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x04D1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS1	0x04D5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS2	0x04D9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x04DD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

8.18.2.10.4 TX_SHAPING_RTRANS_FTRANS_1 (0x04E1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

Table 198. TX_SHAPING_RTRANS_FTRANS_1 (0x04E1)

Function	Address	Bytes	Bits	Description
RTRANS0	0x04E1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS1	0x04E5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS2	0x04E9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
RTRANS3	0x04ED	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the rising edge
FTRANS0	0x04F1	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS1	0x04F5	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS2	0x04F9	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge
FTRANS3	0x04FD	[3:0]	[31:0]	These values apply in case EDGE_STYLE = 0 is configured for the falling edge

8.18.2.11 TX driver NOV (non-overlap) settings configuration.

8.18.2.11.1 EEPROM_TX_DRIVER_NOV_LIST

List of NOV configuration parameters

Table 199. List of NOV configuration parameters

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
NOV_CFG_CAL (0x0501)	PN76_TX_DRIVER_NOV->Cfg NovCal	0x0501	1281	1	EEPROM_SECURE_LIB_CONFIG
NOV_CAL_VAL1 (0x0502)	PN76_TX_DRIVER_NOV->VddpaCalVal1	0x0502	1282	1	EEPROM_SECURE_LIB_CONFIG
NOV_CAL_VAL2 (0x0503)	PN76_TX_DRIVER_NOV->VddpaCalVal2	0x0503	1283	1	EEPROM_SECURE_LIB_CONFIG
NOV_CAL_THRESHOLD (0x0504)	PN76_TX_DRIVER_NOV->Cfg Threshold	0x0504	1284	1	EEPROM_SECURE_LIB_CONFIG
NOV_CAL_OFFSET1 (0x0505)	PN76_TX_DRIVER_NOV->UserOffsets1	0x0505	1285	4	EEPROM_SECURE_LIB_CONFIG
NOV_CAL_OFFSET2 (0x0509)	PN76_TX_DRIVER_NOV->UserOffsets2	0x0509	1289	4	EEPROM_SECURE_LIB_CONFIG

8.18.2.11.2 NOV_CFG_CAL (0x0501)

NOV calibration type

Table 200. NOV_CFG_CAL (0x0501)

Function	bits	Values	Description
RFU	[7:2]	-	Reserved
NOV_CALIBRATION_TYPE	[1:0]	0x00	No calibration performed, needs to be updated to 01 or 10 before the first RF on of the chip is performed.
		0x01	Enable FW calibration after every cold boot.
		0x02	Use calibration value coming from EEPROM NOV_CAL_VAL1, NOV_CAL_VAL2 (Default)
		0x03	RFU

8.18.2.11.3 NOV_CAL_VAL1 (0x0502)

Table 201. NOV_CAL_VAL1 (0x0502)

Function	bits	Values	Description
VDDPACALVAL1	[7:0]	0x03	(1.8 V)
		0x0D	(2.8 V)

8.18.2.11.4 NOV_CAL_VAL2 (0x0503)

Table 202. NOV_CAL_VAL2 (0x0503)

Function	bits	Values	Description
VDDPACALVAL2	[7:0]	0x15	(3.6 V)
		0x24	(5.1 V)

8.18.2.11.5 NOV_CAL_THRESHOLD (0x0504)

Table 203. NOV_CAL_THRESHOLD (0x0504)

Function	bits	Values	Description
VDDPACALVAL2	[7:0]	0x08	(2.3 V)
		0x16	(3.7 V)

8.18.2.11.6 NOV_CAL_OFFSET1 (0x0505)

Table 204. NOV_CAL_OFFSET1 (0x0505)

Function	bits	Values	Description
RFU	[31:29]		Reserved
VDDAPA MIN	[28:24]		Group#1 (VDDPA min to CfgThreshold), offset_2l(1)
	[23:21]		Reserved
	[20:16]		Group#1 (VDDPA min to CfgThreshold), offset_2l(0)
	[15:13]		Reserved
	[12:08]		Group#1 (VDDPA min to CfgThreshold), offset_3l_p2
	[07:05]		Reserved
	[04:00]		Group#1 (VDDPA min to CfgThreshold), offset_3l

8.18.2.11.7 NOV_CAL_OFFSET2 (0x0509)

Table 205. NOV_CAL_OFFSET2 (0x0509)

Function	bits	Values	Description
RFU	[31:29]		Reserved
VDDAPA MAX	[28:24]		Group#1 (VDDPA max to CfgThreshold), offset_2l(1)
	[23:21]		Reserved
	[20:16]		Group#1 (VDDPA max to CfgThreshold), offset_2l(0)
	[15:13]		Reserved
	[12:08]		Group#1 (VDDPA max to CfgThreshold), offset_3l_p2
	[07:05]		Reserved
	[04:00]		Group#1 (VDDPA max to CfgThreshold), offset_3l

8.18.2.12 Active reader mode TX wave shaping configuration

This section provides the active reader mode TX wave shaping configuration settings.

8.18.2.12.1 RESIDUAL_AMPL_LEVEL_ACTIVE_A106 (0X050E)

Table 206. RESIDUAL_AMPL_LEVEL_ACTIVE_A106 (0X050E)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.12.2 EDGE_TYPE_ACTIVE_A106 (0X050F)

Table 207. EDGE_TYPE_ACTIVE_A106 (0X050F)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction
	Others	RFU	
	[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels
		0x03	three linear transitions between amplitude levels
		Others	RFU
		Lookup table based shaping	
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction
0x06		lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
Others	RFU		

8.18.2.12.3 EDGE_STYLE_ACTIVE_A106 (0X0510)

Table 208. EDGE_STYLE_ACTIVE_A106 (0X0510)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]		Defines edge style configuration
			For Firmware based shaping (bEdgeType_A106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_A106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.12.4 EDGE_LENGTH_ACTIVE_A106 (0X0511)

Table 209. EDGE_LENGTH_ACTIVE_A106 (0X0511)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.12.5 RESIDUAL_AMPL_LEVEL_ACTIVE_F212 (0X0512)

Table 210. RESIDUAL_AMPL_LEVEL_ACTIVE_F212 (0X0512)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.12.6 EDGE_TYPE_ACTIVE_F212 (0X0513)

Table 211. EDGE_TYPE_ACTIVE_F212 (0X0513)

Function	bit	Values	Description	
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:		
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
			Firmware based shaping	
			0x01	linear transition between two amplitude levels
	0x02		two linear transitions between amplitude levels	
	0x03		three linear transitions between amplitude levels	
	Others		RFU	
	Lookup table based shaping			
	0x04		lookup table-based transition, no automatic adaptation based on VDDPA	
	0x05		lookup table-based transition, automatic adaptation based on VDDPA including Correction	
0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction			
Others	RFU			

8.18.2.12.7 EDGE_STYLE_ACTIVE_F212 (0X0514)

Table 212. EDGE_STYLE_ACTIVE_F212 (0X0514)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	

Table 212. EDGE_STYLE_ACTIVE_F212 (0X0514)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]		RFU
Edge style configuration rising edge	[2:0]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.12.8 EDGE_LENGTH_ACTIVE_F212 (0X0515)

Table 213. EDGE_LENGTH_ACTIVE_F212 (0X0515)

Function	bit	Values	Description
Edge transition length	[7]	Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)	
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.12.9 RESIDUAL_AMPL_LEVEL_ACTIVE_F424 (0X0516)

Table 214. RESIDUAL_AMPL_LEVEL_ACTIVE_F424 (0X0516)

Function	bit	Values	Description
Residual amplitude level	[7:0]	0x00	0 % carrier
		0xFF	100 % carrier

8.18.2.12.10 EDGE_TYPE_ACTIVE_F424 (0X0517)

Table 215. EDGE_TYPE_ACTIVE_F424 (0X0517)

Function	bit	Values	Description
Edge transition style	[7:4]	Defines style of edge transition of falling edge, Defines style of edge transition:	
		Firmware based shaping	
		0x01	linear transition between two amplitude levels
		0x02	two linear transitions between amplitude levels

Table 215. EDGE_TYPE_ACTIVE_F424 (0X0517)...continued

Function	bit	Values	Description	
		0x03	three linear transitions between amplitude levels	
		Others	RFU	
		Lookup table based shaping		
		0x04	lookup table-based transition, no automatic adaptation based on VDDPA	
		0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction	
		0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction	
		Others	RFU	
		[3:0]	Definition of edge transition style of rising edge, Defines style of edge transition:	
		Firmware based shaping		
		0x01	linear transition between two amplitude levels	
		0x02	two linear transitions between amplitude levels	
		0x03	three linear transitions between amplitude levels	
	Others	RFU		
	Lookup table based shaping			
	0x04	lookup table-based transition, no automatic adaptation based on VDDPA		
	0x05	lookup table-based transition, automatic adaptation based on VDDPA including Correction		
	0x06	lookup table-based transition, automatic adaptation based on VDDPA but no Correction		
	Others	RFU		

8.18.2.12.11 EDGE_STYLE_ACTIVE_F424 (0X0518)

Table 216. EDGE_STYLE_ACTIVE_F424 (0X0518)

Function	bit	Values	Description
RFU	[7]	RFU	
Edge style configuration falling edge	[6:4]	Defines edge style configuration	
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3)
RFU	[3]	RFU	
Edge style configuration rising edge	[2:0]		Defines edge style configuration

Table 216. EDGE_STYLE_ACTIVE_F424 (0X0518)...continued

Function	bit	Values	Description
			For Firmware based shaping (bEdgeType_F424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style)
			For lookup table based shaping (bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3)

8.18.2.12.12 EDGE_LENGTH_ACTIVE_F424 (0X0519)

Table 217. EDGE_LENGTH_ACTIVE_F424 (0X0519)

Function	bit	Values	Description
Edge transition length	[7]		Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)
		0x00	disabled (1 transition state = one carrier cycle)
		0x01	enabled (1 transition state = two carrier cycles)
	[6:5]		RFU
	[4:0]		Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)

8.18.2.13 Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings(0x011D)

8.18.2.13.1 EEPROM_MEASURED_LMA_RSSI_LIST

List of Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings.

Table 218. List of Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings.

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
LMA_RSSI_INTERPOLATED_RSSI (0x0530)	PN76_MEASURED_LMA_RSSI->wMeasuredInterpolatedRSSI	0x0530	1328	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LMA_RSSI_FIELD_STRENGTH (0x0532)	PN76_MEASURED_LMA_RSSI->bMeasuredFieldStrength	0x0532	1330	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.13.2 LMA_RSSI_INTERPOLATED_RSSI (0x0530)

Table 219. LMA_RSSI_INTERPOLATED_RSSI (0x0530)

Function	bits	Values	Description
LMA_RSSI_INTERPOLATED_RSSI	[15:0]		Measured Interpolated RSSI (16 bit, in little-endian format). Each count indicates a value of 1/2048 mV.

8.18.2.13.3 LMA_RSSI_FIELD_STRENGTH (0x0532)

Table 220. LMA_RSSI_FIELD_STRENGTH (0x0532)

Function	bits	Values	Description
LMA_RSSI_FIELD_STRENGTH	[7:0]		Field strength (8 bits, 1/16 A/m LSB) used for bMeasuredLMA and wMeasuredInterpolatedRSSI.

8.18.2.14 Global TX_SHAPING configuration

This section provides configuration global TX waveform shaping settings.

8.18.2.14.1 EEPROM_RM_GLOBAL_TX_SHAPING_LIST

List of Settings related TX_SHAPING configuration.

Table 221. List of Settings related TX_SHAPING configuration.

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
TX_SHAPING_CONIFG (0x058C)	PN76_RM_GLOBAL_TX_SHAPING->bConfig	0x058C	1420	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_INV_RM (0x058D)	PN76_RM_GLOBAL_TX_SHAPING->bTX_INV_RM	0x058D	1421	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_CLK_MODE_1 (0x058E)	PN76_RM_GLOBAL_TX_SHAPING->bCLK_MODE_1	0x058E	1422	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_CLK_MODE_2 (0x058F)	PN76_RM_GLOBAL_TX_SHAPING->bCLK_MODE_2	0x058F	1423	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
GSN_MOD_RM (0x0590)	PN76_RM_GLOBAL_TX_SHAPING->bGSN_MOD_RM	0x0590	1424	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
GSN_CW_RM (0x0591)	PN76_RM_GLOBAL_TX_SHAPING->bGSN_CW_RM	0x0591	1425	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
GSP_RM (0x0592)	PN76_RM_GLOBAL_TX_SHAPING->bGSP_RM	0x0592	1426	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_FRCZERO_THR (0x0593)	PN76_RM_GLOBAL_TX_SHAPING->bTX_FRCZERO_THR	0x0593	1427	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
SIGNAL_SCALING_CONFIG (0x0594)	PN76_RM_GLOBAL_TX_SHAPING->bSignalScaling Config	0x0594	1428	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_PH_SHIFT_DIV10 (0x0595)	PN76_RM_GLOBAL_TX_SHAPING->bTX_PH_SHIFT_DIV10	0x0595	1429	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
TX_PH_SHIFT_MOD10 (0x0596)	PN76_RM_GLOBAL_TX_SHAPING->bTX_PH_SHIFT_MOD10	0x0596	1430	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.14.2 TX_SHAPING_CONIFG (0x058C)

PWM scheme for RM

Table 222. TX_SHAPING_CONIFG (0x058C)

Function	bits	Values	Description
RFU	[7:1]		Reserved
PWM scheme for RM	[0]	0x00	defining 3-levels for drivers TX1/2 - required for balanced antenna (default)
		0x01	defining 2-levels for drivers TX1/2 - required for single ended antenna

8.18.2.14.3 TX_INV_RM (0x058D)

Transmitter configuration

Table 223. TX_INV_RM (0x058D)

Function	bits	Values	Description
RFU	[7:6]		Reserved
TX1 output configuration	[5]	0x00	TX1 non-inverted output (output zero remains zero)
		0x01	TX1 inverted output (common mode operation, output zero becomes one)
TX2 output configuration	[4]	0x00	TX2 non-inverted output (output zero remains zero)
		0x01	TX2 inverted output (common mode operation, output zero becomes one)
RFU	[3:2]		Reserved
TX1 phase shift configuration	[1]	0x00	TX1 no phase shift, 0 deg
		0x01	TX1 phase shifted by 180 deg
TX2 phase shift configuration	[0]	0x00	TX2 no phase shift, 0 deg
		0x01	TX2 phase shifted by 180 deg

8.18.2.14.4 TX_CLK_MODE_1 (0x058E)

Transmitter configuration

Table 224. TX_CLK_MODE_1 (0x058E)

Function	bits	Values	Description
RFU	[7]		Reserved
CLK_MODE_CW_RM	[6:4]		CLK_MODE_CW_RM
RFU	[3]		Reserved
CLK_MODE_MOD_RM	[2:0]		CLK_MODE_MOD_RM

8.18.2.14.5 TX_CLK_MODE_2 (0x058F)

CLK_MODE configuration

Table 225. TX_CLK_MODE_2 (0x058F)

Function	bits	Values	Description
RFU	[7]		Reserved

Table 225. TX_CLK_MODE_2 (0x058F)...continued

Function	bits	Values	Description
CLK_MODE_DEFAULT	[6:4]		CLK_MODE_DEFAULT
RFU	[3]		Reserved
CLK_MODE_TRANS_RM	[2:0]		CLK_MODE_TRANS_RM

8.18.2.14.6 GSN_MOD_RM (0x0590)

GSN_MOD_RM configuration

Table 226. GSN_MOD_RM (0x0590)

Function	bits	Values	Description
RFU	[7:5]		Reserved
GSN_MOD_RM	[4:0]		GSN_MOD_RM

8.18.2.14.7 GSN_CW_RM (0x0591)

GSN_CW_RM configuration

Table 227. GSN_CW_RM (0x0591)

Function	bits	Values	Description
RFU	[7:5]		Reserved
GSN_CW_RM	[4:0]		GSN_CW_RM

8.18.2.14.8 GSP_RM (0x0592)

GSP_RM configuration

Table 228. GSP_RM (0x0592)

Function	bits	Values	Description
RFU	[7:5]		Reserved
GSP_RM	[4:0]		GSP_RM

8.18.2.14.9 TX_FRCZERO_THR (0x0593)

CLIF_SS_TX_CFG_REG configuration

Table 229. TX_FRCZERO_THR (0x0593)

Function	bits	Values	Description
RFU	[7]		Reserved
CLIF_SS_TX_CFG_REG	[6:0]		Defining CLIF_SS_TX_CFG_REG[12:6]

8.18.2.14.10 SIGNAL_SCALING_CONFIG (0x0594)

Global TX_SS_TARGET_SCALE configuration

Table 230. SIGNAL_SCALING_CONFIG (0x0594)

Function	bits	Values	Description
Global TX_SS_TARGET_SCALE	[7:0]		Global TX_SS_TARGET_SCALE configuration for debugging purposes

8.18.2.14.11 TX_PH_SHIFT_DIV10 (0x0595)

Global TX_SS_TARGET_SCALE configuration

Table 231. TX_PH_SHIFT_DIV10 (0x0595)

Function	bits	Values	Description
RFU	[7:5]		Reserved
CLIF_ANACTRL_TX_CONFIG_REG	[4:0]		CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_DIV10

8.18.2.14.12 TX_PH_SHIFT_MOD10 (0x0596)

Global CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_MOD10 configuration

Table 232. TX_PH_SHIFT_MOD10 (0x0596)

Function	bits	Values	Description
RFU	[7:4]		Reserved
CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_MOD10	[3:0]		CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_MOD10

8.18.2.15 Settings for encryption/decryption of keys storage for Symmetric and Asymmetric private keys

This section provides the derivation messages for different operations on application keys.

8.18.2.15.1 APP_ENCRY_DECRY_KEY_DERIV_MSG (0x0550)

Table 233. APP_ENCRY_DECRY_KEY_DERIV_MSG (0x0550)

Function	bytes	Values	Description
abCustEncrDecrDerivMsg	[23:0]		Derivation message for encryption/decryption for Master Keys for interfacing with Mbed.

8.18.2.15.2 APP_ENCRY_KEY_DERIV_MSG_ASYMM_KEY (0x568)

Table 234. APP_ENCRY_KEY_DERIV_MSG_ASYMM_KEY (0x568)

Function	bytes	Values	Description
adwDerivMsgEncDecKeyForAsym	[23:0]		Derivation message for encrypting/decrypting the storing/retrieving of Asymm private key.

8.18.2.16 RFLD and NFCLD settings

8.18.2.16.1 EEPROM_RFLD_NFCLD_SETTINGS_LIST

List of settings related to RFLD and NFCLD

Table 235. List of settings related to RFLD and NFCLD

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
NFCLD_ONOFF_THRESHOLD (0x0597)	PN76_EXT_RF_DETECTION_HW->dwNFCLD_OnOff Threshold	0x0597	1431	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFCLD_ONOFF_MASKTIME (0x059B)	PN76_EXT_RF_DETECTION_HW->dwNFCLD_OnOffMask Time	0x059B	1435	4	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFCLD_ON_THRESHOLD (0x05BF)	PN76_EXT_RF_DETECT_INT_INPUT->wNFCLD_OnThreshold	0x05BF	1471	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFCLD_OFF_THRESHOLD (0x05C1)	PN76_EXT_RF_DETECT_INT_INPUT->wNFCLD_OffThreshold	0x05C1	1473	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
LPDET_ON_THRESHOLD (0x05C3)	PN76_EXT_RF_DETECT_INT_INPUT->wLPDET_OnThreshold	0x05C3	1475	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
NFCLD_RFLD_VALID (0x05C5)	PN76_EXT_RF_DETECT_INT_INPUT->wNFCLD_RFLD_Valid_Bit	0x05C5	1477	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.16.2 NFCLD_ONOFF_THRESHOLD (0x0597)

NFCLD_ON_OFF_THRESHOLD

Note:Value can be overwritten if writing tags A098, A09E or A01F (depends on feature controls: NFCLD interpolation, APC/RX enhancements).

Table 236. NFCLD_ONOFF_THRESHOLD (0x0597)

Function	bits	Values	Description
NFCLD_ON_OFF_THRESHOLD	[31:16]		RF Field OFF Threshold
	[15:0]		RF Field ON Threshold

8.18.2.16.3 NFCLD_ONOFF_MASKTIME (0x059B)

NFCLD_ON_OFF_MASKTIME

Table 237. NFCLD_ONOFF_MASKTIME (0x059B)

Function	bits	Values	Description
RFU	[31:20]	-	Reserved.
NFCLD_ON_OFF_MASKTIME	[19:15]	-	Masking time OFF = 10 µs
	[14:0]	-	Masking time ON = 300 µs

8.18.2.16.4 NFCLD_ON_THRESHOLD (0x05BF)

Table 238. NFCLD_ON_THRESHOLD (0x05BF)

Function	bits	Values	Description
RF Field ON Threshold	[15:0]		RF Field ON Threshold; Code resolution: (1/2048) Vpp @ Vrssi.

8.18.2.16.5 NFCLD_OFF_THRESHOLD (0x05C1)

Table 239. NFCLD_OFF_THRESHOLD (0x05C1)

Function	bits	Values	Description
RF Field OFF Threshold	[15:0]		RF Field ON Threshold; Code resolution: (1/2048) Vpp @ Vrssi.

8.18.2.16.6 LPDET_ON_THRESHOLD (0x05C3)

Table 240. LPDET_ON_THRESHOLD (0x05C3)

Function	bits	Values	Description
LPDET ON Threshold	[15:0]		Code Resolution (1/2048)Vpp at Vrssi 14 = 10 mVpp.

Note:value can be overwritten if writing tags A098 or A09E (depends on feature controls: APC/RX enhancements)

8.18.2.16.7 NFCLD_RFLD_VALID (0x05C5)

Table 241. NFCLD_RFLD_VALID (0x05C5)

Function	bits	Values	Description
RFU	[7:1]		Reserved.
NFCLD_RFLD_VALID	[0:0]		If this bit is set to 1 then the NFCLD Threshold and RFLD Threshold is a valid data and calibration wont be done gain till this bit is cleared and POR is issued.

8.18.2.17 ULPCD related settings

This section provides the ULPCD related configuration settings

8.18.2.17.1 EEPROM_ULPCD_LIST

List of ULPCD related configuration settings

Table 242. List of ULPCD related configuration settings

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
ULPCD_VDDPA_CTRL (0638)	PN76_ULPCD_CONFIG->Vddpa_Ctrl	0x0638	1592	2	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_TIMING_CTRL (063B)	PN76_ULPCD_CONFIG->Timing_Ctrl	0x063B	1595	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

Table 242. List of ULPCD related configuration settings...continued

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
ULPCD_VOLTAGE_CTRL (063D)	PN76_ULPCD_CONFIG->Voltage_Ctrl	0x063D	1597	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_RSSI_GUARD_TIME (0640)	PN76_ULPCD_SETTINGS->brssi_nsp	0x0640	1600	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_RSSI_SAMPLE_CFG (0641)	PN76_ULPCD_SETTINGS->brssi_no_samples	0x0641	1601	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_THRESH_LVL (0642)	PN76_ULPCD_SETTINGS->bthresh_lvl	0x0642	1602	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ULPCD_GPIO3 (0643)	PN76_ULPCD_SETTINGS->bpolarity	0x0643	1603	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.17.2 ULPCD_VDDPA_CTRL (0638)

VDDPA control during ULPCD

Table 243. ULPCD_VDDPA_CTRL (0638)

Function	bits	Values	Description
RFU	[15:9]		Reserved
VDDPA control	[8:3]		TXLDO output voltage during ULPCD polling. Value 0x00 --> 1V50, 0x01 --> 1V60.. with 0.10 voltage increment till value of 0x2A --> 5V70.
RFU	[2:0]		Reserved

8.18.2.17.3 ULPCD_TIMING_CTRL (063B)

ULPCD timing control

Table 244. ULPCD_TIMING_CTRL (063B)

Function	bits	Values	Description
RFON_GUARD_TIME	[7:4]		RFON guard time: (RFON_GUARD_TIME + 2) * LFO-Freq (380 kHz) Guard time: Time between RF-ON and first sampling of data
RFU	[3:0]		Reserved

8.18.2.17.4 ULPCD_VOLTAGE_CTRL (063D)

ULPCD voltage control

Table 245. ULPCD_VOLTAGE_CTRL (063D)

Function	bits	Values	Description
RFU	[7:2]		Reserved
TX_SUPPLY by VUP_TX	[1]	0x00	VUP externally supplied (2.8 V to 6 V)
		0x01	VUP supplied by PN7642 itself (pin VUP_TX connected to VBAT/VBATPWR)
RFU	[0]		Reserved

8.18.2.17.5 ULPCD_RSSI_GUARD_TIME (0640)

Number of RSSI Samples which are internally averaged.

Table 246. ULPCD_RSSI_GUARD_TIME (0640)

Function	bits	Values	Description
RFU	[7]		Reserved
ULPCD RSSI sampling guard time	[6:0]		This is the time between consecutive RSSI samples.

Note: Range - 0 - 127 micro seconds The GPADC RSSI acquisition time can be calculated with $T = (\text{ROUNDS} * (\text{brssi_nsp} + 30 + 3.5) + 11.5) * T_{clk\text{gpadc}}$

8.18.2.17.6 ULPCD_RSSI_SAMPLE_CFG (0641)

Number of RSSI Samples which are internally averaged

Table 247. ULPCD_RSSI_SAMPLE_CFG (0641)

Function	bits	Values	Description
RFU	[7:2]		Reserved
number of RSSI Samples	[1:0]	0x00	4 rounds
		0x01	8 rounds
		0x02	16 rounds
		0x03	32 rounds

8.18.2.17.7 ULPCD_THRESH_LVL (0642)

RSSI Threshold level.

Note: If the difference between the measured RSSI value and the reference (which is derived during calibration) is greater than the threshold, then a card is detected.

Table 248. ULPCD_THRESH_LVL (0642)

Function	bits	Values	Description
RFU	[7:5]		Reserved
RSSI Threshold level	[4:0]		0 - 31

8.18.2.17.8 ULPCD_GPIO3 (0643)

GPIO3 abort polarity configuration

Note: If PN7642 is using the ULPCD, GPIO3 cannot be used for any other purpose than aborting the ULPCD.

Table 249. ULPCD_GPIO3 (0643)

Function	bits	Values	Description
RFU	[7:1]		Reserved
RSSI Threshold level	[0]	0x00	low-level aborts ULPCD
		0x01	high-level aborts ULPCD

8.18.2.18 TEMPERATURE related settings

This section provides the configuration of Temperature warning settings.

8.18.2.18.1 EEPROM_TEMP_WARNING_LIST

List of settings for Temperature related cut-offs and notifications

Table 250. List of settings for Temperature related cut-offs and notifications

Configuration Parameter	Structure Param Reference	Address (Hex)	Address (Decimal)	Size (in bytes)	EEPROM_AREA
TEMP_WARNING (0x0648)	PN76_USER_SMU_CONFIG->bTempWarning	0x0648	1608	1	E_PN76_EEPROM_SECURE_LIB_CONFIG
ENABLE_GPIO0_ON_OVERTEMP (0x0649)	PN76_USER_SMU_CONFIG->bEnableGpio0OnOverTemp	0x0649	1609	1	E_PN76_EEPROM_SECURE_LIB_CONFIG

8.18.2.18.2 TEMP_WARNING (0x0648)

Table 251. TEMP_WARNING (0x0648)

Function	bits	Values	Description
PMU high threshold	[7:6]	0x00	Disabled
		0x01	114 °C
		0x02	125 °C
		0x03	130 °C
PMU low threshold	[5:4]	0x00	Disabled
		0x01	114 °C
		0x02	125 °C
		0x03	130 °C
CLIF high threshold	[3:2]	0x00	Disabled
		0x01	114 °C
		0x02	125 °C
		0x03	130 °C
CLIF low threshold	[1:0]	0x00	Disabled
		0x01	114 °C
		0x02	125 °C
		0x03	130 °C

8.18.2.18.3 ENABLE_GPIO0_ON_OVERTEMP (0x0649)

Enable over temperature indication through GPIO0

Table 252. ENABLE_GPIO0_ON_OVERTEMP (0x0649)

Function	bits	Values	Description
RFU	[7:1]		Reserved

Table 252. ENABLE_GPIO0_ON_OVERTEMP (0x0649)...continued

Function	bits	Values	Description
Gpio0 temp indication	[0]	0x00	temperature event indication through GPIO0 is disabled.
		0x01	temperature event indication through GPIO0 is enabled.

9 Limiting values

Table 253. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(GPIO_x)}$	input voltage on pin used as GPIO	-	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	2	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	2	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM) ^[1]	-2000	2000	V
		charge device model (CDM) ^[2]	-500	500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	150	°C

[1] According to ANSI/ESDA/JEDEC JS-001

[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

10 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

10.1 Static characteristics

Table 254. Supply voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD(VBAT_PWR)}	supply voltage on pin VBAT_PWR (DC-DC input pin)	DC-DC disabled	2.4	-	5.5	V
		DC-DC enabled	2.8	-	4.8	V
V _{DD(VUP_TX)}	supply voltage on pin VUP_TX (TX_LDO input pin)	Remark: If DC-DC is used, its output V _{DD(BOOST)} Min is limited to 3.1 V	2.4	-	6	V
V _{DD(VDDPA)}	supply voltage on pin VDDPA (input of the transmitter power amplifier)	-	1.5	-	5.7	V
V _{DD(VDDPA)}	supply voltage on pin VDDPA		2.4	-	4.7	V
V _{DD(VBAT)}	supply voltage on pin VBAT (analog and digital supply)	VBAT >= VDDIO	2.4	-	5.5	V
V _{DD(VDDIO)}	supply voltage on pin VDDIO (supply for host interface and GPIOs)	typical 1.8 V interface supply voltage	1.62	-	1.98	V
		typical 3.3 V interface supply voltage	2.4	-	3.6	V
V _{I(RXP)}	input voltage on pin RXP	-	-0.5	-	1.8	V
V _{I(RXN)}	input voltage on pin RXN	-	-0.5	-	1.8	V

Note: The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT.

Table 255. Current consumption in active mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD(VBAT)}	system supply		-	-	20	mA
I _{DD(VDDIO)}		This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed I _{DD(VDDIO)} max	-	-	30	mA
I _{DD(BOOST_IN)}	DC-DC boost supply	average input current	-	-	1.0	A
		peak input current (short peak)	-	-	1.7	A

Table 255. Current consumption in active mode...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD(VUP_TX)}	input supply for transmitter LDO	-	-	-	350	mA
I _{DD(VDDPA)}	RF power amplifier (transmitter) current	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and without TXLDO active	-	-	400	mA

Table 256. Current consumption during power-saving modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{OFF Plus Mode (VDDIO+VBAT)}	sum of supply current on pin VDDIO and VBAT in OFF Plus mode	25 °C ambient operating temperature	-	5	-	µA
I _{hard power down (VDDIO+VBAT)}	sum of supply current on pin VDDIO and VBAT in hard Power-down mode	25 °C ambient operating temperature	-	40	105	µA
I _{standby (VDDIO +VBAT)}	sum of supply current on pin VDDIO and VBAT in Standby mode	25 °C ambient operating temperature	-	45	110	µA
I _{suspend (VBAT)}	supply current on pin VBAT in suspend mode	25 °C ambient operating temperature	-	2.5	-	mA
I _{LPCD (VDDIO+VBAT)}	sum of supply current on pin VDDIO and VBAT in LPCD (Enhanced Low-Power Card Detection with highest sensitivity) mode, without DC-DC used	25 °C ambient operating temperature, VBAT supply voltage 3.6 V, antenna matching 50 R, 3x RF-on per second	-	250	-	µA

Table 257. Overcurrent detection function

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD(VUP_TX)}	current of overcurrent detection becoming active	-	450	550	650	mA

The Overcurrent detection function is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

Table 258. VEN pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	HIGH-level input voltage	V _{DD(VDDIO)} ≤ V _{DD(VBAT)}	0.7 × V _{DD(VDDIO)}	-	V _{DD(VDDIO)}	V
V _{IL}	LOW-level input voltage		0	-	0.3 × V _{DD(VDDIO)}	V
I _{IH}	HIGH-level input current	V _I = V _{DD(VBAT)}	-	-	1	µA
I _{IL}	LOW-level input current	V _I = 0 V	-1	-	-	µA

Table 258. VEN pin ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance		-	5	-	pF

Table 259. CLK1, CLK2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage	-	0.4	-	1.65	V
I_{IH}	HIGH-level input current	$V_I = 1.65$ V, no power saving, active mode	-	-	5	μ A
I_{IL}	LOW-level input current	$V_I = 0$ V, no power saving, active mode	-	-	1	μ A
δ	duty cycle	-	35	-	65	%
$C_{i(CLK1)}$	input capacitance on pin CLK1	$V_{DD} = 1.8$ V, $V_{DC} = 0.65$ V, $V_{AC} = 0.9$ V (p-p)	-	1	-	pF
$C_{i(CLK2)}$	input capacitance on pin CLK2	$V_{DD} = 1.8$ V, $V_{DC} = 0.65$ V, $V_{AC} = 0.9$ V (p-p)	-	1	-	pF

Table 260. IRQ1 pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$I_{OH} < 3$ mA	$V_{DD(VDDIO)} - 0.4$	-	$V_{DD(VDDIO)}$	V
V_{OL}	LOW-level output voltage	$I_{OL} < 3$ mA	0	-	0.4	V
I_{OH}	HIGH-level output current		-	-	3	mA
I_{OL}	LOW-level output current		-	-	3	mA
C_L	load capacitance		-	-	10	pF
t_f	fall time	$C_L = 12$ pF max	1	-	3	ns
t_r	rise time	$C_L = 12$ pF max	1	-	3	ns
R_{pd}	pull-down resistance		40	-	62	k Ω

Table 261. SPI SCK / I2C1_SCL, SPI NSS / I2C Adr Bit 0, SPI COTI / I2C Adr Bit 1 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.65 \times V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		- 0.5	-	$0.35 \times V_{DD(VDDIO)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DDIO}$	-	-	1	μ A
I_{IL}	LOW-level input current	$V_I = 0$ V	-	-	1	μ A
C_i	input capacitance		-	5	-	pF

Table 262. I2C1_SDA pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	I _{OH} < 3 mA	V _{DD(VDDIO)} - 0.4	-	V _{DD(VDDIO)}	V
V _{OL}	LOW-level output voltage	I _{OL} < 3 mA	0	-	0.4	V
I _{OH}	HIGH-level output current		-	-	3	mA
I _{OL}	LOW-level output current		-	-	3	mA
C _L	load capacitance		-	-	10	pF
t _f	fall time	C _L = 12 pF max	1	-	3	ns
t _r	rise time	C _L = 12 pF max	1	-	3	ns

Table 263. Mode selection, HOST_IF_SEL0, HOST_IF_SEL1, I2C2_IRQ, WAKEUP pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	HIGH-level input voltage	V _{DD(VDDIO)} ≤ V _{DD(VBAT)} ; 1.62 ≤ VDDIO ≤ 1.98 or 2.4 ≤ VDDIO ≤ 3.6	0.65 × VDDIO	-	VDDIO + 0.5 V	V
V _{IL}	LOW-level input voltage	V _{DD(VDDIO)} ≤ V _{DD(VBAT)} ; 1.62 ≤ VDDIO ≤ 1.98 or 2.4 ≤ VDDIO ≤ 3.6	- 0.5	-	0.35 × VDDIO	V
V _{OH}	HIGH-level output voltage	V _{DD(VDDIO)} = 3.3 V	VDDIO - 0.4	-	VDDIO	V
V _{OL}	LOW-level output voltage	V _{DD(VDDIO)} = 3.3 V	0	-	0.4	V
I _{OH}	HIGH-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
I _{OL}	LOW-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
I _{IH}	HIGH-level input current	V _{DD(VDDIO)} = 3.3 V	-	-	1	μA
I _{IL}	LOW-level input current	V _{DD(VDDIO)} = 3.3 V	-	-	1	μA
R _{PU}	Weak pullup resistor	-	40	50	62	kΩ
R _{PD}	Weak pulldown resistor	-	40	50	62	kΩ

Table 264. RXp, RXn pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{i(dyn)}	dynamic input voltage		-	-	1.8	V
C _i	input capacitance		-	1	-	pF
Z _i	input impedance from RXN, RXP pins to VMID	Reader, card, and P2P modes	-	-	15	kΩ

Table 265. TX1, TX2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	V _{DD(VDDPA)} = 5 V; with internal VDDPA LDO	-	V _{DD(VDDPA)} -150 mV	V _{DD(VDDPA)}	V
V _{OL}	LOW-level output voltage	V _{DD(VDDPA)} = 5 V; with internal VDDPA LDO	0	200	-	mV

Table 266. AUX1, AUX2, AUX3 pins (Debug output)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{AUX_OH}	HIGH-level output voltage	pin used as debug signal output	VDDIO - 0.4	-	VDDIO	V
V _{AUX_OL}	LOW-level output voltage	pin used as debug signal output	0	-	0.4	mV
I _{AUX_OH}	HIGH-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
I _{AUX_OL}	LOW-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
C _{O_LOAD}	output capacitance load of pin		-	5	10	pF

10.2 Timing characteristics

Table 267. Power supply connection timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{rise_vbat}	VBAT supply ramp	VEN = Low	0	-	2.75	V/μs
t _{vbat_vddio}	time between ramping up VBAT and ramping VDDIO	vddio condition: VBAT > 2.4 V, VDDIO supply (External), hpd_off_sel = x	0	500	1000	ms
t _{vbat_ven}	time between ramping VBAT and VEN	vddio condition: VBAT > 2.4 V, VDDIO supply (External), hpd_off_sel = x	0	500.5	1001	ms
t _{boot}	start-up time ^[1]	vddio condition: VBAT > 2.4 V, VDDIO supply (External), hpd_off_sel = x	3.2	3.27	dependent on configuration of XTAL_CHECK_DELAY (0013h) in EEPROM. This configuration can be used to optimize the boot time for crystals which allow a fast settling. This allows to optimize the average current consumption during LPCD.	ms

[1] (PN7220 ready to receive commands on the host interface). For ULPCD and LPCD, the PN7220 indicates the ability to receive commands from a host by raising an IDLE IRQ.

Table 268. Pulse length

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(VEN)}$	on Pin VEN, pulse width to reset the chip or exit from Hard power down State	-	5	-	-	ms

Table 269. I²C timing specification: Standard, Fast Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 400 pF	0	-	0.4	MHz
$t_{SU\ START}$	Set-up time for a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
$t_{HD\ START}$	hold time of a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 400 pF	1.3	-	-	μ s
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 400 pF	600	-	-	ns
$t_{SU\ DATA}$	DATA set-up time	Load capacitance < 400 pF	100	-	-	ns
$t_{HD\ DATA}$	DATA hold-up time	Load capacitance < 400 pF	0	-	900	ns
t_{rDA}	Rise time of SDA	Load capacitance < 400 pF	30	-	250	ns
t_{fDA}	Fall time of SDA	Load capacitance < 400 pF	30	-	250	ns

Table 270. I²C timing specification: High-Speed Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	3.4	MHz
$t_{SU\ START}$	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns

Table 270. I²C timing specification: High-Speed Mode...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{HD START}	hold time of a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t _{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	160	-	-	ns
t _{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	60	-	-	ns
t _{SU DATA}	DATA set-up time	Load capacitance < 100 pF	10	-	-	ns
t _{HD DATA}	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
t _{rDA}	Rise time of SDA	Load capacitance < 100 pF	10	-	80	ns
t _{fDA}	Fall time of SDA	Load capacitance < 100 pF	10	-	80	ns

Table 271. I²C timing specification: Fast + High-Speed-Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	1	MHz
t _{SU START}	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t _{HD START}	hold time of a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t _{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	500	-	-	ns
t _{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	260	-	-	ns
t _{SU DATA}	DATA set-up time	Load capacitance < 100 pF	50	-	-	ns

Table 271. I²C timing specification: Fast + High-Speed-Mode...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{HD DATA}	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
t _{rDA}	Rise time of SDA	Load capacitance < 100 pF	-	-	120	ns
t _{fDA}	Fall time of SDA	Load capacitance < 100 pF	-	-	120	ns

10.3 Clock input

Table 272. Crystal requirements for ISO/IEC14443 compliant operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{xtal}	crystal frequency	ISO/IEC compliancy	-	27.12	-	MHz
delta f _{xtal}	crystal frequency accuracy	for full RF operating range	-40	-	+40	ppm
ESR	equivalent series resistance	-	10	30	100	Ω
C _L	load capacitance	-	6	8	10	pF
t _{startup}	crystal startup time	-	-	-	1	ms
P _{xtal}	crystal power dissipation	-	-	-	100	μW

Table 273. Frequency requirements for a direct clock input (no crystal)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{clk}	clock frequency	ISO/IEC compliancy	-	24	-	MHz
			-	32	-	
			-	48	-	
delta f _{clk}	clock frequency accuracy	for full RF operating range	-40	-	+40	ppm
φ _n	phase noise	input phase noise floor at 100 kHz offset	-	- 150	-145	dBc/Hz
φ _n	phase noise	input phase noise floor at 1 MHz offset	-	- 152	-149	dBc/Hz
V _i	Input voltage boundary	sinus signal	0	-	1.8	V
V _{i(p-p)}	peak-to-peak Input voltage	sinus signal	0.4	-	1.8	V
V _{i(clk)}	clock input voltage	square signal	0	-	1.8 +/-10 %	V

10.4 DPC characteristics

Table 274. Dynamic power control characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Minimum hysteresis configured in EEPROM DPC_HYSTERESIS (address 079h)	depends on application target current	ApplicationTargetCurrent × 0.0609 + 2 mA	-	-	mA
	Max target current configured in EEPROM DPC_TARGET_CURRENT (077h)	hysteresis as configured in DPC_HYSTERESIS (address 079h)		-	350-Hysteresis	mA

10.5 EEPROM characteristics

Table 275. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N _{endu(W)}	write endurance	at ambient temperature T _a = +25 °C	100	-	-	Kcycle
t _{ret}	retention time	at ambient temperature T _a = +25 °C	25	-	-	year

10.6 Thermal characteristics

Table 276. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA	-40	25	85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V	-40	25	105	°C

Table 277. Thermal characteristics VFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64	53	K/W
R _{th(j-c)}	thermal resistance from junction to case	-	22	K/W

Table 278. Junction Temperature

Symbol	Parameter	Conditions	Min	Max	Unit
T _{J_max}	maximum junction temperature	-	-	125	°C

Table 279. Thermal Shutdown Temperature

Symbol	Parameter	Conditions	Typ	Unit
T _{shutdown}	shutdown of chip due to high temperature detected by temp sensor	-	125	°C

11 Package outline

11.1 VFBGA64 package

Table 280. Package outline VFBGA64 (SOT1307-2)

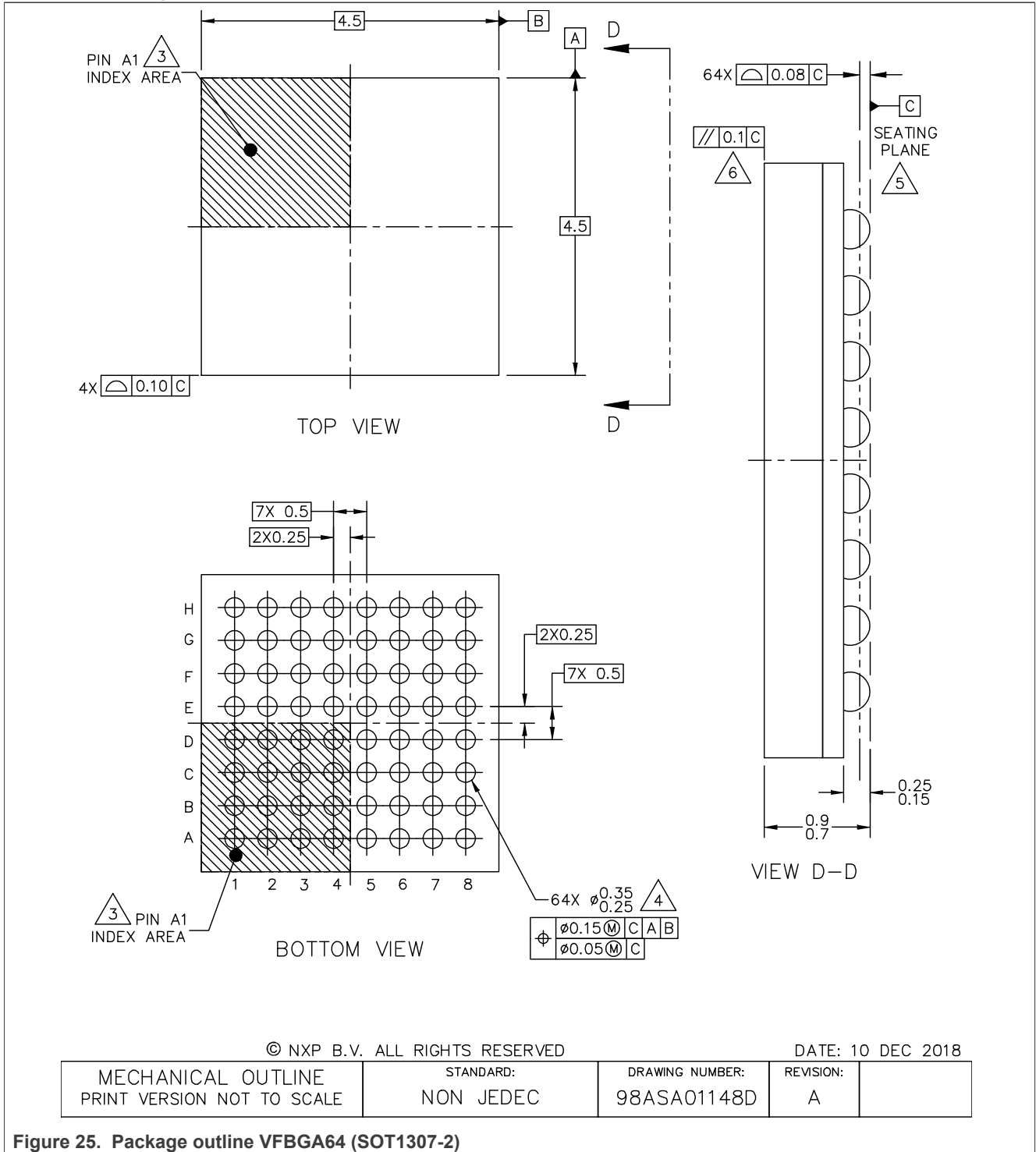


Figure 25. Package outline VFBGA64 (SOT1307-2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

© NXP B.V. ALL RIGHTS RESERVED

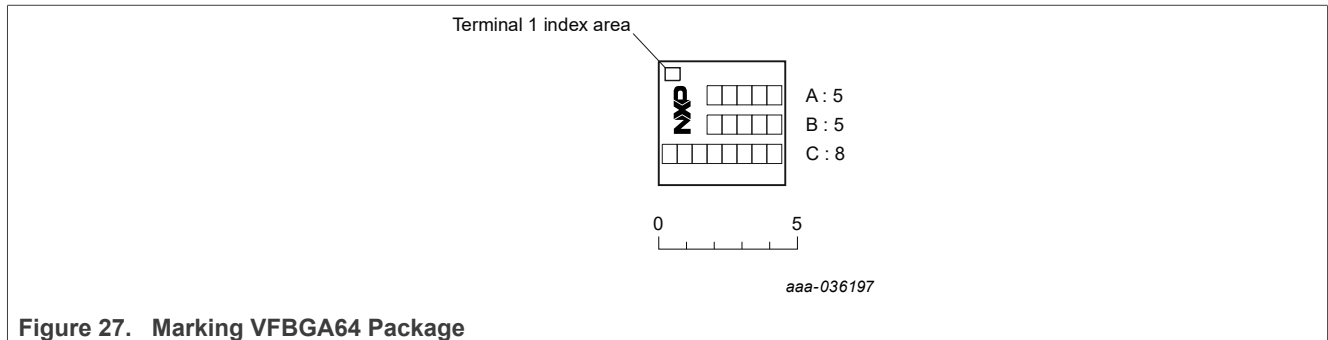
DATE: 10 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01148D	REVISION: A	
--	------------------------	--------------------------------	----------------	--

Figure 26. Package outline note VFBGA64 (SOT1307-2)

12 Package marking

12.1 Package marking drawing VFBGA64



Line A: 4 characters; "7220" (FWx.x)

Line B: 5 characters; contains the diffusion batch identifier (DB ID) and assembly sequence identifier (AS ID)

Line C: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level ("X" = engineering samples, " " = released product)

13 Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

14 Abbreviations

Table 281. Abbreviations

Acronym	Description
AA	audio accelerator
ADC	analog-to-digital converter
AGC	automatic gain control
AHB	advanced high-performance bus
AHB-Lite	advanced high-performance bus (single-controller implementation)
AHB bus	advanced high-performance bus
APB	advanced peripheral bus
API	application programming interface
ARC	adaptive receiver control
Arm	Advanced RISC Machine
AWC	adaptive waveshape control
BBA	baseband amplifier
BOD	brownout detection
CITO	controller input target output (previously master input slave output)
CLIF	contactless interface
COTI	controller output target input (previously master output slave input)
CPU	central processing unit
CRC	cyclic redundancy check
CTR	current transfer ratio
CTS	clear to send
DAC	digital-to-analog converter
DC-DC	switch-mode voltage regulator which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN7220 integrates a step-up/boost converter
DDR	double data rate
DMA	direct memory access
DPC	dynamic power control
ECC	elliptic curve cryptography
EEPROM	electrically erasable programmable read-only memory
EMC	electromagnetic compatibility
EMD	electromagnetic disturbance
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macro
EOF	end-of-frame
Fm+	Fast-mode Plus
FSM	finite state machine

Table 281. Abbreviations...continued

Acronym	Description
GND	Ground
GPIO	general-purpose input output
HID	human interface device
HPD	hard power down
HW	hardware
IC	Integrated Circuit
IIR	infinite impulse response
IrDA	Infrared Data Association
IAP	In-Application Programming
ISP	In-System Programming
I/O	input/output
I/Q	in-phase/quadrature-phase
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout regulator
LPCD	low-power card detection
LPUART	Low-Power Universal Asynchronous Receiver / Transmitter
LSB	least significant bit
LSByte	least significant byte
MISO	SPI interface controller in target out
MSL	moisture sensitivity level
MOSI	SPI interface controller out target In
NFC	near-field communication
NRZ	non-return-to-zero
NSS	SPI interface active-low target-select signal
NTS	not target select (previously not slave select)
NVIC	nested vectored interrupt controller
OS	operating system
OTP	one time programmable
PCB	printed-circuit board
PC	personal computer
PCD	power card detection
PICC	proximity inductive coupling card
PLL	phase-locked loop
PMU	power management unit
PWM	pulse width modulation
RAM	random-access memory

Table 281. Abbreviations...continued

Acronym	Description
RF	radio frequency
RNG	random number generator
ROM	read-only memory
RSA	Rivest, Shamir, and Adleman public key cryptosystem
RSSI	receiver signal strength indicator
RTOS	real-time operating system
RTS	request to send
SCK	SPI interface serial clock
SCL	I ² C interface serial clock
SDA	serial data
SMPS	switch mode power supply
SPI	serial peripheral interface
SRAM	static random-access memory
SWD	serial wire debug
TFT	display technology: thin-film transistor-display
TX	transmit
UART	universal asynchronous receiver transmitter
UID	Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards.
ULPCD	ultra low-power card detection
USB	universal serial bus
VREF	voltage reference

15 Revision history

Table 282. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PN7220 v.3.0	20230705	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

NFC controller with NCI interface supporting EMV and NFC Forum applications

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. - NXP B.V. is not an operating company and it does not distribute or sell products.

16.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

FeliCa — is a trademark of Sony Corporation.

ICODE and I-CODE — are trademarks of NXP B.V.

I2C-bus — logo is a trademark of NXP B.V.

MIFARE Classic — is a trademark of NXP B.V.

MIFARE Plus — is a trademark of NXP B.V.

Tables

Tab. 1.	Quick reference data	5	Tab. 33.	CLIF_RXM_FREQ (0x59) register bit description	58
Tab. 2.	Ordering information	6	Tab. 34.	INTERPOLATED_RSSI_REG (0x5C) register bit description	59
Tab. 3.	Pin description VF6GA64	9	Tab. 35.	TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D) register bit description	59
Tab. 4.	Supply voltage range configuration	24	Tab. 36.	CLIF_SS_TX1_RTRANS0 (0x80) register bit description	59
Tab. 5.	Supply voltage range	25	Tab. 37.	CLIF_SS_TX1_RTRANS1 (0x81) register bit description	59
Tab. 6.	DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage	31	Tab. 38.	CLIF_SS_TX1_RTRANS2 (0x82) register bit description	60
Tab. 7.	ARC_RM_A106 EEPROM configuration bit description	35	Tab. 39.	CLIF_SS_TX1_RTRANS3 (0x83) register bit description	60
Tab. 8.	ARC_RM_A106 EEPROM configuration bit description	36	Tab. 40.	CLIF_SS_TX2_RTRANS0 (0x84) register bit description	60
Tab. 9.	Low-Power Card Detection: relevant EEPROM configuration	38	Tab. 41.	CLIF_SS_TX2_RTRANS1 (0x85) register bit description	60
Tab. 10.	Low-Power Card Detection: relevant EEPROM configuration	39	Tab. 42.	CLIF_SS_TX2_RTRANS2 (0x86) register bit description	61
Tab. 11.	Antenna register configuration	41	Tab. 43.	CLIF_SS_TX2_RTRANS3 (0x87) register bit description	61
Tab. 12.	Antenna EEPROM configuration	41	Tab. 44.	CLIF_SS_TX1_FTRANS0 (0x88) register bit description	61
Tab. 13.	DEBUG SIGNALS	42	Tab. 45.	CLIF_SS_TX1_FTRANS1 (0x89) register bit description	61
Tab. 14.	TRIGGER SIGNALS	44	Tab. 46.	CLIF_SS_TX1_FTRANS2 (0x8A) register bit description	62
Tab. 15.	List of CLIF registers	44	Tab. 47.	CLIF_SS_TX1_FTRANS3 (0x8B) register bit description	62
Tab. 16.	SYSTEM_CONFIG (0x00) register bit description	46	Tab. 48.	CLIF_SS_TX2_FTRANS0 (0x8C) register bit description	62
Tab. 17.	CLIF_RX_STATUS (0x05) register bit description	46	Tab. 49.	CLIF_SS_TX2_FTRANS1 (0x8D) register bit description	62
Tab. 18.	CLIF_RX_STATUS_ERROR (0x06) register bit description	47	Tab. 50.	CLIF_SS_TX2_FTRANS2 (0x8E) register bit description	63
Tab. 19.	CLIF_STATUS (0x07) register bit description	49	Tab. 51.	CLIF_SS_TX2_FTRANS3 (0x8F) register bit description	63
Tab. 20.	CLIF_CRC_TX_CONFIG (0x12) register bit description	51	Tab. 52.	List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks	63
Tab. 21.	CLIF_SS_TX1_RMCFG (0x16) register bit description	52	Tab. 53.	DCDC_PWR_CONFIG (0x0000)	64
Tab. 22.	CLIF_SIGPRO_RM_TECH (0x22) register bit description	52	Tab. 54.	DCDC_CONFIG (0x0001)	65
Tab. 23.	CLIF_SIGPRO_IIR_CONFIG0 (0x2A) register bit description	53	Tab. 55.	TXLDO_CONFIG (0x0002)	65
Tab. 24.	CLIF_DGRM_BBA (0x2D) register bit description	53	Tab. 56.	TXLDO_VDDPA_CONFIG (0x0006)	65
Tab. 25.	CLIF_DGRM_RSSI (0x30) register bit description	54	Tab. 57.	TXLDO_VDDPA_MAX_RDR (0x0007)	65
Tab. 26.	CLIF_CRC_RX_CONFIG (0x31) register bit description	55	Tab. 58.	TXLDO_VDDPA_MAX_CARD (0x0008)	66
Tab. 27.	CLIF_RX_WAIT (0x32) register bit description	56	Tab. 59.	BOOST_DEFAULT_VOLTAGE (0x0009)	66
Tab. 28.	CLIF_SS_TX1_CMCFG (0x3B) register bit description	56	Tab. 60.	XTAL_CONFIG (0x000F)	66
Tab. 29.	CLIF_TIMER1_CONFIG (0x3F) register bit description	56	Tab. 61.	XTAL_TIMEOUT (0x0010)	66
Tab. 30.	CLIF_TIMER1_RELOAD (0x40) register bit description	58	Tab. 62.	CLK_INPUT_FREQ (0x0011)	66
Tab. 31.	TXLDO_VDDPA_CONFIG (0x54) register bit description	58	Tab. 63.	XTAL_CHECK_DELAY (0x0012)	67
Tab. 32.	TXLDO_VOUT_CURR (0x56) register bit description	58	Tab. 64.	VDDPA_DISCHARGE (0x050D)	67
			Tab. 65.	RESIDUAL_AMPL_LEVEL_A106 (0x0014)	68
			Tab. 66.	EDGE_TYPE_A106 (0x0015)	68
			Tab. 67.	EDGE_STYLE_A106 (0x0016)	69
			Tab. 68.	EDGE_LENGTH_A106 (0x0017)	69

NFC controller with NCI interface supporting EMV and NFC Forum applications

Tab. 69.	RESIDUAL_AMPL_LEVEL_A212 (0x0018)	69	Tab. 123.	EDGE_STYLE_V100_26 (0x003E)	94
Tab. 70.	EDGE_TYPE_A212 (0x0019)	70	Tab. 124.	EDGE_LENGTH_V100_26 (0x003F)	95
Tab. 71.	EDGE_STYLE_A212 (0x001A)	70	Tab. 125.	RESIDUAL_AMPL_LEVEL_V100_53 (0x0040)	95
Tab. 72.	EDGE_LENGTH_A212 (0x001B)	71	Tab. 126.	EDGE_TYPE_V100_53 (0x0041)	95
Tab. 73.	RESIDUAL_AMPL_LEVEL_A424 (0x001C)	71	Tab. 127.	EDGE_STYLE_V100_53 (0x0042)	96
Tab. 74.	EDGE_TYPE_A424 (0x001D)	71	Tab. 128.	EDGE_LENGTH_V100_53 (0x0043)	97
Tab. 75.	EDGE_STYLE_A424 (0x001E)	72	Tab. 129.	RESIDUAL_AMPL_LEVEL_V100_106 (0x0044)	97
Tab. 76.	EDGE_LENGTH_A424 (0x001F)	73	Tab. 130.	EDGE_TYPE_V100_106 (0x0045)	97
Tab. 77.	RESIDUAL_AMPL_LEVEL_A848 (0x0020)	73	Tab. 131.	EDGE_STYLE_V100_106 (0x0046)	98
Tab. 78.	EDGE_TYPE_A848 (0x0021)	73	Tab. 132.	EDGE_LENGTH_V100_106 (0x0047)	98
Tab. 79.	EDGE_STYLE_A848 (0x0022)	74	Tab. 133.	RESIDUAL_AMPL_LEVEL_V100_212 (0x0048)	99
Tab. 80.	EDGE_LENGTH_A848 (0x0023)	75	Tab. 134.	EDGE_TYPE_V100_212 (0x0049)	99
Tab. 81.	RESIDUAL_AMPL_LEVEL_B106 (0x0024)	75	Tab. 135.	EDGE_STYLE_V100_212 (0x004A)	100
Tab. 82.	EDGE_TYPE_B106 (0x0025)	75	Tab. 136.	EDGE_LENGTH_V100_212 (0x004B)	100
Tab. 83.	EDGE_STYLE_B106 (0x0026)	76	Tab. 137.	RESIDUAL_AMPL_LEVEL_180003M3_ TARI9P44 (0x0060)	101
Tab. 84.	EDGE_LENGTH_B106 (0x0027)	76	Tab. 138.	EDGE_TYPE_180003M3_TARI9P44 (0x0061)	101
Tab. 85.	RESIDUAL_AMPL_LEVEL_B212 (0x0028)	77	Tab. 139.	EDGE_STYLE_180003M3_TARI9P44 (0x0062)	102
Tab. 86.	EDGE_TYPE_B212 (0x0029)	77	Tab. 140.	EDGE_LENGTH_180003M3_TARI9P44 (0x0063)	102
Tab. 87.	EDGE_STYLE_B212 (0x002A)	78	Tab. 141.	RESIDUAL_AMPL_LEVEL_180003M3_ TARI18P88 (0x005C)	102
Tab. 88.	EDGE_LENGTH_B212 (0x002B)	78	Tab. 142.	EDGE_TYPE_180003M3_TARI18P88 (0x005D)	103
Tab. 89.	RESIDUAL_AMPL_LEVEL_B424 (0x002C)	79	Tab. 143.	EDGE_STYLE_180003M3_TARI18P88 (0x005E)	103
Tab. 90.	EDGE_TYPE_B424 (0x002D)	79	Tab. 144.	EDGE_LENGTH_180003M3_TARI18P88 (0x005F)	104
Tab. 91.	EDGE_STYLE_B424 (0x002E)	80	Tab. 145.	RESIDUAL_AMPL_LEVEL_B_PRIME106 (0x0064)	104
Tab. 92.	EDGE_LENGTH_B424 (0x002F)	80	Tab. 146.	EDGE_TYPE_B_PRIME106 (0x0065)	105
Tab. 93.	RESIDUAL_AMPL_LEVEL_B848 (0x0030)	80	Tab. 147.	EDGE_STYLE_B_PRIME106 (0x0066)	105
Tab. 94.	EDGE_TYPE_B848 (0x0031)	81	Tab. 148.	EDGE_LENGTH_B_PRIME106 (0x0067)	106
Tab. 95.	EDGE_STYLE_B848 (0x0032)	81	Tab. 149.	DPC_CONFIG (0x0068)	106
Tab. 96.	EDGE_LENGTH_B848 (0x0033)	82	Tab. 150.	DPC_TARGET_CURRENT (0x0069)	107
Tab. 97.	RESIDUAL_AMPL_LEVEL_F212 (0x0034)	82	Tab. 151.	DPC_HYSTERESIS_LOADING (0x006B)	107
Tab. 98.	EDGE_TYPE_F212 (0x0035)	82	Tab. 152.	DPC_ALGO_INTERVAL (0x006C)	107
Tab. 99.	EDGE_STYLE_F212 (0x0036)	83	Tab. 153.	DPC_HYSTERESIS_UNLOADING (0x006E)	108
Tab. 100.	EDGE_LENGTH_F212 (0x0037)	84	Tab. 154.	DPC_TXLDOVDDPALow (0x006F)	108
Tab. 101.	RESIDUAL_AMPL_LEVEL_F424 (0x0038)	84	Tab. 155.	DPC_TXGSN (0x0070)	108
Tab. 102.	EDGE_TYPE_F424 (0x0039)	84	Tab. 156.	DPC_RDON_CONTROL (0x0071)	108
Tab. 103.	EDGE_STYLE_F424 (0x003A)	85	Tab. 157.	DPC_InitialRDOOn_RFOOn (0x0072)	108
Tab. 104.	EDGE_LENGTH_F424 (0x003B)	86	Tab. 158.	DPC_TXLDO_MAX_DROPOUT (0x0073)	108
Tab. 105.	RESIDUAL_AMPL_LEVEL_V10_26 (0x004C)	86	Tab. 159.	DPC_GUARD_TIME (0x0079)	109
Tab. 106.	EDGE_TYPE_V10_26 (0x004D)	86	Tab. 160.	DPC_ENABLE_DURING_FDT (0x007A)	109
Tab. 107.	EDGE_STYLE_V10_26 (0x004E)	87	Tab. 161.	DPC_GUARD_TIME_AFTER_RX (0x007B)	109
Tab. 108.	EDGE_LENGTH_V10_26 (0x004F)	87	Tab. 162.	DPC lookup table entries	109
Tab. 109.	RESIDUAL_AMPL_LEVEL_V10_53 (0x0050)	88	Tab. 163.	ARC_SETTINGS_BARCCONFIG (0x0129) ..	111
Tab. 110.	EDGE_TYPE_V10_53 (0x0051)	88	Tab. 164.	ARC_SETTINGS_WARCVDDPA (0x012B) ...	112
Tab. 111.	EDGE_STYLE_V10_53 (0x0052)	89	Tab. 165.	ARC_SETTINGS_WRMARCA_106 (0x0130)	112
Tab. 112.	EDGE_LENGTH_V10_53 (0x0053)	89			
Tab. 113.	RESIDUAL_AMPL_LEVEL_V10_106 (0x0054)	90			
Tab. 114.	EDGE_TYPE_V10_106 (0x0055)	90			
Tab. 115.	EDGE_STYLE_V10_106 (0x0056)	91			
Tab. 116.	EDGE_LENGTH_V10_106 (0x0057)	91			
Tab. 117.	RESIDUAL_AMPL_LEVEL_V10_212 (0x0058)	91			
Tab. 118.	EDGE_TYPE_V10_212 (0x0059)	92			
Tab. 119.	EDGE_STYLE_V10_212 (0x005A)	92			
Tab. 120.	EDGE_LENGTH_V10_212 (0x005B)	93			
Tab. 121.	RESIDUAL_AMPL_LEVEL_V100_26 (0x003C)	93			
Tab. 122.	EDGE_TYPE_V100_26 (0x003D)	93			

NFC controller with NCI interface supporting EMV and NFC Forum applications

Tab. 166. ARC_SETTINGS_TABLE for other technologies	114	Tab. 214. RESIDUAL_AMPL_LEVEL_ACTIVE_F424 (0X0516)	145
Tab. 167. ARC_RM_A106_FDT (0x051B)	117	Tab. 215. EDGE_TYPE_ACTIVE_F424 (0X0517)	145
Tab. 168. List of RSSI settings for card emulation only	118	Tab. 216. EDGE_STYLE_ACTIVE_F424 (0X0518)	146
Tab. 169. RSSI_TIMER (0x020C)	119	Tab. 217. EDGE_LENGTH_ACTIVE_F424 (0X0519) ...	147
Tab. 170. RSSI_TIMER_FIRST_PERIOD (0x020E)	119	Tab. 218. List of Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings.	147
Tab. 171. RSSI_CTRL_00_AB (0x0210)	119	Tab. 219. LMA_RSSI_INTERPOLATED_RSSI (0x0530)	147
Tab. 172. RSSI_NB_ENTRIES_AB (0x0211)	119	Tab. 220. LMA_RSSI_FIELD_STRENGTH (0x0532) ...	148
Tab. 173. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B	119	Tab. 221. List of Settings related TX_SHAPING configuration.	148
Tab. 174. RSSI_CTRL_00_F (0x0272)	121	Tab. 222. TX_SHAPING_CONIFG (0x058C)	149
Tab. 175. RSSI_NB_ENTRIES_F (0x0273)	121	Tab. 223. TX_INV_RM (0x058D)	149
Tab. 176. RSSI_THRESHOLD_PHASE_TABLE for Type-F	121	Tab. 224. TX_CLK_MODE_1 (0x058E)	149
Tab. 177. TX_PARAM_ENTRY_00_ID (0x02D4)	123	Tab. 225. TX_CLK_MODE_2 (0x058F)	149
Tab. 178. List of Autocoll configuration settings	130	Tab. 226. GSN_MOD_RM (0x0590)	150
Tab. 179. RF_DEBOUNCE_TIMEOUT (0x03C4)	130	Tab. 227. GSN_CW_RM (0x0591)	150
Tab. 180. SENSE_RES (0x03C5)	131	Tab. 228. GSP_RM (0x0592)	150
Tab. 181. NFC_ID1 (0x03C7)	131	Tab. 229. TX_FRCZERO_THR (0x0593)	150
Tab. 182. SEL_RES (0x03CA)	131	Tab. 230. SIGNAL_SCALING_CONFIG (0x0594)	151
Tab. 183. FELICA_POLLRES (0x03CB)	131	Tab. 231. TX_PH_SHIFT_DIV10 (0x0595)	151
Tab. 184. RANDOM_UID_ENABLE (0x03DD)	132	Tab. 232. TX_PH_SHIFT_MOD10 (0x0596)	151
Tab. 185. List of LPCD related configuration settings	132	Tab. 233. APP_ENCRY_DECRY_KEY_DERIV_MSG (0x0550)	151
Tab. 186. LPCD_AVG_SAMPLES (0x03DE)	132	Tab. 234. APP_ENCRY_KEY_DERIV_MSG_ ASYMM_KEY (0x568)	151
Tab. 187. LPCD_RSSI_TARGET (0x03E0)	133	Tab. 235. List of settings related to RFLD and NFCLD .	152
Tab. 188. LPCD_RSSI_HYST (0x03E2)	133	Tab. 236. NFCLD_ONOFF_THRESHOLD (0x0597)	152
Tab. 189. LPCD_CONFIG (0x03E3)	133	Tab. 237. NFCLD_ONOFF_MASKTIME (0x059B)	152
Tab. 190. LPCD_THRESHOLD (0x03E6)	134	Tab. 238. NFCLD_ON_THRESHOLD (0x05BF)	153
Tab. 191. LPCD_WAIT_RX_SETTLE (0x03F7)	135	Tab. 239. NFCLD_OFF_THRESHOLD (0x05C1)	153
Tab. 192. LPCD_VDDPA (0x03FB)	135	Tab. 240. LPDET_ON_THRESHOLD (0x05C3)	153
Tab. 193. LPCD_CHECK_PERIOD (0x03FC)	135	Tab. 241. NFCLD_RFLD_VALID (0x05C5)	153
Tab. 194. CORRECTION_ENTRY_TABLE	135	Tab. 242. List of ULPCD related configuration settings	153
Tab. 195. TX_SHAPING_RTRANS_FTRANS_1 (0x0481)	137	Tab. 243. ULPCD_VDDPA_CTRL (0638)	154
Tab. 196. TX_SHAPING_RTRANS_FTRANS_2 (0x4A1)	138	Tab. 244. ULPCD_TIMING_CTRL (063B)	154
Tab. 197. TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)	138	Tab. 245. ULPCD_VOLTAGE_CTRL (063D)	154
Tab. 198. TX_SHAPING_RTRANS_FTRANS_1 (0x04E1)	139	Tab. 246. ULPCD_RSSI_GUARD_TIME (0640)	155
Tab. 199. List of NOV configuration parameters	140	Tab. 247. ULPCD_RSSI_SAMPLE_CFG (0641)	155
Tab. 200. NOV_CFG_CAL (0x0501)	140	Tab. 248. ULPCD_THRESH_LVL (0642)	155
Tab. 201. NOV_CAL_VAL1 (0x0502)	140	Tab. 249. ULPCD_GPIO3 (0643)	155
Tab. 202. NOV_CAL_VAL2 (0x0503)	140	Tab. 250. List of settings for Temperature related cut-offs and notifications	156
Tab. 203. NOV_CAL_THRESHOLD (0x0504)	141	Tab. 251. TEMP_WARNING (0x0648)	156
Tab. 204. NOV_CAL_OFFSET1 (0x0505)	141	Tab. 252. ENABLE_GPIO0_ON_OVERTEMP (0x0649)	156
Tab. 205. NOV_CAL_OFFSET2 (0x0509)	141	Tab. 253. Limiting values	158
Tab. 206. RESIDUAL_AMPL_LEVEL_ACTIVE_A106 (0X050E)	142	Tab. 254. Supply voltage	159
Tab. 207. EDGE_TYPE_ACTIVE_A106 (0X050F)	142	Tab. 255. Current consumption in active mode	159
Tab. 208. EDGE_STYLE_ACTIVE_A106 (0X0510)	143	Tab. 256. Current consumption during power-saving modes	160
Tab. 209. EDGE_LENGTH_ACTIVE_A106 (0X0511) ...	143	Tab. 257. Overcurrent detection function	160
Tab. 210. RESIDUAL_AMPL_LEVEL_ACTIVE_F212 (0X0512)	143	Tab. 258. VEN pin	160
Tab. 211. EDGE_TYPE_ACTIVE_F212 (0X0513)	144	Tab. 259. CLK1, CLK2 pins	161
Tab. 212. EDGE_STYLE_ACTIVE_F212 (0X0514)	144	Tab. 260. IRQ1 pin	161
Tab. 213. EDGE_LENGTH_ACTIVE_F212 (0X0515) ...	145		

Tab. 261. SPI SCK / I2C1_SCL, SPI NSS / I2C Adr Bit 0 , SPI COTI / I2C Adr Bit 1 pins	161	Tab. 272. Crystal requirements for ISO/IEC14443 compliant operation	166
Tab. 262. I2C1_ SDA pin	162	Tab. 273. Frequency requirements for a direct clock input (no crystal)	166
Tab. 263. Mode selection, HOST_IF_SEL0, HOST_IF_SEL1, I2C2_IRQ, WAKEUP pins	162	Tab. 274. Dynamic power control characteristics	167
Tab. 264. RXp, RXn pins	162	Tab. 275. EEPROM characteristics	167
Tab. 265. TX1, TX2 pins	163	Tab. 276. Operating conditions	167
Tab. 266. AUX1, AUX2, AUX3 pins (Debug output)	163	Tab. 277. Thermal characteristics VFBGA64 package ..	167
Tab. 267. Power supply connection timing	163	Tab. 278. Junction Temperature	168
Tab. 268. Pulse length	164	Tab. 279. Thermal Shutdown Temperature	168
Tab. 269. I2C timing specification: Standard, Fast Mode	164	Tab. 280. Package outline VFBGA64 (SOT1307-2)	169
Tab. 270. I2C timing specification: High-Speed Mode ...	164	Tab. 281. Abbreviations	173
Tab. 271. I2C timing specification: Fast + High-Speed-Mode	165	Tab. 282. Revision history	176

Figures

Fig. 1.	System connections	7	Fig. 16.	System overview: DPC, AWC, and ARC	29
Fig. 2.	Pin configuration for VFBGA64	9	Fig. 17.	System overview: DPC, AWC, and ARC	30
Fig. 3.	Byte and bit order examples	16	Fig. 18.	Waveshaping transitions (example falling edge)	32
Fig. 4.	Blocking capacitors	19	Fig. 19.	One linear transition (example falling edge)	33
Fig. 5.	Transmitter supply	20	Fig. 20.	Two linear transitions (example falling edge)	33
Fig. 6.	Direct transmitter supply	20	Fig. 21.	Three linear transitions (example falling edge)	34
Fig. 7.	Transmitter supply by DC-DC	21	Fig. 22.	Push-Pull driver configuration	40
Fig. 8.	DC-DC active	21	Fig. 23.	Push-Push driver configuration	40
Fig. 9.	DC-DC bypassed (in DCDC_PWR_CONFIG)	22	Fig. 24.	Receiver block diagram	42
Fig. 10.	No DC-DC used	22	Fig. 25.	Package outline VFBGA64 (SOT1307-2)	169
Fig. 11.	No DC-DC used	23	Fig. 26.	Package outline note VFBGA64 (SOT1307-2)	170
Fig. 12.	No DC-DC used - no TX_LDO	23	Fig. 27.	Marking VFBGA64 Package	171
Fig. 13.	Clocking by crystal	25			
Fig. 14.	System overview: DPC, AWC, and ARC	28			
Fig. 15.	System overview: DPC, AWC, and ARC	29			

Contents

1	General description	1	8.12	Adaptive receiver control (ARC)	34
2	Features and benefits	2	8.13	Energy-saving card detection	37
2.1	RF functionality	2	8.13.1	Low-power card detection (LPCD)	37
2.1.1	ISO/IEC14443-A	2	8.14	RF-level detection	39
2.1.2	ISO/IEC 14443-B	2	8.15	Antenna connection	40
2.1.3	FeliCa	2	8.16	RF debug signals	41
2.1.4	Tag type reading	2	8.17	Polling loop	44
2.1.5	MIFARE card reading	2	8.18	System settings and configuration	44
2.1.6	ISO/IEC 15693	2	8.18.1	CLIF Register description	44
2.1.7	NFC Forum compliancy	2	8.18.1.1	List of CLIF registers	44
2.1.8	EMVCo compliancy	2	8.18.1.2	SYSTEM_CONFIG (0x00)	45
2.1.9	Host interface	2	8.18.1.3	CLIF_RX_STATUS (0x05)	46
2.2	Transmitter	3	8.18.1.4	CLIF_RX_STATUS_ERROR (0x06)	47
2.3	Receiver	3	8.18.1.5	CLIF_STATUS (0x07)	49
2.4	Integrated polling loop	3	8.18.1.6	CLIF_CRC_TX_CONFIG (0x12)	51
2.5	Integrated DC-DC	3	8.18.1.7	CLIF_SS_TX1_RMCFG (0x16)	52
2.6	RF debugging support	3	8.18.1.8	CLIF_SIGPRO_RM_TECH (0x22)	52
3	Applications	4	8.18.1.9	CLIF_SIGPRO_IIR_CONFIG0 (0x2A)	53
4	Quick reference data	5	8.18.1.10	CLIF_DGRM_BBA (0x2D)	53
5	Ordering information	6	8.18.1.11	CLIF_DGRM_RSSI (0x30)	54
6	Block diagram	7	8.18.1.12	CLIF_CRC_RX_CONFIG (0x31)	55
7	Pinning information	9	8.18.1.13	CLIF_RX_WAIT (0x32)	56
7.1	Pin description VFBGA64	9	8.18.1.14	CLIF_SS_TX1_CMCFG (0x3B)	56
8	Functional description	13	8.18.1.15	CLIF_TIMER1_CONFIG (0x3F)	56
8.1	Functional overview	13	8.18.1.16	CLIF_TIMER1_RELOAD (0x40)	58
8.2	NCI interface	15	8.18.1.17	TXLDO_VDDPA_CONFIG (0x54)	58
8.3	Byte and bit order	15	8.18.1.18	TXLDO_VOUT_CURR (0x56)	58
8.4	Initial calibration	17	8.18.1.19	CLIF_RXM_FREQ (0x59)	58
8.5	System power states	17	8.18.1.20	INTERPOLATED_RSSI_REG (0x5C)	59
8.6	Power supply	18	8.18.1.21	TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D)	59
8.6.1	System power supply overview	18	8.18.1.22	CLIF_SS_TX1_RTRANS0 (0x80)	59
8.6.2	Connecting blocking capacitors	19	8.18.1.23	CLIF_SS_TX1_RTRANS1 (0x81)	59
8.6.3	Transmitter power supply	19	8.18.1.24	CLIF_SS_TX1_RTRANS2 (0x82)	60
8.6.3.1	TX_LDO transmitter supply	19	8.18.1.25	CLIF_SS_TX1_RTRANS3 (0x83)	60
8.6.3.2	Direct transmitter supply	20	8.18.1.26	CLIF_SS_TX2_RTRANS0 (0x84)	60
8.6.3.3	DC-DC (boost) supply	21	8.18.1.27	CLIF_SS_TX2_RTRANS1 (0x85)	60
8.6.3.4	Configuration example 1: TX_LDO transmitter supply - DC-DC active	21	8.18.1.28	CLIF_SS_TX2_RTRANS2 (0x86)	61
8.6.3.5	Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed	21	8.18.1.29	CLIF_SS_TX2_RTRANS3 (0x87)	61
8.6.3.6	Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC	22	8.18.1.30	CLIF_SS_TX1_FTRANS0 (0x88)	61
8.6.3.7	Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC	22	8.18.1.31	CLIF_SS_TX1_FTRANS1 (0x89)	61
8.6.3.8	Configuration example 5: TX_LDO not used - no DC-DC	23	8.18.1.32	CLIF_SS_TX1_FTRANS2 (0x8A)	62
8.6.3.9	Supply voltage range for transmitter supply configuration examples	24	8.18.1.33	CLIF_SS_TX1_FTRANS3 (0x8B)	62
8.7	Clock generation	25	8.18.1.34	CLIF_SS_TX2_FTRANS0 (0x8C)	62
8.8	External interfaces	25	8.18.1.35	CLIF_SS_TX2_FTRANS1 (0x8D)	62
8.9	Transmitter overcurrent and temperature protection	25	8.18.1.36	CLIF_SS_TX2_FTRANS2 (0x8E)	63
8.10	Dynamic power control (DPC)	26	8.18.1.37	CLIF_SS_TX2_FTRANS3 (0x8F)	63
8.10.1	DPC algorithm	30	8.18.2	EEPROM configuration description	63
8.11	Adaptive waveshaping control (AWC)	31	8.18.2.1	EEPROM configuration for power, TXLDO, XTAL and Clocks	63
			8.18.2.2	RM_TX_SHAPING - TX wave shaping for passive reader mode	67
			8.18.2.3	DPC Settings	106
			8.18.2.4	ARC Settings for passive reader modes	111
			8.18.2.5	RSSI configuration parameters (applicable for card emulation)	118

8.18.2.6	RSSI APC algorithm table output settings TX_PARAM_ENTRY_TABLE. Applicable only for card emulation.	123
8.18.2.7	Autocol configuration settings.	130
8.18.2.8	LPCD related configuration parameters	132
8.18.2.9	CORRECTION_ENTRY_TABLE TX wave shaping for proprietary correction configuration	135
8.18.2.10	TX_SHAPING_RTRANS_FTRANS_TABLE TX wave shaping for proprietary correction configuration for rising edge and falling edges. (0x0481)	137
8.18.2.11	TX driver NOV (non-overlap) settings configuration.	139
8.18.2.12	Active reader mode TX wave shaping configuration	141
8.18.2.13	Settings related to NFCLD and RFLD. For Card Mode Dynamic LMA settings(0x011D) ..	147
8.18.2.14	Global TX_SHAPING configuration	148
8.18.2.15	Settings for encryption/decryption of keys storage for Symmetric and Asymmetric private keys	151
8.18.2.16	RFLD and NFCLD settings	151
8.18.2.17	ULPCD related settings	153
8.18.2.18	TEMPERATURE related settings	156
9	Limiting values	158
10	Characteristics	159
10.1	Static characteristics	159
10.2	Timing characteristics	163
10.3	Clock input	166
10.4	DPC characteristics	167
10.5	EEPROM characteristics	167
10.6	Thermal characteristics	167
11	Package outline	169
11.1	VFPGA64 package	169
12	Package marking	171
12.1	Package marking drawing VFPGA64	171
13	Handling information	172
14	Abbreviations	173
15	Revision history	176
16	Legal information	177

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.
