National Semiconductor

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LM2747
Synchronous Buck Controller with Pre-bias Startup, and Optional Clock Synchronization

General Description

The LM2747 is a high-speed synchronous buck regulator controller with a feedback voltage accuracy of ±1%. It can provide simple down conversion to output voltages as low as 0.6V. Though the control section of the IC is rated for 3 to 6V, the driver section is designed to accept input supply rails as high as 14V. The use of adaptive non-overlapping MOSFET gate drivers helps avoid potential shoot-through problems while maintaining high efficiency. The IC is designed for the more cost-effective option of driving only N-channel MOSFETs in both the high-side and low-side positions. It senses the low-side switch voltage drop for providing a simple, adjustable current limit.

The LM2747 features a fixed-frequency voltage-mode PWM control architecture which is adjustable from 50 kHz to 1 MHz with one external resistor. In addition, the LM2747 also allows the switching frequency to be synchronized to an external clock signal over the range of 250 kHz to 1 MHz. This wide range of switching frequency gives the power supply designer the flexibility to make better tradeoffs between component size, cost and efficiency.

Features include the ability to startup with a pre-biased load on the output, soft-start, input undervoltage lockout (UVLO) and Power Good (based on both undervoltage and overvoltage detection). In addition, the shutdown pin of the IC can be used for providing startup delay, and the soft-start pin can be used for implementing precise tracking, for the purpose of sequencing with respect to an external rail.

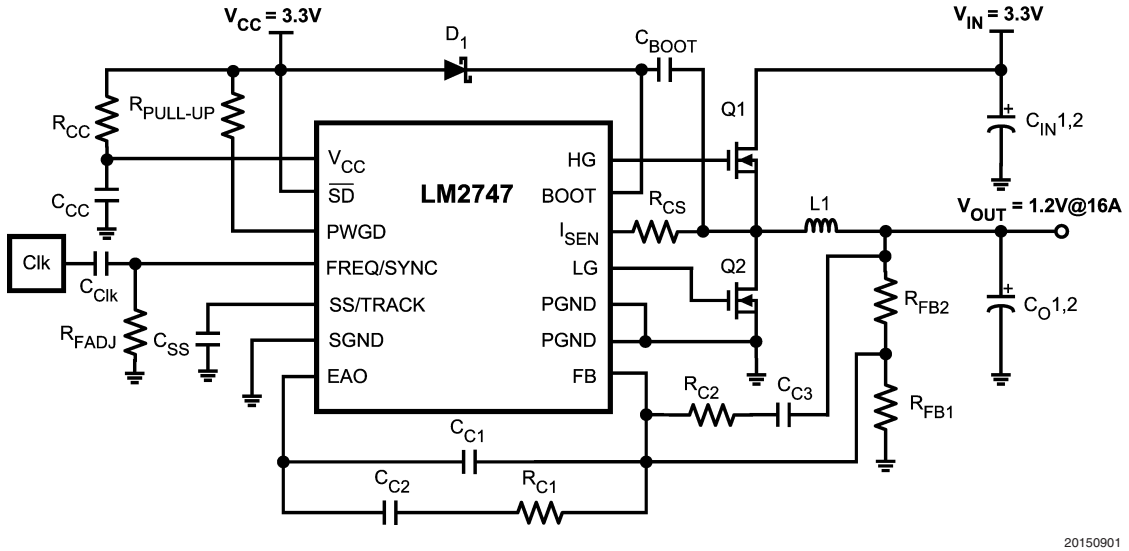
Features

- ±1% feedback voltage accuracy over temperature
- Switching frequency from 50 kHz to 1 MHz
- Switching frequency synchronize range 250 kHz to 1 MHz
- Startup with a pre-biased output load
- Power stage input voltage from 1V to 14V
- Control stage input voltage from 3V to 6V
- Output voltage adjustable down to 0.6V
- Power Good flag and shutdown
- Output overvoltage and undervoltage detection
- Low-side adjustable current sensing
- Adjustable soft-start
- Tracking and sequencing with shutdown and soft start pins
- TSSOP-14 package

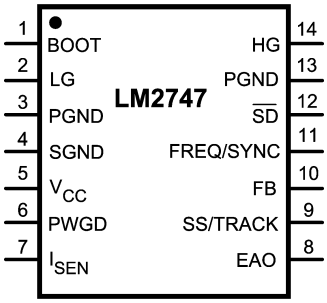
Applications

- Down Conversion from 3.3V
- Cable Modem, DSL and ADSL
- Laser Jet and Ink Jet Printers
- Low Voltage Power Modules
- DSP, ASIC, Core and I/O

Typical Application



Connection Diagram



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14-Lead Plastic TSSOP
θ_{JA} = 155˚C/W
NS Package Number MTC14

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2747MTC	TSSOP-14	MTC14	94 Units on Rail
LM2747MTCX			2500 Units on Tape and Reel

Pin Description

BOOT (Pin 1) - Bootstrap pin. This is the supply rail for the high-side gate driver. When the high-side MOSFET turns on, the voltage on this pin should be at least one gate threshold above the regulator input voltage V_{IN} to properly turn on the MOSFET. See MOSFET Gate Drivers in the Application Information section for more details on how to select MOSFETs.

LG (Pin 2) - Low-gate drive pin. This is the gate drive for the low-side N-channel MOSFET. This signal is interlocked with the high-side gate drive HG (Pin 14), so as to avoid shoot-through.

PGND (Pins 3, 13) - Power ground. This is also the ground for the low-side MOSFET driver. Both the pins must be connected together on the PCB and form a ground plane, which is usually also the system ground.

SGND (Pin 4) - Signal ground. It should be connected appropriately to the ground plane with due regard to good layout practices in switching power regulator circuits.

V_{CC} (Pin 5) Supply rail for the control sections of the IC.

PWGD (Pin 6) - Power Good pin. This is an open drain output, which is typically meant to be connected to V_{CC} or any other low voltage source through a pull-up resistor. Choose the pull-up resistor so that the current going into this pin is kept below 1 mA. A recommended value for the pull-up resistor is 100 kΩ for most applications. The voltage on this pin is thus pulled low under output undervoltage or overvoltage fault conditions and also under input UVLO.

I_{SEN} (Pin 7) - Current limit threshold setting pin. This sources a fixed 40 µA current. A resistor of appropriate value should be connected between this pin and the drain of the low-side MOSFET (switch node). The minimum value for this resistor is 1 kΩ.

EAO (Pin 8) - Output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp signal to determine the duty cycle. This pin is necessary for compensating the control loop.

SS/TRACK (Pin 9) - Soft-start and tracking pin. This pin is internally connected to the non-inverting input of the error amplifier during soft-start, and in fact any time the SS/TRACK pin voltage happens to be below the internal reference voltage. For the basic soft-start function, a capacitor of minimum value 1 nF is connected from this pin to ground. To track the rising ramp of another power supply's output, connect a resistor divider from the output of that supply to this pin as described in Application Information.

FB (Pin 10) - Feedback pin. This is the inverting input of the error amplifier, which is used for sensing the output voltage and compensating the control loop.

FREQ/SYNC (Pin 11) - Frequency adjust pin. The switching frequency is set by connecting a resistor of suitable value between this pin and ground. Some typical values (rounded up to the nearest standard values) are 150 kΩ for 200 kHz, 100 kΩ for 300 kHz, 51.1 kΩ for 500 kHz, 18.7 kΩ for 1 MHz. This pin is also used to synchronize to an external clock within the range of 250kHz to 1MHz.

$\overline{SD}$ (Pin 12) - IC shutdown pin. Pull this pin to V_{CC} to ensure the IC is enabled. Connect to ground to disable the IC. Under shutdown, both high-side and low-side drives are off. This pin also features a precision threshold for power supply sequencing purposes, as well as a low threshold to ensure minimal quiescent current.

HG (Pin 14) - High-gate drive pin. This is the gate drive for the high-side N-channel MOSFET. This signal is interlocked with LG (Pin 2) to avoid shoot-through.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}	-0.3 to 7V
BOOT Voltage	-0.3 to 18V
I_{SEN}	-0.3 to 14V
FREQ/SYNC Voltage	-0.5 to V_{CC} + 0.3V
All other pins	-0.3 to V_{CC} + 0.3V
Junction Temperature	150˚C
Storage Temperature	–65˚C to 150˚C
Soldering Information	
Lead Temperature (soldering, 10sec)	260˚C
Infrared or Convection (20sec)	235˚C
ESD Rating (Note 3)	2kV

Operating Ratings

Supply Voltage Range, V_{CC} (Note 2)	3V to 6V
BOOT Voltage Range	1V to 17V
Junction Temperature Range (T_J)	–40˚C to +125˚C
Thermal Resistance (θ_{JA})	155˚C/W

Electrical Characteristics

V_{CC} = 3.3V unless otherwise indicated. Typicals and limits appearing in plain type apply for T_A= T_J= 25˚C. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	FB Pin Voltage	V_{CC} = 3V to 6V	**0.594**	0.6	**0.606**	V
V_{ON}	UVLO Thresholds	V_{CC} Rising V_{CC} Falling		2.79 2.42		V
I_{Q_VCC}	Operating V_{CC} Current	V_{CC} = 3.3V, V_{SD} = 3.3V f_{SW} = 600 kHz	**1.1**	1.7	**2.3**	mA
		V_{CC} = 5V, V_{SD} = 3.3V f_{SW} = 600 kHz	**1.3**	2	**2.6**	
	Shutdown V_{CC} Current	V_{CC} = 3.3V, V_{SD} = 0V		1	**3**	µA
t_{PWGD1}	PWGD Pin Response Time	V_{FB} Rising		10		µs
t_{PWGD2}	PWGD Pin Response Time	V_{FB} Falling		10		µs
I_{SS-ON}	SS Pin Source Current	V_{SS} = 0V	**7**	10	**14**	µA
I_{SS-OC}	SS Pin Sink Current During Over Current	V_{SS} = 2.0V		90		µA
I_{SEN-TH}	I_{SEN} Pin Source Current Trip Point		**25**	40	**55**	µA
I_{FB}	FB Pin Current	Sourcing		20		nA
ERROR AMPLIFIER						
GBW	Error Amplifier Unity Gain Bandwidth			9		MHz
G	Error Amplifier DC Gain			118		dB
SR	Error Amplifier Slew Rate			2		V/µs
I_{EAO}	EAO Pin Current Sourcing and Sinking Capability			14 16		mA
V_{EAO}	Error Amplifier Output Voltage	Minimum		1		V
		Maximum		2.2		V

Electrical Characteristics (Continued)

V_{CC} = 3.3V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J = 25^{\circ}C$. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GATE DRIVE						
$I_{Q\text{-}BOOT}$	BOOT Pin Quiescent Current	V_{BOOT} = 12V, V_{SD} = 0		18	**90**	µA
R_{HG_UP}	High-Side MOSFET Driver Pull-Up ON resistance	V_{BOOT} = 5V @ 350 mA Sourcing		2.7		Ω
R_{HG_DN}	High-Side MOSFET Driver Pull-Down ON resistance	350 mA Sinking		0.8		Ω
R_{LG_UP}	Low-Side MOSFET Driver Pull-Up ON resistance	V_{BOOT} = 5V @ 350 mA Sourcing		2.7		Ω
R_{LG_DN}	Low-Side MOSFET Driver Pull-Down ON resistance	350 mA Sinking		0.8		Ω
OSCILLATOR						
f_{SW}	PWM Frequency	R_{FADJ} = 750 kΩ		50		kHz
		R_{FADJ} = 100 kΩ		300		
		R_{FADJ} = 42.2 kΩ	**475**	600	**725**	
		R_{FADJ} = 18.7 kΩ		1000		
	External Synchronizing Signal Frequency	Voltage Swing = 0V to V_{CC}	250		1000	
$SYNC_L$	Synchronization Signal Low Threshold	f_{SW} = 250 kHz to 1 MHz			1	V
$SYNC_H$	Synchronization Signal High Threshold	f_{SW} = 250 kHz to 1 MHz	2			V
D_{MAX}	Max High-Side Duty Cycle	f_{SW} = 300 kHz f_{SW} = 600 kHz f_{SW} = 1 MHz		86 78 67		%
LOGIC INPUTS AND OUTPUTS						
$V_{STBY\text{-}IH}$	Standby High Trip Point	V_{FB} = 0.575V, V_{BOOT} = 3.3V V_{SD} Rising			**1.1**	V
$V_{STBY\text{-}IL}$	Standby Low Trip Point	V_{FB} = 0.575V, V_{BOOT} = 3.3V V_{SD} Falling	**0.232**			V
$V_{SD\text{-}IH}$	$\overline{SD}$ Pin Logic High Trip Point	V_{SD} Rising			**1.3**	V
$V_{SD\text{-}IL}$	$\overline{SD}$ Pin Logic Low Trip Point	V_{SD} Falling	**0.8**			V
$V_{PWGD\text{-}TH\text{-}LO}$	PWGD Pin Trip Points	V_{FB} Falling	**0.408**	0.434	**0.457**	V
$V_{PWGD\text{-}TH\text{-}HI}$	PWGD Pin Trip Points	V_{FB} Rising	**0.677**	0.710	**0.742**	V
$V_{PWGD\text{-}HYS}$	PWGD Hysteresis	V_{FB} Falling V_{FB} Rising		60 90		mV

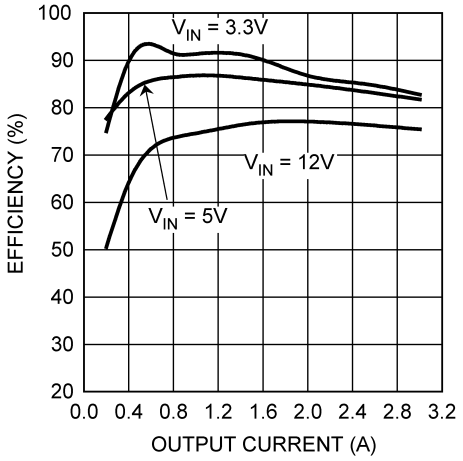
Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. **Operating ratings** indicate conditions for which the device operates correctly. **Operating Ratings** do not imply guaranteed performance limits.

Note 2: The power MOSFETs can run on a separate 1V to 14V rail (Input voltage, V_{IN}). Practical lower limit of V_{IN} depends on selection of the external MOSFET. See the MOSFET GATE DRIVERS section under Application Information for further details.

Note 3: ESD using the human body model which is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Typical Performance Characteristics

Efficiency (V_{OUT} = 1.2V)
V_{CC} = 3.3V, f_{SW} = 1 MHz



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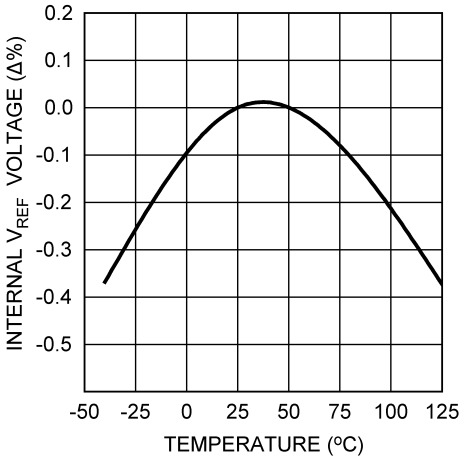
Internal Reference Voltage vs Temperature



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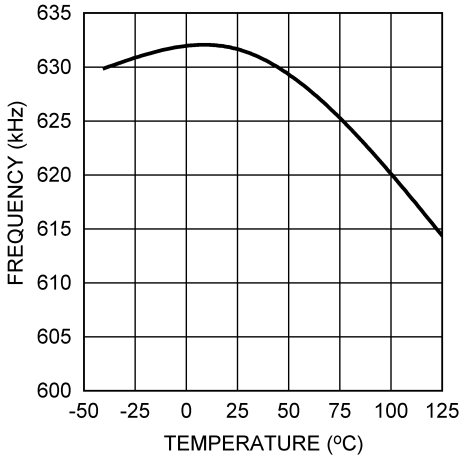
Frequency vs Temperature



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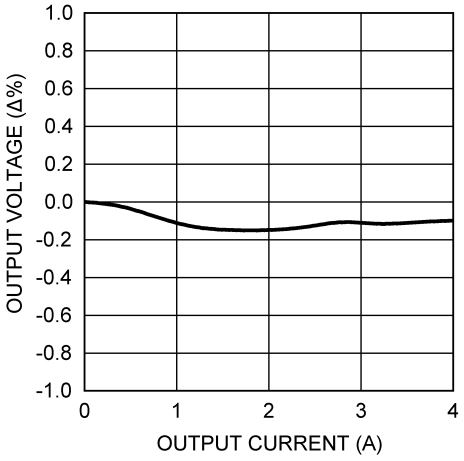
Output Voltage vs Output Current



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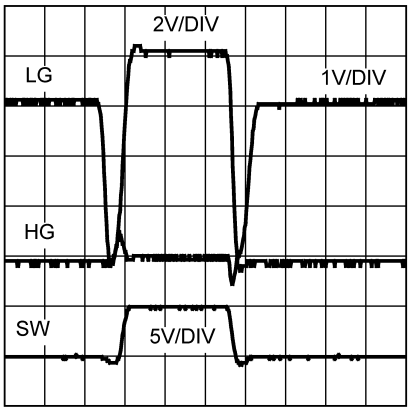
Switch Waveforms
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 3A, C_{SS} = 12 nF, f_{SW} = 1 MHz



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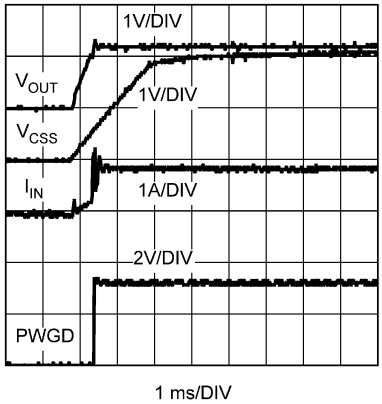
Start-Up (Full-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 3A, C_{SS} = 12 nF, f_{SW} = 1 MHz



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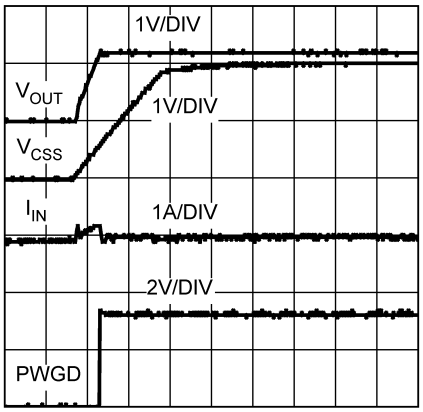
Typical Performance Characteristics (Continued)

Start-Up (No-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
C_{SS} = 12 nF, f_{SW} = 1 MHz



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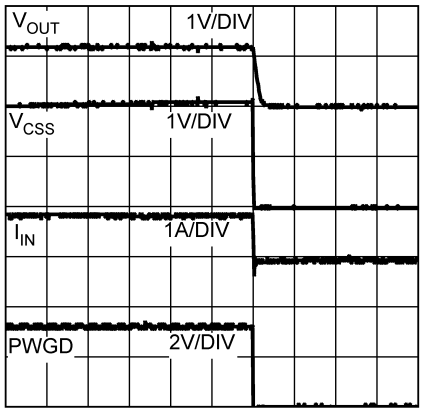
Shutdown (Full-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 3A, C_{SS} = 12 nF, f_{SW} = 1 MHz



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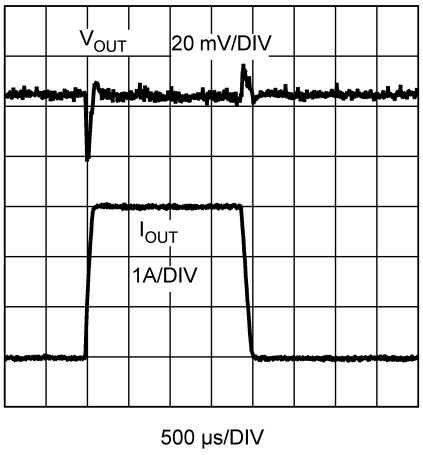
Load Transient Response
V_{CC} = 3.3V, V_{IN} = 14V, V_{OUT} = 1.2V
f_{SW} = 1 MHz



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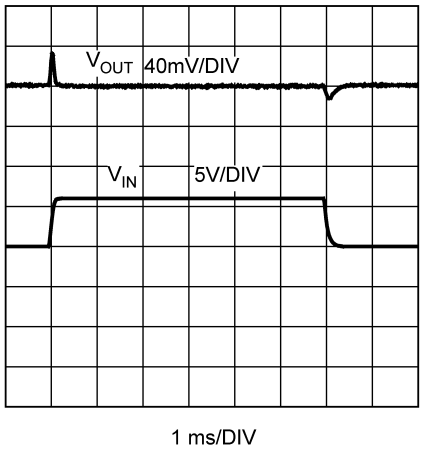
Line Transient Response (V_{IN} = 3V to 9V)
V_{CC} = 3.3V, V_{OUT} = 1.2V
I_{OUT} = 2A, f_{SW} = 1 MHz



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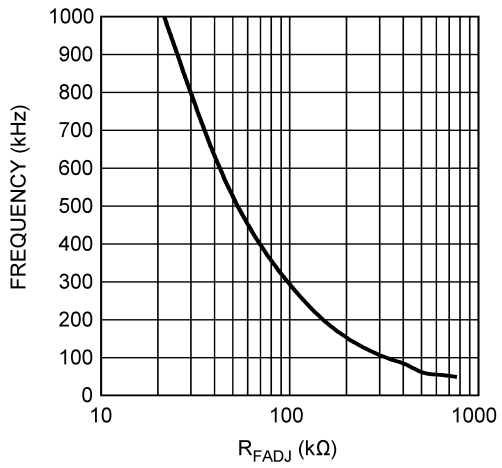
Frequency vs. Frequency Adjust Resistor



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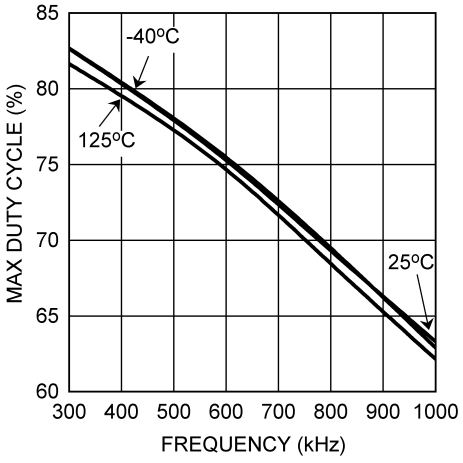
Maximum Duty Cycle vs Frequency
V_{CC} = 3.3V



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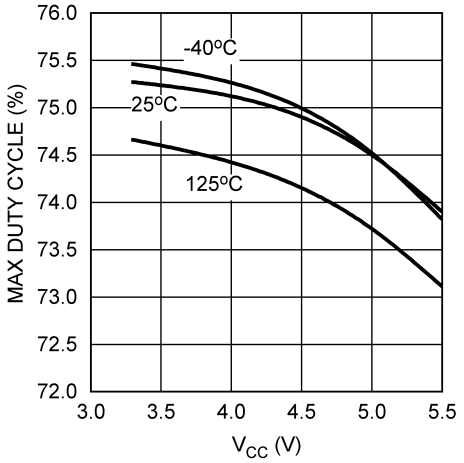
Typical Performance Characteristics (Continued)

Maximum Duty Cycle vs V_{CC}
f_{SW} = 600 kHz



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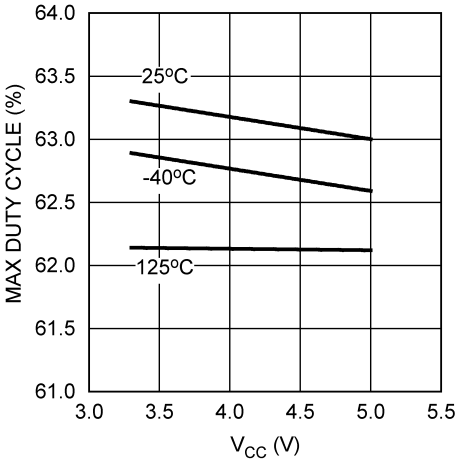
Maximum Duty Cycle vs V_{CC}
f_{SW} = 1 MHz



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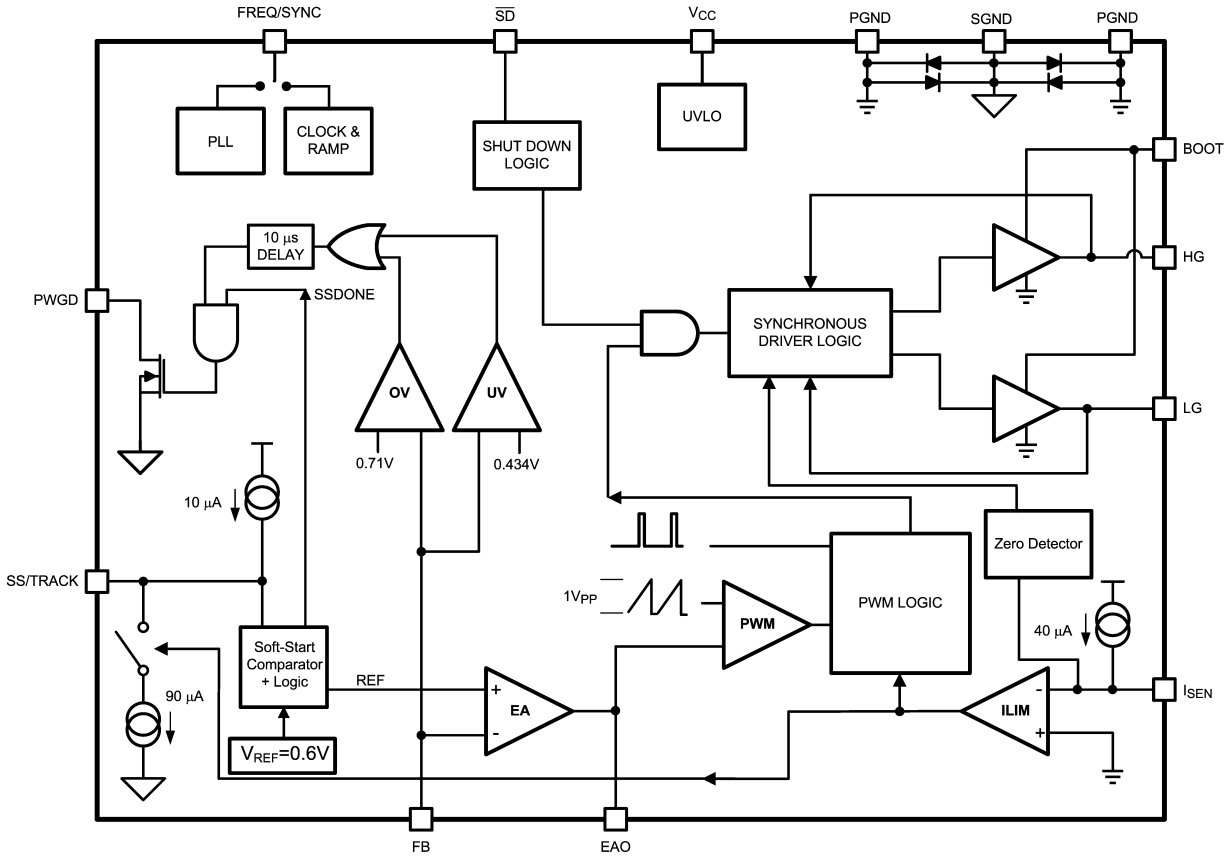
Block Diagram



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Application Information

The LM2747 is a voltage-mode, high-speed synchronous buck regulator with a PWM control scheme. It is designed for use in set-top boxes, thin clients, DSL/Cable modems, and other applications that require high efficiency buck converters. It has output shutdown ($\overline{SD}$), input undervoltage lock-out (UVLO) mode and power good (PWGD) flag (based on overvoltage and undervoltage detection). The overvoltage and undervoltage signals are OR-gated to drive the power good signal and provide a logic signal to the system if the output voltage goes out of regulation. Current limit is achieved by sensing the voltage V_{DS} across the low side MOSFET. The LM2747 is also able to start-up with the output pre-biased with a load and allows for the switching frequency to be synchronized with an external clock source.

START UP/SOFT-START

When V_{CC} exceeds 2.79V and the shutdown pin ($\overline{SD}$) sees a logic high, the soft-start period begins. Then an internal, fixed 10 µA source begins charging the soft-start capacitor. During soft-start the voltage on the soft-start capacitor C_{SS} is connected internally to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the LM2747 reference voltage of 0.6V. At this point the reference voltage takes over at the non-inverting error amplifier input. The capacitance of C_{SS} determines the length of the soft-start period, and can be approximated by:

$$C_{SS} = \frac{t_{SS}}{60}$$

Where C_{SS} is in µF and t_{SS} is in ms.

During soft start the Power Good flag is forced low and it is released when the FB pin voltage reaches 70% of 0.6V. At this point the chip enters normal operation mode, and the output overvoltage and undervoltage monitoring starts.

SETTING THE OUTPUT VOLTAGE

The LM2747 regulates the output voltage by controlling the duty cycle of the high side and low side MOSFETs (see Typical Application Circuit).The equation governing output voltage is:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB1}} V_{FB}$$

$$(V_{FB} = 0.6V)$$

SETTING THE SWITCHING FREQUENCY

During fixed-frequency mode of operation the PWM frequency is adjustable between 50 kHz and 1 MHz and is set by an external resistor, R_{FADJ}, between the FREQ/SYNC pin and ground. The resistance needed for a desired frequency

Application Information (Continued)

is approximated by the curve FREQUENCY vs. FREQUENCY ADJUST RESISTOR in the Typical Performance Characteristics section.

When it is desired to synchronize the switching frequency with an external clock source, the LM2747 has the unique ability to synchronize from this external source within the range of 250 kHz to 1 MHz. The external clock signal should be AC coupled to the FREQ/SYNC pin as shown below in *Figure 1*, where the R_{FADJ} is chosen so that the fixed frequency is approximately within ±30% of the external synchronizing clock frequency. An internal protection diode clamps the low level of the synchronizing signal to approximately -0.5V. The internal clock synchrinizes to the rising edge of the external clock.

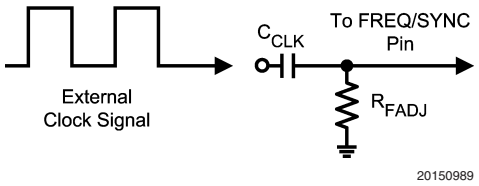


FIGURE 1. AC Coupled Clock

It is recommended to choose an AC coupling capacitance in the range of 50 pF to 100 pF. Exceeding the recommended capacitance may inject excessive energy through the internal clamping diode structure present on the FREQ/SYNC pin.

The typical trip level of the synchronization pin is 1.5V. To ensure proper synchronization and to avoid damaging the IC, the peak-to-peak value (amplitude) should be between 2.5V and V_{CC}. The minimum width of this pulse must be greater than 100 ns, and it's maximum width must be 100ns less than the period of the switching cycle.

The external clock synchronization process begins once the LM2747 is enabled and an external clock signal is detected. During the external clock synchronization process the internal clock initially switches at approximately 1.5 MHz and decreases until it has matched the external clock's frequency. The lock-in period is approximately 30 µs if the external clock is switching at 1 MHz, and about 100 µs if the external clock is at 200 kHz. When there is no clock signal present, the LM2747 enters into fixed-frequency mode and begins switching at the frequency set by the R_{FADJ} resistor. If the external clock signal is removed after frequency synchronization, the LM2747 will enter fixed-frequency mode within two clock cycles. If the external clock is removed within the 30 µs lock-in period, the LM2747 will re-enter fixed-frequency mode within two internal clock cycles after the lock-in period.

OUTPUT PRE-BIAS STARTUP

If there is a pre-biased load on the output of the LM2747 during startup, the IC will disable switching of the low-side MOSFET and monitor the SW node voltage during the off-time of the high-side MOSFET. There is no load current sensing while in pre-bias mode because the low-side MOSFET never turns on. The IC will remain in this pre-bias mode until it sees the SW node stays below 0V during the entire high-side MOSFET's off-time. Once it is determined that the SW node remained below 0V during the high-side off-time, the low-side MOSFET begins switching during the next switching cycle. *Figure 2* shows the SW node, HG, and LG signals during pre-bias startup. The pre-biased output voltage should not exceed V_{CC} + V_{GS} of the external High-Side MOSFET to ensure that the High-Side MOSFET will be able to switch during startup.

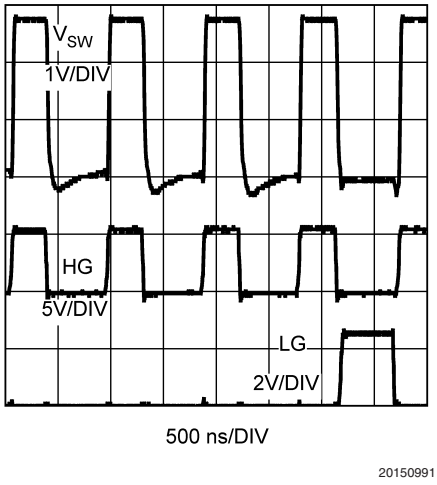


FIGURE 2. Output Pre-Bias Mode Waveforms

TRACKING A VOLTAGE LEVEL

The LM2747 can track the output of a master power supply during soft-start by connecting a resistor divider to the SS/TRACK pin. In this way, the output voltage slew rate of the LM2747 will be controlled by the master supply for loads that require precise sequencing. When the tracking function is used no soft-start capacitor should be connected to the SS/TRACK pin. However in all other cases, a C_{SS} value of at least 1 nF between the soft-start pin and ground should be used.

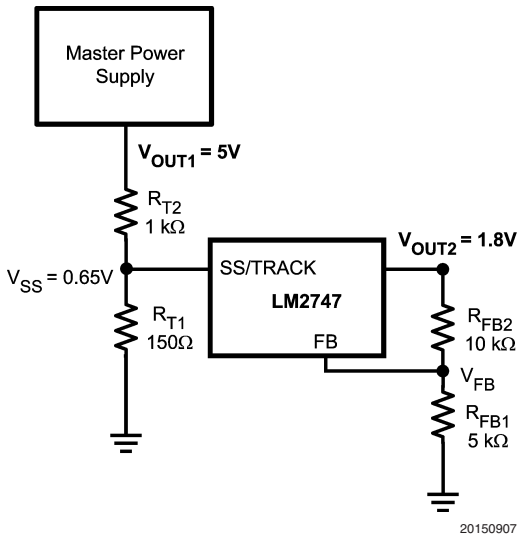


FIGURE 3. Tracking Circuit

One way to use the tracking feature is to design the tracking resistor divider so that the master supply's output voltage (V_{OUT1}) and the LM2747's output voltage (represented symbolically in *Figure 3* as V_{OUT2}, i.e. without explicitly showing the power components) both rise together and reach their

Application Information (Continued)

target values at the same time. For this case, the equation governing the values of the tracking divider resistors R_{T1} and R_{T2} is:

$$0.65 = V_{OUT1} \frac{R_{T1}}{R_{T1} + R_{T2}}$$

The current through R_{T1} should be about 4 mA for precise tracking. The final voltage of the SS/TRACK pin should be set higher than the feedback voltage of 0.6V (say about 0.65V as in the above equation). If the master supply voltage was 5V and the LM2747 output voltage was 1.8V, for example, then the value of R_{T1} needed to give the two supplies identical soft-start times would be 150Ω. A timing diagram for the equal soft-start time case is shown in *Figure 4*.

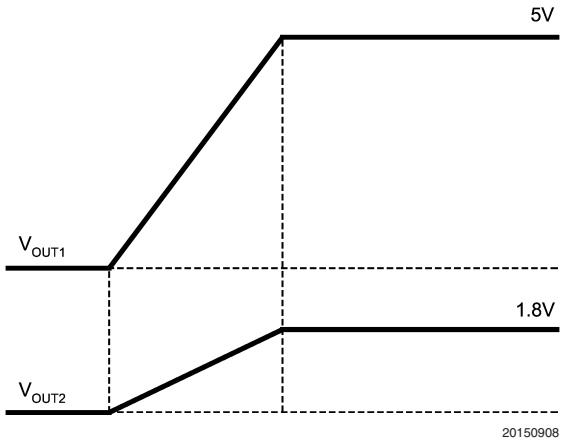


FIGURE 4. Tracking with Equal Soft-Start Time

TRACKING A VOLTAGE SLEW RATE

The tracking feature can alternatively be used not to make both rails reach regulation at the same time but rather to have similar rise rates (in terms of output dV/dt). This method ensures that the output voltage of the LM2747 always reaches regulation before the output voltage of the master supply. In this case, the tracking resistors can be determined based on the following equation:

$$0.65 = V_{OUT2} \frac{R_{T1}}{R_{T1} + R_{T2}}$$

For the example case of V_{OUT1} = 5V and V_{OUT2} = 1.8V, with R_{T1} set to 150Ω as before, R_{T2} is calculated from the above equation to be 265Ω. A timing diagram for the case of equal slew rates is shown in *Figure 5*.

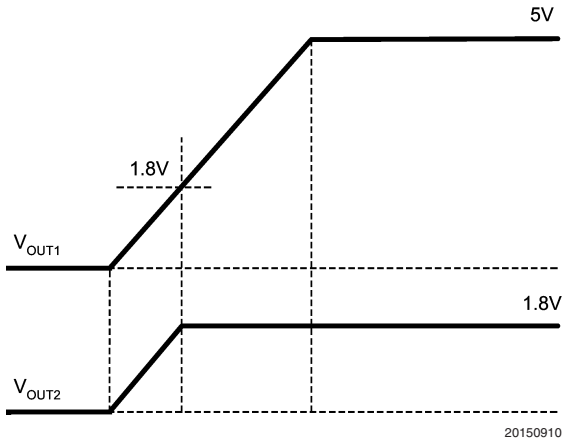


FIGURE 5. Tracking with Equal Slew Rates

SEQUENCING

The start up/soft-start of the LM2747 can be delayed for the purpose of sequencing by connecting a resistor divider from the output of a master power supply to the $\overline{SD}$ pin, as shown in *Figure 6*.

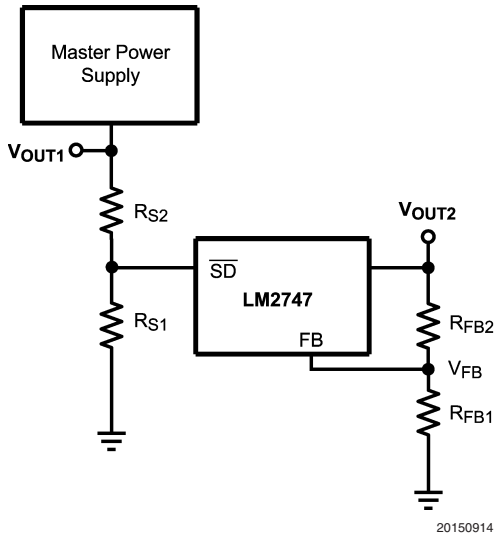


FIGURE 6. Sequencing Circuit

A desired delay time t_{DELAY} between the startup of the master supply output voltage and the LM2747 output voltage can be set based on the $\overline{SD}$ pin low-to-high threshold V_{SD-IH} and the slew rate of the voltage at the $\overline{SD}$ pin, SR_{SD}:

$$t_{DELAY} = V_{SD-IH} / SR_{SD}$$

Note again, that in *Figure 6*, the LM2747's output voltage has been represented symbolically as V_{OUT2}, i.e. without explicitly showing the power components.

V_{SD-IH} is typically 1.08V and SR_{SD} is the slew rate of the $\overline{SD}$ pin voltage. The values of the sequencing divider resistors R_{S1} and R_{S2} set the SR_{SD} based on the master supply output voltage slew rate, SR_{OUT1}, using the following equation:

Application Information (Continued)

$$SR_{SD} = SR_{OUT1} \frac{R_{S1}}{R_{S1} + R_{S2}}$$

For example, if the master supply output voltage slew rate was 1V/ms and the desired delay time between the startup of the master supply and LM2747 output voltage was 5 ms, then the desired $\overline{SD}$ pin slew rate would be (1.08V/5 ms) = 0.216V/ms. Due to the internal impedance of the $\overline{SD}$ pin, the maximum recommended value for R_{S2} is 1 kΩ. To achieve the desired slew rate, R_{S1} would then be 274Ω. A timing diagram for this example is shown in *Figure 7*.

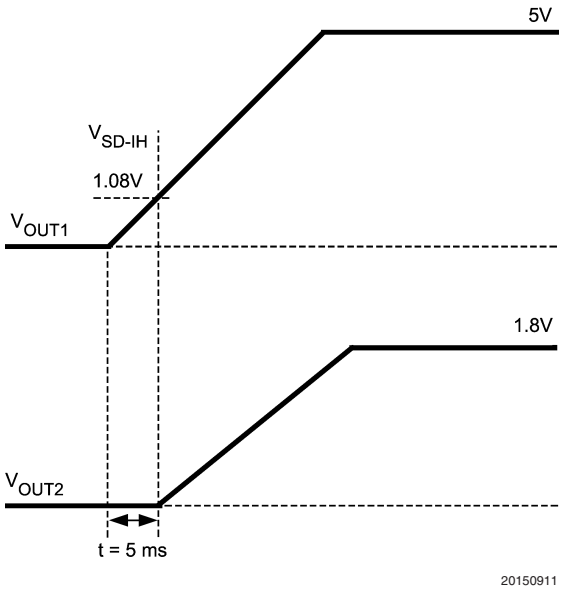


FIGURE 7. Delay for Sequencing

$\overline{SD}$ PIN IMPEDANCE

When connecting a resistor divider to the $\overline{SD}$ pin of the LM2747 some care has to be taken. Once the $\overline{SD}$ voltage goes above V_{SD-IH}, a 17 µA pull-up current is activated as shown in *Figure 8*. This current is used to create the internal hysteresis (≈170 mV); however, high external impedances will affect the $\overline{SD}$ pin logic thresholds as well. The external impedance used for the sequencing divider network should preferably be a small fraction of the impedance of the $\overline{SD}$ pin for good performance (around 1 kΩ).

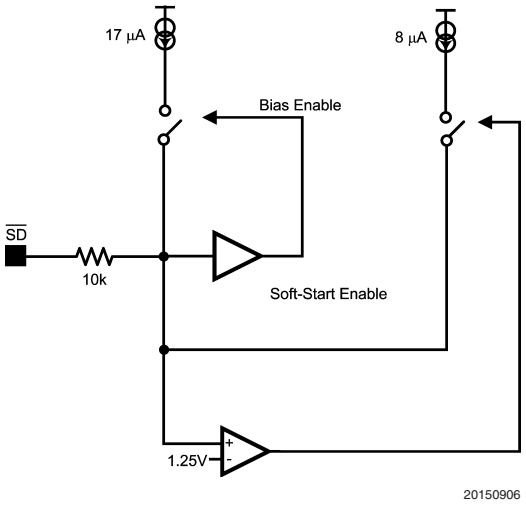


FIGURE 8. $\overline{SD}$ Pin Logic

MOSFET GATE DRIVERS

The LM2747 has two gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Note that unlike most other synchronous controllers, the bootstrap capacitor of the LM2747 provides power not only to the driver of the upper MOSFET, but the lower MOSFET driver too (both drivers are ground referenced, i.e. no floating driver).

Two things must be kept in mind here. First, the BOOT pin has an absolute maximum rating of 18V. This must never be exceeded, even momentarily. Since the bootstrap capacitor is connected to the SW node, the peak voltage impressed on the BOOT pin is the sum of the input voltage (V_{IN}) plus the voltage across the bootstrap capacitor (ignoring any forward drop across the bootstrap diode). The bootstrap capacitor is charged up by a given rail (called V_{BOOT_DC} here) whenever the upper MOSFET turns off. This rail can be the same as V_{CC} or it can be any external ground-referenced DC rail. But care has to be exercised when choosing this bootstrap DC rail that the BOOT pin is not damaged. For example, if the desired maximum V_{IN} is 14V, and V_{BOOT_DC} is chosen to be the same as V_{CC}, then clearly if the V_{CC} rail is 6V, the peak voltage on the BOOT pin is 14V + 6V = 20V. This is unacceptable, as it is in excess of the rating of the BOOT pin. A V_{CC} of 3V would be acceptable in this case. Or the V_{IN} range must be reduced accordingly. There is also the option of deriving the bootstrap DC rail from another 3V external rail, independent of V_{CC}.

The second thing to be kept in mind here is that the output of the low-side driver swings between the bootstrap DC rail level of V_{BOOT_DC} and Ground, whereas the output of the high-side driver swings between V_{IN}+ V_{BOOT_DC} and Ground. To keep the high-side MOSFET fully on when desired, the Gate pin voltage of the MOSFET must be higher than its instantaneous Source pin voltage by an amount equal to the 'Miller plateau'. It can be shown that this plateau is equal to the threshold voltage of the chosen MOSFET plus a small amount equal to Io/g. Here Io is the maximum load current of the application, and g is the transconductance of this MOSFET (typically about 100 for logic-level devices). That means we must choose V_{BOOT_DC} to at least exceed

Application Information (Continued)

the Miller plateau level. This may therefore affect the choice of the threshold voltage of the external MOSFETs, and that in turn may depend on the chosen V_{BOOT_DC} rail.

So far, in the discussion above, the forward drop across the bootstrap diode has been ignored. But since that does affect the output of the driver somewhat, it is a good idea to include this drop in the following examples. Looking at the Typical Application schematic, this means that the difference voltage V_{CC} - V_{D1}, which is the voltage the bootstrap capacitor charges up to, must always be greater than the maximum tolerance limit of the threshold voltage of the upper MOSFET. Here V_{D1} is the forward voltage drop across the bootstrap diode D1. This may place restrictions on the minimum input voltage and/or type of MOSFET used.

A basic bootstrap circuit can be built using one Schottky diode and a small capacitor, as shown in *Figure 9*. The capacitor C_{BOOT} serves to maintain enough voltage between the top MOSFET gate and source to control the device even when the top MOSFET is on and its source has risen up to the input voltage level. The charge pump circuitry is fed from V_{CC}, which can operate over a range from 3.0V to 6.0V. Using this basic method the voltage applied to the gates of both high-side and low-side MOSFETs is V_{CC} - V_D. This method works well when V_{CC} is 5V±10%, because the gate drives will get at least 4.0V of drive voltage during the worst case of V_{CC-MIN} = 4.5V and V_{D-MAX} = 0.5V. Logic level MOSFETs generally specify their on-resistance at V_{GS} = 4.5V. When V_{CC} = 3.3V±10%, the gate drive at worst case could go as low as 2.5V. Logic level MOSFETs are not guaranteed to turn on, or may have much higher on-resistance at 2.5V. Sub-logic level MOSFETs, usually specified at V_{GS} = 2.5V, will work, but are more expensive, and tend to have higher on-resistance. The circuit in *Figure 9* works well for input voltages ranging from 1V up to 14V and V_{CC} = 5V±10%, because the drive voltage depends only on V_{CC}.

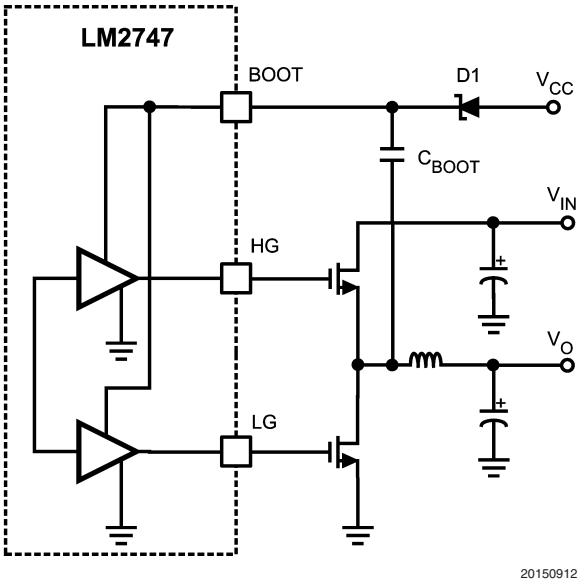


FIGURE 9. Basic Charge Pump (Bootstrap)

Note that the LM2747 can be paired with a low cost linear regulator like the LM78L05 to run from a single input rail between 6.0 and 14V. The 5V output of the linear regulator powers both the V_{CC} and the bootstrap circuit, providing efficient drive for logic level MOSFETs. An example of this circuit is shown in *Figure 10*.

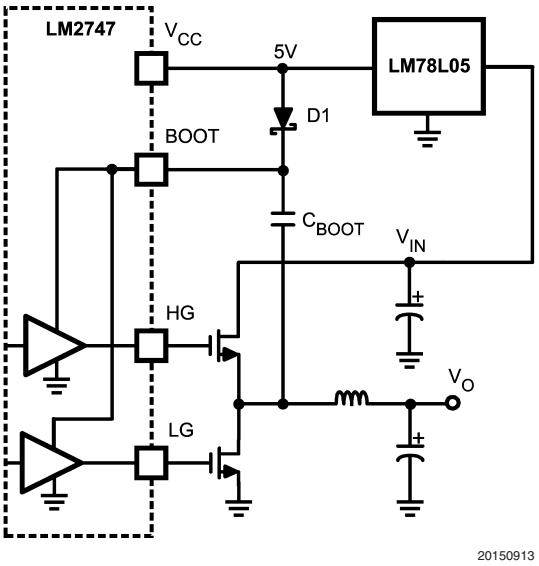


FIGURE 10. LM78L05 Feeding Basic Charge Pump

Figure 11 shows a second possibility for bootstrapping the MOSFET drives using a doubler. This circuit provides an equal voltage drive of V_{CC} - $3V_D$ + V_{IN} to both the high-side and low-side MOSFET drives. This method should only be used in circuits that use 3.3V for both V_{CC} and V_{IN}. Even with V_{IN} = V_{CC} = 3.0V (10% lower tolerance on 3.3V) and V_D = 0.5V both high-side and low-side gates will have at least 4.5V of drive. The power dissipation of the gate drive circuitry is directly proportional to gate drive voltage, hence the thermal limits of the LM2747 IC will quickly be reached if this circuit is used with V_{CC} or V_{IN} voltages over 5V.

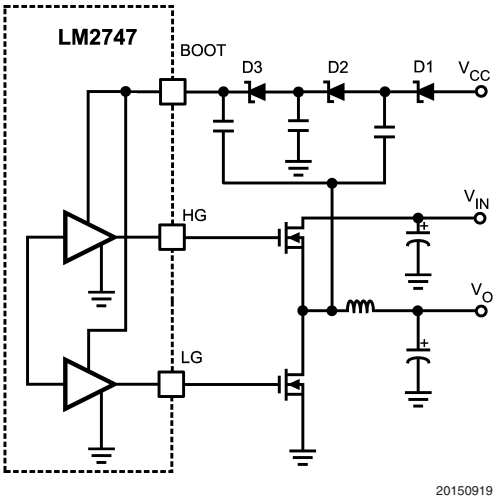


FIGURE 11. Charge Pump with Added Gate Drive

All the gate drive circuits shown in the above figures typically use 100 nF ceramic capacitors in the bootstrap locations.

Application Information (Continued)

POWER GOOD SIGNAL

The open drain output on the Power Good pin needs a pull-up resistor to a low voltage source. The pull-up resistor should be chosen so that the current going into the Power Good pin is less than 1 mA. A 100 kΩ resistor is recommended for most applications.

The Power Good signal is an OR-gated flag which takes into account both output overvoltage and undervoltage conditions. If the feedback pin (FB) voltage is 18% above its nominal value (118% x V_{FB} = 0.708V) or falls 28% below that value (72% x V_{FB} = 0.42V) the Power Good flag goes low. The Power Good flag can be used to signal other circuits that the output voltage has fallen out of regulation, however the switching of the LM2747 continues regardless of the state of the Power Good signal. The Power Good flag will return to logic high whenever the feedback pin voltage is between 72% and 118% of 0.6V.

UVLO

The 2.79V turn-on threshold on V_{CC} has a built in hysteresis of about 300 mV. If V_{CC} drops below 2.42V, the chip definitely enters UVLO mode. UVLO consists of turning off the top and bottom MOSFETS and remaining in that condition until V_{CC} rises above 2.79V. As with normal shutdown initiated by the $\overline{SD}$ pin, the soft-start capacitor is discharged through an internal MOSFET, ensuring that the next start-up will be controlled by the soft-start circuitry.

CURRENT LIMIT

Current limit is realized by sensing the voltage across the low-side MOSFET while it is on. The R_{DSON} of the MOSFET is a known value; hence the current through the MOSFET can be determined as:

$$V_{DS} = I_{OUT} \times R_{DSON}$$

The current through the low-side MOSFET while it is on is also the falling portion of the inductor current. The current limit threshold is determined by an external resistor, R_{CS}, connected between the switching node and the I_{SEN} pin. A constant current (I_{SEN-TH}) of 40 µA typical is forced through R_{CS}, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the current limit of the chip has been reached. To obtain a more accurate value for R_{CS} you must consider the operating values of R_{DSON} and I_{SEN-TH} at their operating temperatures in your application and the effect of slight parameter differences from part to part. R_{CS} can be found by using the following equation using the R_{DSON} value of the low side MOSFET at it's expected hot temperature and the absolute minimum value expected over the full temperature range for the for the I_{SEN-TH} which is 25 µA:

$$R_{CS} = R_{DSON-HOT} \times I_{LIM} / I_{SEN-TH}$$

For example, a conservative 15A current limit in a 10A design with a $R_{DSON-HOT}$ of 10 mΩ would require a 6 kΩ resistor. The minimum value for R_{CS} in any application is 1 kΩ. Because current sensing is done across the low-side MOSFET, no minimum high-side on-time is necessary. The LM2747 enters current limit mode if the inductor current exceeds the current limit threshold at the point where the high-side MOSFET turns off and the low-side MOSFET turns on. (The point of peak inductor current, see *Figure 12*). Note that in normal operation mode the high-side MOSFET always turns on at the beginning of a clock cycle. In current limit mode, by contrast, the high-side MOSFET on-pulse is skipped. This causes inductor current to fall. Unlike a normal operation switching cycle, however, in a current limit mode switching cycle the high-side MOSFET will turn on as soon as inductor current has fallen to the current limit threshold. The LM2747 will continue to skip high-side MOSFET pulses until the inductor current peak is below the current limit threshold, at which point the system resumes normal operation.

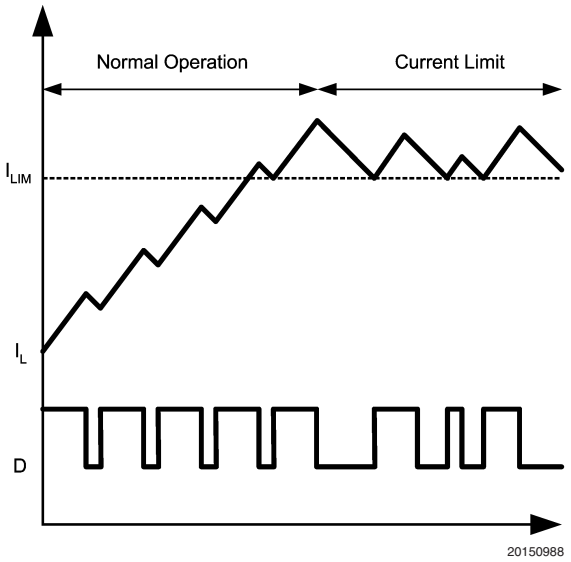


FIGURE 12. Current Limit Threshold

Unlike a high-side MOSFET current sensing scheme, which limits the peaks of inductor current, low-side current sensing is only allowed to limit the current during the converter off-time, when inductor current is falling. Therefore in a typical current limit plot the valleys are normally well defined, but the peaks are variable, according to the duty cycle. The PWM error amplifier and comparator control the off-pulse of the high-side MOSFET, even during current limit mode, meaning that peak inductor current can exceed the current limit threshold. Assuming that the output inductor does not saturate, the maximum peak inductor current during current limit mode can be calculated with the following equation:

$$I_{PK-CL} = I_{LIM} + (T_{SW} - 200\ ns)\ \frac{V_{IN} - V_O}{L}$$

Where T_{SW} is the inverse of switching frequency f_{SW}. The 200 ns term represents the minimum off-time of the duty cycle, which ensures enough time for correct operation of the current sensing circuitry.

In order to minimize the time period in which peak inductor current exceeds the current limit threshold, the IC also discharges the soft-start capacitor through a fixed 90 µA sink. The output of the LM2747 internal error amplifier is limited by the voltage on the soft-start capacitor. Hence, discharging the soft-start capacitor reduces the maximum duty cycle D of the controller. During severe current limit this reduction in duty cycle will reduce the output voltage if the current limit conditions last for an extended time. Output inductor current

Application Information (Continued)

will be reduced in turn to a flat level equal to the current limit threshold. The third benefit of the soft-start capacitor discharge is a smooth, controlled ramp of output voltage when the current limit condition is cleared.

SHUTDOWN

If the shutdown pin is pulled low, (below 0.8V) the LM2747 enters shutdown mode, and discharges the soft-start capacitor through a MOSFET switch. The high and low-side MOSFETs are turned off. The LM2747 remains in this state as long as V_{SD} sees a logic low (see the Electrical Characteristics table). To assure proper IC start-up the shutdown pin should not be left floating. For normal operation this pin should be connected directly to V_{CC} or to another voltage between 1.3V to V_{CC} (see the Electrical Characteristics table).

DESIGN CONSIDERATIONS

The following is a design procedure for all the components needed to create the Typical Application Circuit shown on the front page. This design converts 3.3V (V_{IN}) to 1.2V (V_{OUT}) at a maximum load of 4A with an efficiency of 89% and a switching frequency of 300 kHz. The same procedures can be followed to create many other designs with varying input voltages, output voltages, and load currents.

Input Capacitor

The input capacitors in a Buck converter are subjected to high stress due to the input current trapezoidal waveform. Input capacitors are selected for their ripple current capability and their ability to withstand the heat generated since that ripple current passes through their ESR. Input rms ripple current is approximately:

$$I_{RMS\_RIP} = I_{OUT} \times \sqrt{D(1 - D)}$$

Where duty cycle $D = V_{OUT}/V_{IN}$.

The power dissipated by each input capacitor is:

$$P_{CAP} = \frac{(I_{RMS\_RIP})^2 \times ESR}{n^2}$$

where n is the number of paralleled capacitors, and ESR is the equivalent series resistance of each capacitor. The equation above indicates that power loss in each capacitor decreases rapidly as the number of input capacitors increases. The worst-case ripple for a Buck converter occurs during full load and when the duty cycle (D) is 0.5. For this 3.3V to 1.2V design the duty cycle is 0.364. For a 4A maximum load the ripple current is 1.92A.

Output Inductor

The output inductor forms the first half of the power stage in a Buck converter. It is responsible for smoothing the square wave created by the switching action and for controlling the output current ripple (ΔI_{OUT}). The inductance is chosen by selecting between tradeoffs in efficiency and response time. The smaller the output inductor, the more quickly the converter can respond to transients in the load current. However, as shown in the efficiency calculations, a smaller inductor requires a higher switching frequency to maintain the same level of output current ripple. An increase in frequency can mean increasing loss in the MOSFETs due to the charging and discharging of the gates. Generally the switching frequency is chosen so that conduction loss outweighs switching loss. The equation for output inductor selection is:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{OUT} \times f_{SW}} \times D$$

$$L = \frac{3.3V - 1.2V}{0.4 \times 4A \times 300\ kHz} \times \frac{1.2V}{3.3V}$$

$$L = 1.6\ \mu H$$

Here we have plugged in the values for output current ripple, input voltage, output voltage, switching frequency, and assumed a 40% peak-to-peak output current ripple. This yields an inductance of 1.6 µH. The output inductor must be rated to handle the peak current (also equal to the peak switch current), which is (I_{OUT} + (0.5 x ΔI_{OUT})) = 4.8A, for a 4A design.

The Coilcraft DO3316P-222P is 2.2 µH, is rated to 7.4A peak, and has a direct current resistance (DCR) of 12 mΩ. After selecting the Coilcraft DO3316P-222P for the output inductor, actual inductor current ripple should be recalculated with the selected inductance value, as this information is needed to select the output capacitor. Rearranging the equation used to select inductance yields the following:

$$\Delta I_{OUT} = \frac{V_{IN(MAX)} - V_O}{f_{SW} \times L_{ACTUAL}} \times D$$

$V_{IN(MAX)}$ is assumed to be 10% above the steady state input voltage, or 3.6V at V_{IN} = 3.3V. The re-calculated current ripple will then be 1.2A. This gives a peak inductor/switch current will be 4.6A.

Output Capacitor

The output capacitor forms the second half of the power stage of a Buck switching converter. It is used to control the output voltage ripple (ΔV_{OUT}) and to supply load current during fast load transients.

In this example the output current is 4A and the expected type of capacitor is an aluminum electrolytic, as with the input capacitors. Other possibilities include ceramic, tantalum, and solid electrolyte capacitors, however the ceramic type often do not have the large capacitance needed to supply current for load transients, and tantalums tend to be more expensive than aluminum electrolytic. Aluminum capacitors tend to have very high capacitance and fairly low ESR, meaning that the ESR zero, which affects system stability, will be much lower than the switching frequency. The large capacitance means that at the switching frequency, the ESR is dominant, hence the type and number of output capacitors is selected on the basis of ESR. One simple formula to find the maximum ESR based on the desired output voltage ripple, ΔV_{OUT} and the designed output current ripple, ΔI_{OUT}, is:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

Application Information (Continued)

In this example, in order to maintain a 2% peak-to-peak output voltage ripple and a 40% peak-to-peak inductor current ripple, the required maximum ESR is 20 mΩ. The Sanyo 4SP560M electrolytic capacitor will give an equivalent ESR of 14 mΩ. The capacitance of 560 µF is enough to supply energy even to meet severe load transient demands.

MOSFETs

Selection of the power MOSFETs is governed by a trade-off between cost, size, and efficiency. One method is to determine the maximum cost that can be endured, and then select the most efficient device that fits that price. Breaking down the losses in the high-side and low-side MOSFETs and then creating spreadsheets is one way to determine relative efficiencies between different MOSFETs. Good correlation between the prediction and the bench result is not guaranteed, however. Single-channel buck regulators that use a controller IC and discrete MOSFETs tend to be most efficient for output currents of 2 to 10A.

Losses in the high-side MOSFET can be broken down into conduction loss, gate charging loss, and switching loss. Conduction, or I^2R loss, is approximately:

$$P_C = D\ (I_O^2 \times R_{DSON\text{-}HI} \times 1.3)$$
(High-Side MOSFET)

$$P_C = (1 - D) \times (I_O^2 \times R_{DSON\text{-}LO} \times 1.3)$$
(Low-Side MOSFET)

In the above equations the factor 1.3 accounts for the increase in MOSFET R_{DSON} due to heating. Alternatively, the 1.3 can be ignored and the R_{DSON} of the MOSFET estimated using the R_{DSON} Vs. Temperature curves in the MOSFET datasheets.

Gate charging loss results from the current driving the gate capacitance of the power MOSFETs, and is approximated as:

$$P_{GC} = n \times (V_{DD}) \times Q_G \times f_{SW}$$

where 'n' is the number of MOSFETs (if multiple devices have been placed in parallel), V_{DD} is the driving voltage (see MOSFET Gate Drivers section) and Q_{GS} is the gate charge of the MOSFET. If different types of MOSFETs are used, the 'n' term can be ignored and their gate charges simply summed to form a cumulative Q_G. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the LM2747, and not in the MOSFET itself.

Switching loss occurs during the brief transition period as the high-side MOSFET turns on and off, during which both current and voltage are present in the channel of the MOSFET. It can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_r + t_f) \times f_{SW}$$

where t_r and t_f are the rise and fall times of the MOSFET. Switching loss occurs in the high-side MOSFET only.

For this example, the maximum drain-to-source voltage applied to either MOSFET is 3.6V. The maximum drive voltage at the gate of the high-side MOSFET is 3.1V, and the maximum drive voltage for the low-side MOSFET is 3.3V. Due to the low drive voltages in this example, a MOSFET that turns on fully with 3.1V of gate drive is needed. For designs of 5A and under, dual MOSFETs in SO-8 provide a good trade-off between size, cost, and efficiency.

Support Components

$C_{IN}2$ - A small (0.1 to 1 µF) ceramic capacitor should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET (dual MOSFETs make this easy). This capacitor should be X5R type dielectric or better.

R_{CC}, C_{CC}- These are standard filter components designed to ensure smooth DC voltage for the chip supply. R_{CC} should be 1 to 10Ω. C_{CC} should 1 µF, X5R type or better.

C_{BOOT}- Bootstrap capacitor, typically 100 nF.

$R_{PULL\text{-}UP}$ – This is a standard pull-up resistor for the open-drain power good signal (PWGD). The recommended value is 100 kΩ connected to V_{CC}. If this feature is not necessary, the resistor can be omitted.

D_1 - A small Schottky diode should be used for the bootstrap. It allows for a minimum drop for both high and low-side drivers. The MBR0520 or BAT54 work well in most designs.

R_{CS} - Resistor used to set the current limit. Since the design calls for a peak current magnitude (I_{OUT} + (0.5 x ΔI_{OUT})) of 4.8A, a safe setting would be 6A. (This is below the saturation current of the output inductor, which is 7A.) Following the equation from the Current Limit section, a 1.3 kΩ resistor should be used.

R_{FADJ} - This resistor is used to set the switching frequency of the chip. The resistor value is approximated from the *Frequency vs Frequency Adjust Resistor* curve in the Typical Performance Characteristics section. For 300 kHz operation, a 100 kΩ resistor should be used.

C_{SS} - The soft-start capacitor depends on the user requirements and is calculated based on the equation given in the section titled *START UP/SOFT-START*. Therefore, for a 7 ms delay, a 12 nF capacitor is suitable.

Control Loop Compensation

The LM2747 uses voltage-mode ('VM') PWM control to correct changes in output voltage due to line and load transients. VM requires careful small signal compensation of the control loop for achieving high bandwidth and good phase margin.

The control loop is comprised of two parts. The first is the power stage, which consists of the duty cycle modulator, output inductor, output capacitor, and load. The second part is the error amplifier, which for the LM2747 is a 9 MHz op-amp used in the classic inverting configuration. *Figure 13* shows the regulator and control loop components.

Application Information (Continued)

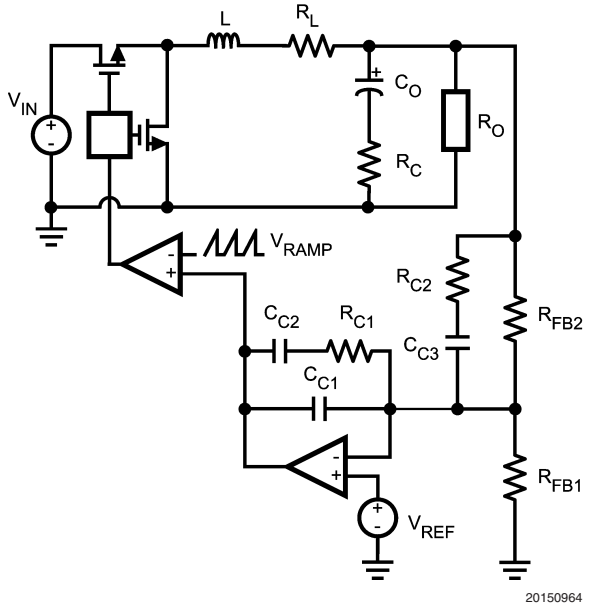


FIGURE 13. Power Stage and Error Amp

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to see. Software tools such as Excel, MathCAD, and Matlab are useful for showing how changes in compensation or the power stage affect system gain and phase.

The power stage modulator provides a DC gain A_{DC} that is equal to the input voltage divided by the peak-to-peak value of the PWM ramp. This ramp is $1.0V_{pk-pk}$ for the LM2747. The inductor and output capacitor create a double pole at frequency f_{DP}, and the capacitor ESR and capacitance create a single zero at frequency f_{ESR}. For this example, with V_{IN} = 3.3V, these quantities are:

$$A_{DC} = \frac{V_{IN}}{V_{RAMP}} = \frac{3.3}{1.0} = 10.4\ dB$$

$$f_{DP} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_L}{LC_O(R_O + ESR)}} = 4.5\ kHz$$

$$f_{ESR} = \frac{1}{2\pi C_O ESR} = 20.3\ kHz$$

In the equation for f_{DP}, the variable R_L is the power stage resistance, and represents the inductor DCR plus the on resistance of the top power MOSFET. R_O is the output voltage divided by output current. The power stage transfer function G_{PS} is given by the following equation, and *Figure 14* shows Bode plots of the phase and gain in this example.

$$G_{PS} = \frac{V_{IN} \times R_O}{V_{RAMP}} \times \frac{sC_OR_C + 1}{as^2 + bs + c}$$

$a = LC_O(R_O + R_C)$

$b = L + C_O(R_OR_L + R_OR_C + R_CR_L)$

$c = R_O + R_L$

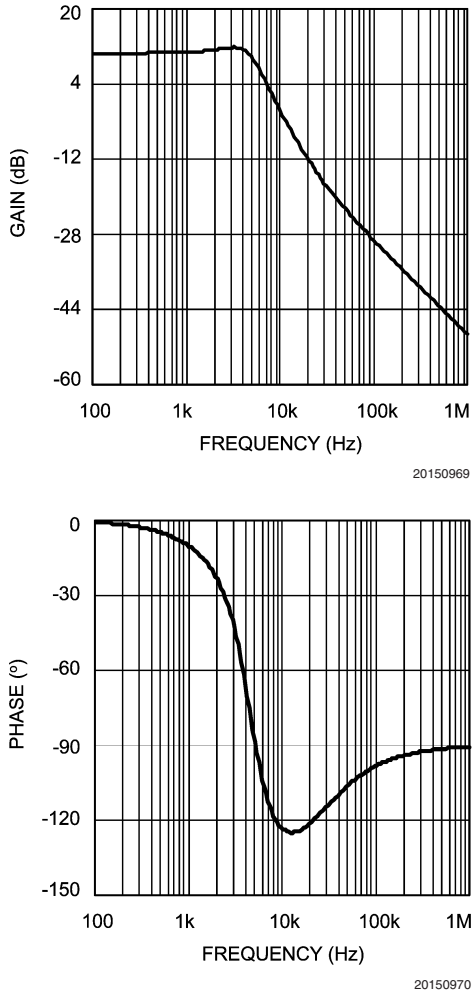


FIGURE 14. Power Stage Gain and Phase

The double pole at 4.5 kHz causes the phase to drop to approximately -130˚ at around 10 kHz. The ESR zero, at 20.3 kHz, provides a +90˚ boost that prevents the phase from dropping to -180°. If this loop were left uncompensated, the bandwidth would be approximately 10 kHz and the phase margin 53˚. In theory, the loop would be stable, but would suffer from poor DC regulation (due to the low DC gain) and would be slow to respond to load transients (due to the low bandwidth.) In practice, the loop could easily become unstable due to tolerances in the output inductor, capacitor, or changes in output current, or input voltage. Therefore, the loop is compensated using the error amplifier and a few passive components.

For this example, a Type III, or three-pole-two-zero approach gives optimal bandwidth and phase.

In most voltage mode compensation schemes, including Type III, a single pole is placed at the origin to boost DC gain

Application Information (Continued)

as high as possible. Two zeroes f_{Z1} and f_{Z2} are placed at the double pole frequency to cancel the double pole phase lag. Then, a pole, f_{P1} is placed at the frequency of the ESR zero. A final pole f_{P2} is placed at one-half of the switching frequency. The gain of the error amplifier transfer function is selected to give the best bandwidth possible without violating the Nyquist stability criteria. In practice, a good crossover point is one-fifth of the switching frequency, or 60 kHz for this example. The generic equation for the error amplifier transfer function is:

$$G_{EA} = A_{EA} \times \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)}$$

In this equation the variable A_{EA} is a ratio of the values of the capacitance and resistance of the compensation components, arranged as shown in *Figure 13*. A_{EA} is selected to provide the desired bandwidth. A starting value of 80,000 for A_{EA} should give a conservative bandwidth. Increasing the value will increase the bandwidth, but will also decrease phase margin. Designs with 45-60˚ are usually best because they represent a good trade-off between bandwidth and phase margin. In general, phase margin is lowest and gain highest (worst-case) for maximum input voltage and minimum output current. One method to select A_{EA} is to use an iterative process beginning with these worst-case conditions.

1. Increase A_{EA}
2. Check overall bandwidth and phase margin
3. Change V_{IN} to minimum and recheck overall bandwidth and phase margin
4. Change I_O to maximum and recheck overall bandwidth and phase margin

The process ends when the both bandwidth and the phase margin are sufficiently high. For this example input voltage can vary from 3.0 to 3.6V and output current can vary from 0 to 4A, and after a few iterations a moderate gain factor of 101dB is used.

The error amplifier of the LM2747 has a unity-gain bandwidth of 9 MHz. In order to model the effect of this limitation, the open-loop gain can be calculated as:

$$OPG = \frac{2\pi \times 9\ MHz}{s}$$

The new error amplifier transfer function that takes into account unity-gain bandwidth is:

$$H_{EA} = \frac{G_{EA} \times OPG}{1 + G_{EA} + OPG}$$

The gain and phase of the error amplifier are shown in *Figure 15*.

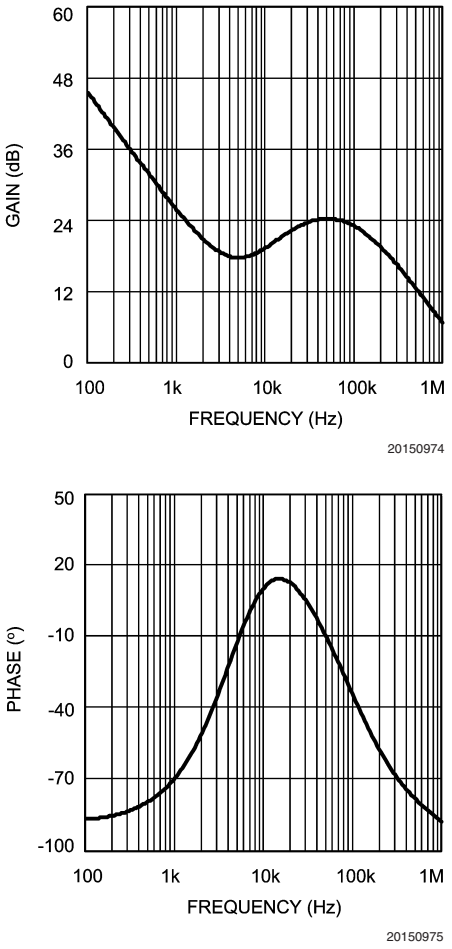


FIGURE 15. Error Amp. Gain and Phase

In VM regulators, the top feedback resistor R_{FB2} forms a part of the compensation. Setting R_{FB2} to 10 kΩ±1%, usually gives values for the other compensation resistors and capacitors that fall within a reasonable range. (Capacitances > 1 pF, resistances <1 MΩ) C_{C1}, C_{C2}, C_{C3}, R_{C1}, and R_{C2} are selected to provide the poles and zeroes at the desired frequencies, using the following equations:

$$C_{C1} = \frac{f_{Z1}}{A_{EA} \times 10{,}000 \times f_{P2}} = 27\ pF$$

$$C_{C2} = \frac{1}{A_{EA} \times 10{,}000} - C_{C1} = 882\ pF$$

$$C_{C3} = \frac{1}{2\pi \times 10{,}000} \times \left(\frac{1}{f_{Z2}} - \frac{1}{f_{P1}}\right) = 2.73\ nF$$

$$R_{C1} = \frac{1}{2\pi \times C_{C2} \times f_{Z1}} = 39.8\ k\Omega$$

Application Information (Continued)

$$R_{C2} = \frac{1}{2\pi \times C_{C3} \times f_{P1}} = 2.55\ k\Omega$$

In practice, a good trade off between phase margin and bandwidth can be obtained by selecting the closest ±10% capacitor values above what are suggested for C_{C1} and C_{C2}, the closest ±10% capacitor value below the suggestion for C_{C3}, and the closest ±1% resistor values below the suggestions for R_{C1}, R_{C2}. Note that if the suggested value for R_{C2} is less than 100Ω, it should be replaced by a short circuit. Following this guideline, the compensation components will be:

C_{C1} = 27 pF±10%, C_{C2} = 820 pF±10%

C_{C3} = 2.7 nF±10%, R_{C1} = 39.2 kΩ±1%

R_{C2} = 2.55 kΩ±1%

The transfer function of the compensation block can be derived by considering the compensation components as impedance blocks Z_F and Z_I around an inverting op-amp:

$$G_{EA\text{-}ACTUAL} = \frac{Z_F}{Z_I}$$

$$Z_F = \frac{\frac{1}{sC_{C1}} x \left(10{,}000 + \frac{1}{sC_{C2}}\right)}{10{,}000 + \frac{1}{sC_{C1}} + \frac{1}{sC_{C2}}}$$

$$Z_I = \frac{R_{C1}\left(R_{C2} + \frac{1}{sC_{C3}}\right)}{R_{C1} + R_{C2} + \frac{1}{sC_{C3}}}$$

As with the generic equation, $G_{EA\text{-}ACTUAL}$ must be modified to take into account the limited bandwidth of the error amplifier. The result is:

$$H_{EA} = \frac{G_{EA\text{-}ACTUAL} \times OPG}{1 + G_{EA\text{-}ACTUAL} + OPG}$$

The total control loop transfer function H is equal to the power stage transfer function multiplied by the error amplifier transfer function.

$$H = G_{PS} \times H_{EA}$$

The bandwidth and phase margin can be read graphically from Bode plots of H_{EA} as shown in *Figure 16*.

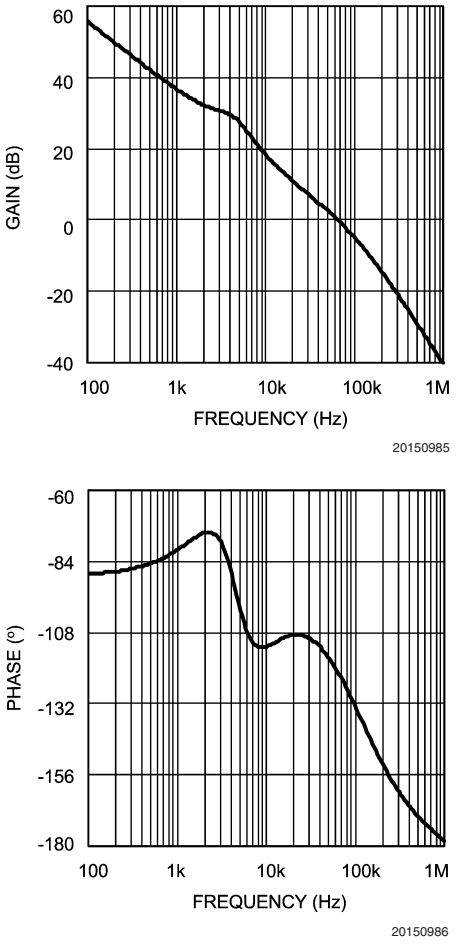


FIGURE 16. Overall Loop Gain and Phase

The bandwidth of this example circuit is 59 kHz, with a phase margin of 60˚.

EFFICIENCY CALCULATIONS

The following is a sample calculation.

A reasonable estimation of the efficiency of a switching buck controller can be obtained by adding together the Output Power (P_{OUT}) loss and the Total Power (P_{TOTAL}) loss:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\%$$

The Output Power (P_{OUT}) for the Typical Application Circuit design is (1.2V x 4A) = 4.8W. The Total Power (P_{TOTAL}), with an efficiency calculation to complement the design, is shown below.

The majority of the power losses are due to the low side and high side MOSFET's losses. The losses in any MOSFET are group of switching (P_{SW}) and conduction losses (P_{CND}).

$$P_{FET} = P_{SW} + P_{CND} = 61.38\ mW + 270.42\ mW$$

$$P_{FET} = 331.8\ mW$$

FET Switching Loss (P_{SW})

$$P_{SW} = P_{SW(ON)} + P_{SW(OFF)}$$

$$P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}$$

Application Information (Continued)

$$P_{SW} = 0.5 \times 3.3V \times 4A \times 300\ kHz \times 31\ ns$$

$$P_{SW} = 61.38\ mW$$

The FDS6898A has a typical turn-on rise time t_r and turn-off fall time t_f of 15 ns and 16 ns, respectively. The switching losses for this type of dual N-Channel MOSFETs are 0.061W.

FET Conduction Loss (P_{CND})

$$P_{CND} = P_{CND1} + P_{CND2}$$

$$P_{CND1} = I^2_{OUT} \times R_{DS(ON)} \times k \times D$$

$$P_{CND2} = I^2_{OUT} \times R_{DS(ON)} \times k \times (1-D)$$

$R_{DS(ON)}$ = 13 mΩ and the factor is a constant value (k = 1.3) to account for the increasing $R_{DS(ON)}$ of a FET due to heating.

$$P_{CND1} = (4A)^2 \times 13\ m\Omega \times 1.3 \times 0.364$$

$$P_{CND2} = (4A)^2 \times 13\ m\Omega \times 1.3 \times (1 - 0.364)$$

$$P_{CND} = 98.42\ mW + 172\ mW = 270.42\ mW$$

There are few additional losses that are taken into account:

IC Operating Loss (P_{IC})

$$P_{IC} = I_{Q\_VCC} \times V_{CC},$$

where $I_{Q\text{-}VCC}$ is the typical operating V_{CC} current

$$P_{IC} = 1.7\ mA \times 3.3V = 5.61\ mW$$

FET Gate Charging Loss (P_{GATE})

$$P_{GATE} = n \times V_{CC} \times Q_{GS} \times f_{SW}$$

$$P_{GATE} = 2 \times 3.3V \times 3\ nC \times 300\ kHz$$

$$P_{GATE} = 5.94\ mW$$

The value n is the total number of FETs used and Q_{GS} is the typical gate-source charge value, which is 3 nC. For the FDS6898A the gate charging loss is 5.94 mW.

Input Capacitor Loss (P_{CAP})

$$P_{CAP} = \frac{(I_{RMS\_RIP})^2 \times ESR}{n^2}$$

where,

$$I_{RMS\_RIP} = I_{OUT} \times \sqrt{D(1 - D)}$$

Here n is the number of paralleled capacitors, ESR is the equivalent series resistance of each, and P_{CAP} is the dissipation in each. So for example if we use only one input capacitor of 24 mΩ.

$$P_{CAP} = \frac{(1.924A)^2 \times 24\ m\Omega}{1^2}$$

$$P_{CAP} = 88.8\ mW$$

Output Inductor Loss (P_{IND})

$$P_{IND} = I^2_{OUT} \times DCR$$

where DCR is the DC resistance. Therefore, for example

$$P_{IND} = (4A)^2 \times 11\ m\Omega$$

$$P_{IND} = 176\ mW$$

Total System Efficiency

$$P_{TOTAL} = P_{FET} + P_{IC} + P_{GATE} + P_{CAP} + P_{IND}$$

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\%$$

$$\eta = \frac{4.8W}{4.8W + 0.6W} = 89\%$$

Example Circuits

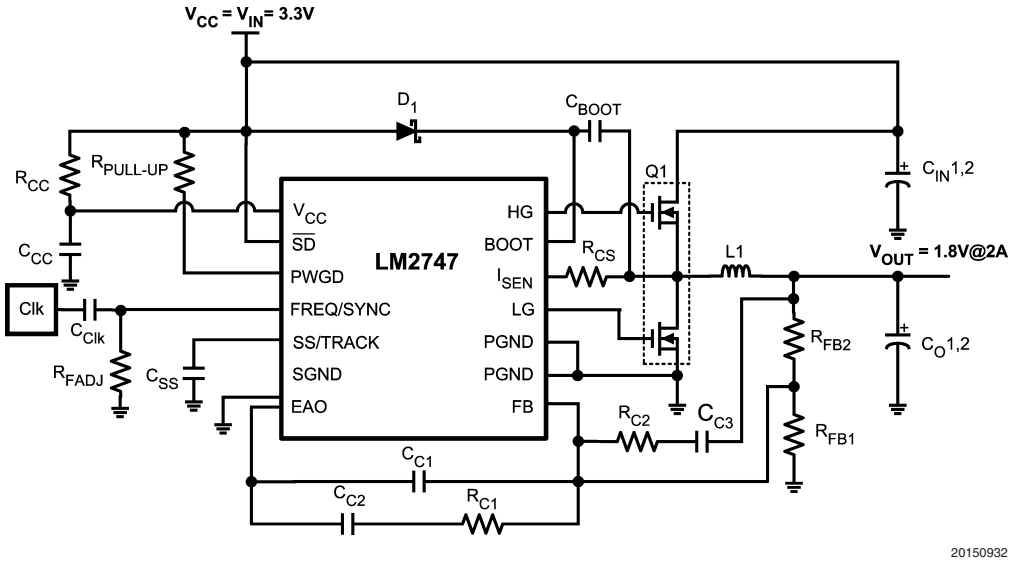


FIGURE 17. 3.3V to 1.8V @ 2A, f_{SW} = 300 kHz

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U1	LM2747	Synchronous Controller	TSSOP-14		NSC
Q1	FDS6898A	Dual N-MOSFET	SO-8	20V, 10 mΩ @ 4.5V, 16nC	Fairchild
D1	MBR0520LTI	Schottky Diode	SOD-123		
L1	DO3316P-472	Inductor		4.7 µH, 4.8Arms 18 mΩ	Coilcraft
$C_{IN}1$	16SP100M	Aluminum Electrolytic	10mm x 6mm	100 µF, 16V, 2.89Arms	Sanyo
C_O1	6SP220M	Aluminum Electrolytic	10mm x 6mm	220 µF, 6.3V 3.1Arms	Sanyo
C_{CC}, C_{BOOT}, $C_{IN}2$, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1 µF, 10%	Vishay
C_{C3}	VJ0805Y332KXXA	Capacitor	0805	3300 pF, 10%	Vishay
C_{SS}	VJ0805A123KXAA	Capacitor	0805	12 nF, 10%	Vishay
C_{C2}	VJ0805A821KXAA	Capacitor	0805	820 pF 10%	Vishay
C_{C1}	VJ0805A220KXAA	Capacitor	0805	22 pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	0805	10.0 kΩ 1%	Vishay
R_{FB1}	CRCW08054991F	Resistor	0805	4.99 kΩ1%	Vishay
R_{FADJ}	CRCW08051003F	Resistor	0805	100 kΩ 1%	Vishay
R_{C2}	CRCW08052101F	Resistor	0805	2.1 kΩ 1%	Vishay
R_{CS}	CRCW08052101F	Resistor	0805	2.1 kΩ 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	0805	10.0Ω 1%	Vishay
R_{C1}	CRCW08055492F	Resistor	0805	54.9 kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	0805	100 kΩ 5%	Vishay
C_{CLK}	VJ0805A560KXAA	Capacitor	0805	56 pF, 10%	Vishay

Example Circuits (Continued)

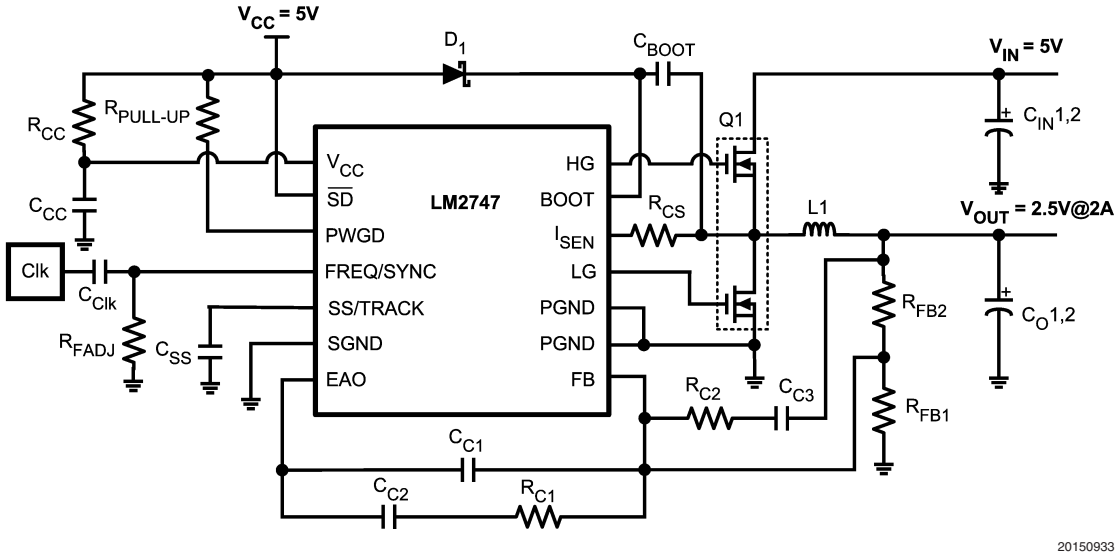


FIGURE 18. 5V to 2.5V @ 2A, f_{sw} = 300 kHz

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U1	LM2747	Synchronous Controller	TSSOP-14		NSC
Q1	FDS6898A	Dual N-MOSFET	SO-8	20V, 10 mΩ @ 4.5V, 16 nC	Fairchild
D1	MBR0520LTI	Schottky Diode	SOD-123		
L1	DO3316P-682	Inductor		6.8 µH, 4.4Arms, 27 mΩ	Coilcraft
$C_{IN}1$	16SP100M	Aluminum Electrolytic	10mm x 6mm	100 µF, 16V, 2.89Arms	Sanyo
C_O1	10SP56M	Aluminum Electrolytic	6.3mm x 6mm	56 µF, 10V 1.7Arms	Sanyo
C_{CC}, C_{BOOT}, $C_{IN}2$, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1 µF, 10%	Vishay
C_{C3}	VJ0805Y182KXXA	Capacitor	0805	1800 pF, 10%	Vishay
C_{SS}	VJ0805A123KXAA	Capacitor	0805	12 nF, 10%	Vishay
C_{C2}	VJ0805A821KXAA	Capacitor	0805	820 pF 10%	Vishay
C_{C1}	VJ0805A330KXAA	Capacitor	0805	33 pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	0805	10.0 kΩ 1%	Vishay
R_{FB1}	CRCW08053161F	Resistor	0805	3.16 kΩ 1%	Vishay
R_{FADJ}	CRCW08051003F	Resistor	0805	100 kΩ 1%	Vishay
R_{C2}	CRCW08051301F	Resistor	0805	1.3 kΩ 1%	Vishay
R_{CS}	CRCW08052101F	Resistor	0805	2.1 kΩ 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	0805	10.0Ω 1%	Vishay
R_{C1}	CRCW08053322F	Resistor	0805	33.2 kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	0805	100 kΩ 5%	Vishay
C_{CLK}	VJ0805A560KXAA	Capacitor	0805	56 pF, 10%	Vishay

Example Circuits (Continued)

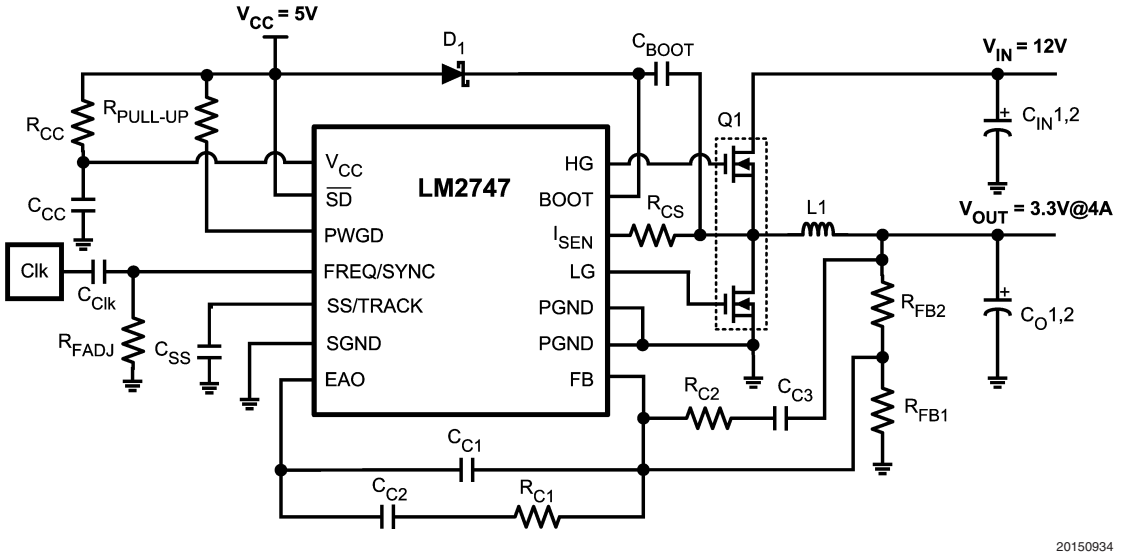
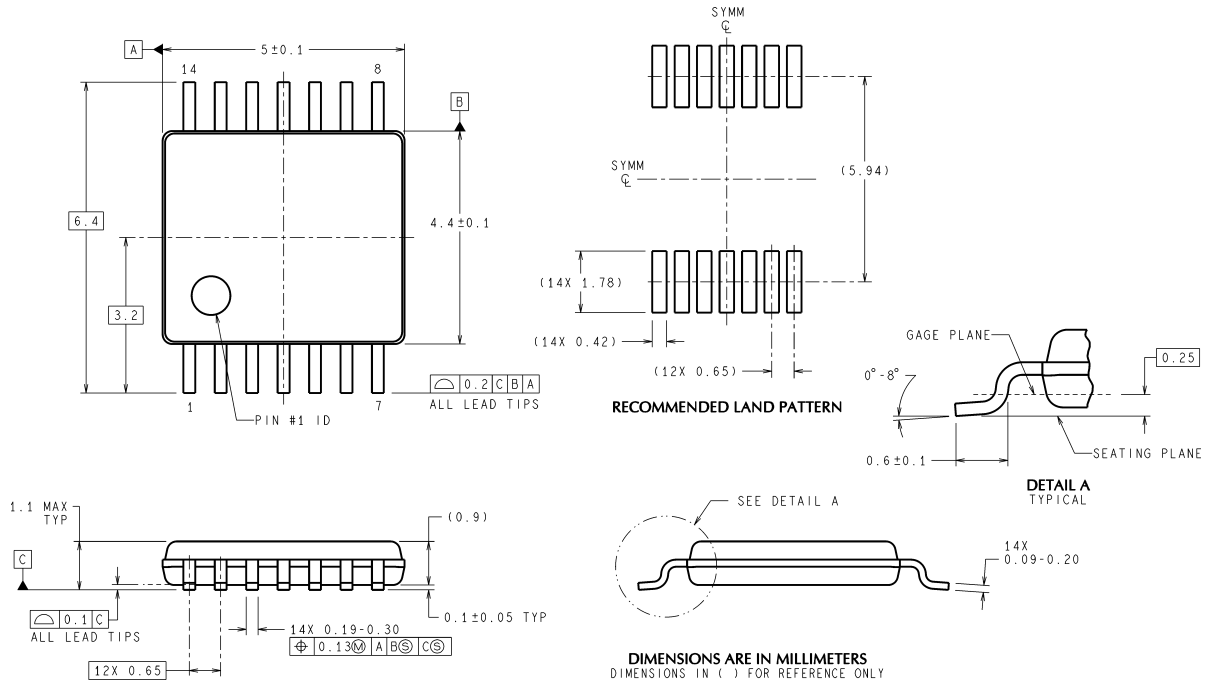


FIGURE 19. 12V to 3.3V @ 4A, f_{SW} = 300kHz

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U1	LM2747	Synchronous Controller	TSSOP-14		NSC
Q1	FDS6898A	Dual N-MOSFET	SO-8	20V, 10 mΩ @ 4.5V, 16 nC	Fairchild
D1	MBR0520LTI	Schottky Diode	SOD-123		
L1	DO3316P-332	Inductor		3.3 µH, 5.4Arms 15 mΩ	Coilcraft
$C_{IN}1$	16SP100M	Aluminum Electrolytic	10mm x 6mm	100 µF, 16V, 2.89Arms	Sanyo
C_O1	6SP220M	Aluminum Electrolytic	10mm x 6mm	220 µF, 6.3V 3.1Arms	Sanyo
C_{CC}, C_{BOOT}, $C_{IN}2$, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1 µF, 10%	Vishay
C_{C3}	VJ0805Y222KXXA	Capacitor	0805	2200 pF, 10%	Vishay
C_{SS}	VJ0805A123KXAA	Capacitor	0805	12 nF, 10%	Vishay
C_{C2}	VJ0805Y332KXXA	Capacitor	0805	3300 pF 10%	Vishay
C_{C1}	VJ0805A820KXAA	Capacitor	0805	82 pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	0805	10.0 kΩ 1%	Vishay
R_{FB1}	CRCW08052211F	Resistor	0805	2.21 kΩ 1%	Vishay
R_{FADJ}	CRCW08051003F	Resistor	0805	100 kΩ 1%	Vishay
R_{C2}	CRCW08052611F	Resistor	0805	2.61 kΩ 1%	Vishay
R_{CS}	CRCW08054121F	Resistor	0805	4.12 kΩ 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	0805	10.0Ω 1%	Vishay
R_{C1}	CRCW08051272F	Resistor	0805	12.7kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	0805	100 kΩ 5%	Vishay
C_{CLK}	VJ0805A560KXAA	Capacitor	0805	56 pF, 10%	Vishay

Physical Dimensions inches (millimeters) unless otherwise noted



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