

MOSFET - Power, Single N-Channel

100 V, 10.5 mΩ, 51 A

FDD86069-F085

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Wettable Flank for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	100	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	51	A
		$T_C = 100^\circ\text{C}$		36	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D	68.2	W
		$T_C = 100^\circ\text{C}$		34.1	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	10.9	A
		$T_A = 100^\circ\text{C}$		7.7	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	3.1	W
		$T_A = 100^\circ\text{C}$		1.6	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM}	328	A	
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)			I_S	56.8	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 3.7 \text{ A}$)			E_{AS}	245	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	2.2	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	48.1	

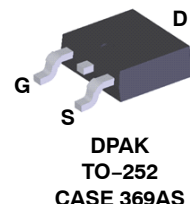
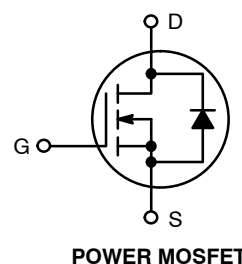
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



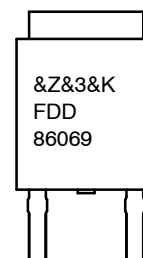
ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	10.5 mΩ @ 10 V	51 A



MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = Data Code (Year & Week)
 &K = Lot
 FDD86069 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDD86069–F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			58		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V, T _J = 25°C			1	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 109 μA	2	3.1	4.5	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			–7.45		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 19.5 A		8.9	10.5	mΩ

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V		1332		pF
Output Capacitance	C _{oss}			825		
Reverse Transfer Capacitance	C _{rss}			12		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 50 V, I _D = 19.5 A		19		nC
Threshold Gate Charge	Q _{G(TH)}			2.5		
Gate-to-Source Charge	Q _{GS}			8		
Gate-to-Drain “Miller” Charge	Q _{GD}			4		
Plateau Voltage	V _{GP}			6		

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, V _{GS} = 10 V, I _D = 19.5 A, R _G = 6 Ω		7.7		ns
Turn-On Rise Time	t _r			15		
Turn-Off Delay Time	t _{d(off)}			15.1		
Turn-Off Fall Time	t _f			11		

DRAIN-SOURCE DIODE CHARACTERISTICS

Source-to-Drain Diode Voltage	V _{SD}	I _{SD} = 19.5 A, V _{GS} = 0 V		0.85	1.2	V
Reverse Recovery Time	T _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 19.5 A		48		ns
Charge Time	t _a			22		
Discharge Time	t _b			26		
Reverse Recovery Charge	Q _{RR}			37		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

DEVICE ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Shipping†
FDD86069–F085	FDD86069	DPAK (TO–252) (Pb–Free)	13"	16 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

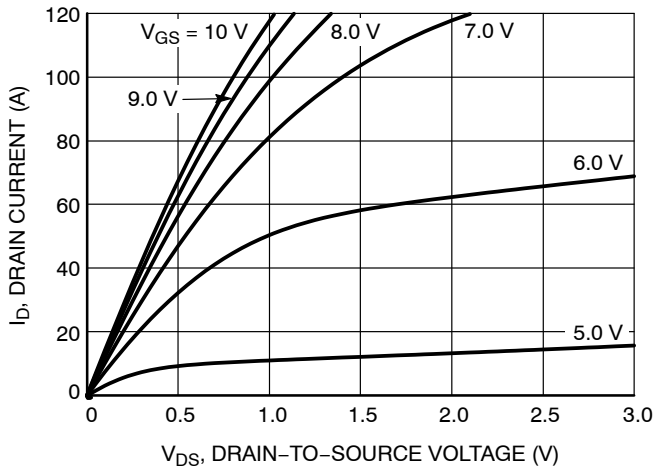


Figure 1. On-Region Characteristics

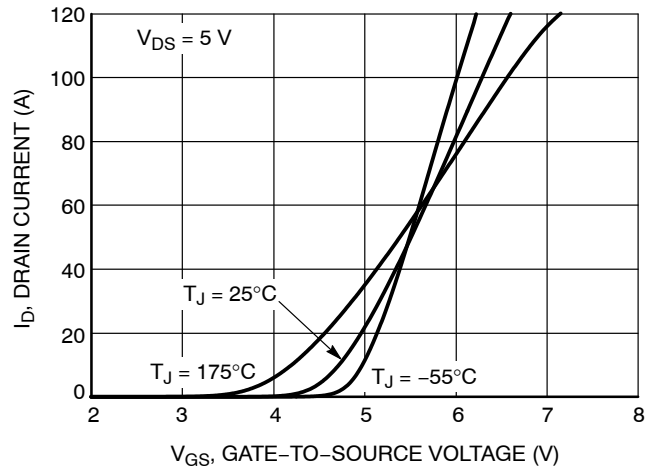


Figure 2. Transfer Characteristics

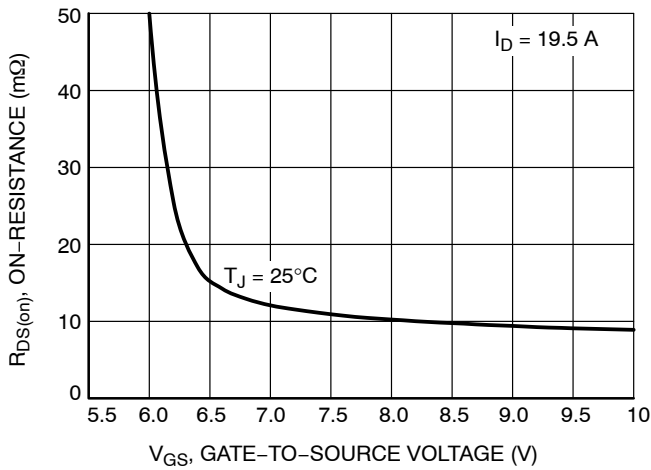


Figure 3. On-Resistance vs. Gate-to-Source Voltage

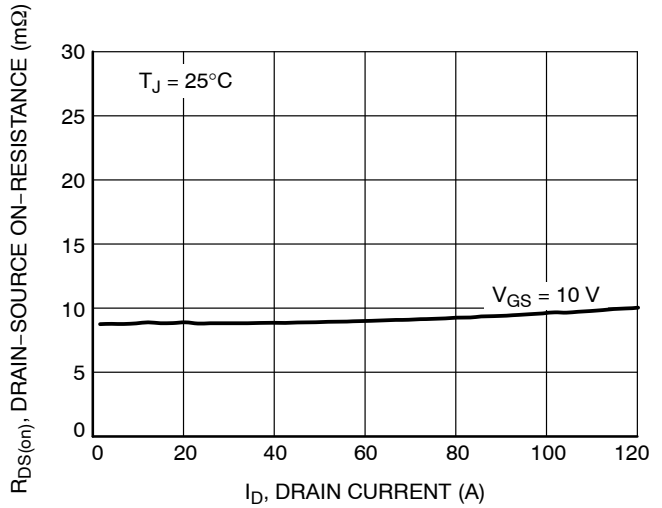


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

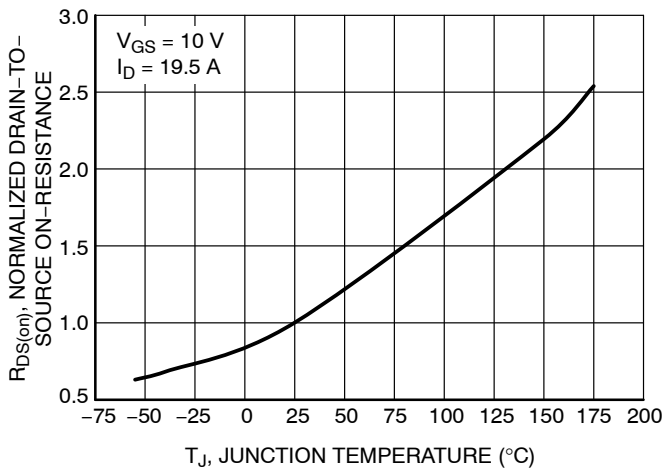


Figure 5. On-Resistance Variation with Temperature

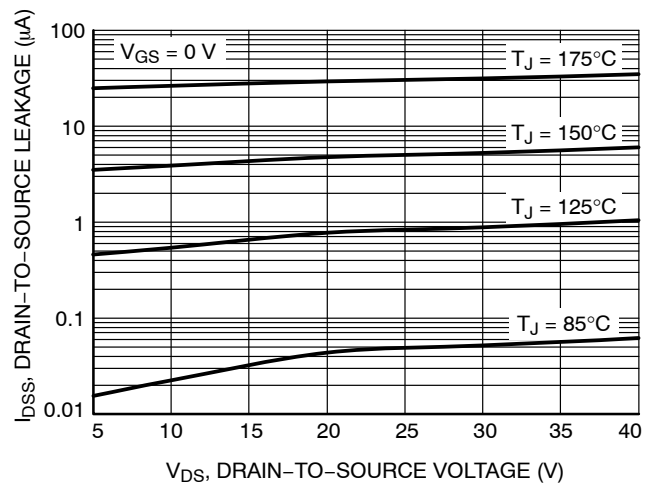


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

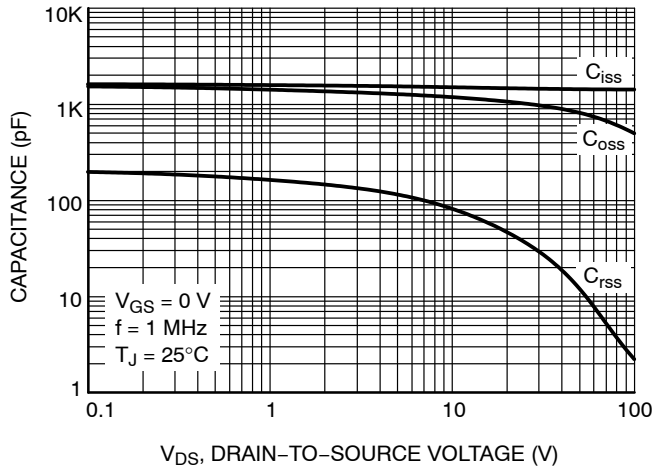


Figure 7. Capacitance Variation

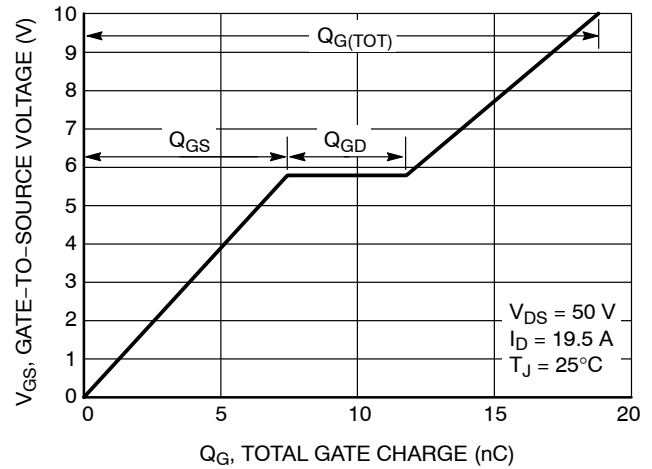


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

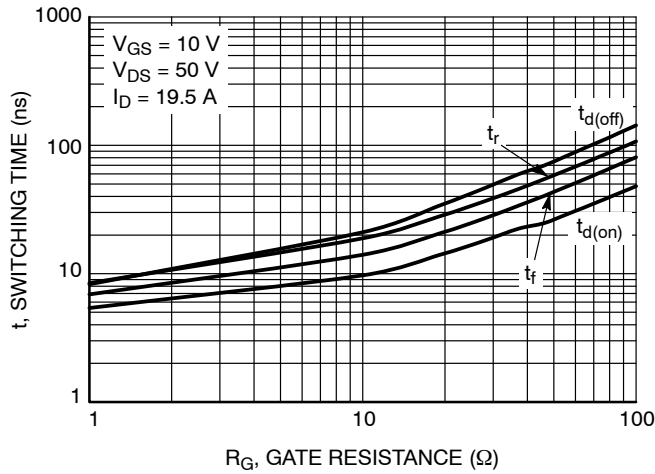


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

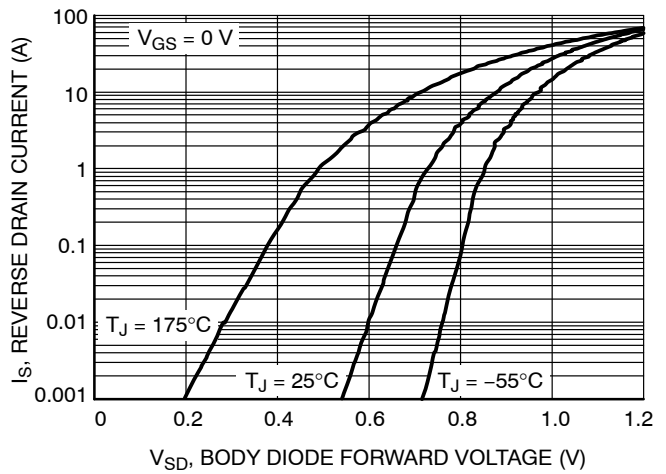


Figure 10. Diode Forward Voltage vs. Current

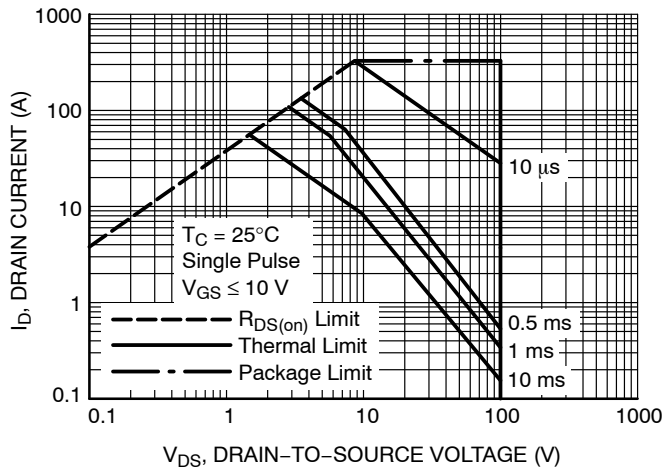


Figure 11. Forward Biased Safe Operating Area

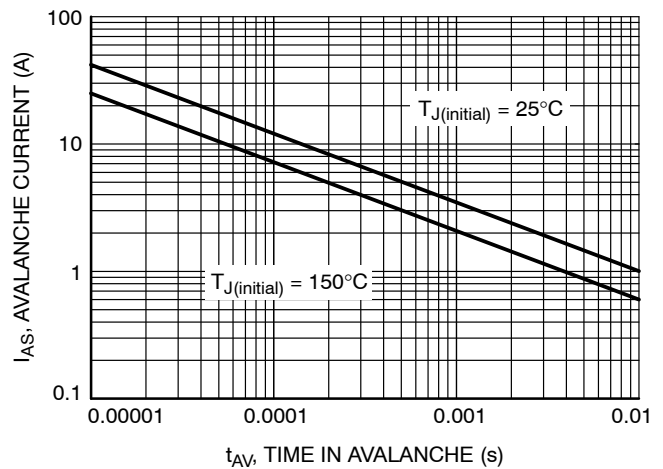


Figure 12. Avalanche Characteristics

TYPICAL CHARACTERISTICS

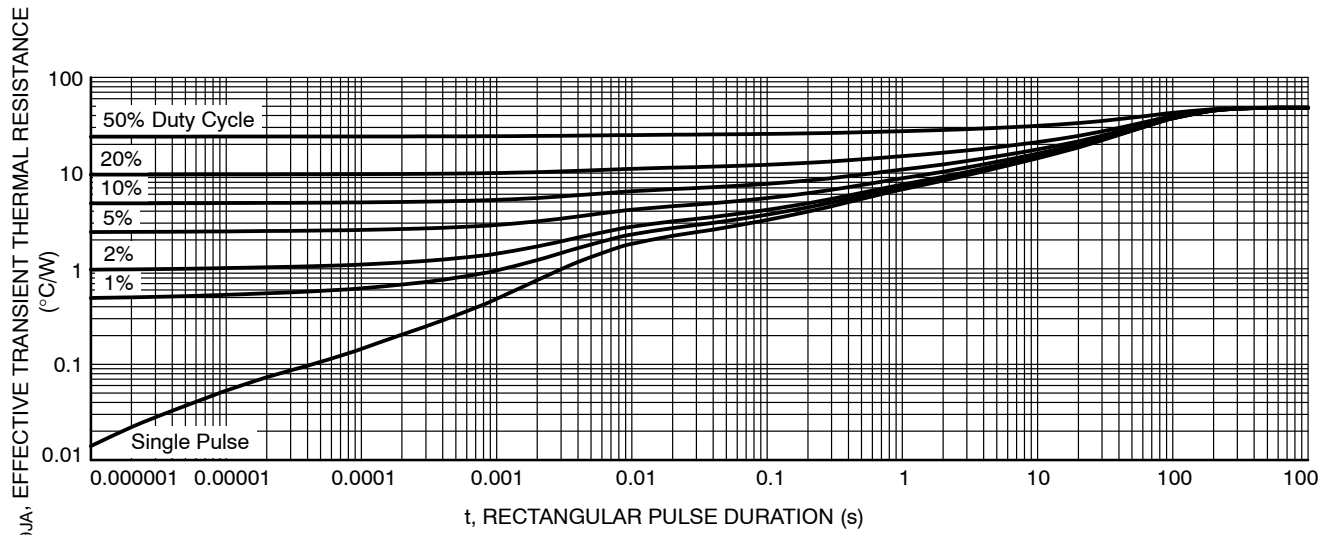
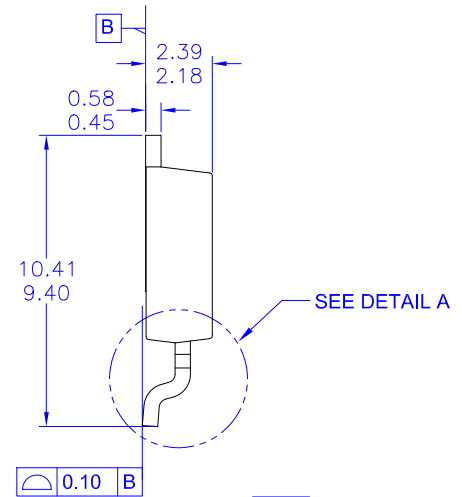
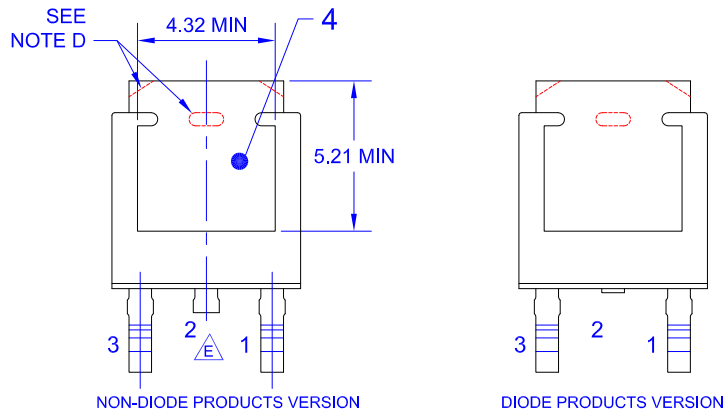
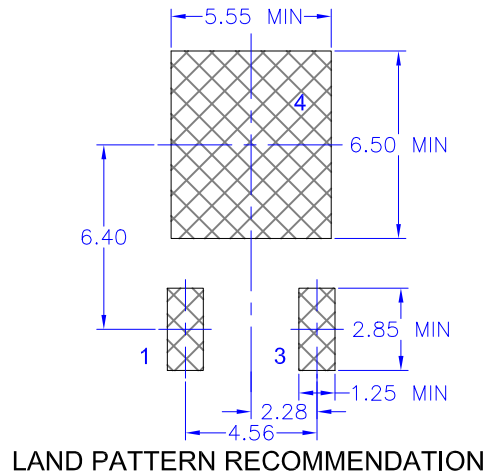
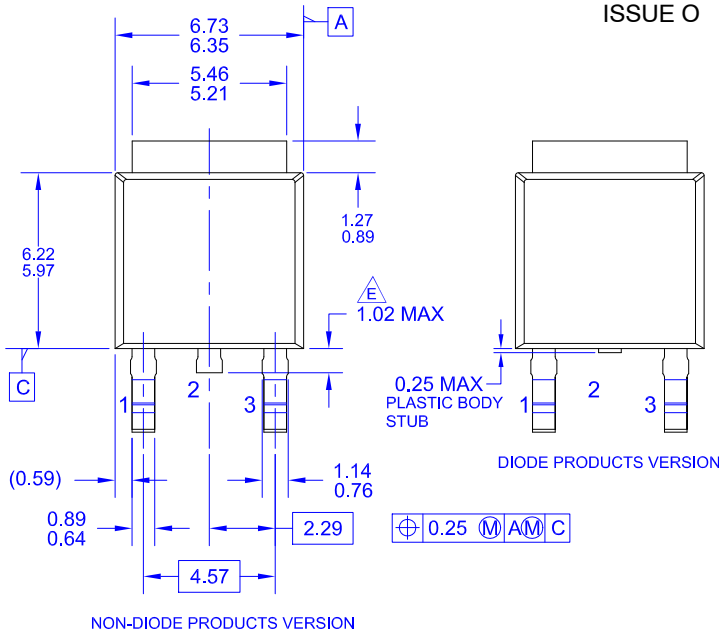


Figure 13. Thermal Response

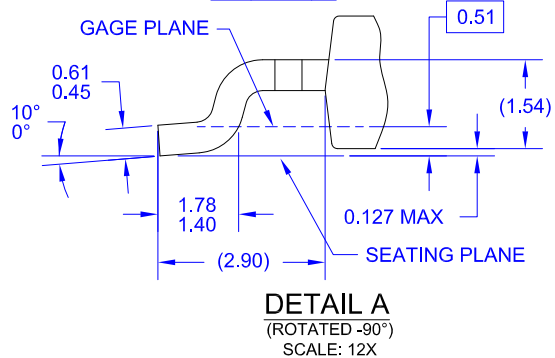
PACKAGE DIMENSIONS

DPAK3 (TO-252 3 LD)
CASE 369AS
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

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