

Lower Power 3.3V CMOS Fast SRAM 256K (32K x 8-Bit)

Features

- Ideal for high-performance processor secondary cache
- Commercial (0°C to +70°C) and Industrial (-40°C to +85°C) temperature range options
- Fast access times:
- Commercial and Industrial: 12/15/20ns
- Low standby current (maximum):
 - 2mA full standby
- Small packages for space-efficient layouts:
 - 28-pin 300 mil SOJ
 - 28-pin TSOP Type I
- Produced with advanced high-performance CMOS technology
- Inputs and outputs are LVTTL-compatible
- Single 3.3V(±0.3V) power supply
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram

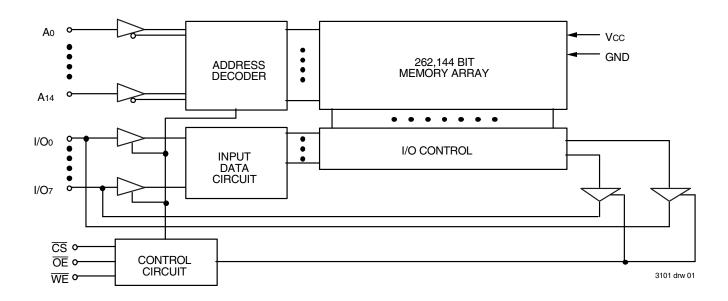
Description

The IDT71V256SA is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using a high-performance, high-reliability CMOS technology.

The IDT71V256SA has outstanding low power characteristics while at the same time maintaining very high performance. Address access times of as fast as 12ns are ideal for 3.3V secondary cache in 3.3V desktop designs.

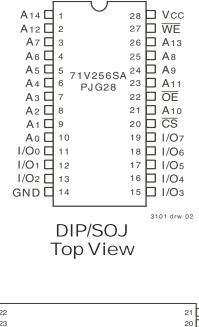
When power management logic puts the IDT71V256SA in standby mode, its very low power characteristics contribute to extended battery life. By taking \overline{CS} HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as \overline{CS} remains HIGH. Furthermore, under full standby mode (\overline{CS} at CMOS level, f=0), power consumption is guaranteed to always be less than 6.6mW and typically will be much smaller.

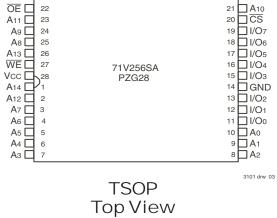
The IDT71V256SA is packaged in a 28-pin 300 mil SOJ and a 28-pin 300 mil TSOP Type I.





Pin Configurations⁽¹⁾





NOTE:

1. This text does not indicate orientation of actual part-marking.

Pin Descriptions

Name	Description
A0 - A14	Addresses
I/O0 - I/O7	Data Input/Output
<u>C</u> S	Chip Select
WE	Write Enable
ŌĒ	Output Enable
GND	Ground
Vcc	Power

3101 tbl 01

Truth Table⁽¹⁾

WE	<u>CS</u>	ŌĒ	I/O	Function
Х	Н	Х	High-Z	Standby (IsB)
Х	Vнс	Х	High-Z	Standby (Isb1)
Н	L	Н	High-Z	Output Disable
Н	L	L	Dout	Read
L	L	Х	Din	Write
				3101 tbl 02

NOTE:

1. H = VIH, L = VIL, X = Don't Care

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l	Unit
Vcc	Supply Voltage Relative to GND	-0.5 to +4.6	V
VTERM ⁽²⁾	Terminal Voltage Relative to GND	-0.5 to Vcc+0.5	V
Tbias	Temperature Under Bias	-55 to +125	٥C
Tstg	Storage Temperature	-55 to +125	٥C
Рт	Power Dissipation	1.0	W
Ιουτ	DC Output Current	50	mA
		-	3101 tbl 03

NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Input, Output, and I/O terminals; 4.6V maximum.

Capacitance

 $(TA = +25^{\circ}C, f = 1.0MHz, SOJ package)$

Symbol	Parameter ⁽¹⁾	Conditions	Мах.	Unit
Cin	Input Capacitance	VIN = 3dV	6	pF
Соит	Output Capacitance	Vout = 3dV	7	pF
				3101 tbl 04

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	$3.3V \pm 0.3V$
Industrial	-40°C to +85°C	0V	$3.3V \pm 0.3V$

3101 tbl 05



Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	۷
GND	Ground	0	0	0	V
Vih	Input High Voltage - Inputs	2.0		Vcc +0.3	V
Vih	Input High Voltage - I/O	2.0		Vcc +0.3	V
VIL	Input Low Voltage	-0.3(1)		0.8	V
NOTE				3	101 tbl 06

NOTE:

1. VIL (min.) = -2.0V for pulse width less than 5ns, once per cycle.

DC Electrical Characteristics⁽¹⁾

(Vcc = 3.3V ± 0.3V, VLc = 0.2V, VHc = Vcc - 0.2V, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	71V256SA12	71V256SA15	71V256SA20	Unit
lcc	Dynamic Operating Current $\overline{\text{CS}} \leq \text{VIL}$, Outputs Open, Vcc = Max., f = fMax ⁽²⁾	90	85	85	mA
ISB	$\frac{Standby Power Supply Current (TTL Level)}{CS} = VIH, Vcc = Max., Outputs Open, f = fmax(2)$	20	20	20	mA
ISB1	$ \begin{array}{l} \hline Full Standby Power Supply Current (CMOS Level) \\ \hline CS \\ \geq VHC, Vcc = Max., Outputs Open, f = 0^{(2)}, \\ \hline VIN \\ \leq VLc \ or \ VIN \\ \geq VHc \end{array} $	2	2	2	mA
					3101 tbl 07

NOTES:

1. All values are maximum guaranteed values.

2. fmax = 1/trc, only address inputs cycling at fmax; f = 0 means that no inputs are cycling.

DC Electrical Characteristics

 $(VCC = 3.3V \pm 0.3V)$

				IDT71V256SA	l	
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
ILI	Input Leakage Current	Vcc = Max., VIN = GND to Vcc			2	μA
Ilo	Output Leakage Current	Vcc = Max., \overline{CS} = VIH, Vout = GND to Vcc	_	_	2	μA
Vol	Output Low Voltage	Iol = 8mA, Vcc = Min.	_	_	0.4	V
Vон	Output High Voltage	IOH = -4mA, Vcc = Min.	2.4			V

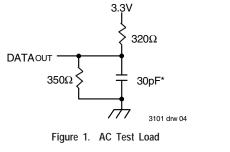
3101 tbl 08

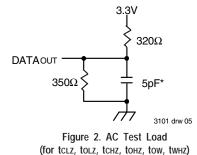


AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3101 tbl 09





*Includes scope and jig capacitances

AC Electrical Characteristics

(Vcc = 3.3V ± 0.3V, Commercial and Industrial Temperature Ranges)

		71V25	6SA12	71V25	6SA15	71V25	6SA20	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cy	cle							
trc	Read Cycle Time	12		15		20		ns
taa	Address Access Time		12		15		20	ns
tacs	Chip Select Access Time		12		15		20	ns
tclz ⁽¹⁾	Chip Select to Output in Low-Z	5		5	_	5		ns
tcHz ⁽¹⁾	Chip Select to Output in High-Z	0	8	0	9	0	10	ns
toe	Output Enable to Output Valid		6		7		8	ns
tolz ⁽¹⁾	Output Enable to Output in Low-Z	3		0		0		ns
tohz ⁽¹⁾	Output Disable to Output in High-Z	2	6	0	7	0	8	ns
tон	Output Hold from Address Change	3		3		3		ns
Write Cy	/cle							
twc	Write Cycle Time	12		15		20		ns
taw	Address Valid to End-of-Write	9		10		15		ns
tcw	Chip Select to End-of-Write	9		10		15		ns
tas	Address Set-up Time	0		0		0		ns
twp	Write Pulse Width	9		10		15		ns
twr	Write Recovery Time	0		0		0		ns
tdw	Data to Write Time Overlap	6		7	_	8		ns
tdн	Data Hold from Write Time	0		0		0		ns
tow ⁽¹⁾	Output Active from End-of-Write	4		4		4		ns
twHz ⁽¹⁾	Write Enable to Output in High-Z	1	8	1	9	1	10	ns

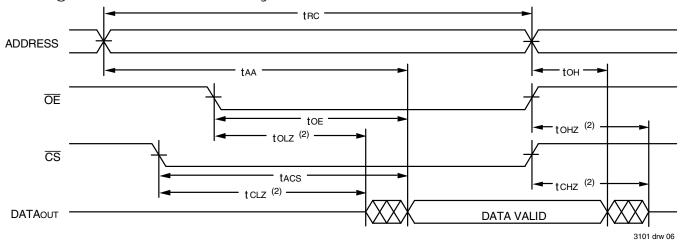
3101 tbl 10

NOTE:

1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.



Timing Waveform of Read Cycle No. 1⁽¹⁾

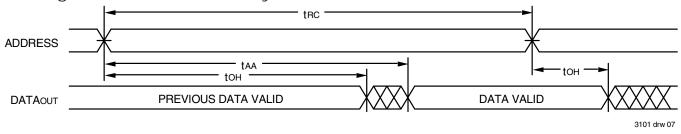


NOTES:

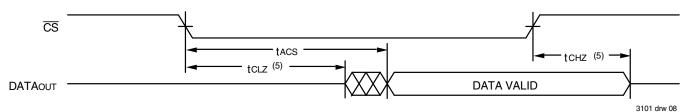
1. WE is HIGH for Read cycle.

2. Transition is measured ±200mV from steady state.

Timing Waveform of Read Cycle No. 2^(1,2,4)



Timing Waveform of Read Cycle No. 3^(1,3,4)



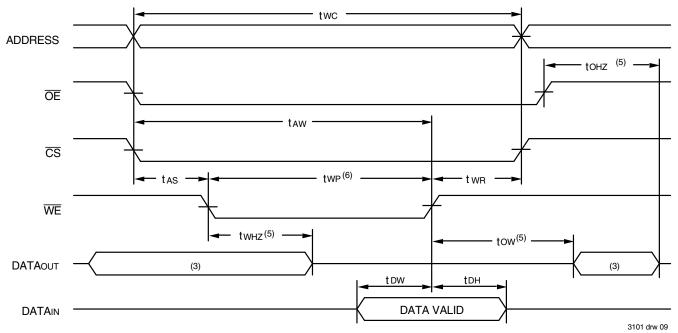
NOTES:

- 1. WE is HIGH for Read cycle.
- 2. Device is continuously selected, \overline{CS} is LOW.
- 3. Address valid prior to or coincident with \overline{CS} transition LOW.
- 4. $\overline{\text{OE}}$ is LOW.
- 5. Transition is measured ±200mV from steady state.



Commercial and Industrial Temperature Ranges

Timing Waveform of Write Cycle No. 1 (WE Controlled Timing)^(1,2,4,6)

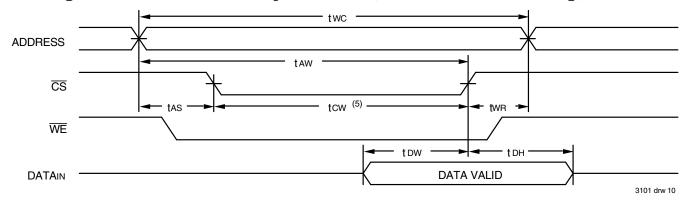


NOTES:

- 1. A write occurs during the overlap of a LOW CS and a LOW WE.
- 2. two is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
- 3. During this period, I/O pins are in the output state so that the input signals must not be applied.
- 4. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
- 5. Transition is measured ±200mV from steady state.

6. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of twp or (twHz + tbw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

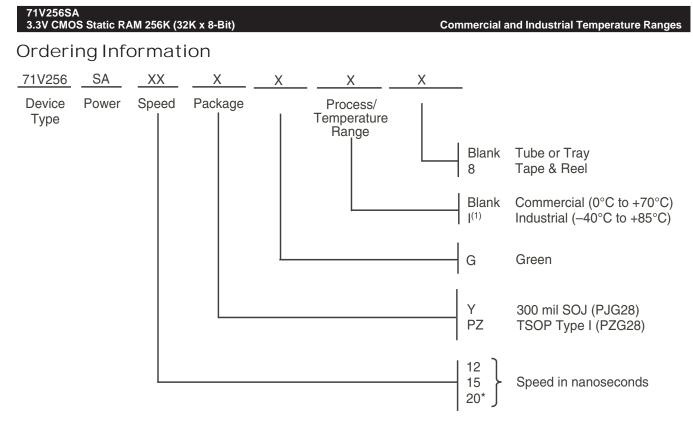
Timing Waveform of Write Cycle No. 2 (CS Controlled Timing)^(1,2,3,4)



NOTES:

- 1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be HIGH during all address transitions.
- 2. A write occurs during the overlap of a LOW $\overline{\text{CS}}$ and a LOW $\overline{\text{WE}}$.
- 3. two is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
- 4. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
- 5. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of twp or (twHz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.





* Available in TSOP package only.

3101 drw 11

NOTE:

1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
12	71V256SA12PZG	PZG28	TSOP	С
	71V256SA12PZG8	PZG28	TSOP	С
	71V256SA12PZGI	PZG28	TSOP	I
	71V256SA12PZGI8	PZG28	TSOP	I
	71V256SA12YG	PJG28	SOJ	С
	71V256SA12YG8	PJG28	SOJ	С
	71V256SA12YGI	PJG28	SOJ	I
	71V256SA12YGI8	PJG28	SOJ	I
15	71V256SA15PZG	PZG28	TSOP	С
	71V256SA15PZG8	PZG28	TSOP	С
	71V256SA15PZGI	PZG28	TSOP	Ι
	71V256SA15PZGI8	PZG28	TSOP	I
	71V256SA15YG	PJG28	SOJ	С
	71V256SA15YG8	PJG28	SOJ	С
	71V256SA15YGI	PJG28	SOJ	Ι
	71V256SA15YGI8	PJG28	SOJ	Ι
20	71V256SA20PZG	PZG28	TSOP	С
	71V256SA20PZG8	PZG28	TSOP	С
	71V256SA20PZGI	PZG28	TSOP	Ι
	71V256SA20PZGI8	PZG28	TSOP	Ι

Datasheet Document History

1/7/00		Updated to new format
	Pg. 1, 3, 4, 7	Expanded Industrial Temperature offerings
	Pg. 1, 2, 7	Removed 28-pin 300 mil plastic DIP package offering
	Pg. 6	Removed Note No. 1 from Write Cycle No. 1 diagram; renumbered notes and footnotes
	Pg. 7	Revised Ordering Information
	Pg. 8	Added Datasheet Document History
08/09/00	. 9. 0	Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
06/21/02	Pg. 7	Added tape and reel option to the ordering information
01/30/04	Pg. 7	Added "restricted hazardous substance device" to order information.
02/20/09	Pg. 7	Removed "IDT" from ordering parts
06/11/12	Pg. 3	Corrected Recommended DC Operation Conditions Max VIH from 5.0 to Vcc+0.3V
	Pg. 7	Added Green designator to ordering information
	Pg. 7	Corrected footnote in the ordering information from "available in SOJ package only" to
		"available in TSOP package only"
07/24/14	Pg.7	Added tube or tray to the ordering information
08/18/15	Pg.1 & 7	Removed commercial 10ns speed offering & added green parts available to features
	Pg.2 & 7	Removed "-X" extensions from all pin configurations SOJ28 & TSOP28
	Pg. 3 & 4	Removed commercial 10ns speed offering columns from the DC & AC Elec tables
	Pg.7	Updated the Industrial and Green footnotes in the Ordering Information
06/02/20	Pg.1 - 9	Rebranded as Renesas datasheet
	Pg.2 & 7	Updated package codes
	Pg.7	Added Orderable Part Information
	5	

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