Datasheet

Power Supply IC Series for TFT-LCD Panels

Output voltage fixed-type Multi-channel System Power Supply IC

BD8174MUV

General Description

The BD8174MUV is a system power supply IC that generates 6 power supply channels required by TFT-LCD panels on a single chip.
Output voltage and sequence is fixed so that it is possible to control output with few external components.

Features

- Step-up DC/DC Converter with Built-in 3A FET
- Synchronous Step-down DC/DC Converter with Built-in 2A FET
- High Voltage LDO (50mA)
- Low Voltage LDO (400mA)
- Positive/ Negative Charge Pumps (Integrated-diode)
- 10bit DAC 4CH
- VCOM Amplifier
- Gate Shading Function
- All-output Shut Down Function
- Power Good Function
- Protection Circuits:
  - Under-Voltage Lockout Protection Circuit
  - Thermal Shutdown Circuit
  - Over Current Protection Circuit
  - Over Voltage Protection Circuit
  - Timer Latch Type Short-Circuit Protection Circuit
- Constant Startup Sequence

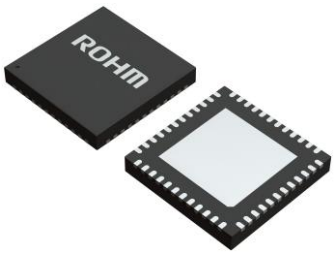
Applications

LCD TV power supplies

Key Specifications

- Power Supply Voltage 1 Range: 10V to 14V
- Oscillating Frequency: 700kHz(Typ)
- Operating Temperature Range: -40°C to +105°C

Package W(Typ) x D(Typ) x H(Max)

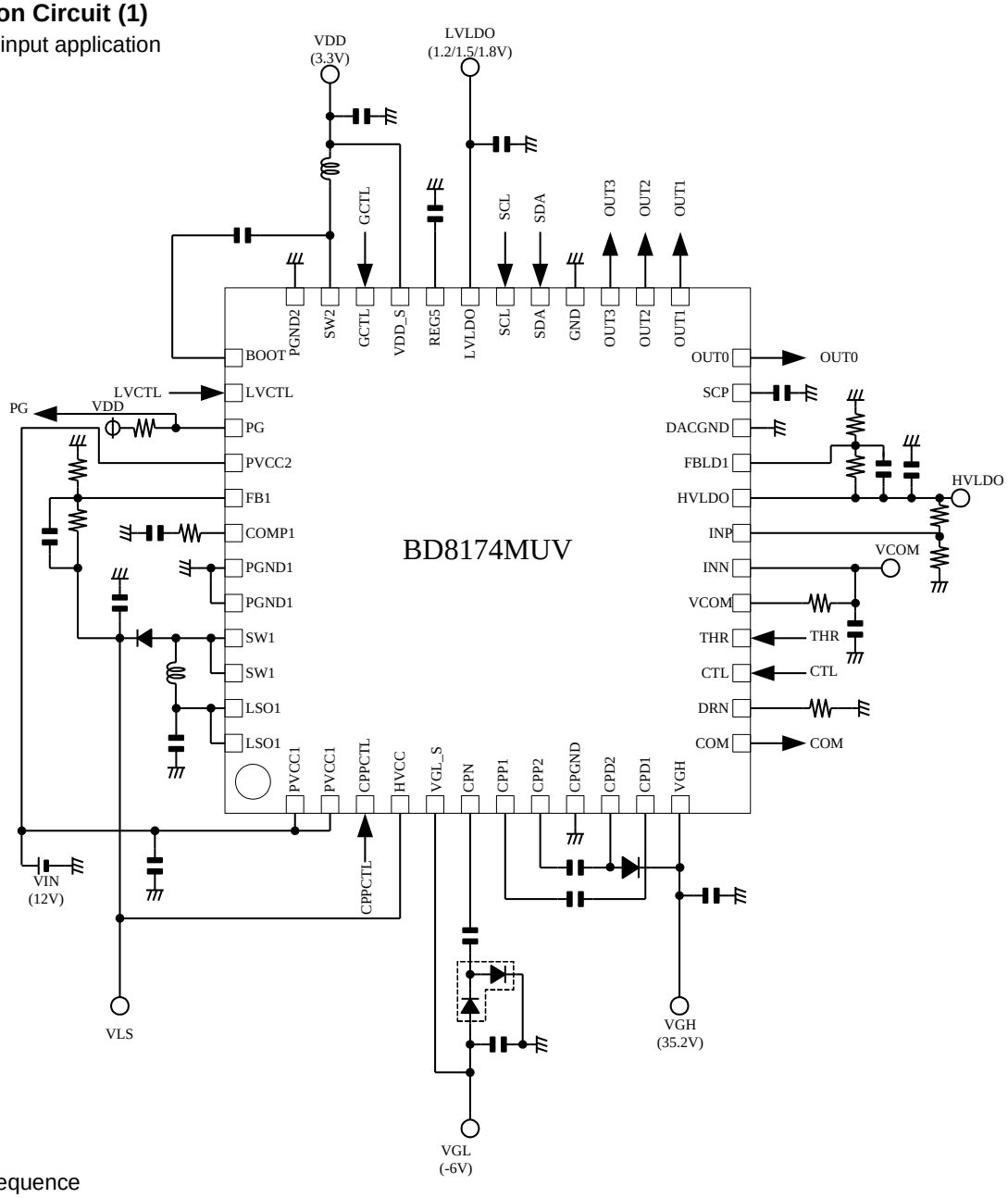


VQFN048V7070
7.00mm x 7.00mm x 1.00mm

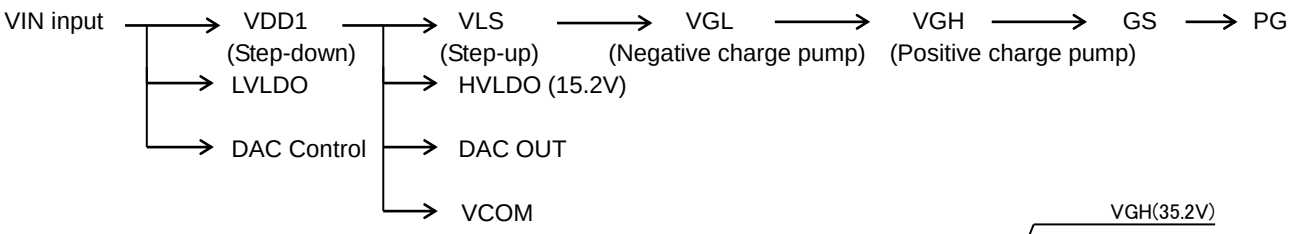
○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Typical Application Circuit (1)

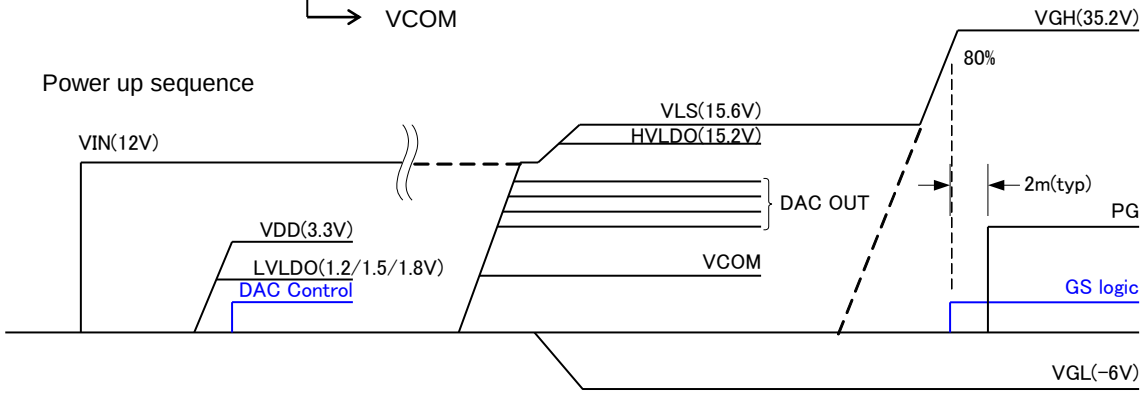
1. VCC12V input application



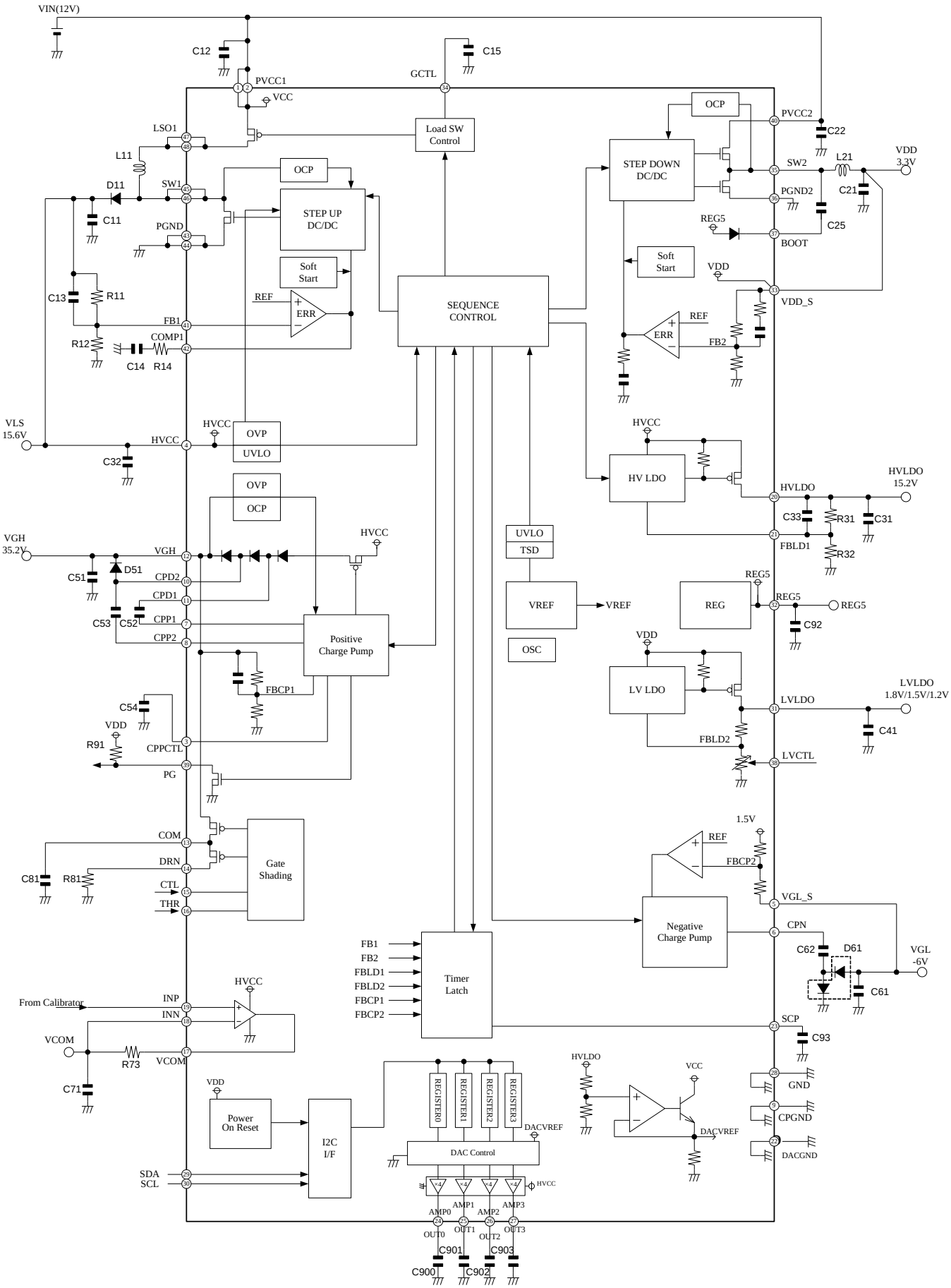
2. Startup sequence



3. Power up sequence



Block Diagram

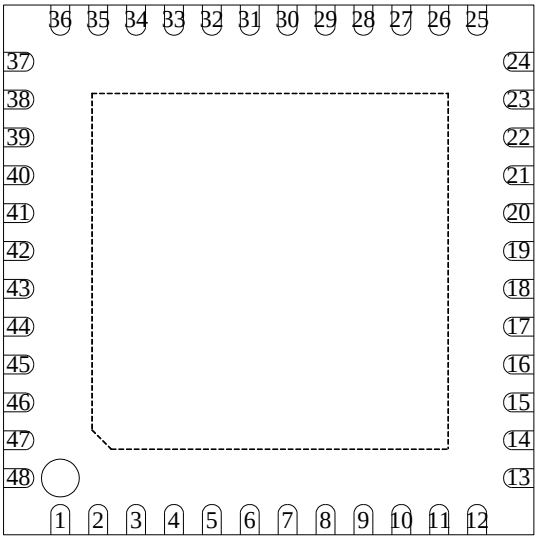


Application Parts List (When VLS=15.6V, HVLDO=15.2V is configured)

PARTS LOCATION	Value	Company	PRODUCT NUMBER
R11	130kΩ+16kΩ	ROHM	MCR01MZPD
R12	10kΩ	ROHM	MCR01MZPD
R14	3kΩ	ROHM	MCR01MZPD
R31	130kΩ+12kΩ	ROHM	MCR01MZPD
R32	10kΩ	ROHM	MCR01MZPD
R73	430Ω	ROHM	MCR18EZHF
R81	4.3kΩ	ROHM	MCR03EZPD
R91	100kΩ	ROHM	MCR01MZPD
C11	10μF	Murata	GRM31CB31E106KA75
C12	10μF	Murata	GRM31CB31E106KA75
C13	100pF	Murata	GRM1882C1H101JA01
C14	2200pF	Murata	GRM188B11H222KA01
C15	-	-	-
C21	10μF	Murata	GRM31CB31E106KA75
C22	10μF	Murata	GRM31CB31E106KA75
C25	0.1μF	Murata	GRM188R11H104KA93
C31	4.7μF	Murata	GRM319B31E475KA75
C32	10μF	Murata	GRM31CB31E106KA75
C33	22pF	Murata	GRM1882C1H220JA01
C41	4.7μF	Murata	GRM21BB31C475KA75
C51	1.0μF	Murata	GRM21BB31H105KA12
C52	0.1μF	Murata	GRM188R11H104KA93
C53	0.1μF	Murata	GRM188R11H104KA93
C54	-	-	-
C61	1.0μF	Murata	GRM188R11H104KA93
C62	22000pF	Murata	GRM188B11H223KA01
C71	1.0μF	Murata	GRM21BB31H105KA12
C81	1000pF	Murata	GRM188B11H102KA01
C92	1.0μF	Murata	GRM21BB31H105KA12
C93	0.1μF	Murata	GRM188R11H104KA93
C900	10μF	Murata	GRM31CB31E106KA75
C901	10μF	Murata	GRM31CB31E106KA75
C902	10μF	Murata	GRM31CB31E106KA75
C903	10μF	Murata	GRM31CB31E106KA75
L11	10μH	TAIYOYUDEN	NR6045T100M
L21	10μH	TAIYO YUDEN	NR6045T100M
D11	-	ROHM	RSX501L-20
D51	-	ROHM	RB162M-40
D61	-	ROHM	RB550EATR

Pin Configuration

TOP VIEW



Pin Description

PIN NO.	Pin name	Function
1	PVCC1	Boost DC/DC load switch input. See Boost DC/DC (1) for more information.
2	PVCC1	Boost DC/DC load switch input. See Boost DC/DC (1) for more information.
3	CPPCTL	Positive charge pump control input. See charge pump (4) for more information.
4	HVCC	Power supply pin for charge pump, buffer amplifier and HV_LDO.
5	VGL_S	Negative charge pump output VGL feedback input.
6	CPN	Negative charge pump regulator driver output. Drive pin for negative charge pump. See charge pump (4) for more information.
7	CPP1	Positive charge pump regulator driver output1. Drive pin for positive charge pump. See charge pump (4) for more information.
8	CPP2	Positive charge pump regulator driver output2. Drive pin for positive charge pump. See charge pump (4) for more information.
9	CPGND	Power grounding pin at charge pump.
10	CPD2	Positive charge pump internal switching diode output2.
11	CPD1	Positive charge pump internal switching diode output1.
12	VGH	Positive charge pump output VGH. Connect output capacitor from this pin to GND.
13	COM	Gate shading output pin.
14	DRN	Termination of the low side switch of the gate voltage shading block.
15	CTL	Gate shading control input pin.
16	THR	Gate shading Low level setting pin.
17	VCOM	VCOM Output
18	INN	VCOM input-.
19	INP	VCOM input+.
20	HVLDO	HV_LDO output pin. Insert output capacitance for GND.
21	FBLD1	HV_LDO feedback input pin.
22	DACGND	GND pin for DAC.
23	SCP	Short protection delay pin. To set short protection delay time, connect capacitor for GND pair. For details, refer to information in common block (6).
24	OUT0	Gamma output pin.
25	OUT1	Gamma output pin.
26	OUT2	Gamma output pin.
27	OUT3	Gamma output pin.
28	GND	Grounding pin.
29	SDA	Serial data input pin.
30	SCL	Serial clock input pin.
31	LVLDO	LV_LDO output pin. Output outputs 1.8V/ 1.5V/ 1.2V (typ). Insert output capacitance for GND.
32	REG5	Internal power supply 5.0V output pin. Connect 0.1µF from this pin to ground.
33	VDD_S	Buck DC/DC output VDD feedback input. No external registance necessary for feedback register.
34	GCTL	Boost DC/DC load switch PGATE control input. For details, refer to information in Boost DC/DC (1).
35	SW2	Buck DC/DC switching output. Due to reduce EMI, make a wiring thick and short.
36	PGND2	Buck DC/DC switching node power grounding pin. Due to reduce EMI, make a wiring thick and short.
37	BOOT	Buck DC/DC bootstrap pin. This pin generates the gate drive voltage for the Buck converter. Connect 0.1µF from this pin to the switch pin of step down converter, SW2.
38	LVCTL	LVLDO output voltage setting pin.
39	PG	Power good output. After positive charge pump output VGH startup, It will be ON. For Buck DC/DC output, Pull-UP and use it. If you don't use it, It will open.
40	PVCC2	Buck DC/DC high side MOSFET power supply input. Connect a capacitor as close to PVCC pin as possiple.

Pin Description – Continued

PIN NO.	Pin name	Function
41	FB1	Boost DC/DC output VLS feedback input. Connect a external resister and insert resistance for phase compensation setting between VLS. For details, refer to information in Boost DC/DC (1).
42	COMP1	Boost DC/DC error amplifier output pin. Connect a resistance for phase compensation and capacitor. For details, refer to information in Boost DC/DC (1).
43	PGND1	Boost DC/DC switching node power ground pin. Due to reduce EMI, make a wiring thick and short.
44	PGND1	Boost DC/DC switching node power ground pin. Due to reduce EMI, make a wiring thick and short.
45	SW1	Boost DC/DC switching output. Due to reduce EMI, make a wiring thick and short.
46	SW1	Boost DC/DC switching output. Due to reduce EMI, make a wiring thick and short.
47	LSO1	Boost DC/DC load switch output. For details, refer to information in Boost DC/DC (1).
48	LSO1	Boost DC/DC load switch output. For details, refer to information in Boost DC/DC (1).

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage 1	V_{PVCC1},V_{PVCC2}	15	V
Power Supply Voltage 2	V_{HVCC}	20	V
SW1 Pin Voltage	V_{SW1}	20	V
VGH Pin Voltage	V_{VGH}	40	V
Maximum Junction Temperature	Tjmax	150	°C
Power Dissipation	Pd	4.83 (Note 1)	W
Operating Temperature Range	Topr	-40 to 105	°C
Storage Temperature Range	Tstg	-55 to 150	°C

(Note 1) To use the IC at temperatures over Ta=25°C, derate power rating by 38.61mW/°C.
When mounted on a four-layer glass epoxy board measuring 74.2mm x 74.2mm x 1.6mm (with all layer of copper foil 5505mm^2).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +105°C)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage 1	V_{PVCC1},V_{PVCC2}	10	14	V
Power Supply Voltage 2	V_{HVCC}	10	18	V
SW1 Pin Voltage	V_{SW1}	-	18	V
SW1 Pin Current	I_{SW1}	-	3 (Note 2)	A
SW2 Pin Current	I_{SW2}	-	2 (Note 2)	A
Power Good Pull-up Voltage	V_{PG}	-	5.5	V
CTL Pin Voltage	V_{GCTL}, V_{CPPCTL}, V_{CTL}	-	5.5	V
THR Pin Voltage	V_{THR}	1.0	2.5	V
LVCTL Pin Voltage	V_{LVCTL}	-	14	V
INP,INN Pin Voltage	V_{INP},V_{INN}	-	14	V

(Note 2) Not to exceed Pd.

Electrical Characteristics (Unless otherwise noted, Ta=25°C, V_{CC}=12V, V_{HVCC}=15V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
【DC/DC】						
Step Up Reference Voltage	V_{LSREF1}	0.985	1.00	1.015	V	
	V_{LSREF2}	0.982	-	1.018	V	-25°C < Ta < 105°C
Step Down Output Voltage	V_{DD1}	3.25	3.30	3.35	V	
	V_{DD2}	3.24	-	3.36	V	-25°C < Ta < 105°C
COMP1 Source Current	I_{CSO}	-	-20	-	μA	V_{COMP1}=1.0V, V_{FB1}=0.5V -25°C < Ta < 105°C
COMP1 Sink Current	I_{CSI}	-	+20	-	μA	V_{COMP1}=1.0V, V_{FB1}=1.5V -25°C < Ta < 105°C
SW1,2, MAX Duty	MDT	75	90	99	%	
SW1 ON Resistance	R_{ON11}	-	0.2	-	Ω	I_{SW}=0.8A
	R_{ON12}	-	0.2	-	Ω	I_{SW}=10mA, -25°C < Ta < 105°C
SW1 Current Limit	I_{SW1OCP}	3	-	-	A	-25°C < Ta < 105°C
SW2 High side ON Resistance	R_{ON2H1}	-	0.2	-	Ω	I_{SW}=0.8A
	R_{ON2H2}	-	0.2	-	Ω	I_{SW}=10mA, -25°C < Ta < 105°C
SW2 Low side ON Resistance	R_{ON2L1}	-	0.2	-	Ω	I_{SW}=0.8A
	R_{ON2L2}	-	0.2	-	Ω	I_{SW}=10mA, -25°C < Ta < 105°C
SW1,2 Leakage Current	I_{SWLEAK}	-5	0	+5	μA	
SW2 Current Limit	I_{SW2OCP}	2	-	-	A	-25°C < Ta < 105°C
GCTL Input High Voltage	V_{GCTLH}	2	-	-	V	-25°C < Ta < 105°C
GCTL Input Low Voltage	V_{GCTLL}	-	-	0.2	V	-25°C < Ta < 105°C
GCTL Input Current	I_{GCTL}	-20	-14.5	-9	μA	V_{GCTL}=0V
VLS Over Voltage Threshold	V_{OVP1}	18	19	20	V	-25°C < Ta < 105°C
【Load Switch】						
ON Resistance	$R_{ONLSO11}$	-	0.2	-	Ω	I_O=-0.8A
	$R_{ONLSO12}$	-	0.2	-	Ω	I_O=-10mA, -25°C < Ta < 105°C
Soft Start Period 85%	t_{SS_LSO1}	0.75	1.5	3.0	ms	R_{LSO1}=10kΩ, -25°C < Ta < 105°C
【High Voltage LDO】						
LDO_H Reference Voltage	V_{HVLDO_H1}	0.99	1.00	1.01	V	
	V_{HVLDO_H2}	0.982	-	1.018	V	-25°C < Ta < 105°C
I/O Voltage Differential H	$V_{HVDPLDH}$	-	0.2	0.5	V	V_{HVCC}=15V, I_O=50mA
【Low Voltage LDO】						
LDO Output Voltage	V_{LVLDO_H1}	1.18	1.2	1.22	V	LVCTL=H
	V_{LVLDO_H2}	1.16	-	1.24	V	-25°C < Ta < 105°C,LVCTL=H
	V_{LVLDO_M1}	1.77	1.8	1.83	V	LVCTL=M
	V_{LVLDO_M2}	1.74	-	1.86	V	-25°C < Ta < 105°C,LVCTL=M
	V_{LVLDO_L1}	1.48	1.5	1.52	V	LVCTL=L
	V_{LVLDO_L2}	1.45	-	1.55	V	-25°C < Ta < 105°C,LVCTL=L
I/O Voltage Differential H	$V_{LVDPLDH}$	-	0.2	0.5	V	V_{DD}=3.3V, I_O=200mA

Electrical Characteristics – continued (Unless otherwise noted, Ta=25°C, V_{CC}=12V, V_{HVCC}=15V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
【Charge pumps】						
VGH Output Voltage	V_{VGH1}	34.6	35.2	35.8	V	
	V_{VGH2}	34.5	-	35.9	V	-25°C < Ta < 105°C
VGL Output Voltage	V_{VGL1}	-6.12	-6.0	-5.88	V	
	V_{VGL2}	-6.15	-	-5.85	V	-25°C < Ta < 105°C
CPP1,2,CPN High side ON Resistance	R_{ONCH}	-	5	-	Ω	-25°C < Ta < 105°C
CPP1,2,CPN Low side ON Resistance	R_{ONCL}	-	5	-	Ω	-25°C < Ta < 105°C
CPPCTL Input High Voltage	V_{CPCTLH}	2	-	-	V	-25°C < Ta < 105°C
CPPCTL Input Low Voltage	V_{CPCTLL}	-	-	0.2	V	-25°C < Ta < 105°C
CPPCTL Pin Input Current	I_{CPCTL}	-20	-14.5	-9	μA	V_{CPPCTL}=0V
PG ON Voltage	PGH	-	80	-	%	
PG OFF Voltage	PGL	-	60	-	%	
VGH Over Voltage Threshold	V_{OVP2}	36.5	37.5	38.5	V	
	V_{OVP3}	36	-	39	V	-25°C < Ta < 105°C
【Gate Shading】						
CTL Input High Voltage	V_{CTLH}	2.3	-	-	V	-25°C < Ta < 105°C
CTL Input Low Voltage	V_{CTLL}	-	-	1.0	V	-25°C < Ta < 105°C
VGH-COM ON Resistance	R_{ONSRC}	-	5	-	Ω	-25°C < Ta < 105°C
COM-DRN ON Resistance	R_{ONDRN}	-	30	-	Ω	-25°C < Ta < 105°C
CTL High Input Current	I_{CTLH}	16.5	33	66	μA	Input Voltage=3.3V, -25°C < Ta < 105°C
【Operation amplifier】						
Input Offset Voltage	V_{OFF}	-15	-	+15	mV	
Input Bias Current	I_{BAMP}	-1.2	-	+1.2	μA	
VCOM Output Current Capability	I_{COM}	50	150	-	mA	V_{VCOM}=0V,INN=VCOM,V_{INP}=15V, -25°C < Ta < 105°C
Slew Rate	SRCOM	-	15	-	V/μs	Without external components
Load Stability	Δ Vo	-15	0	+15	mV	I_O=-1mA to +1mA
Output Swing-High	V_{OH}	V_{HVCC}-1.0	V_{HVCC}-0.8	-	V	I_O=-1mA, V_{INP}=14V, V_{INN}=0V -25°C < Ta < 105°C
Output Swing-Low	V_{OL}	-	0.1	0.2	V	I_O=1mA, V_{INP}=0V, V_{INN}=14V -25°C < Ta < 105°C
【Gamma Amplifier】						
Source Current Capability	I_{ooA}	-	-	30	mA	DAC=1B5h, V_{OUT}=0V, -25°C < Ta < 105°C
Sink Current Capability	I_{oiA}	-30	-	-	mA	DAC=1B5h, OUT=HVCC, -25°C < Ta < 105°C
Load Regulation	Δ Vo	-	15	-	mV	I_O=-15mA to 15mA
Output Swing - High	V_{OH1}	V_{HVCC}-0.2	-	-	V	I_O=-4mA
	V_{OH2}	V_{HVCC}-0.3	-	-	V	I_O=-4mA, -25°C < Ta < 105°C
Output Swing – Low	V_{OL1}	-	-	0.2	V	I_O=4mA
	V_{OL2}	-	-	0.3	V	I_O=4mA, -25°C < Ta < 105°C
【DAC】						
Resolution	Res		10		Bit	
Integral Non-linearity Error (INL)	LE	-2	-	+2	LSB	00A to 3F5 is the allowable margin of error against the ideal linear.
Differential Non-linearity Error (DNL)	DLE	-2	-	+2	LSB	00A to 3F5 is the allowable margin of error against the ideal increase of
【Control Signal SDA, SCL】						
Input Voltage H	V_{TH1}	1.7	-	-	V	-25°C < Ta < 105°C
Input Voltage L	V_{TH2}	-	-	0.5	V	-25°C < Ta < 105°C
Min Output Voltage	V_{SDA}	-	-	0.4	V	I_{SDA}=3mA

Electrical Characteristics – continued (Unless otherwise noted, Ta=25°C, V_{CC}=12V, V_{HVCC}=15V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
【Overall】						
Oscillator Frequency	f_{SW1}	600	700	800	kHz	
	f_{SW2}	500	-	900	kHz	-25°C < Ta < 105°C
VCC Under-Voltage Lockout Threshold ON/OFF Voltage	V_{CCUV}	7.6	8.0	8.4	V	-25°C < Ta < 105°C
HVCC Under-Voltage Lockout Threshold ON/OFF Voltage	V_{HVCCUV}	-	8.5	-	V	-25°C < Ta < 105°C
SCP Source Current	I_{SCPSO}	2	5	8	μA	
SCP Sink Current	I_{SCPSI}	1	2	6	mA	-25°C < Ta < 105°C
SCP Threshold Voltage	V_{SCP}	-	1.5	-	V	-25°C < Ta < 105°C
Average Current Consumption 1 (VCC,PVCC)	I_{CC1}	-	3.5	-	mA	No Switching
Average Current Consumption 2 (VCC,PVCC)	I_{CC2}	-	3.5	-	mA	-25°C < Ta < 105°C, No Switching
Average Current Consumption 3 (HVCC)	I_{HICC1}	-	3.5	-	mA	No Switching
Average Current Consumption 4 (HVCC)	I_{HICC2}	-	3.5	-	mA	-25°C < Ta < 105°C, No Switching

Typical Performance Curves

(Unless otherwise noted, Ta=25°C)

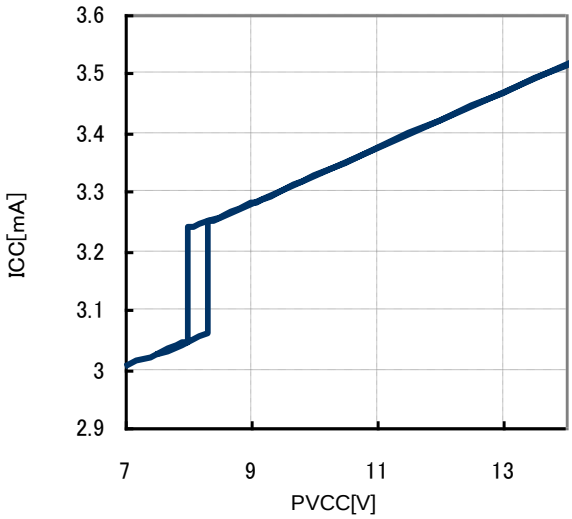


Figure 1. ICC vs PVCC

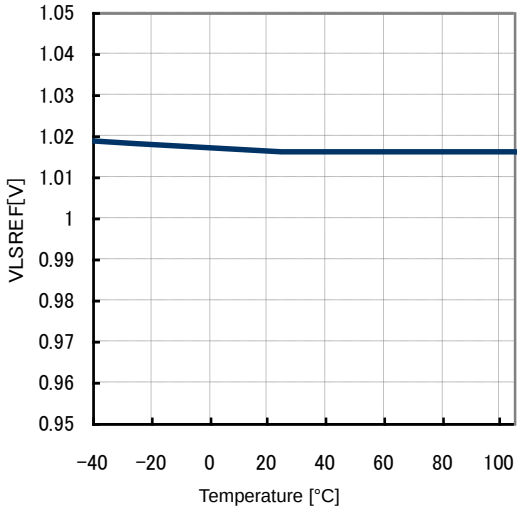


Figure 2. VLSREF vs Temperature

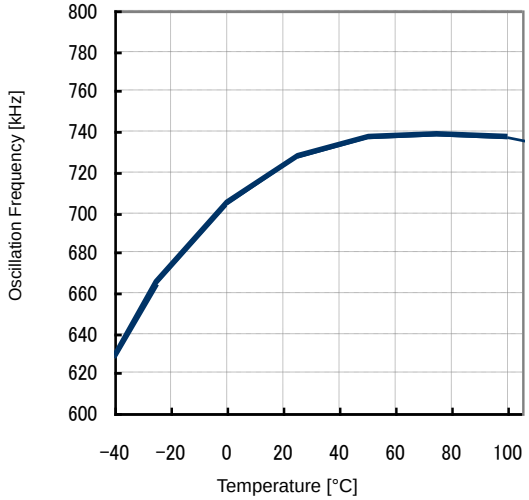


Figure 3. Oscillation Frequency vs Temperature

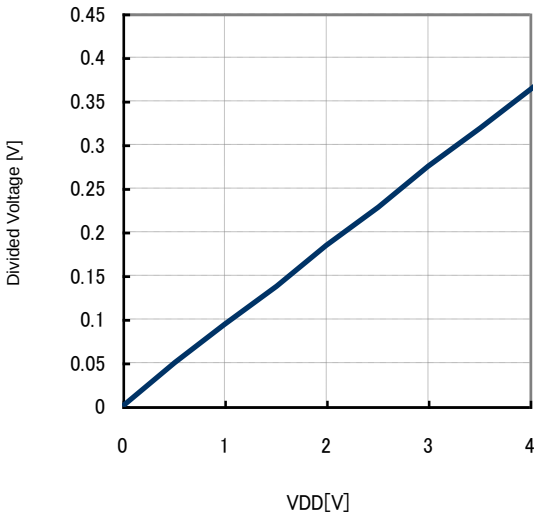


Figure 4. Divided Voltage vs VDD

Typical Performance Curves – continued

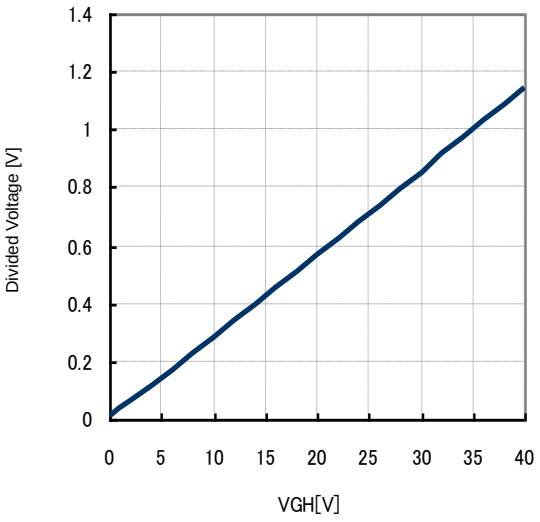


Figure 5. Divided Voltage vs VGH

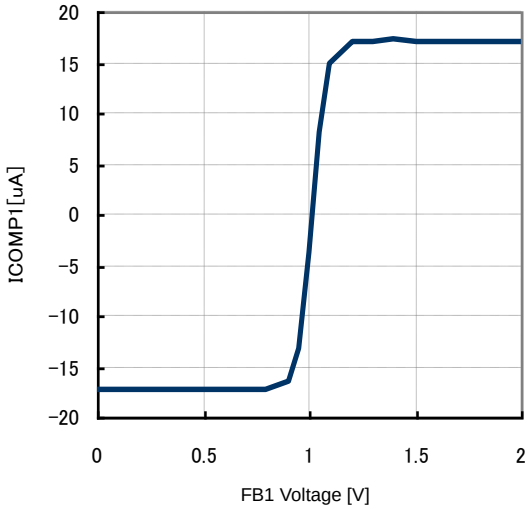


Figure 6. ICOMP vs FB1 Voltage

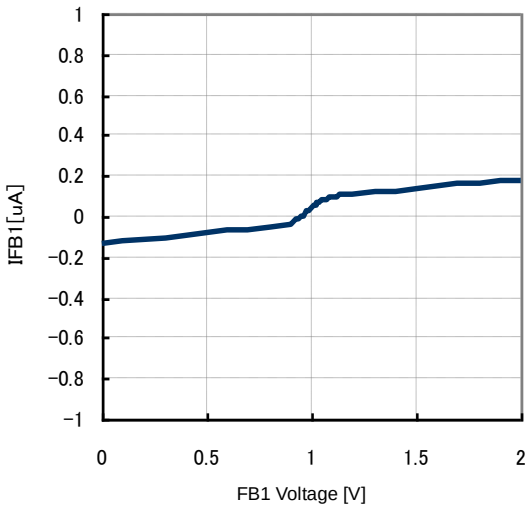


Figure 7. IFB1 vs FB1 Voltage

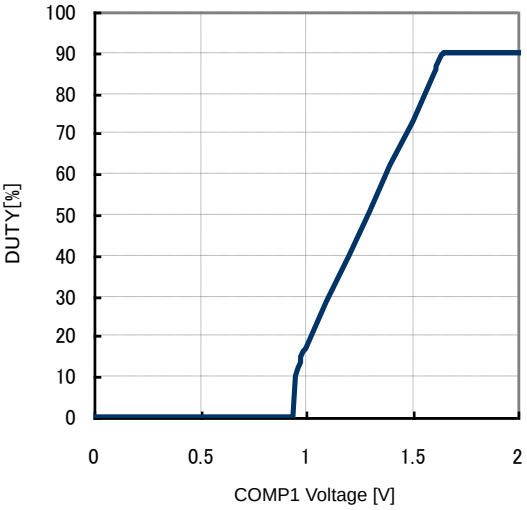


Figure 8. DUTY vs COMP1 Voltage

Typical Performance Curves – continued

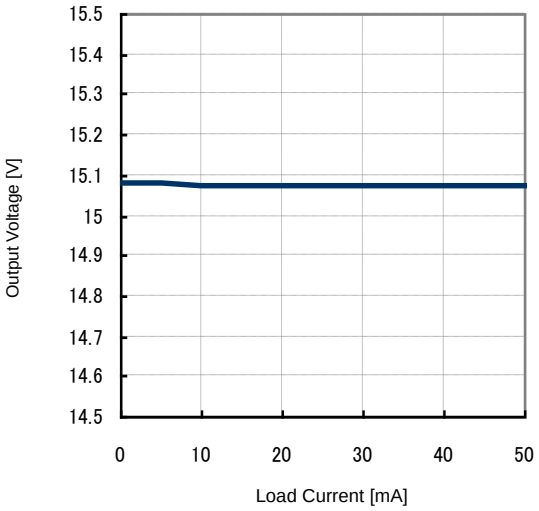


Figure 9. Output Voltage vs Load Current

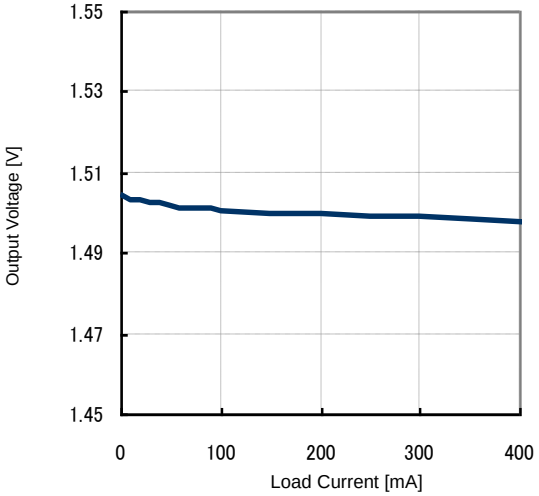


Figure 10. Output Voltage vs Load Current

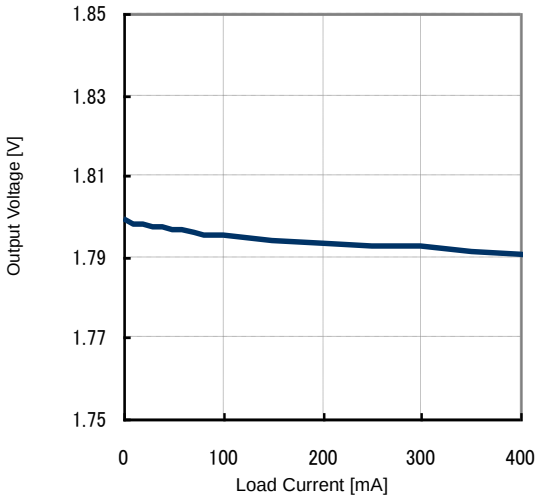


Figure 11. Output Voltage vs Load Current

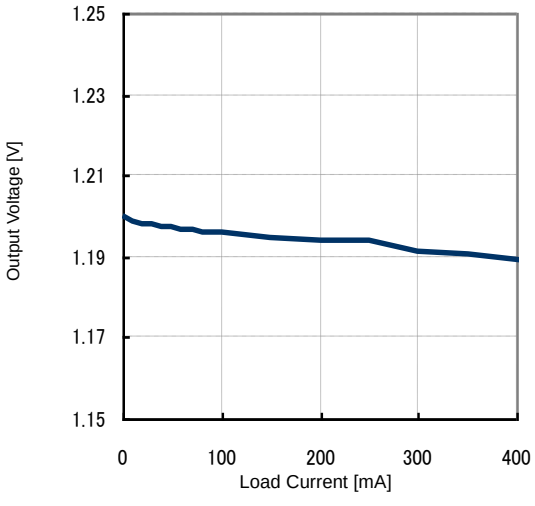


Figure 12. Output Voltage vs Load Current

Typical Performance Curves – continued

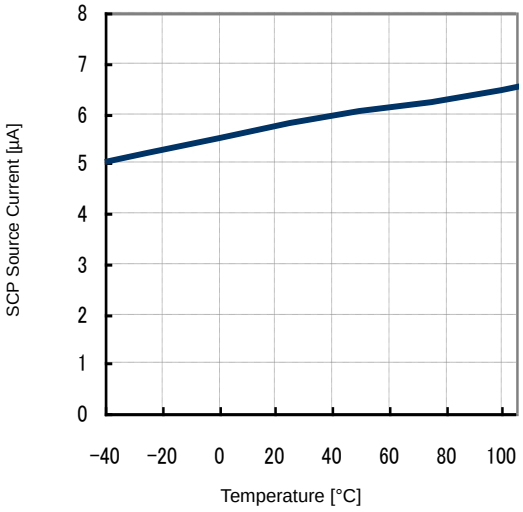


Figure 13. SCP Source Current vs Temperature

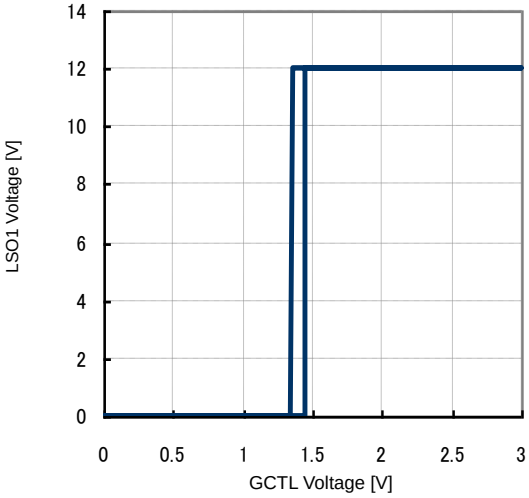


Figure 14. LSO1 Voltage vs GCTL Voltage

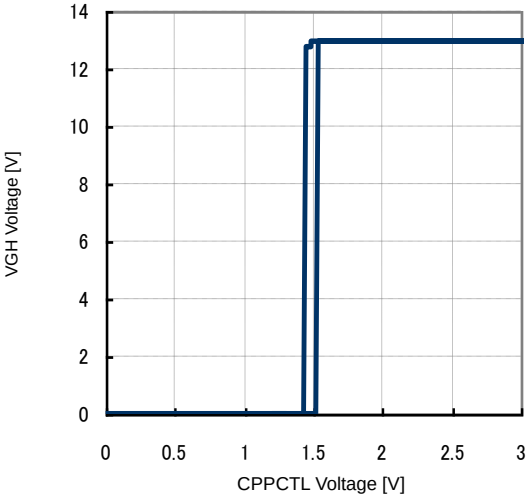


Figure 15. VGH Voltage vs CPPCTL Voltage

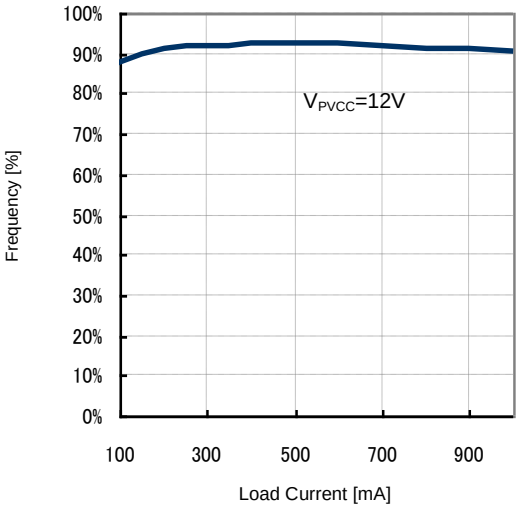


Figure 16. Frequency vs Load Current

Typical Performance Curves – continued

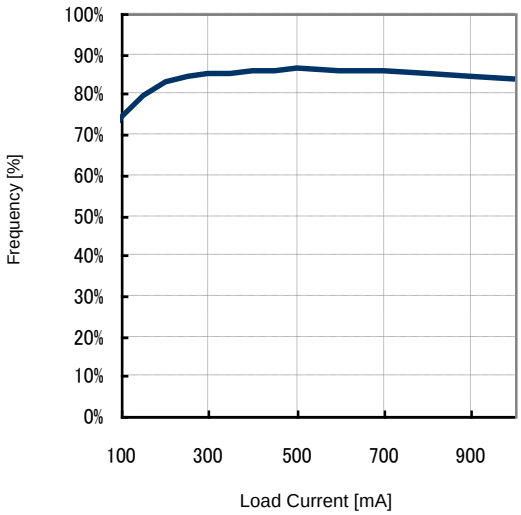


Figure 17. Frequency vs Load Current

Typical Waveforms

(Unless otherwise noted, Ta=25°C)

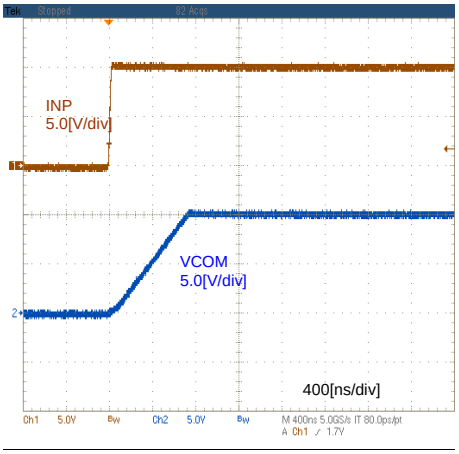


Figure 18. VCOMAMP slew rate

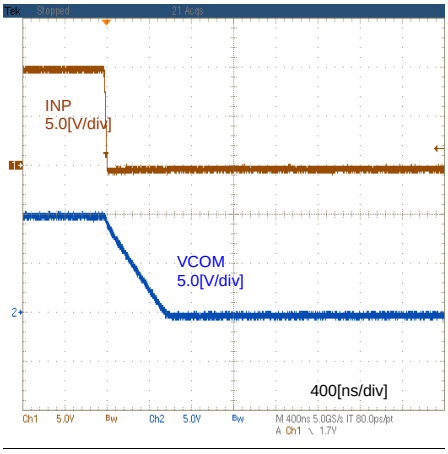


Figure 19. VCOMAMP slew rate

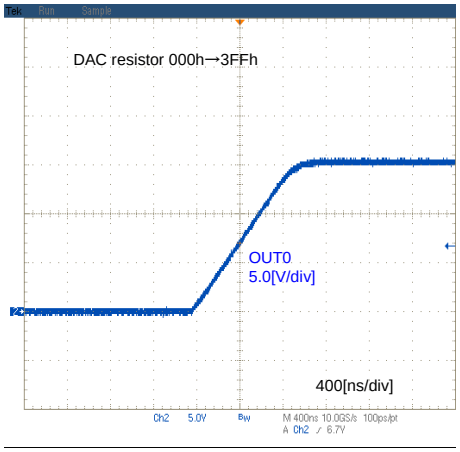


Figure 20. DAC slew rate

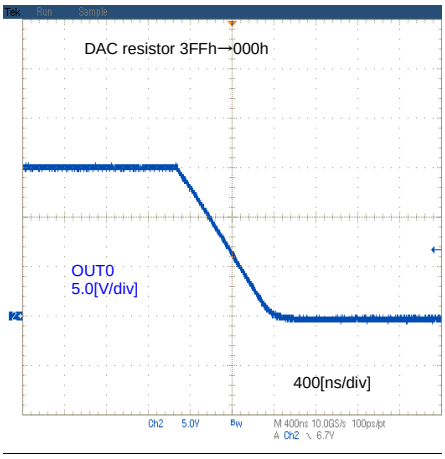


Figure 21. DAC slew rate

Typical Waveforms – continued

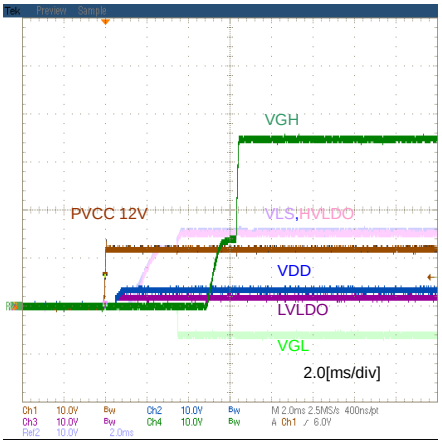


Figure 22. Startup sequence1

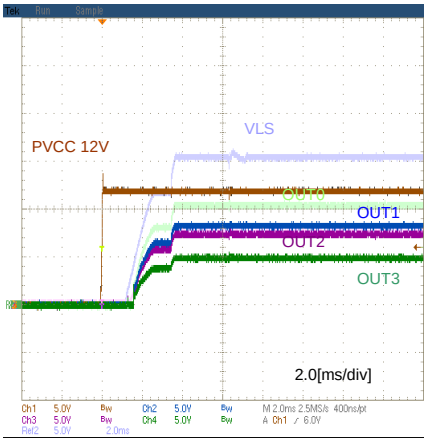


Figure 23. Startup sequence2

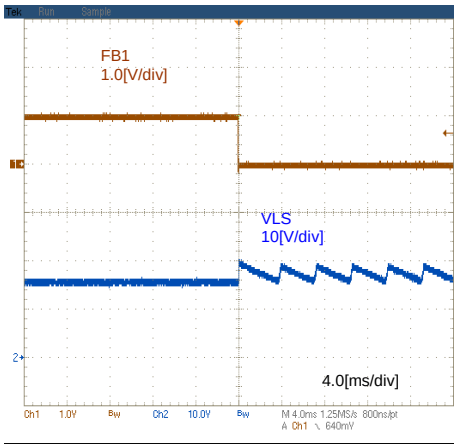


Figure 24. VLS OVP operation

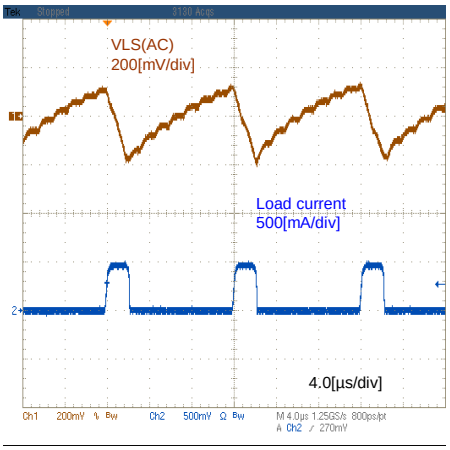


Figure 25. Step-up DC/DC transient response

Typical Waveforms – continued

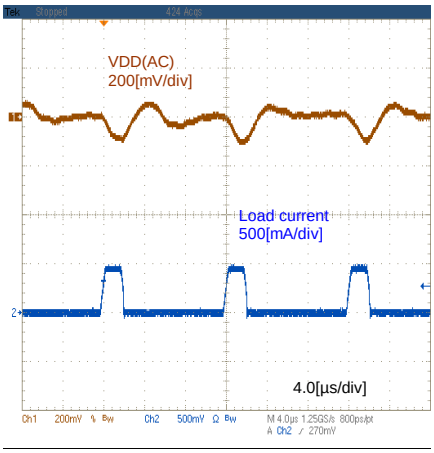


Figure 26. Step-down DC/DC transient response

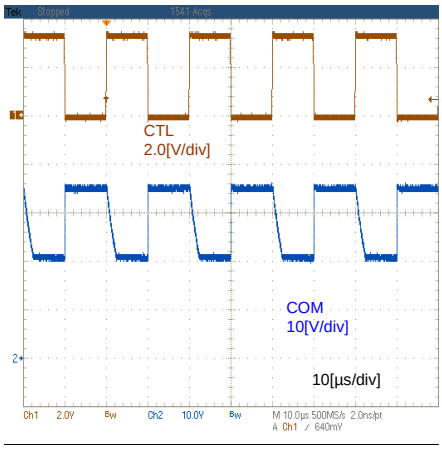


Figure 27. Gate shading waveform

Description of Operation of Each Block and Procedure for Selecting Application Components

(1) Step-up DC/DC Converter Block

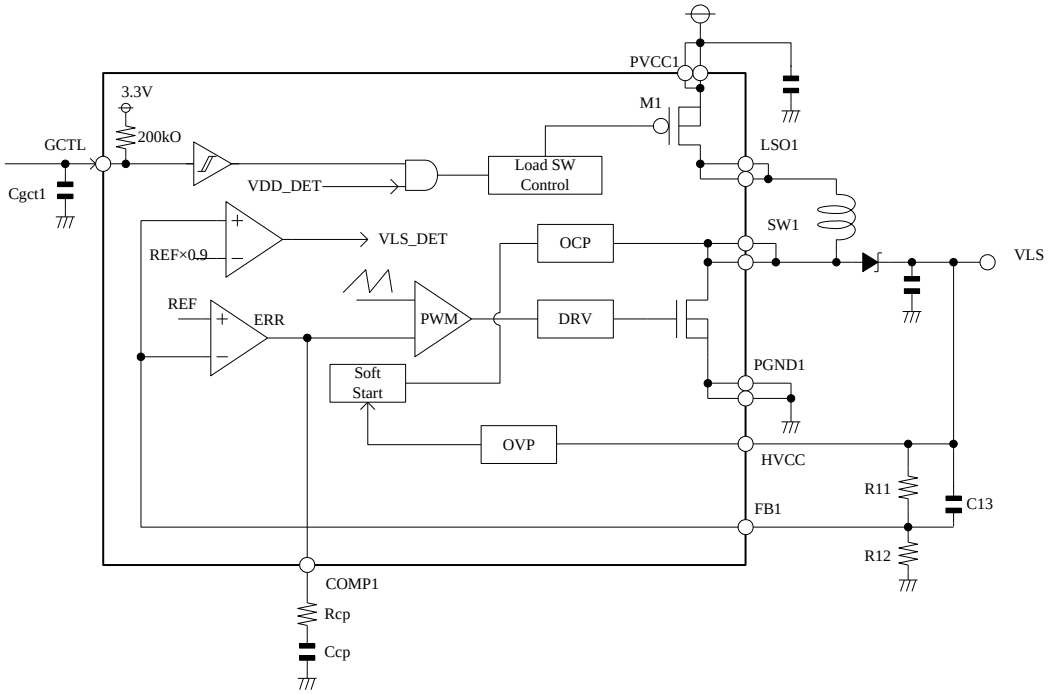


Figure 28. Step-up DC/DC Converter Block

Step-up DC/DC block is able to set output voltage by an external feedback resistor R11, R12.
Output voltage VLS is calculated by equation below.

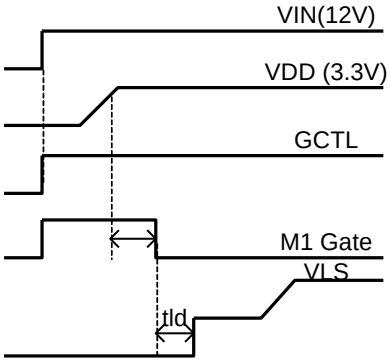
$$VLS = 1.0 \times \frac{R11 + R12}{R12}$$

Also, OVP function is incorporated for protecting output voltage overshoot, so that if VLS voltage overshoots over 19V(Typ), prevents over voltage output by stopping switching.

(1.1) Startup sequence

After step-down DC/DC converter startup, Start-up sequence is fixed to start up.
When Step-down DC/DC(3.3V output) reaches 90% of the set voltage, step-up DC/DC will start operation.
Soft start function is incorporated (About 1.5ms typ) in order to prevent overshooting during startup.
Also, controlling the startup timing of load switch (M1) by GCTL pin enables to control the VLS rising sequence.
For the startup timing of load switch (M1), there are two patterns: Use or Not use the GCTL pin.

① Case of Not using GCTL pin（Connect GCTL pin to OPEN or 3.3V.）
When disuse GCTL pin, if step-down DC/DC output (VDD) reach 90% of the configured voltage, load switch (M1) turns ON.



・Setting of load switch (M1) ON delay time (tld)

② Case of using GCTL pin

Using GCTL pin makes it possible to have ON timing of load switch (M1) can be delayed more than not using GCTL pin.

There are two methods for setting delay time by GCTL pin: Set the timing by inputting H/L logic signal to GCTL pin, or Set by constant time by inserting capacitor to GCTL pin.

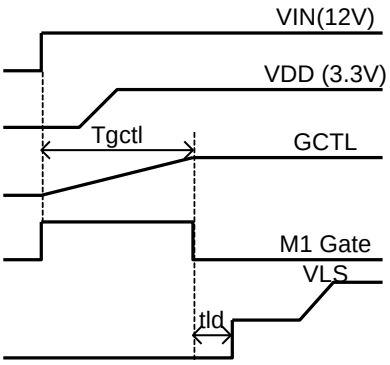
When setting the PGATE ON timing by constant time, ON delay time Tgctl is determined by the equation below.

$$Tgctl = -Cgctl \cdot Rgct \cdot In\frac{VREF - Vth}{VREF}$$

$$= -Cgctl \cdot 200k \cdot In\frac{3.3-1.6}{3.3}$$

■ About GCTL delay time fluctuation

The rgdt1 has variation in current and voltage of ±50% that includes absolute variations and temperature characteristic, design systems with sufficient margin.



(1.2) Selecting the output L constant

The inductance L to be used for output is determined by the rated current I_{LR} and the maximum input current value I_{INMAX} of the inductor.

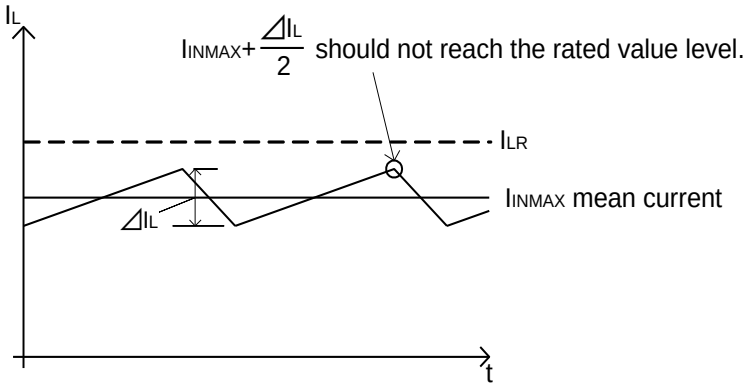


Figure 29. Coil Current Waveform (Step-up DC/DC Converter)

Make adjustments so that $I_{INMAX} + \Delta I_L / 2$ will not reach the rated current I_{LR}. At this time, ΔI_L is obtained by the following equation.

$$\Delta I_L = \frac{1}{L} V_{CC} \times \frac{V_O - V_{CC}}{V_O} \times \frac{1}{f} \quad [A]$$

wherein f : Switching frequency

In addition, since the coil L value may have variations in the range of approximately ±30%, set this value with sufficient margin.
If the coil current exceeds the rated current I_{LR}, the internal IC element may be damaged because of Large – current.

(1.3) Output capacitor setting

For capacitor C_O to be used for output, set it to the permissible value of the ripple voltage VPP or that of the drop voltage at the time of a sudden load change, whichever is large.

The output ripple voltage is obtained by the following equation.

$$\Delta VPP = I_{LMAX} \times R_{ESR} + \frac{1}{fC_O} \times \frac{V_{CC}}{V_O} \times (I_{LMAX} - \frac{\Delta I_L}{2})$$

Make this setting so that the voltage will fall within the permissible ripple voltage range.
For the drop voltage VDR during a sudden load change, estimate the VDR with the following equation.

$$VDR = \frac{\Delta I}{C_O} \times 10\mu\text{sec} \quad [V]$$

Wherein, 10 µsec is the estimate of DC/DC response speed. Set C_O so that these two values will fall within the limit values.

Since the DC/DC converter causes a peak current to flow between input and output, capacitors must also be mounted on the input side. For this reason, it is recommended to use low-ESR capacitors above 10µF and below 100mΩ as the input capacitors. Using input capacitors outside of this range may superimpose excess ripple voltage upon the input voltage, causing the IC to malfunction.

However, since the aforementioned conditions vary with load current, input voltage, output voltage, inductor value, and switching frequency, be sure to verify the margin using the actual product.

(1.4) Output rectifier diode setting

For the rectifier diodes to be used as the output stage of the DC/DC converter, it is recommended to use Schottky diodes. Select diodes with careful attention paid to the maximum inductance current, maximum output voltage, and power supply voltage.

Maximum inductance current: $I_{INMAX} + \frac{\Delta I_L}{2}$ < Rated current of diode

Maximum output voltage: V_{OMAX} < Rated voltage of diode

In addition, since each parameter has variation in current and voltage of 30% to 40%, design systems with sufficient margin.

(1.5) Phase compensation setting

Phase setting procedure
The following conditions are required to ensure the stability of the negative feedback system.

・When the gain is set to “1” (0 dB), the phase leg should not be more than 150°
(i.e., phase margin should not be less than 30°).

In addition, since DC/DC converter applications are sampled according to the switching frequency, the overall system GBW should be set to not more than 1/10 of the switching frequency. The targeted characteristics of the applications can be summarized as follows.

- When the gain is set to “1” (0 dB), the phase lag should not be more than 150° (i.e., phase margin should not be less than 30°).
- The GBW at that time (i.e., frequency when the gain is set to “0 dB”) should not be more than 1/10 of the switching frequency.

The responsiveness is determined by the GBW limitation. Consequently, to raise the responsiveness, higher switching frequencies are required.
To ensure the stability through the phase compensation, it is necessary to cancel the secondary phase delay (-180°) caused by LC resonance with the secondary phase lead (in other words, by adding two phase leads).
The GBW (i.e., frequency when the gain is set to “0 dB”) is determined by phase compensation capacitance connected to the error amplifier. If GBW needs to be reduced, increase the capacitance of the capacitor.

Open loop characteristics of integrator

(i) Ordinary integrator(Low-pass filter)

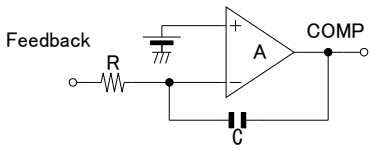


Figure 30

(ii) Open loop characteristics of integrator

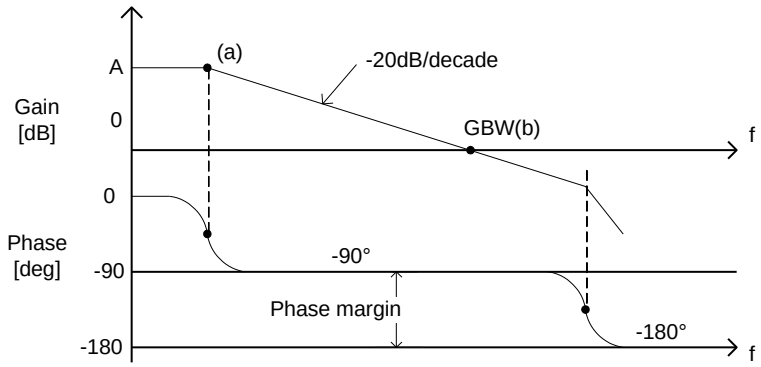


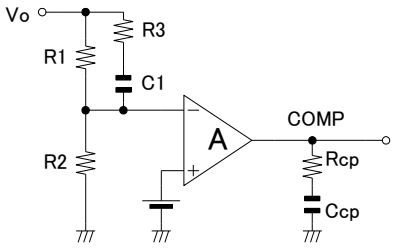
Figure 31

$$Point(a) \quad fa = \frac{1}{2\pi RCA} \quad [Hz]$$

$$Point(b) \quad fb = GBW = \frac{1}{2\pi RC} \quad [Hz]$$

Since the phase compensation like that shown in (a) and (b) applies to the error amplifier, it will act as a low-pass filter.
For DC/DC converter applications, R represents feedback resistors connected in parallel.

According to the LC resonance of the output, two phase leads should be added.



$$LC\ resonant\ frequency \quad fp = \frac{1}{2\pi\sqrt{LC}} \quad [Hz]$$

$$Phase\ lead \quad fz1 = \frac{1}{2\pi R1C1} \quad [Hz]$$

$$Phase\ lead \quad fz2 = \frac{1}{2\pi RcpCcp} \quad [Hz]$$

Figure 32

Set the lead frequency of one of the phases close to the LC resonant frequency for the purpose of canceling the LC resonance.

Note: If high-frequency noise occurs in output, it will pass through capacitor C1 and affect the feedback. To avoid this problem, add resistor R3 of approximately 1kΩ in series with capacitor C1.

(2) Step-down DC/DC block

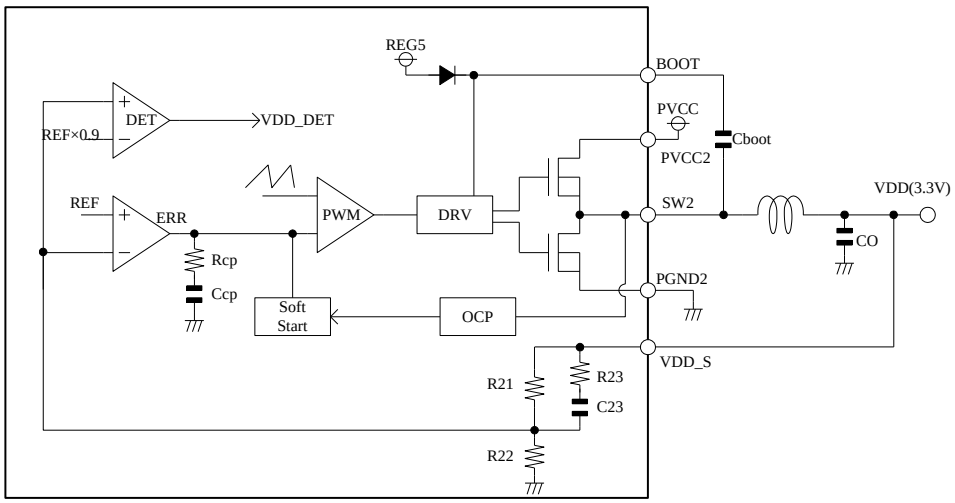


Figure 33. Step-down DC/DC

Step-down DC/DC block incorporates feedback resistor, and output voltage is 3.3V(TYP) fixed.
Also, built-in error amp (ERR) phase compensation (Rcp,Ccp) minimizes the external components.

(2.1) Startup sequence

After VIN12V startup, step-down DC/DC starts up with UVLO cancellation as trigger.
Soft start function (about 2ms Typ) is built in to limit overshooting while startup.

(2.2) Selecting the output L constant

The inductor to be used for output is determined by the rated current I_{LR} and the maximum input current value I_{OMAX} of the inductor.

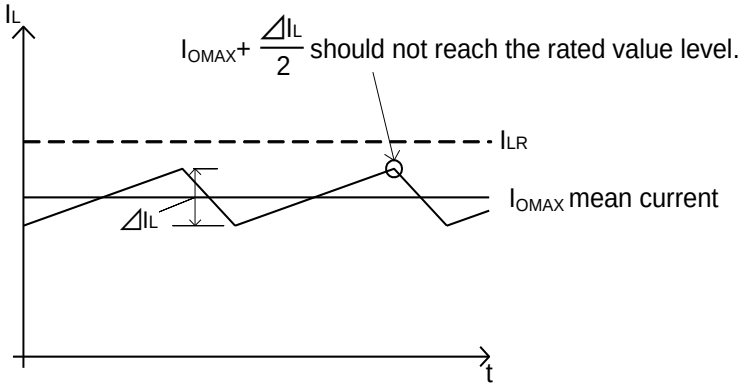


Figure 34. Inductor Current Waveform Step-down DC/DC)

Make adjustments so that $I_{OMAX} + \Delta I_L / 2$ will not reach the rated current I_{LR}. At this time, ΔI_L is obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (V_{CC} - V_O) \times \frac{V_O}{V_{CC}} \times \frac{1}{f}$$

Wherein f : Switching frequency

In addition, sine the inductor L value may have variations in the range of approximately ±30%, set this value with sufficient margin.
If the inductor current exceeds the rated current I_{LR}, the internal IC element may be damaged because of large rush current.

(2.3) Selecting I/O capacitors

To select I/O capacitors, refer to information in Section (1.3).
However, the output ripple voltage of the step-down DC/DC converter is calculated by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2C_O} \times \frac{V_O}{V_{CC}} \times \frac{1}{f} \quad [V]$$

Cboot is a flying capacitor in bootstrap circuit for driving high side switch. 0.1µF is recommended.

(3) HV_LDO block

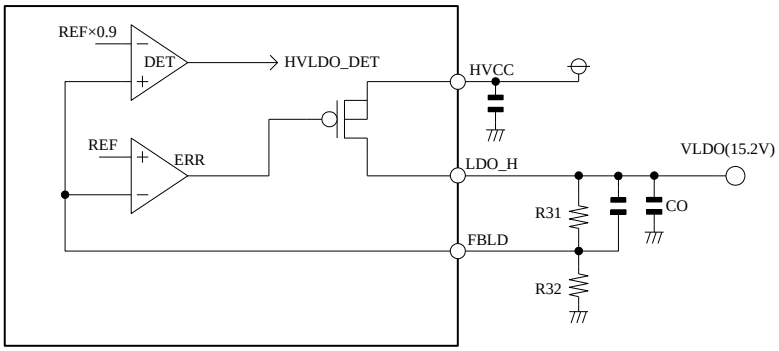


Figure 35. HV_LDO block

(3.1) Selecting I/O capacitors

The HV_LDO is ceramic capacitor compatible.
Capacitance in the range of 4.7µF to 10µF is recommended.

(3.2) Output voltage setting

Output voltage is variable output by the external resistor R31,R32.
Output voltage HVLDO is calculated by the equation below.

$$HVLDO = 1.0 \times \frac{R31 + R32}{R32}$$

(3.3) Startup sequence

After under voltage protection for VCC release, starts up with HVCC startup.

(4) LV_LDO block

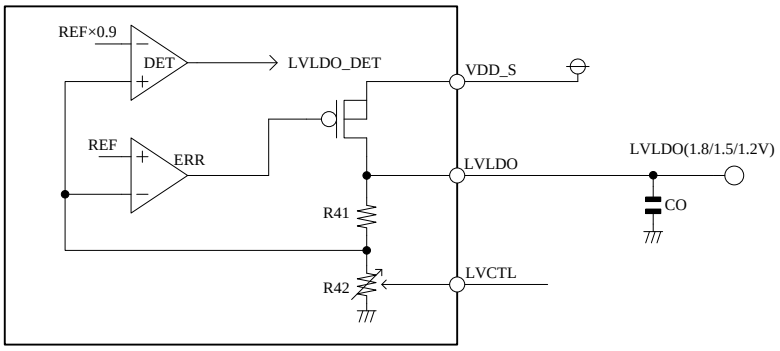


Figure 36. LV_LDO block

(4.1) Selecting I/O capacitors

LV_LDO is ceramic capacitor compatible.
Capacitance in the range of 4.7µF to 10µF is recommended.

(4.2) Output voltage setting

Output voltage is switching output by LVCTL pin.

Where LVCTL pin=VIN(PVCC1,2)、	LVLDO output = 1.2[V]
Where LVCTL pin=M（OPEN） 、	LVLDO output = 1.8[V]
Where LVCTL pin= GND、	LVLDO output = 1.5[V]

(4.3) Startup sequence

After under voltage protection for VCC release, starts up with VDD startup.

(5) Charge pump block

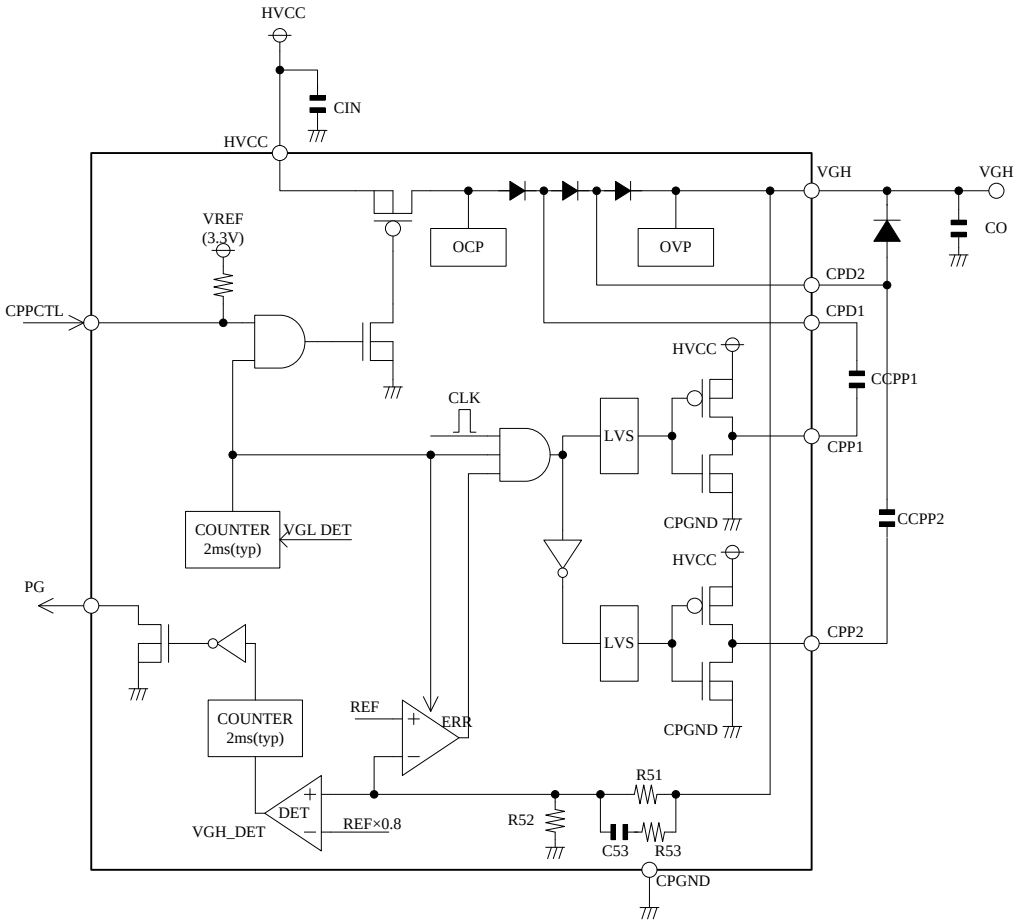


Figure 37. Positive charge pump block

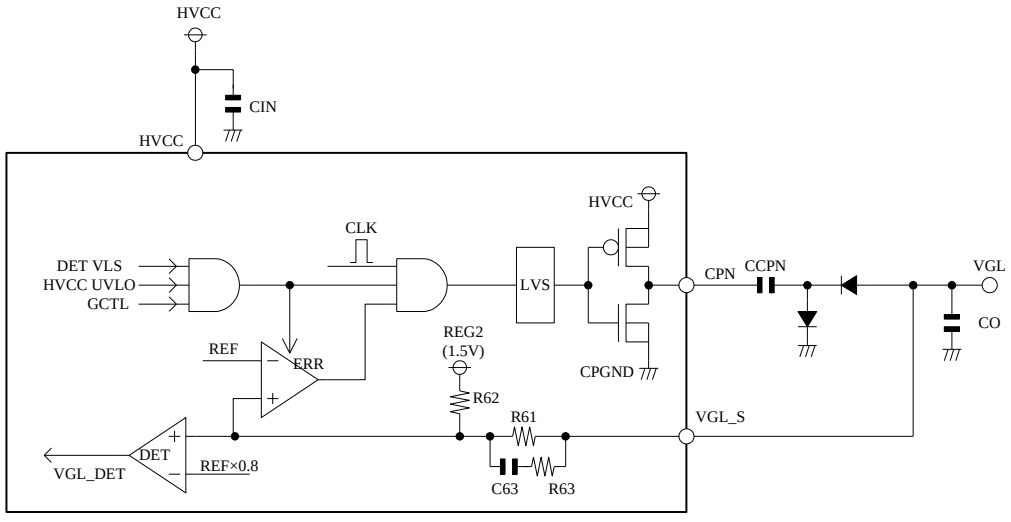


Figure 38. Negative charge pump block

The charge pump block starts operation, when it reaches 90% of Boost DC/DC output, GCTL=High and cancels HVCC low voltage protection. The startup sequences are internally fixed. First, negative-side charge pump starts operation. Next, when the negative-side charge pump reaches 80% of the set voltage, after 2ms (typ), the positive-side charge pump will start operation. When both negative and positive-side charge pumps reach 80% of the set voltage, after 2ms (typ), the power-good signal outputs from the CPPG pin.
The positive-side charge pump have an overvoltage protection function that turns off HVCC-side load switch and prevents overshoot of output voltage, When VGH voltage reaches 37.5V (typ).

(5.1) Selecting output diodes

Select Schottky diodes having a current capability two times (negative side) as high as the maximum output current and a withstand voltage higher than the output voltage.
Due to the aforementioned requirements, it is recommended to use the RB550EA dual Schottky barrier diode.

(5.2) Selecting output capacitors

CCPP1,CCPP2,CCPN is flying capacitor. A capacitance in the range of 0.01µF to 1µF is recommended.
CO serves as charge pump output capacitors; a capacitance in the range of 0.47µF to 10µF is recommended.

(5.3) Output voltage setting

Positive charge pump output VGH is 35.2V(TYP) fixed output.
Negative charge pump output VGL is -6V(TYP) fixed output.

(6) Gate shading block

Gate shading block activates when positive charge pump output (VGH) is over 80%, CTL logic comes in.
Inside FET M1 turns ON and FET M2 turns OFF when positive charge pump output (VGH) is below 80%.
When CTL logic is LOW, inside FET M1 turns ON and M2 turns OFF.
When CTL logic is HIGH, inside FET M1 turns OFF and M2 turns ON. While M2 turns ON, if DRN pin voltage reaches ten times of a voltage inputting to THR, M2 turns OFF.

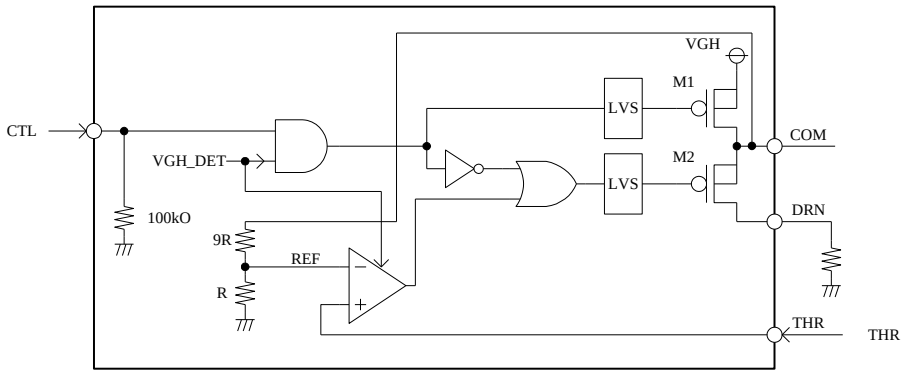


Figure 39. Gate shading block

	VGH voltage under 80%		VGH voltage over 80%	
CTL logic	FET M1	FET M2	FET M1	FET M2
L	ON	OFF	ON	OFF
H	ON	OFF	OFF	ON

Common amplifier

VCOM operates in the range of 0.1V to HVCC-0.8V(TYP). Normally, use the VCOM amplifier as a buffer type amplifier as shown in (a).
Use the output voltage of the HVLDO block for power supply on the reference side.
To increase the current drive capability, use the PNP and NPN transistors as shown in (b).
When the VCOM amplifier is not used, set the block to the buffer type as shown in (a) and ground the INP pin.
In this case, it is recommended to set the RCOM1 and RCOM2 resistors in the range of 10kΩ to 100kΩ .
Setting them to not more than 10kΩ may increase current consumption, thus resulting in degraded power efficiency.
Setting them to not less than 100kΩ may result in higher offset voltage due to the input bias current of 0.1μA (Typ).

(a) (b)

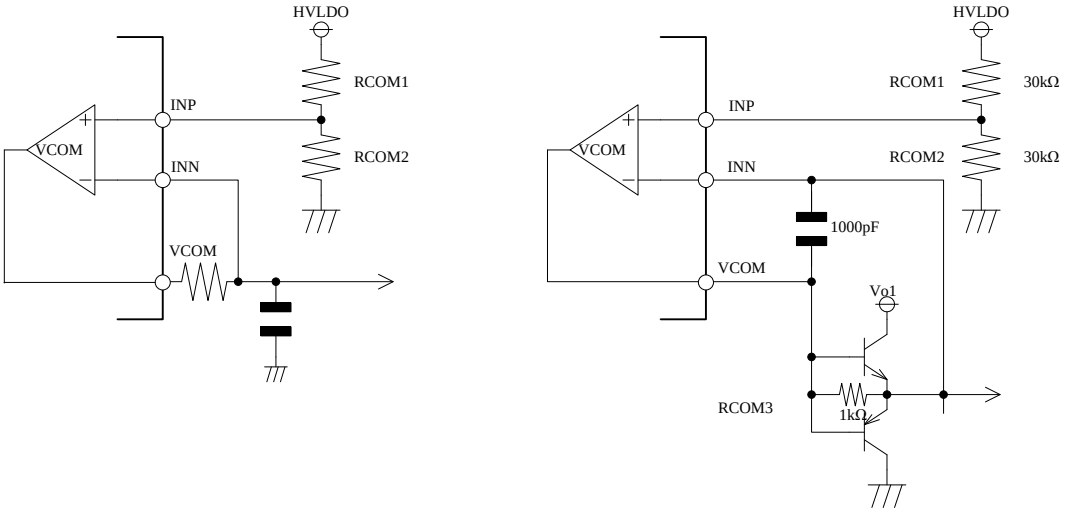


Figure 40. VCOM

$$VCOM = \frac{RCOM2}{RCOM1 + RCOM2} \times HVLDO$$

(7) DAC block

The serial data control block consists of a register that stores data from the SDA, SCL pins, and a DAC circuit that receives the output from this register and provides adjusted voltages to other IC blocks.

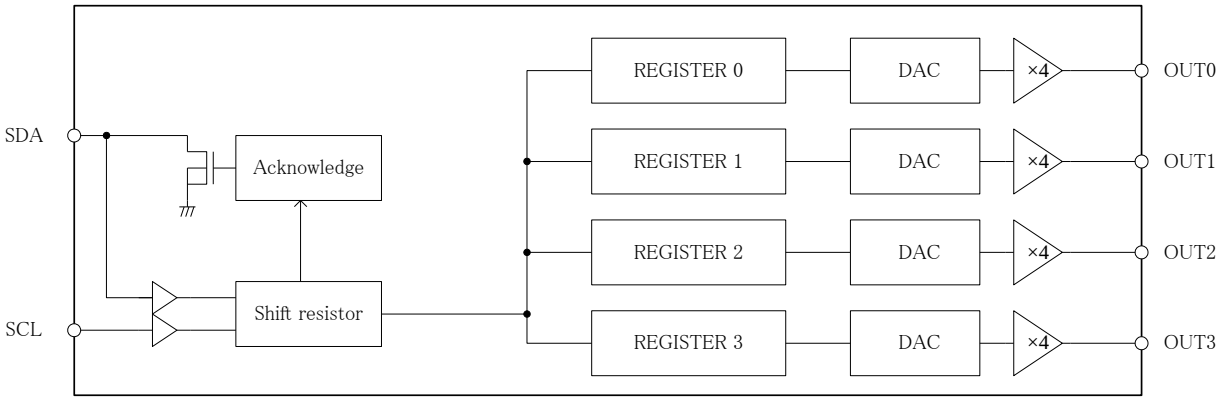
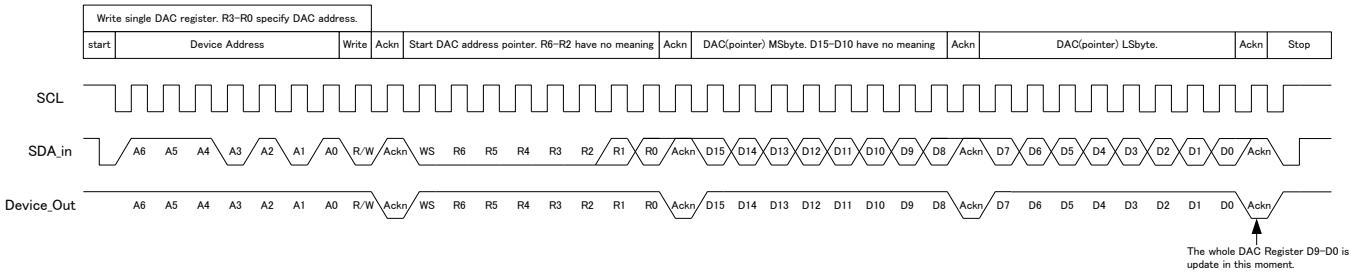


Figure 41. Serial block

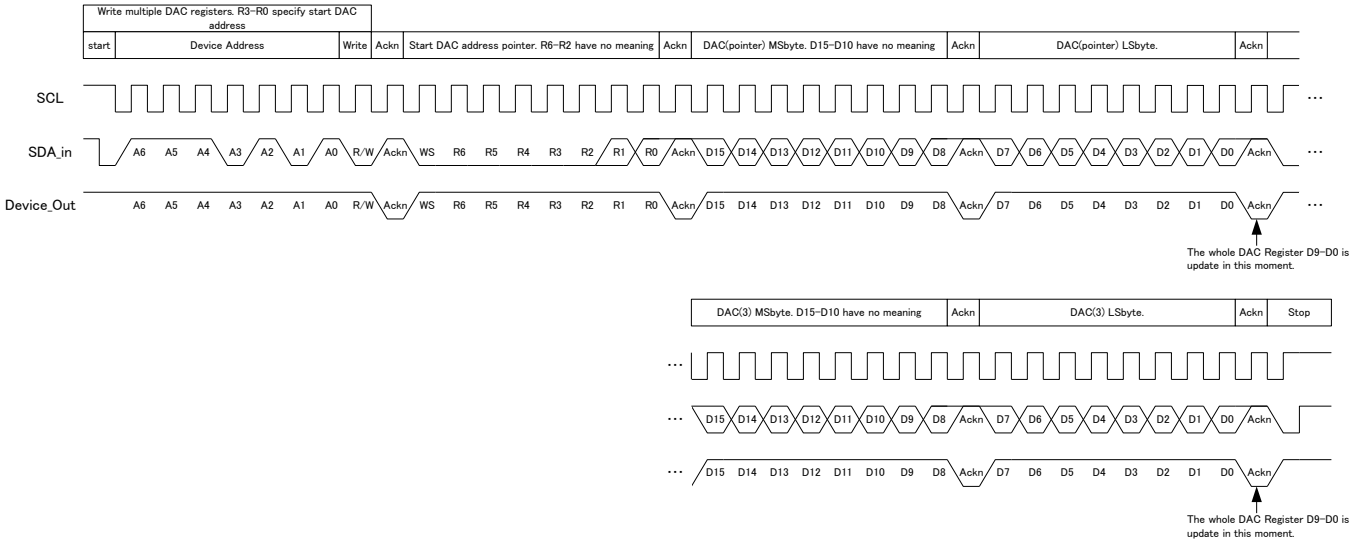
- **Output Voltage setting mode**

  Writes to a register address specified by I²C BUS.
  For writing mode from I²C BUS to register, there are (ⅰ)Single mode , (ⅱ)Multi mode.
  On single mode, write data to one designated register.
  On multi mode, as a start address register specified in the second byte of data entry by multiple data write can be performed continuously.
  Single mode or multi mode can be configured by having or not having “stop bit”.

(i). Single mode timing chart



(ii). Multi mode timing chart



Resistor address		Register name		BIT								Initial value	Output pin
R1	R0			7	6	5	4	3	2	1	0		
0	0	Register 0	DATA0	X	X	X	X	X	X	D9	D8	02C5h	OUT0
			DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	1	Register 1	DATA0	X	X	X	X	X	X	D9	D8	0230h	OUT1
			DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	0	Register 2	DATA0	X	X	X	X	X	X	D9	D8	01EDh	OUT2
			DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	1	Register 3	DATA0	X	X	X	X	X	X	D9	D8	014Dh	OUT3
			DATA1	D7	D6	D5	D4	D3	D2	D1	D0		

DATA0：Upper 8 bits, DATA1：Lower 8 bits, X：don't care, D9 to D0：Data bit

REGISTER ADDRESS
Device addresses A6 to A0 are specific to the IC and should be set as follows: （A6 to A0）=1110101.
The lower 2 bits (R1 to R0) of the second byte are used to store the register address. R6 to R2 should be set to 0 as usual.

- **Command interface**

Use I^2C BUS for command interface with host. Writing or reading by specifying 1 byte select address, along with slave address. I^2C BUS Slave mode format is shown below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	DATA	A	P

S : Start condition
Slave Address : After slave mode (7bit),, with read mode (H) or light mode (L), send 8 bit data in all.
A : Acknowledge Added acknowledge bit per byte in sending and receiving data.
If the data is sent/ received properly, "L" is send/receives.
Sending/ Receiving "H" means lack of acknowledge.
Select Address : Use 1 byte select address.
DATA : Data byte. Sending/ Receiving data（MSB first）
P : Stop condition

The case where writing 3FCh to DAC1（Single mode）

S	Slave Address	A	Select Address	A	Register1 DATA0	A	Register1 DATA1	A	P
(ex.)	EAh		01h		03h		FCh		

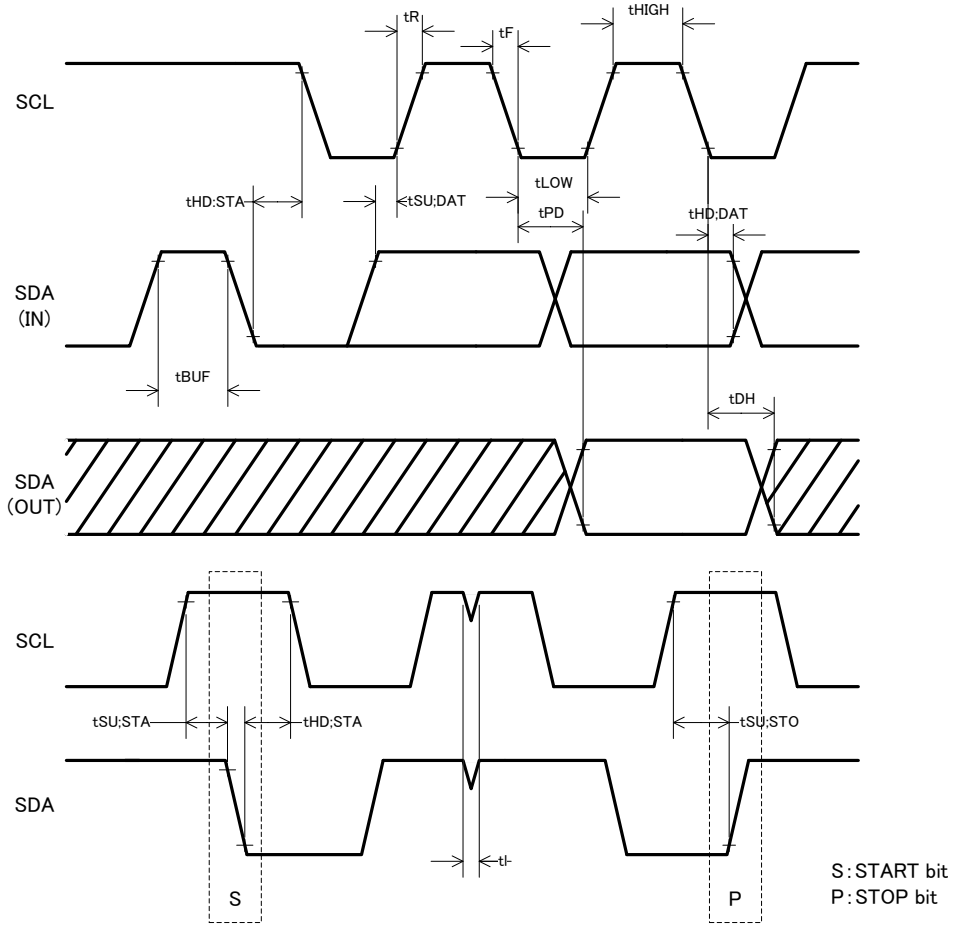
: Slave from master Master from slave

The case where writing 3FCh from DAC0 to DAC3 (Multi mode)

S	Slave Address	A	Select Address	A	Register 0 DATA0	A	Register 0 DATA1	A	Register 1 DATA0	A	Register1 to 3 DATA0,DATA1	A	P
(ex.)	EAh		00h		03h		FCh		03h				

: Slave from master Master from slave

- **I²C Timing**



- Timing regulation

Parameter	Symbol	FAST mode			Unit
		MIN	TYP	MAX	
SCL Frequency	f_{SCL}	-	-	400	kHz
SCL "H" Time	t_{HIGH}	0.6	-	-	µs
SCL "L" Time	t_{LOW}	1.2	-	-	µs
Rise Time	t_R	-	-	0.3	µs
Fall Time	t_F	-	-	0.3	µs
Start Condition Holding Time	$t_{HD;STA}$	0.6	-	-	µs
Start Condition Setup Time	$t_{SU;STA}$	0.6	-	-	µs
SDA Holding Time	$t_{HD;DAT}$	100	-	-	ns
SDA Setup Time	$t_{SU;DAT}$	100	-	-	ns
Acknowledge Delay Time	t_{PD}	-	-	0.9	µs
Acknowledge Holding Time	t_{DH}	-	0.1	-	µs
Stop Condition Setup Time	$t_{SU;STO}$	0.6	-	-	µs
BUS Open Time	t_{BUF}	1.2	-	-	µs
Noise Spike Width	t_I	-	0.1	-	µs

- **Buffer output setting**

The relation between buffer output voltage (OUT0 to OUT3) and DAC setting value is shown below.

$$Output\ voltage\ (OUT0\ to\ OUT3) = \frac{DAC\ setting\ value + 1}{1024} \times HVLDO$$

Buffer output terminals OUT0 to OUT3 output after UVLO release of HVCC.
While UVLO detection, the output is HiZ.

(8) Common block

(8.1) UVLO function

When VCC is below 8.0V(TYP), UVLO function activates and be canceled when VCC is over 8.4V(TYP).

(8.2) SCP function

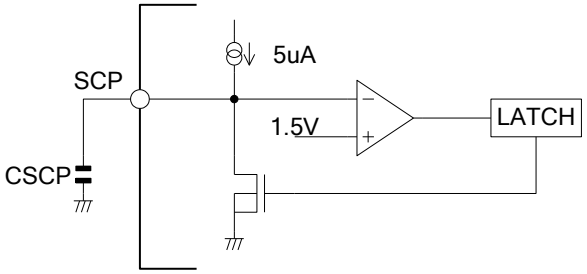


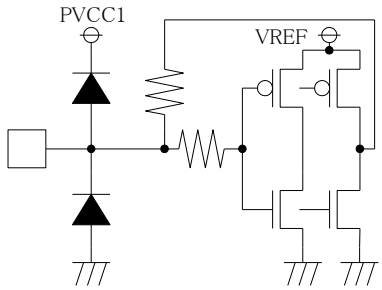
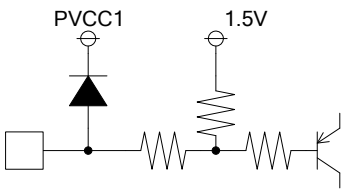
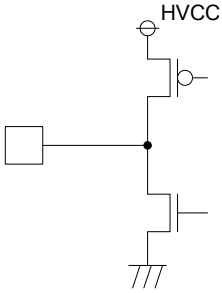
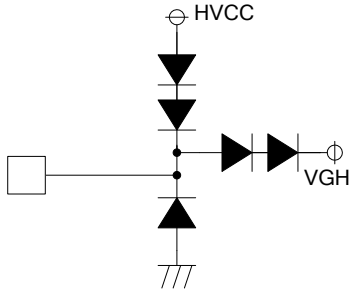
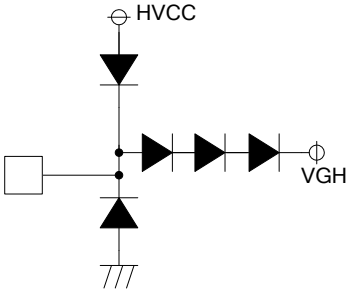
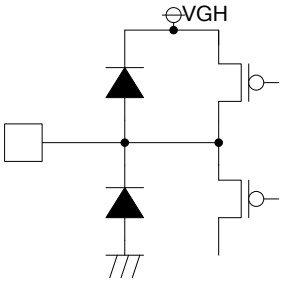
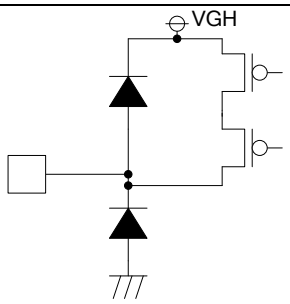
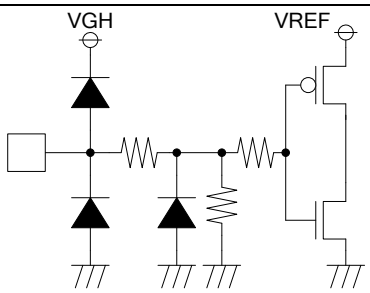
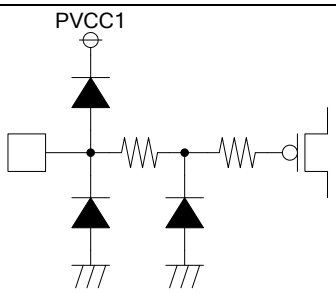
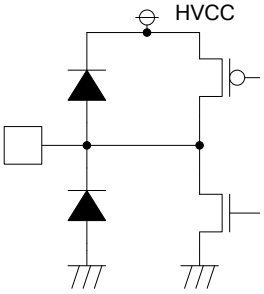
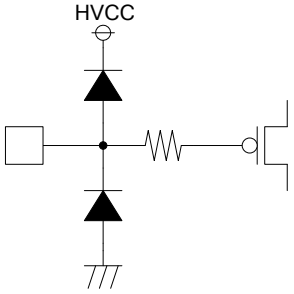
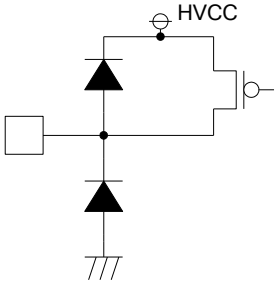
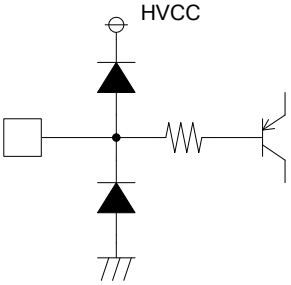
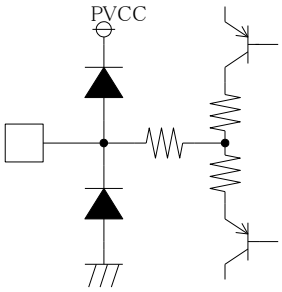
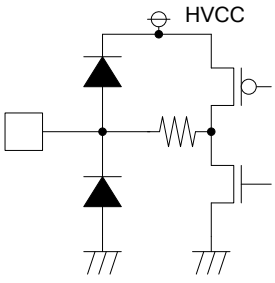
Figure 42. SCP

The SCP function protects against short-circuits in the outputs of the step-up DC/DC converter, step-down DC/DC converter, HV_LDO, LV_LDO and charge pump blocks. When any one of these outputs falls below 60% of the set voltage, it will be regarded as a short-circuit in output, thus activating the short-circuit protection function.
If a short-circuit is detected, source current of 5 μA (Typ) will be output from the SCP pin. Then, delay time will be set with external capacitance. When the SCP pin voltage exceeds 1.5V (Typ), the state will be latched to shut down all outputs. Once the state has been latched, it will not be canceled unless VCC restarts. The delay time setting is obtained by using the following equation.

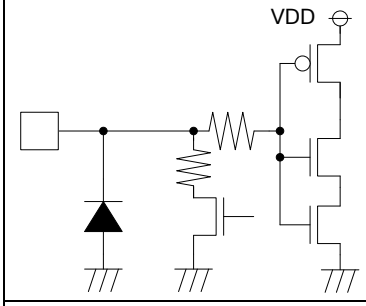
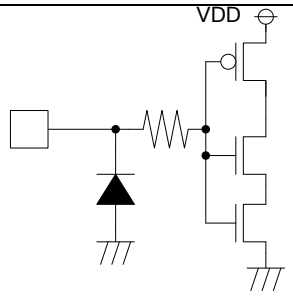
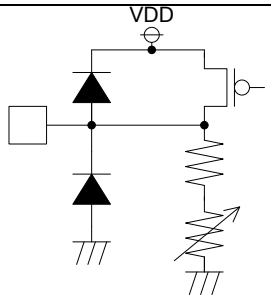
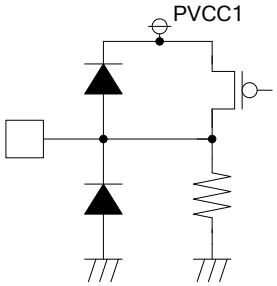
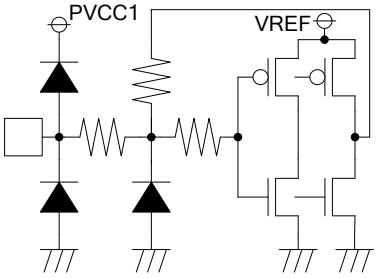
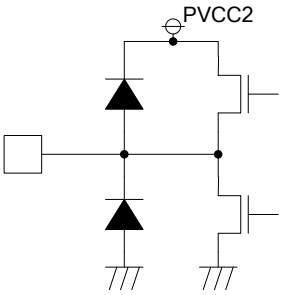
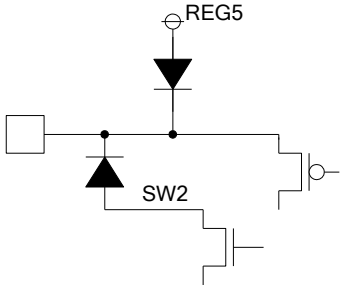
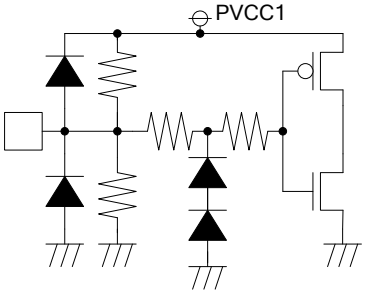
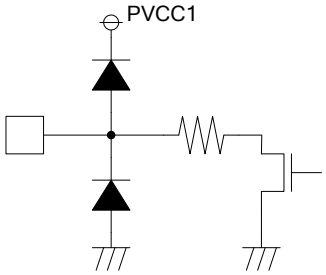
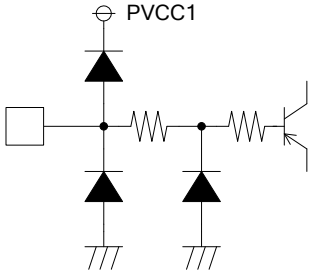
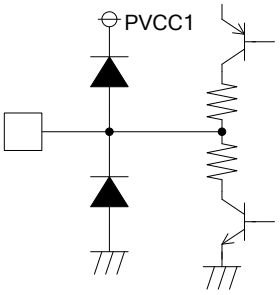
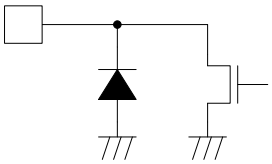
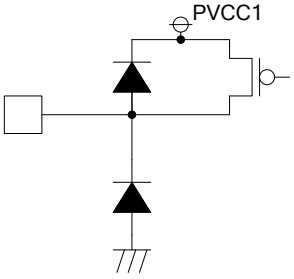
$$TL[s] = \frac{C_{SCP} \times 1.5}{5 \times 10^{-6}}$$

Even if none of the output startup sequences is complete at startup of the IC, short-circuits will be detected and the SCP function activated. For this reason, set the delay time substantially longer than the startup time.

I/O Equivalent Circuits

3.CPPCTL	5.VGL_S	6.CPN 7.CPP1 8.CPP2
		
10.CPD2	11.CPD1	13.COM
		
14.DRN	15.CTL	16.THR
		
17.VCOM	18.INN 19.INP	20.HVLDO
		
21.FBLD1	23.SCP	24.OUT0 25.OUT1 26.OUT2 27.OUT3
		

I/O Equivalent Circuits - Continued

29.SDA	30.SCL	31.LVLDO
		
32.REG5	34.GCTL	35.SW2
		
37.BOOT	38.LVCTL	39.PG
		
41.FB1	42.COMP1	45.SW1 46.SW1
		
47.LSO1 48.LSO1		
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

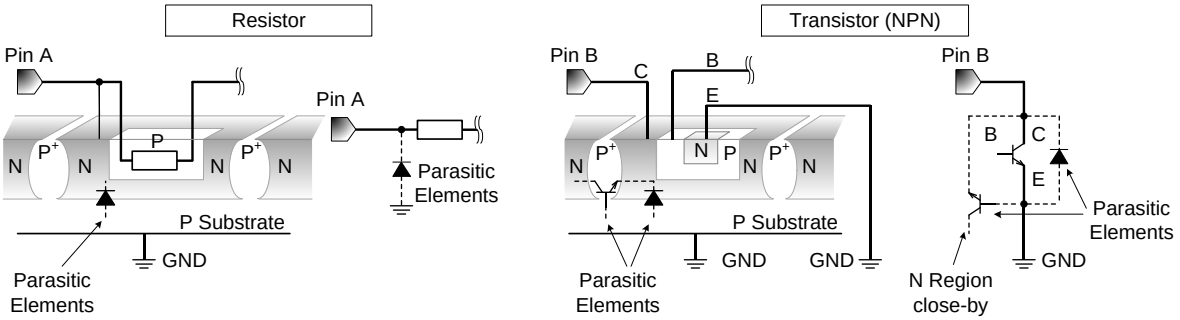


Figure 43. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

15. DC/DC switching line wiring pattern

DC/DC converter switching line (wiring from switching pin to inductor, Nch MOS) should be connected with short and wide wiring. If the wiring is long, ringing by switching would increase. That may cause excess voltage of absolute maximum ratings. If the wiring is obliged to lengthen by parts location limits, please consider inserting snubber circuit.

16. Discontinuous mode

The step-up and step-down DC/DC converters used in this IC have been designed on the assumption that the converters are used in continuous mode. Using the IC constantly while in discontinuous mode may result in malfunctions. To avoid this problem, make coil adjustments or insert a resistor between output and GND to prevent the IC from entering discontinuous mode while in use.

Ordering Information

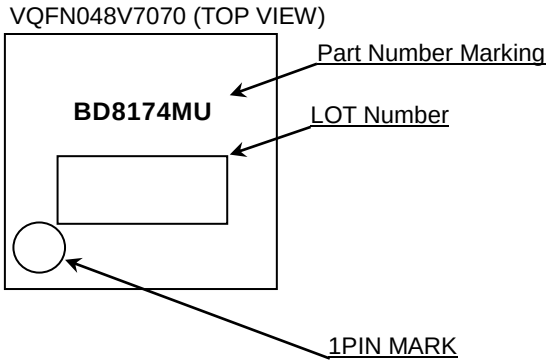
B	D	8	1	7	4	M	U	V	-	E 2

Part number

Package
MUV: VQFN048V7070

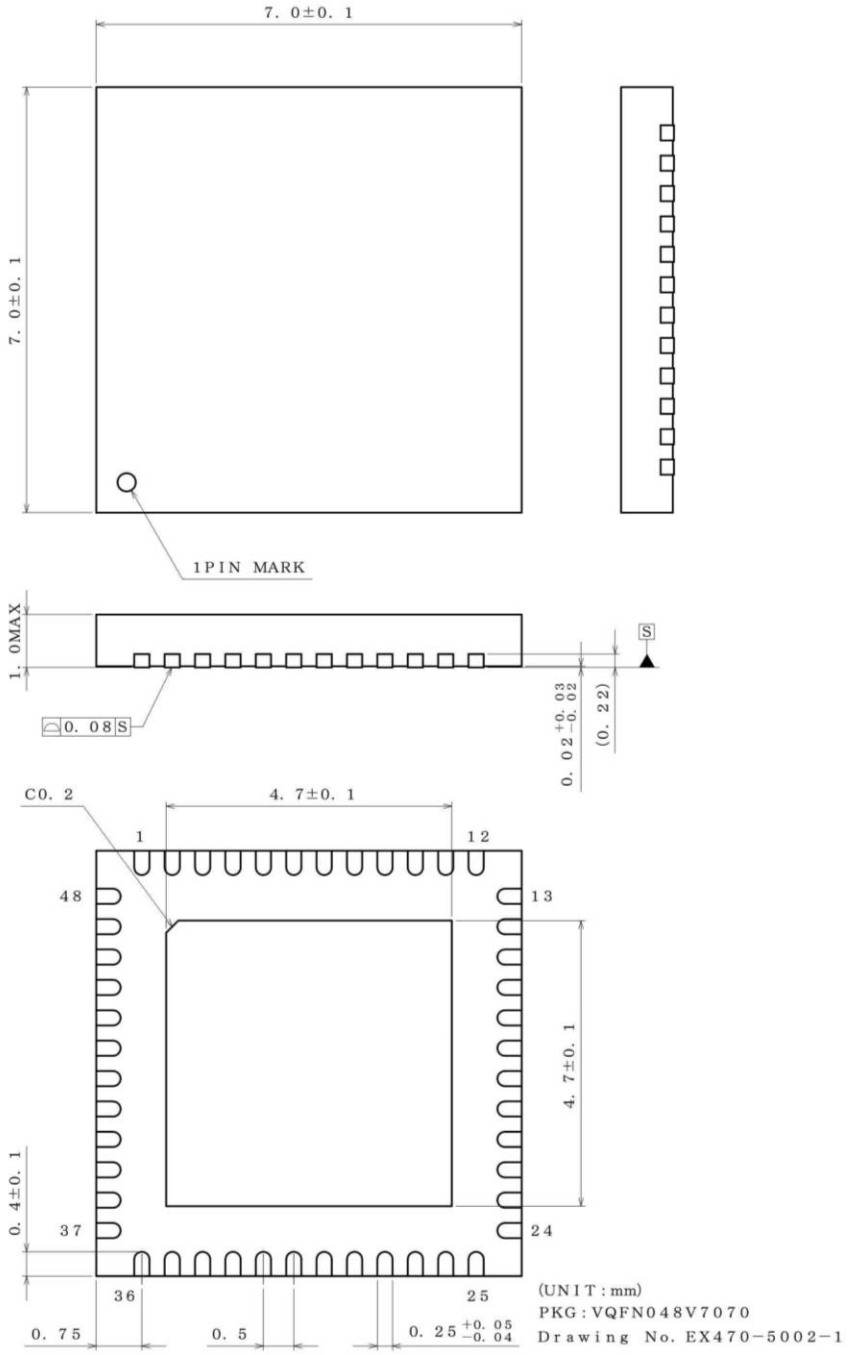
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



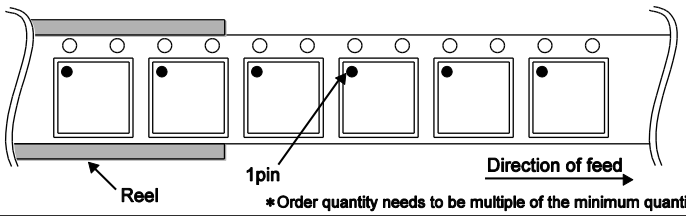
Physical Dimension, Tape and Reel Information

Package Name	VQFN048V7070



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
17.Feb.2016	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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