

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied supply voltage	VMAX	-0.3 ~ +6.5	V
Power dissipation	Pd	680 *1 (HVSO6)	mW
		410 *2 (HVSO5)	
		540 *3 (SSOP5)	
Operating temperature range	Topr	-40*4 ~ +85	°C
Storage temperature range	Tstg	-55 ~ +125	°C

*1 Derated at 6.8mW/°C for temperature above Ta = 25°C, when mounted on a glass epoxy PCB (70 mm X 1.6 mm).
 *2 Derated at 4.1mW/°C for temperature above Ta = 25°C, when mounted on a glass epoxy PCB (70 mm X 1.6 mm).
 *3 Derated at 5.4mW/°C for temperature above Ta = 25°C, when mounted on a glass epoxy PCB (70 mm X 1.6 mm).
 *4 BH□□FB1W series: -30°C and up.

● Recommended operating range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VIN	2.5	-	5.5	V
Output current	BH□□MA3W	-	-	300	mA
	BH□□FB1W	-	-	150	mA
	BH□□LB1W	-	-	150	mA

● Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input capacitor	CIN	0.1 *1	-	-	μF	Ceramic capacitor recommended
Output capacitor	Co	1.0 *2	-	-	μF	Ceramic capacitor recommended
Noise decrease capacitor	Cn	-	0.01	0.22	μF	Ceramic capacitor recommended

*1 BH□□MA3WHFV: 1.0 μF
 *2 The output may become unstable at low temperatures and with light loads, so a capacitance of 2.2 μF or much more is recommended when using at low temperatures. (BH□□FB1W)

● Electrical characteristics (Unless otherwise noted, Ta=25°C, VIN=VOUT+1V*2, STBY=1.5V, CIN=0.1μF, Co=1μF)

■ BH□□FB1WHFV/WG, BH□□LB1WHFV/WG

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output voltage *1	VOUT	VOUT ~ 0.99	VOUT	VOUT ~ 1.01	V	IOUT=1mA
Circuit current	I GND	-	40	70	μA	IOUT=50mA
Circuit current (STBY)	I STBY	-	-	1.0	μA	STBY=0V
Ripple rejection ratio	RR	-	70	-	dB	VRR=-20dBv, fRR=1kHz, IOUT=10mA
Load response 1	LTV1	-	50	-	mV	IOUT=1mA to 30mA
Load response 2	LTV2	-	50	-	mV	IOUT=30mA to 1mA
Dropout voltage *3	VSAT	-	250	450	mV	VIN=0.98 ~ VOUT, IOUT=100mA
Line regulation	VDL1	-	2	20	mV	VIN=VOUT+0.5V to 5.5V *4
Load regulation (1)	VDL01	-	10	30	mV	IOUT=1mA to 100mA
Load regulation (2)	VDL02	-	15	90	mV	IOUT=1mA to 150mA
Over current protection limit current	ILMAX	150 *3	250 *3	420 *3	mA	Vo=VOUT ~ 0.98
		150 *5	300 *5	450 *5		
Short current	I SHORT	-	50 *3	-	mA	Vo=0V
		-	40 *5	-		
STBY pull-down resistor	RSTB	550	1100	2200	kΩ	
STBY control voltage	ON	VSTBH	1.5	-	Vcc	V
	OFF	VSTBL	-0.3	-	0.3	V

* This product is not designed for protection against radio active rays.
 *1 BH15, 18LB1WHFV/WG: ±25 mV precision *3 Excluding BH15, 18LB1WHFV/WG *5 Excluding BH25,28,29,30,31,33WHFV/G
 *2 BH15, 18LB1WHFV/WG: VIN = 3.5 V *4 BH15, 18LB1WHFV/WG: VIN = 3.0 to 5.5 V

● Electrical characteristics (Unless otherwise noted, Ta=25°C, VIN=VOUT+1V*4, STBY=1.5V, CIN=1μF, Co=1μF)

■ BH□□MA3WHFV

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output voltage*1	VOUT	VOUT X 0.99	VOUT	VOUT X 1.01	V	IOUT=1mA
Circuit current	I GND	-	65	95	μA	IOUT=1mA
Circuit current (STBY)	I STBY	-	-	1.0	μA	STBY=0V
Ripple rejection ratio	RR	-	60	-	dB	VRR=-20dBv, fRR=1kHz, IOUT=10mA
Dropout voltage*2	VSAT1	-	60	90	mV	VIN=0.98 X VOUT, IOUT=100mA
Line regulation	VDL1	-	2	20	mV	VIN=VOUT+0.5V to 5.5V *3
Load regulation 1	VDL01	-	6	30	mV	IOUT=1mA to 100mA
Load regulation 2	VDL02	-	18	90	mV	IOUT=1mA to 300mA
Output voltage temperature	ΔVOUT/ΔT	-	±100	-	ppm/°C	IOUT=1mA, Ta=-40 to +85°C
Over current protection limit current	ILMAX	-	600	-	mA	Vo=VOUT X 0.85
Short current	I SHORT	-	100	-	mA	Vo=0V

* This product is not designed for protection against radio active rays.
 *1 BH15, 18MA3WHFV: ±25 mV precision *3 BH15, 18MA3WHFV: 3.0 to 5.5 V
 *2 Excluding BH15, 18MA3WHFV *4 BH15, 18MA3WHFV: 3.5 V

● Typical characteristics

● Output voltage–input voltage

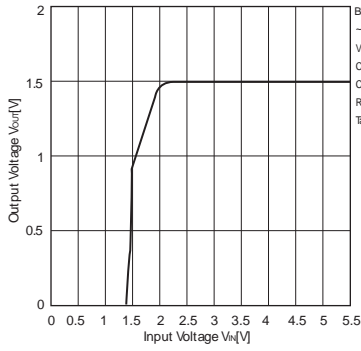


Fig.1

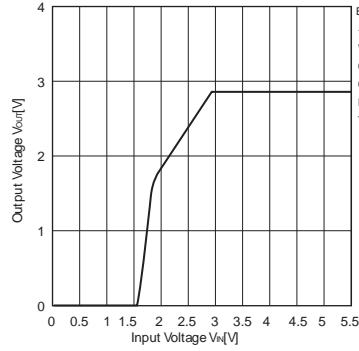


Fig.2

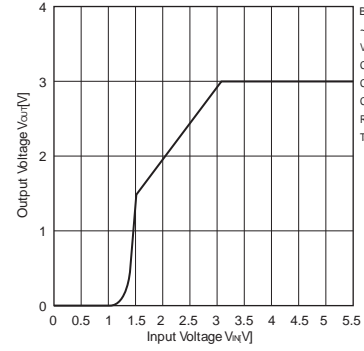


Fig.3

● GND current–input voltage

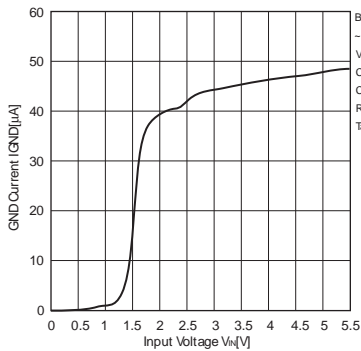


Fig.4

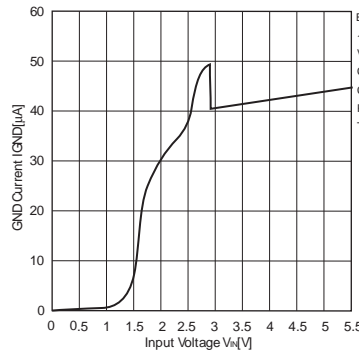


Fig.5

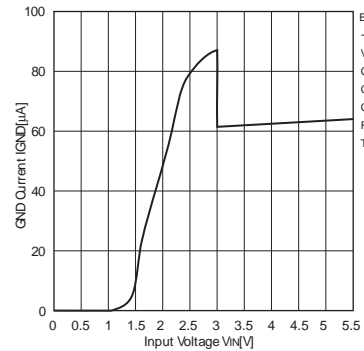


Fig.6

● Output voltage–output current

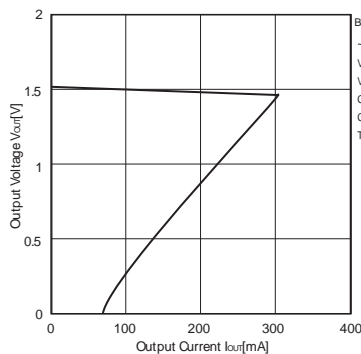


Fig.7

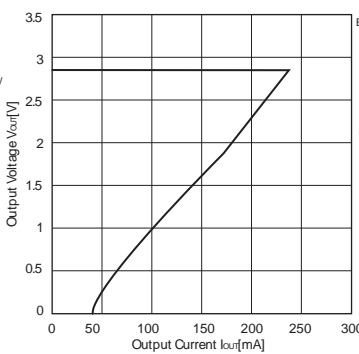


Fig.8

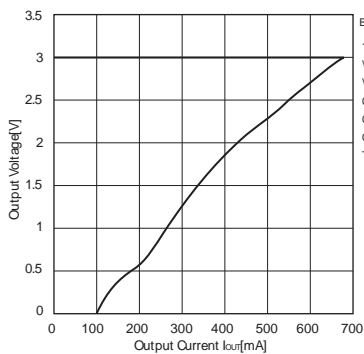


Fig.9

● Dropout voltage–output current

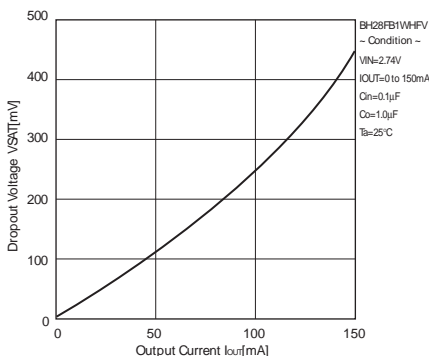


Fig.10

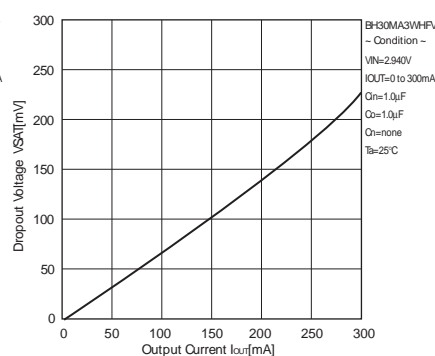


Fig.11

● Typical Characteristics
 • Output voltage–temperature

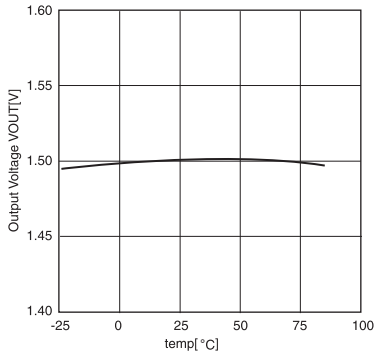


Fig.12

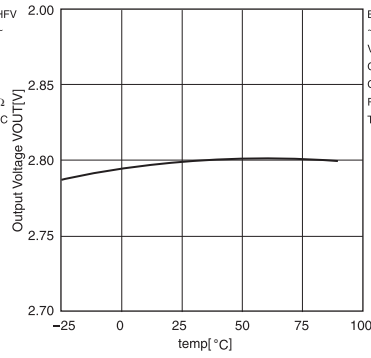


Fig.13

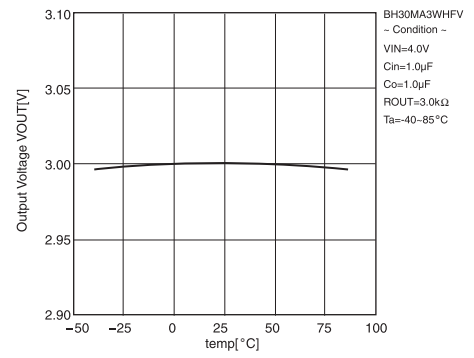


Fig.14

• Ripple reflection–frequency

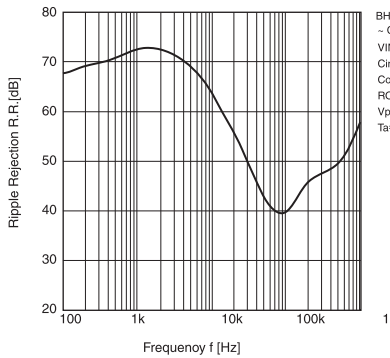


Fig.15

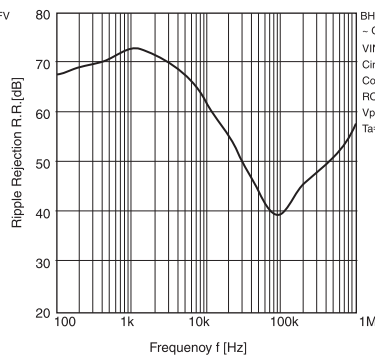


Fig.16

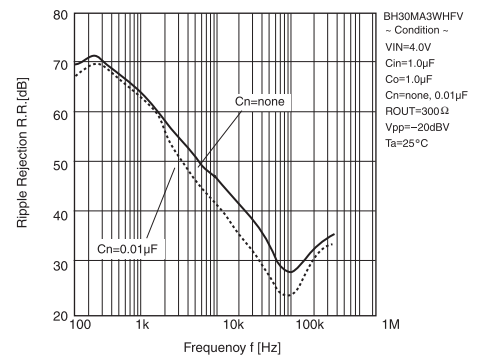


Fig.17

• Load response characteristics (CO = 1.0 μF)

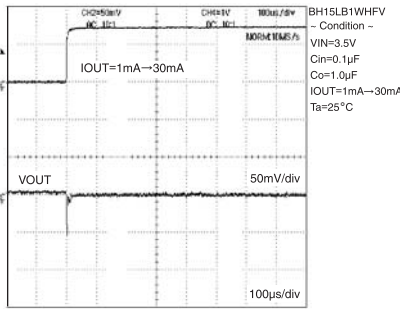


Fig.18

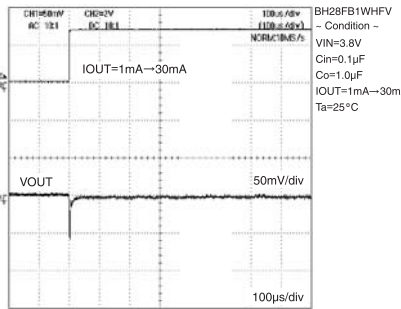


Fig.19

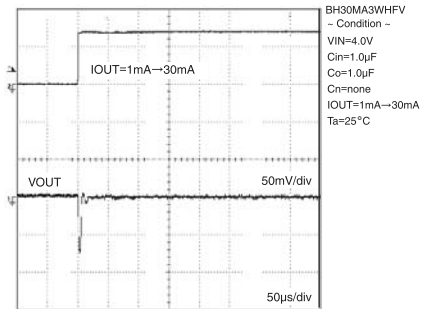


Fig.20

• Output voltage startup time

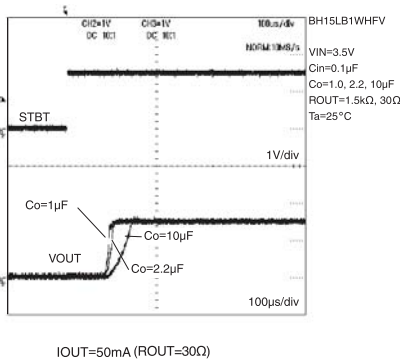


Fig.21

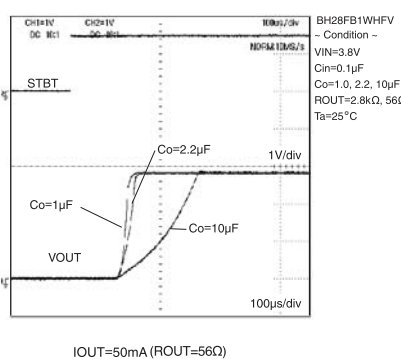


Fig.22

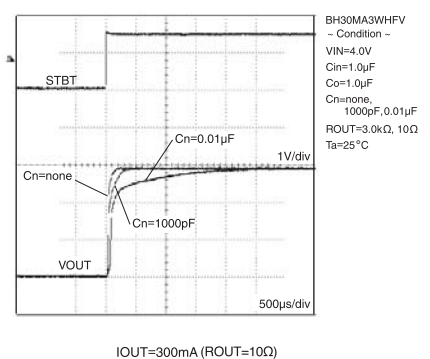


Fig.23

● Block diagrams

BH□□FB1WHFV/WG
BH□□LB1WHFV/WG

Fig.24

PIN No.	Symbol	Function
1	V _{IN}	Power supply input
2	GND	Ground
3	STBY	Output voltage ON/OFF control (High: ON, Low: OFF)
4	N. C.	NO CONNECT
5	V _{OUT}	Voltage output

PIN No.	Symbol	Function
1	STBY	Output voltage ON/OFF control (High: ON, Low: OFF)
2	GND	Ground
3	V _{IN}	Power supply input
4	V _{OUT}	Voltage output
5	N. C.	NO CONNECT

BH□□MA3WHFV

Fig.25

Terminal No.	Terminal Name	Function
1	V _{IN}	Power supply input
2	V _{OUT}	Voltage output
3	V _{OUT}	Voltage output
4	NOISE	Noise reducing capacitor ground terminal
5	GND	Ground
6	STBY	Output voltage ON/OFF control (High: ON, Low: OFF)

● Power dissipation Pd

1. Power dissipation

Power dissipation calculation include estimates of power dissipation characteristics and internal IC power consumption and should be treated as guidelines. In the event that the IC is used in an environment where this power dissipation is exceeded, the attendant rise in the junction temperature will trigger the thermal shutdown circuit, reducing the current capacity and otherwise degrading the IC's design performance. Allow for sufficient margins so that this power dissipation is not exceeded during IC operation.

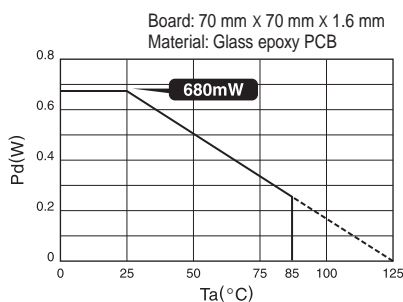
Calculating the maximum internal IC power consumption (P_{MAX})

$$P_{MAX} = (V_{IN} - V_{OUT}) \times I_{OUT}(MAX.)$$

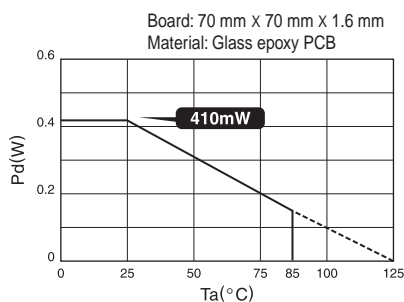
V_{IN} : Input voltage
V_{OUT} : Output voltage
I_{OUT}(MAX.) : Output current

2. Power dissipation characteristics (Pd)

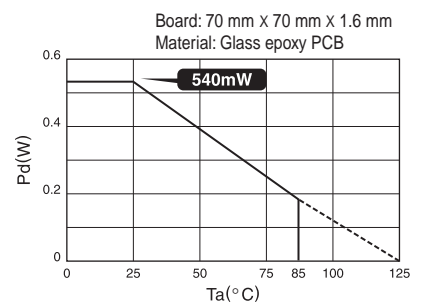
HVSO6



HVSO5



SSOP5



* Circuit design should allow a sufficient margin for the temperature range so that P_{MAX} < Pd.

● Input capacitor

It is recommended to insert bypass capacitors between input and GND pins, positioning them as close to the pins as possible. These capacitors will be used when the power supply impedance increases or when long wiring routes are used, so they should be checked once the IC has been mounted.

Ceramic capacitors generally have temperature and DC bias characteristics. When selecting ceramic capacitors, use X5R or X7R or better models that offer good temperature and DC bias characteristics and high torelant voltages.

Examples of ceramic capacitor characteristics

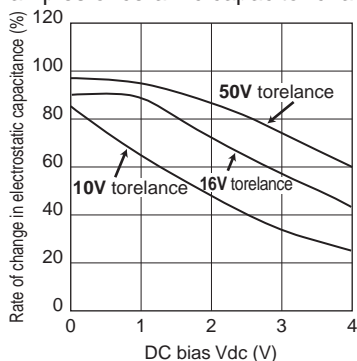


Fig. 29: Capacitance-bias characteristics (Y5V)

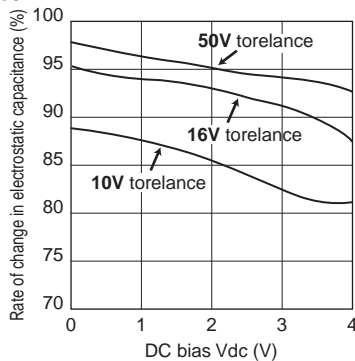


Fig. 30: Capacitance-bias characteristics (X5R, X7R)

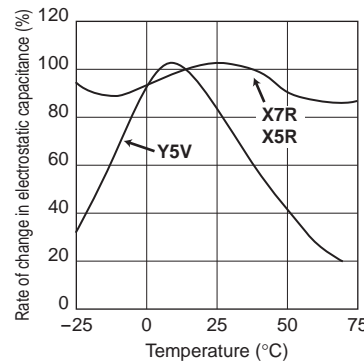


Fig. 31: Capacitance-temperature characteristics (X5R, X7R, Y5V)

● Output capacitor

To prevent oscillation at the output, it is recommended that the IC be operated at the stable region show in below Fig. It operates at the capacitance of more than 1.0μF. As capacitance is larger, stability becomes more stable and characteristic of output load fluctuation is also improved.

BH □ □ LB1WHFV/WG

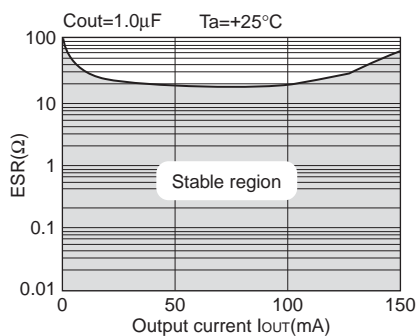


Fig. 32 BH □ □ LB1WHFV/WG Stable operating region characteristics (Example)

BH □ □ FB1WHFV/WG

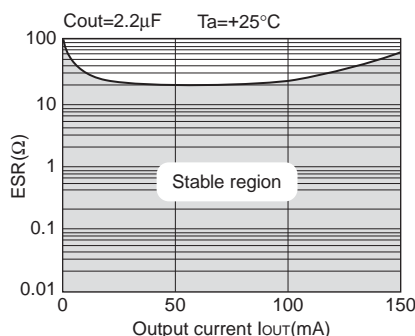


Fig. 33 BH □ □ FB1WHFV/WG Stable operating region characteristics (Example)

BH □ □ MA3WHFV

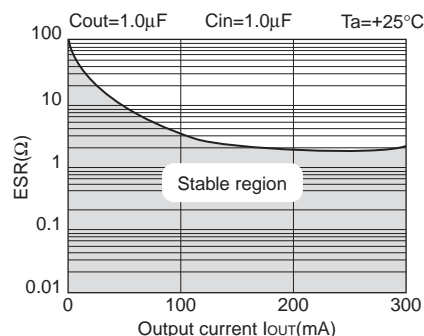


Fig. 34 BH □ □ MA3WHFV Stable operating region characteristics (Example)

● Other precautions

• Over current protection circuit

The IC incorporates a built-in over current protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuits use fold-back type current limiting and are designed to limit current flow by not latching up in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits.

• Thermal shutdown circuit

This system has a built-in thermal shutdown circuit for the purpose of protecting the IC from thermal damage. As shown above, this must be used within the range of power dissipation, but if the power dissipation happens to be continuously exceeded, the chip temperature increases, causing the thermal shutdown circuit to operate. When the thermal shutdown circuit operates, the operation of the circuit is suspended. The circuit resumes operation immediately after the chip temperature decreases, so the output repeats the ON and OFF states. There are cases in which the IC is destroyed due to thermal runaway when it is left in the overloaded state. Be sure to avoid leaving the IC in the overloaded state.

• Actions in strong magnetic fields

Use caution when using the IC in the presence of a strong magnetic field as such environments may occasionally cause the chip to malfunction.

• Back current

In applications where the IC may be exposed to back current flow, it is recommended to create a route to dissipate this current by inserting a bypass diode between the VIN and VOUT pins.

• GND potential

Ensure a minimum GND pin potential in all operating conditions.

In addition, ensure that no pins other than the GND pin carry a voltage less than or equal to the GND pin, including during actual transient phenomena.

● Noise terminal (BH□□MA3WHFV)

The terminal is directly connected to inward normal voltage source. Because this has low current ability, load exceeding 100nA will cause some instability at the output. For such reasons, we urge you to use ceramic capacitors which have less leak current. When choosing noise the current reduction capacitor, there is a trade-off between boot-up time and stability. A bigger capacitor value will result in lesser oscillation but longer boot-up time for VOUT.

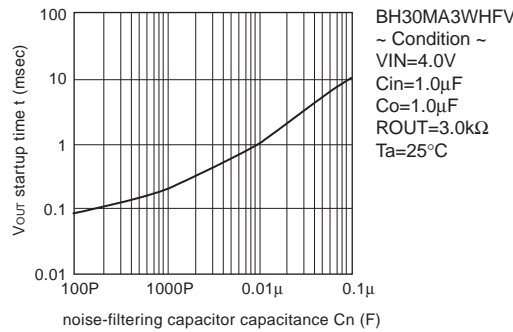


Fig. 35: V_{OUT} startup time vs. noise-filtering capacitor capacitance characteristics (Example)

● Regarding input pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when a resistor and transistor are connected to pins as shown in Fig.37

- The P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltage lower than the GND (P substrate) voltage to input pins.

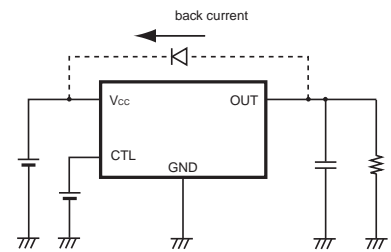


Fig. 36: Example of bypass diode connection

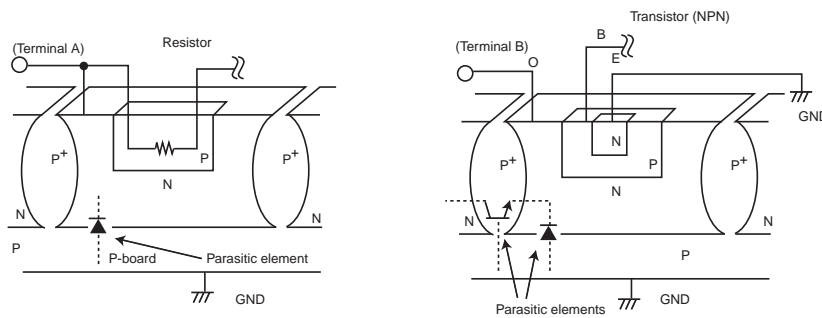
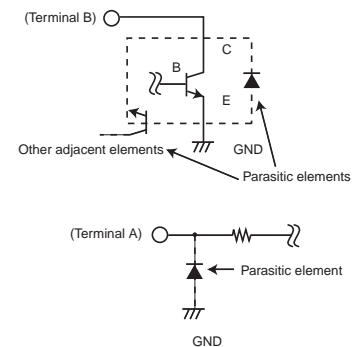
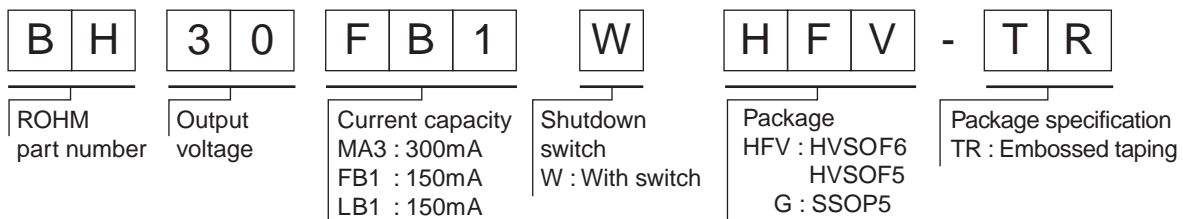
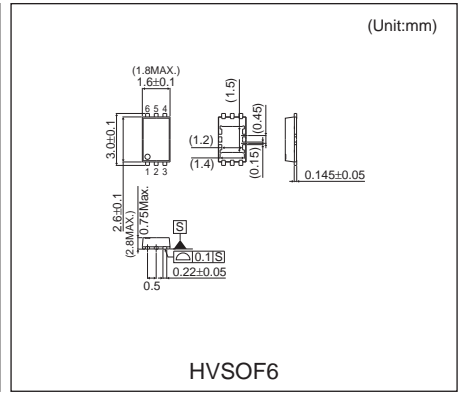
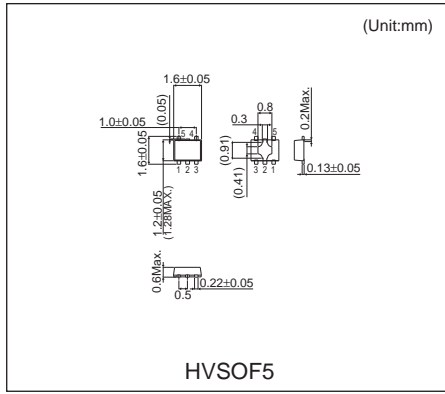
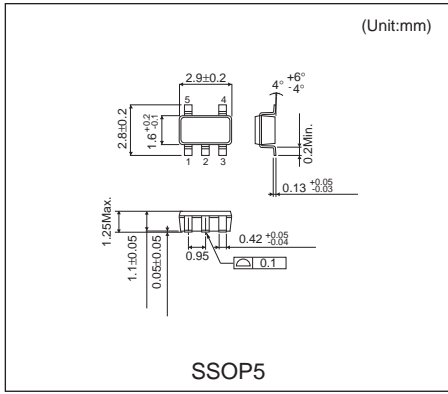


Fig.37



● Part number selection





(Package Specification) SSOP5, HVSOF5

Package Form	Embossed taping
Package Quantity	3000pcs
Package Orientation	TR (When the reel is held with the left hand and the tape is drawn out with the right hand, the No. 1 pin of the product faces the upper right direction.)

* Please make orders in multiples of the package quantity.

Detailed description: This diagram illustrates the package orientation for SSOP5 and HVSOF5. It shows a sequence of five packages on a reel. The reel is held on the left, and the tape is pulled out to the right. The packages are oriented such that the No. 1 pin of each package faces the upper right direction. The diagram is labeled 'Reel' on the left and 'Pulling side' on the right.

(Package Specification) HVSOF6

Package Form	Embossed taping
Package Quantity	3000pcs
Package Orientation	TR (When the reel is held with the left hand and the tape is drawn out with the right hand, the No. 1 pin of the product faces the upper right direction.)

* Please make orders in multiples of the package quantity.

Detailed description: This diagram illustrates the package orientation for HVSOF6. It shows a sequence of five packages on a reel. The reel is held on the left, and the tape is pulled out to the right. The packages are oriented such that the No. 1 pin of each package faces the upper right direction. The diagram is labeled 'Reel' on the left and 'Pulling side' on the right.

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