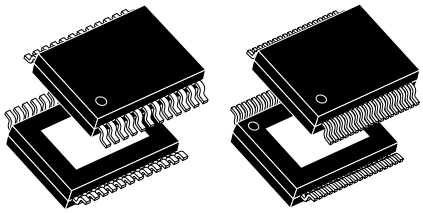
L9969x

Datasheet

Automotive chip for single and dual H-bridge



PowerSSO24 PowerSSO36

Product status links
L9969S
L9969T
L9969U

Product summary		
Order code	Package	Packing
L9969S	PSSO24	Tape and reel
L9969T	PSSO36	
L9969U		

Features

- AEC-Q100 qualification ongoing
- Full path RDSON less than 540 mΩ
- Nominal continuous load current > 3 A
- Operating battery supply voltage 4.5 V to 28 V
- Operating VDD supply voltage 4.5 V to 5.5 V
- All ECU internal pins can withstand up to 18 V
- Output switching frequency up to 20 kHz
- Monitoring of VDD supply voltage including bidirectional switch-off pin NABE
- Over temperature and short circuit protection
- Full diagnosis capability
- Output stage with SPI-adjustable current limitation 5-8.6 A in 3 steps (Two-point regulation)
- Fast switch-off open-drain input/output
- Current-monitoring with current feedback output signal CF
- Reliable full diagnostic capability
- Settable chip-address via bond-wire configuration on the silicon or E-Fuse
- SPI-interface for configuration and diagnosis
- Error history in diagnosis register
- Two independent enable pins: "NABE" and "DIS"
- Control of power stages by SPI or two input signals, PWM and DIR (configurable via SPI)
- Logic levels 5 V compatible
- Conformity to improved EMC requirements due to smart H-bridge switching
- Full ISO 26262 compliant, ASIL-B (D) systems ready

Description

L9969S/L9969U and L9969T are single and dual integrated H-bridges for resistive and inductive loads featuring output current direction and supervising functions.

The PowerSSO24 houses one full H-bridge, while the PowerSSO36 houses both two H-bridges that can work in parallel, through independent input driving commands.

Target application ranges from throttle control actuators to exhaust gas recirculation control valves in automotive domain to a more general use to drive DC and Stepper motors.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. L9969S/L9969U single bridge IC block diagram

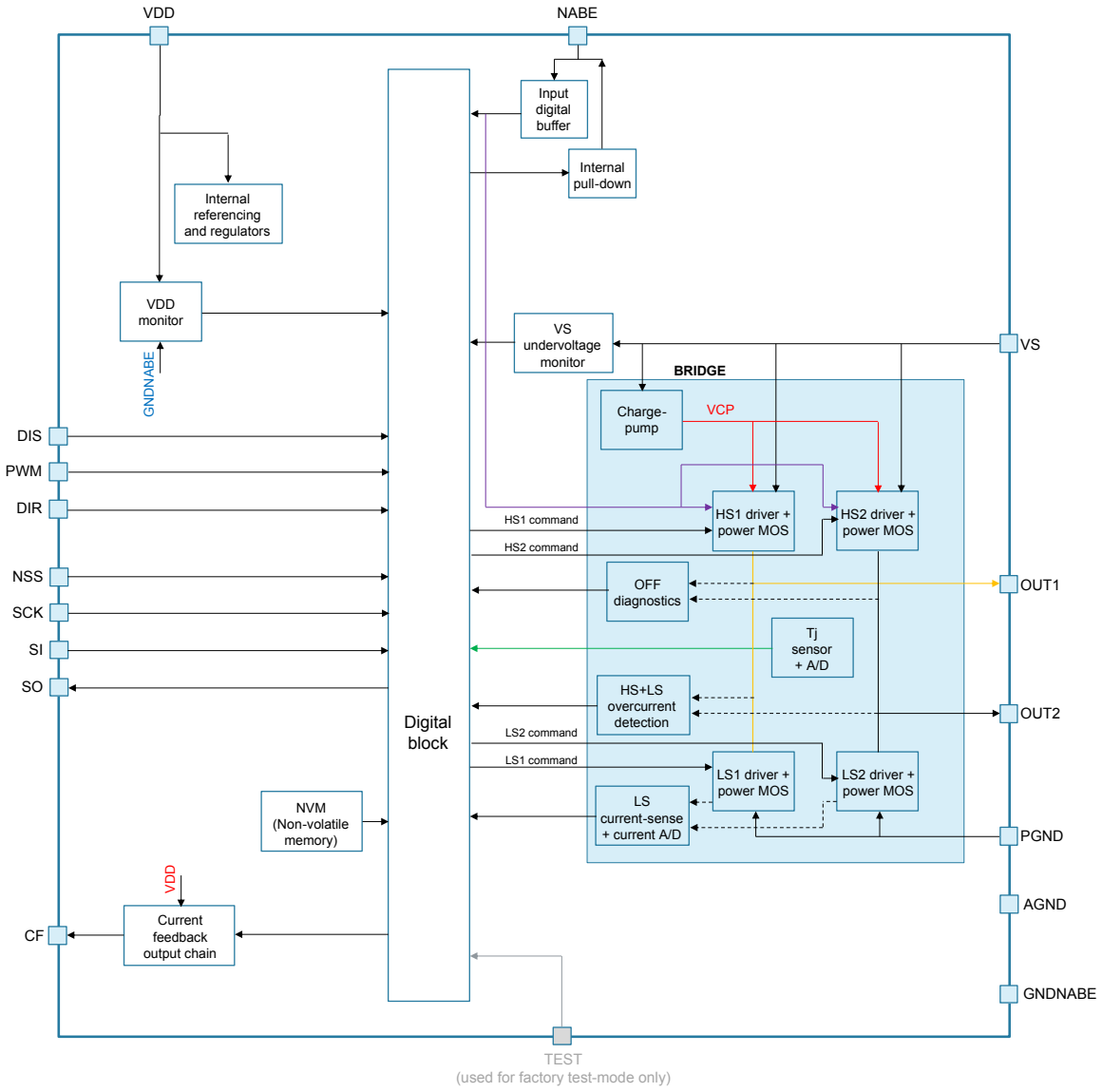
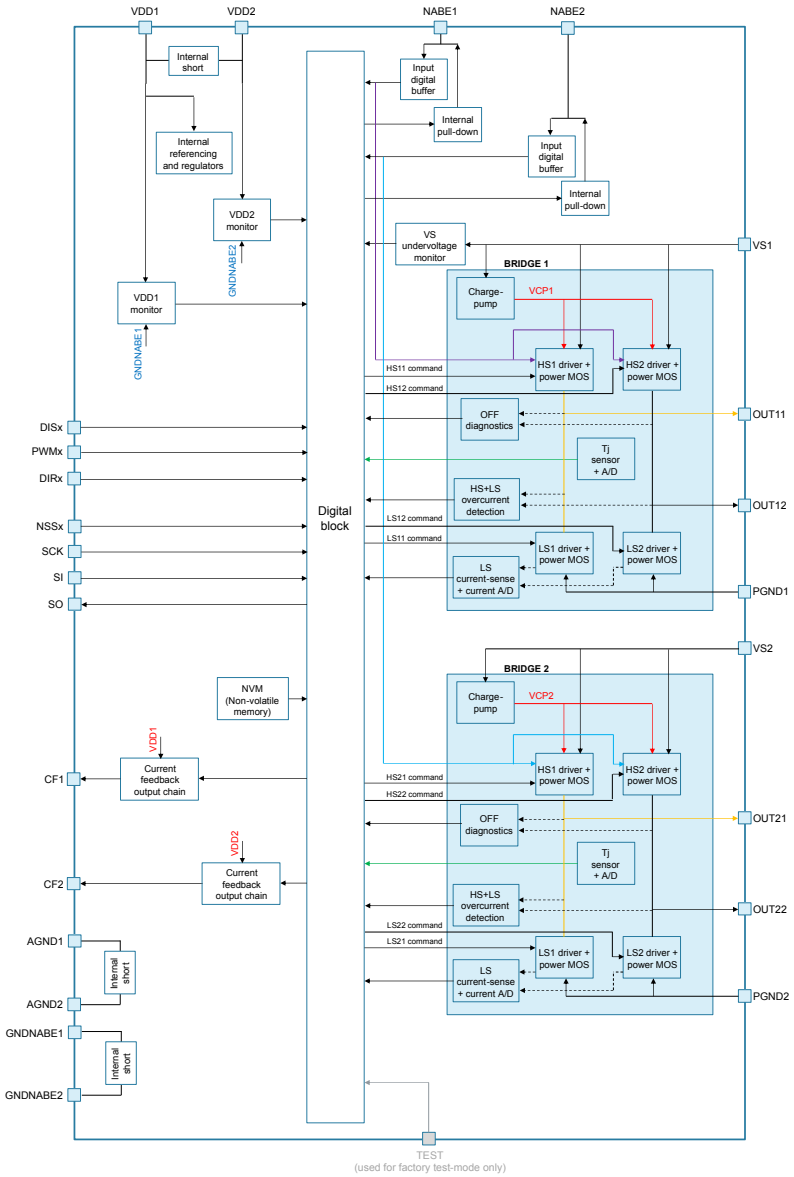


Figure 2. **L9969T twin bridge IC block diagram**



1.2 Pin description

Figure 3. **L9969S - pin connection (top view)**

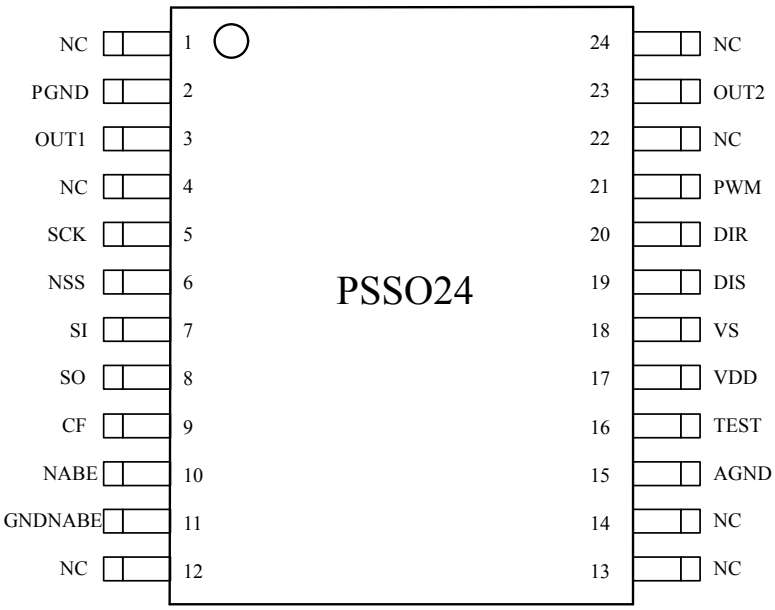


Figure 4. **L9969U - pin connection (top view)**

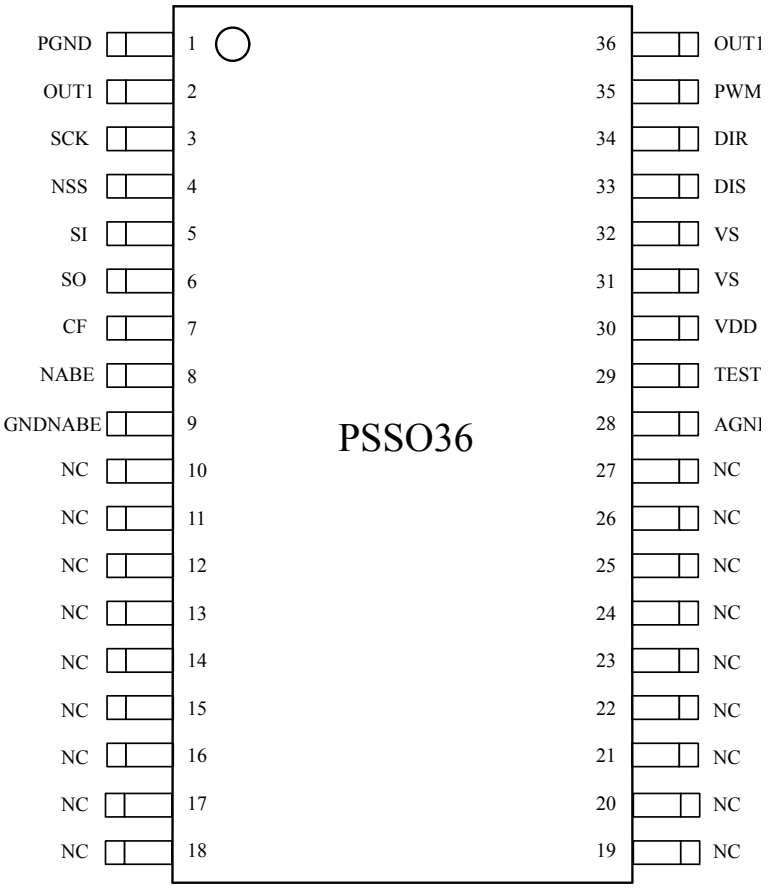
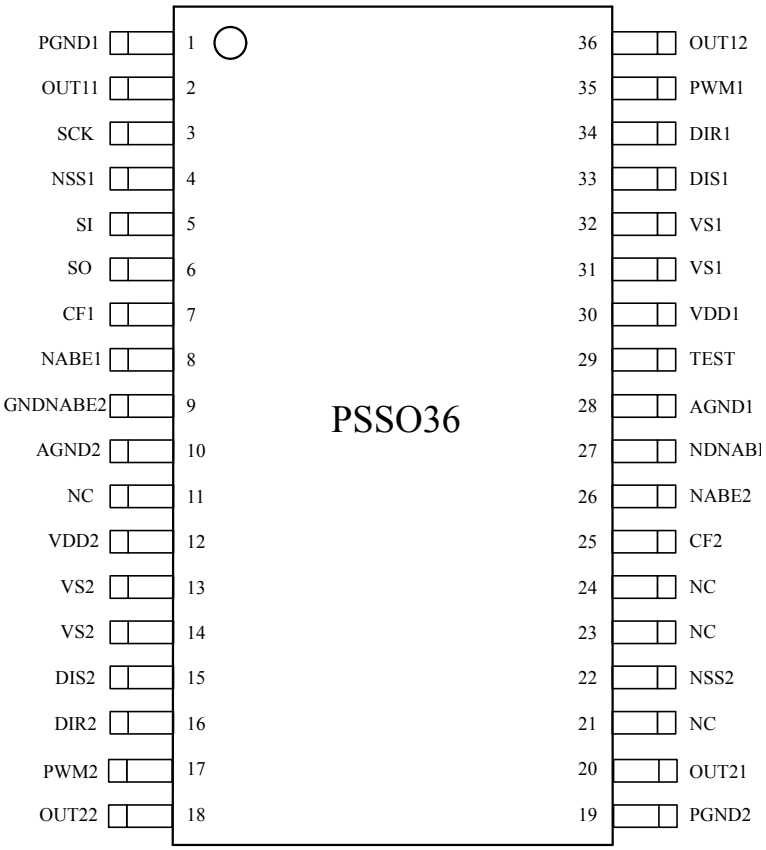


Figure 5. **L9969T - pin connection (top view)**



1.3 Pin definitions and functions

Table 1. **L9969S pin-out**

Pin #	Pin name	Description	I/O type	Class
1	NC	Not connected	-	-
2	PGND	Power Ground of H-bridge	G	Global
3	OUT1	Output 1 of H-bridge	O	Global
4	NC	Not connected	-	-
5	SCK	SPI-Clock input of H-bridge	I	Local
6	NSS	SPI-Slave Select input of H-bridge	I	Local
7	SI	SPI-Slave In (data receive) input of H-bridge	I	Local
8	SO	SPI-Slave Out (data transceive) output of H-bridge	O	Local
9	CF	Current feedback of H-bridge. Signal is proportional to the positive current in active LS-transistor of H-bridge.	O	Local
10	NABE	Bidirectional Enable/Disable in-/output. Open-drain output, switched to low at VDD over and undervoltage condition. Low level disables the power stage. (OUT1 and OUT2)	I/O	Local
11	GNDNABE	Reference Ground of VDD-monitoring.	G	Local
12	NC	Not connected	-	-

Pin #	Pin name	Description	I/O type	Class
13	NC	Not connected	-	-
14	NC	Not connected	-	-
15	AGND	Ground connection of H-bridge	G	Local
16	TEST	Factory test-mode activation	I	Local
17	VDD	5 V Supply for H-bridge. Input for VDD monitoring.	P	Local
18	VS	Supply voltage for H-bridge power stage	P	Global
19	DIS	Disable input for H-bridge. High-level disables the power stage (OUT1 and OUT2)	I	Local
20	DIR	Direction input of H-bridge.	I	Local
21	PWM	PWM input of H-bridge. Controls the frequency and the duty cycle of the power stage (OUT1 and OUT2).	I	Local
22	NC	Not connected	-	-
23	OUT2	Output 2 of H-bridge.	O	Global
24	NC	Not connected	-	-
-	Exp. PAD	Exposed pad is connected to AGND	-	-

Note: ***Legenda:*** *I = Input, O = Output, P = Power Supply, G = Ground, I/O = Input/Output*

Table 2. L9969U pin-out

Pin #	Pin name	Description	I/O type	Class
1	PGND	Power Ground of H-bridge	G	Global
2	OUT1	Output 1 of H-bridge	O	Global
3	SCK	SPI-Clock input	I	Local
4	NSS	SPI-Slave Select input	I	Local
5	SI	SPI-Slave In (data receive) input	I	Local
6	SO	SPI- Slave Out (data transceive) outpu	O	Local
7	CF	Current feedback of H-bridge Signal is proportional to the positive current in active LS-transistor of H-bridge.	O	Local
8	NABE	Bidirectional Enable/Disable in-/output. Open-drain output, switched to low at VDD over and undervoltage condition. Low level disables the power stage. (OUT1 and OUT2)	I/O	Local
9	GNDNABE	Reference Ground for VDD-monitoring of H-bridge	G	Local
10	NC	Not connected.	-	-
11	NC	Not connected.	-	-
12	NC	Not connected.	-	-
13	NC	Not connected.	-	-
14	NC	Not connected.	-	-
15	NC	Not connected.	-	-
16	NC	Not connected.	-	-
17	NC	Not connected.	-	-
18	NC	Not connected.	-	-

Pin #	Pin name	Description	I/O type	Class
19	NC	Not connected.	-	-
20	NC	Not connected.	-	-
21	NC	Not connected.	-	-
22	NC	Not connected.	-	-
23	NC	Not connected.	-	-
24	NC	Not connected.	-	-
25	NC	Not connected.	-	-
26	NC	Not connected.	-	-
27	NC	Not connected.	-	-
28	AGND	Ground connection for H-bridge (Device ground)	G	Local
29	TEST	Factory test-mode activation	I	Local-
30	VDD	5 V Supply for H-bridge. Input for VDD monitoring.	P	Local
31	VS	Supply voltage of H-bridge power stage	P	Global
32	VS	Supply voltage of H-bridge power stage	P	Global
33	DIS	Disable input of H-bridge. High-level disables the power stage (OUT1 and OUT2)	I	Local
34	DIR	Direction input of H-bridge	I	Local
35	PWM	PWM input of H-bridge Controls the frequency and the duty cycle of the power stage (OUT1 and OUT2).	I	Local
36	OUT2	Output 2 of H-bridge	O	Global
-	Exp. PAD	Exposed pad is connected to AGND	-	-

Note: ***Legenda:*** *I = Input, O = Output, P = Power Supply, G = Ground, I/O = Input/Output*

Table 3. L9969T pin-out

Pin #	Pin name	Description	I/O type	Class
1	PGND1	Power Ground of H-bridge1	G	Global
2	OUT11	Output 1 of H-bridge1	O	Global
3	SCK	SPI-Clock input	I	Local
4	NSS1	SPI-Slave Select input of H-bridge1	I	Local
5	SI	SPI-Slave In (data receive) input	I	Local
6	SO	SPI-Slave Out (data transceive) output	O	Local
7	CF1	Current feedback for H-bridge1. Signal is proportional to the positive current in active LS-transistor of H-bridge1.	O	Local
8	NABE1	Bidirectional Enable/Disable in-/output. Open-drain output, switched to low at VDDx over and undervoltage condition. Low level disables the power stage. (OUT11 and OUT12)	I/O	Local
9	GNDNABE2	Reference Ground for VDD2-monitoring of H-bridge 2	G	Local
10	AGND2	Ground connection for H-bridge2 (Device ground)	G	Local
11	NC	Not connected.	-	-
12	VDD2	5 V Supply for H-bridge (2). Input for VDD (2) monitoring.	P	Local

Pin #	Pin name	Description	I/O type	Class
13	VS2	Supply voltage for H-bridge2 power stage	P	Global
14	VS2	Supply voltage for H-bridge2 power stage	P	Global
15	DIS2	Disable input for H-bridge2. High-level disables the power stage (OUT21 and OUT22)	I	Local
16	DIR2	Direction input of H-bridge2.	I	Local
17	PWM2	PWM input of H-bridge2. Controls the frequency and the duty cycle of the power stage (OUT21 and OUT22).	I	Local
18	OUT22	Output 2 of H-bridge2	O	Global
19	PGND2	Power ground connection for H-bridge2.	G	Global
20	OUT21	Output 1 of H-bridge2	O	Global
21	NC	not connected.	-	-
22	NSS2	SPI-Slave Select input of H-bridge2.	I	Local
23	NC	not connected.	-	-
24	NC	not connected.	-	-
25	CF2	Current feedback of H-bridge2. Signal is proportional to the positive current in active LS-transistor of H-bridge2.	O	Local
26	NABE2	Bidirectional Enable/Disable in-/output. Open-drain output, switched to low at VDDx over and undervoltage condition. Low level disables the power stage. (OUT21 and OUT22)	I/O	Local
27	GNDNABE1	Reference Ground of VDD1-monitoring of H-bridge 1	G	Local
28	AGND1	Ground connection for H-bridge1 (Device ground)	G	Local
29	TEST	Factory test-mode activation	I	Local
30	VDD1	5 V Supply for H-bridge1. Input for VDD1 monitoring.	P	Local
31	VS1	Supply voltage of H-bridge1 power stage	P	Global
32	VS1	Supply voltage of H-bridge1 power stage	P	Global
33	DIS1	Disable input of H-bridge1. High-level disables the power stage (OUT11 and OUT12)	I	Local
34	DIR1	Direction input of H-bridge1.	I	Local
35	PWM1	PWM input of H-bridge1. Controls the frequency and the duty cycle of the power stage (Out11 and Out 12).	I	Local
36	OUT12	Output 2 of H-bridge1.	O	Global
-	Exp. PAD	Exposed pad is connected to AGNDx	-	-

Note: ***Legenda:*** *I = Input, O = Output, P = Power Supply, G = Ground, I/O = Input/Output*

2 Electrical specifications

2.1 Operating range

Within the operating range the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.

Table 4. Operating range

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VS_or	VS operative range	-	5	-	18	V
VDD_or	VDD operative range	-	4.5	-	5.2	V
T_j	Junction temperature	-	-40	-	150	°C
V_{VS_slew}	Maximum slew rate on V_S (no change of parameters)	VDD = 5 V IOUT = 3 A V_S = 6 V, 10 V, 14 V, 18 V	-	-	20	V/µs
V_{GND_DELTA}	Voltage differences between GND pins	-	-0.3	-	0.3	V

2.2 Thermal data

Table 5. Temperature data

Symbol	Description	Min	Typ	Max	Unit
T_{amb}	Operating temperature (ECU environment)	-40	-	125	°C
T_j	Operating junction temperature	-40	-	150	°C
T_{stg}	Storage temperature	-55	-	150	°C
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient for L9969T PSSO36	-	23.9	-	°C/W
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient for L9969S PSSO36	-	25.4	-	°C/W
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient for L9969S PSSO24	-	25.4	-	°C/W
$R_{Th\ j\text{-}case\_bot}$	Thermal resistance junction-to-case bottom for L9969T PSSO36	-	1	-	°C/W
$R_{Th\ j\text{-}case\_bot}$	Thermal resistance junction-to-case bottom for L9969S PSSO36	-	2	-	°C/W
$R_{Th\ j\text{-}case\_bot}$	Thermal resistance junction-to-case bottom for L9969S PSSO24	-	2	-	°C/W

2.2.1 Temperature and load profile

The IC is designed for temperature profile that is transferred for T_j = 175 °C at t ≥ 1500 h.

2.3 Absolute maximum ratings

2.3.1 Supply voltage

There is no special sequence to switch on the different voltages (V_S, VDD and voltages on any input pins).

Even if there is only V_S applied, signals on the internal inputs or outputs, even up to 18 V, must not result in any kind of faulty reaction of the H-bridge or in a destruction of the H-bridge.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VS}	VS Static destruction proof	VDD = 0 V VDD = 5 V	-1.0	-	28	V
V_{VS}	VS Dynamic destruction proof; see load dump pulse	VDD = 0 V VDD = 5 V	-1.0	-	40	V
$I_{VS,INV}$	Dynamic destruction proof t < 0.25 s	VDD = 0 V VDD = 5 V	-	-	5.0	A
V_{VDD}	VDD Static destruction proof	V_S = 0 V V_S = 18 V	-0.5	-	18	V
V_{cp}	Charge Pump Destruction proof	VDD = 0 V VDD = 5 V	-	-	V_{VS} + CP voltage	V
V_{Outx}	Vout static destruction proof	V_S = 28 V VDD = 0 V VDD = 5 V I_x = 3 A	-1.0	-	VS +Vf	V
V_{Outx}	V_{out} dynamic destruction proof, see load dump pulse) load condition: 0.8 mH to 1 mH, PWM f_{max} = 20 kHz)	V_S = 40 V VDD = 0 V VDD = 5 V I_x = 10 A	-	-	VS +Vf	V
I_{Outx}	Iout dynamic destruction proof t < 0.5 s (load condition: 0.8 mH to 1 mH, PWM f_{max} = 20 kHz)	VOUTx ≤ V_S + Vf VDD = 0 V VDD = 5 V	-	-	10	A
V_x	Static destruction proof for internal pins	V_S = 0 V V_S = 18 V VDD = 0 V VDD = 5 V VDD = 18 V	-0.5	-	18	V
V_{VS_slew}	Maximum slew rate on V_S (no destruction and no change of parameters)	VDD = 5 V IOUT = 3 A V_S = 6 V, 10 V, 14 V, 18 V	-	-	60	V/µs

Note: Vf is the voltage drop (by the defined current) over the body diode of the H-bridge driver.

2.4 Quiescent current consumption

L9969 can guarantee quiescent current values below defined values. Table 7 reports all cases of interest, varying from disabled bridge, to bridge driven ON at different PWM frequencies, but without any output current to loads.
5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 7. Quiescent current consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VS}	Quiescent current consumption	5 V < V_S < 18 V Bridge disabled VDD = 5 V	-	-	15	mA
I_{VS}	Stand-by current consumption	V_S = 14 V Bridge disabled VDD = 0 V	10	-	100	µA
I_{VS}	Quiescent current consumption	5 V < V_S < 18 V f_{OUT} = 2 kHz VDD = 5 V IOUT = 0 A	-	-	18	mA
I_{VS}	Quiescent current consumption	5 V < V_S < 18 V f_{OUT} = 10 kHz VDD = 5V IOUT = 0 A	-	-	21	mA
I_{VS}	Quiescent current consumption	V_S = 28 V f_{OUT} = 10 kHz VDD = 5 V IOUT = 0 A	-	-	25	mA

2.5 ESD protection

Table 8. ESD protection

Item	Parameter	Condition	Min	Typ	Max	Unit
All pins	-	HBM	-2	-	2	kV
All pins	-	CDM (values for corner pins in brackets)	-500/(-750)	-	500/(750)	V
Pins to connector (1)	-	HBM	-4	-	4	kV

1. *Pins are all GND connected together.*

2.6 Power Supply

Figure 6 shows the connections between power supplies and L9969 internal blocks.

Figure 6. Schematic of internal power supply

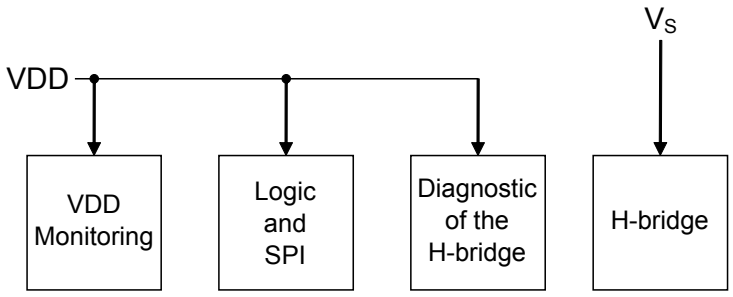


Table 9. VDD current absorption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{VDD\_SINGLE\_OFF}$	Single bridge IC VDD supply current, bridge disabled	VDD = 4.5 V to 5.5 V DIS = VDD NABE = 0 V R_{CF} = 5.1 kΩ CL4	-	-	11	mA
$I_{VDD\_SINGLE\_ON\_3A}$	Single bridge IC VDD supply current, bridge enabled with 3 A load	VDD = 4.5 V to 5.5 V DIS = 0 V NABE = VDD R_{CF} = 5.1 kΩ PWM = DIR = 0 V I_{OUT} = 3 A CL4	-	-	13.4	mA
$I_{VDD\_TWIN\_OFF}$	Twin bridge IC VDD supply current (VDD1 + VDD2), both bridges disabled	VDDx = 4.5 V to 5.5 V DISx = VDD NABEx = 0 V R_{CFx} = 5.1 kΩ CL4	-	-	18.3	mA
$I_{VDD\_TWIN\_ON\_3A}$	Twin bridge IC VDD supply current (VDD1 + VDD2), both bridges enabled with 3 A load	VDDx = 4.5 V to 5.5 V DISx=0V NABEx = VDD R_{CFx} = 5.1 kΩ PWMx = DIRx = 0 V I_{OUTx2} = 3 A CL4	-	-	23.1	mA

2.6.1 Power-ON reset

VDD is internally monitored, to keep the output stages in tristate in case VDD is incorrect.

Two internal monitoring/resetting sources are implemented:

- The internal reset function in the H-bridge if VDD is decreasing down to V_{DD_RES}. That function resets the SPI registers, switches the output stages to tristate and switches NABE to low.
- The internal VDD monitoring, that is working, if the VDD > VDD_POR for longer than tPOR. In this case, the SPI is working; the VDD monitoring is active and sets the SPI registers, switches the output stages to tristate and switches NABE to low, if VDD is incorrect. In any cases, after a Power-ON Reset, the H-bridge is completely functional again, but the outputs are disabled. They can only be enabled by ENDISR.

5 V < VBATT < 18 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 10. VDD monitoring thresholds

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD_RES}	VDD Undervoltage Threshold (VDD: 'H' → 'L') Below this threshold the device is in reset state, all registers are cleared.	-	3.3	3.6	3.9	V
V_{DD_POR}	Power On Reset Threshold (VDD: 'L' → 'H') Below this threshold the device is in reset state, all registers are cleared. The device starts operation (VDD monitoring forces stages off) not later than t_{POR}, when VDD is rising above this threshold. SPI is functional.	-	3.5	3.8	4.1	V
t_{POR}	Power On Reset Extension Time	-	-	-	1000	µs

2.6.2 NABE and VDD monitoring

2.6.2.1 General functions of VDD monitoring

V_{DD} is measured with reference to pin GND_{ABE}. Inside the H-bridge, GND_{ABE} is routed separately to avoid internal cross talking from power lines.

The state of V_{DD} monitoring is stored in STATCON_REG and is read/write via SPI.

V_{DD} monitoring detects faulty supply voltages at V_{DD}. It disables the output stages but does not reset registers DIA_REG1, DIA_REG2, CONFIG_REG or STATCON_REG.

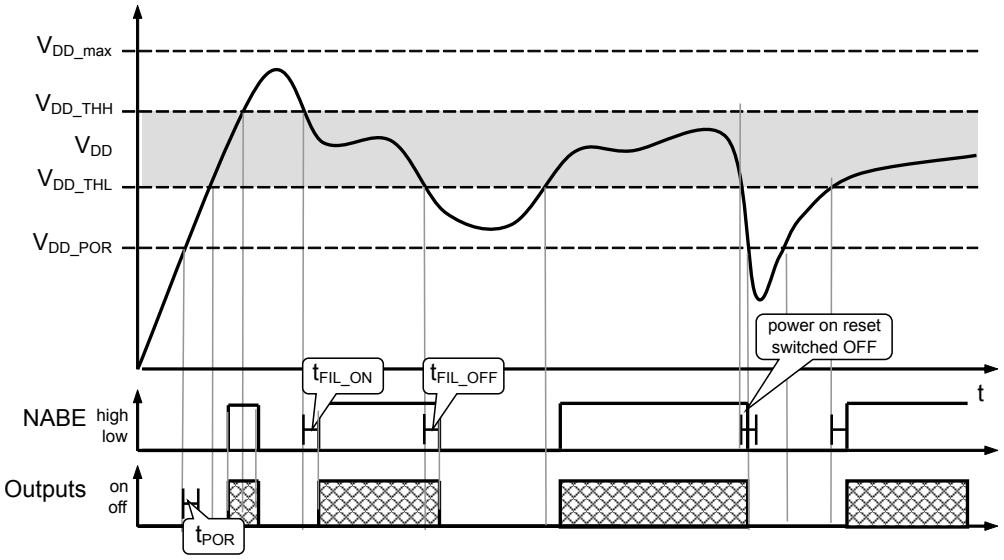
In case of V_{DD} failure, the output stages are switched off, even if the voltage at pin NABE is a high level, for example because of an external short circuit to V_{DD} or to the battery voltage (up to 18 V).

OUT1 and OUT2 cannot be switched on in over or undevoltage condition at V_{DD}.

POR (V_{DD} < V_{DD_RES}) switches off all output stages without delay.

Detailed information (differentiation of over and undervoltage detection) is possible by SPI interface.

Figure 7. **VDD Monitoring and dependencies**



2.6.2.2 *VDD undervoltage*

If the voltage between pins V_{DD} and GND_{ABE} is below the lower V_{DD}-monitoring threshold (V_{DD_THL}), the output stages are switched off after a filtering time (t_{FIL_OFF}) and an active low signal is generated at the bi-directional pin NABE. After a transition from an undervoltage to a regular voltage between pins V_{DD} and GND_{ABE}, the signal at pin NABE is (automatically) set high again once the filtering time (t_{FIL_ON}) has expired. Writing new information to configuration registers is possible.

If VDD falls below the power-on-reset supply voltage (V_{DD_RES}) all stages are switched off and NABE is switched active low. When VDD is rising above the power-on-reset supply voltage threshold (V_{DD_POR}), the ASIC will remain in POR until a time t_{POR} is run out, then all registers will be reset to their respective default state (all registers cleared to default).

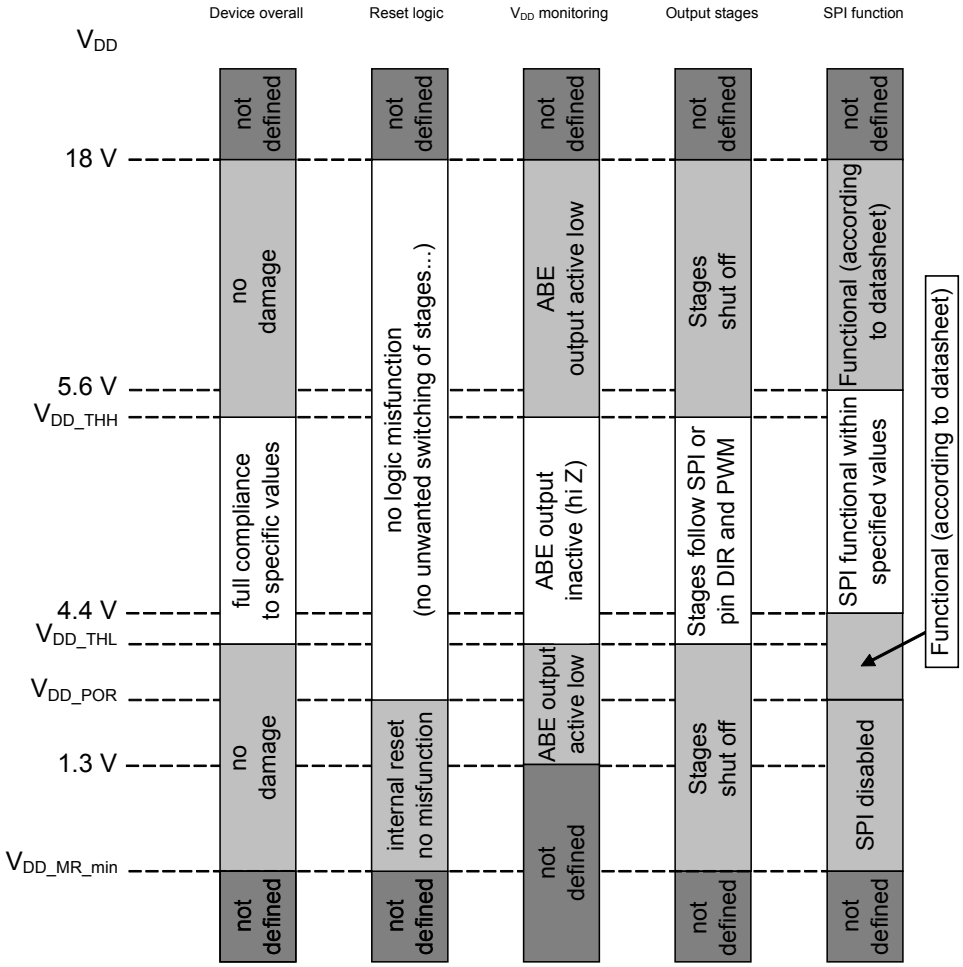
2.6.2.3 *VDD overvoltage*

If the voltage between pins V_{DD} and GND_{ABE} is above the upper V_{DD}- monitoring threshold (V_{DD_THH}), all output stages are switched off after a filtering time (t_{FIL_OFF}) and an active low signal is generated at the bi-directional pin NABE.

After a transition from an overvoltage to a regular voltage between pins V_{DD} and GND_{ABE}, the behavior of the NABE level and the output stages depend on the configuration of the bit CONFIG0 of STATCON_REG:

- 1: NABE is latched and the outputs remain off. A return to normal operation is only possible with power-on reset or by changing the bit STATCON_REG.CONFIG0 via SPI → 0.
- 0: NABE is inactive after VDD returned to its regular operating voltage and the filtering time has expired. The power stages are enabled again automatically. Writing new information to configure registers is possible.

Figure 8. **Overview of VDD voltage ranges**



2.6.2.4 *Behavior on pin NABE in case of external short circuit*

In case a short circuit on the PCB pulls both pins NABE and V_{DD} for example, to the battery voltage (max. 18 V), the internal power-stage at pin NABE is designed in such a way that the H-bridge is not damaged, in case NABE is pulled-down internally to GND, even though an external battery voltage is applied low-ohmic to pin NABE. The internal power-stage sustains such short-circuit for a few hours.

2.6.2.5 *NABE Pin*

NABE is a bidirectional pin (input and output). As an input function, all output power-stages are permanently switched off if an external low signal is applied to pin NABE. NABE output is realized as an open drain low side switch. During a V_{DD} over-voltage (above V_{DD_THH}) or undervoltage (below V_{DD_THL}), the pin is pulled to GND (logic low). Refer also to Section 2.6.2.4 Behavior on pin NABE in case of external short circuit in case of an external short circuit at pin NABE.

The NABE-Pin is made redundant to the DIS-Pin to reach the ISO26262 Safety Goals. The NABE goes directly to the Gate-Driver of the Bridge.

The default signal level of “NABE” (for example in case of ECU initialization) is low-level with integrated pull down-current source.

A low logic level at “NABE” and/or a high logic level at “DIS” switch off all output stages. In this case the access to the SPI is possible and the bit NABE_DIS in the DIA_REG1 is set to low.

Two separate pins are provided for NABE and DIS. For safety reasons, these signals are routed separately and ideally with a certain distance from each other on the silicon.

2.6.2.6 *Testing of VDD monitoring*

VDD Monitoring cannot be switched off. The output stages are switched off by V_{DD} monitoring if under or overvoltage on V_{DD} is detected. Testing of V_{DD} monitoring is possible via SPI.

Testing of upper thresholds:

By writing STATCON_REG, bit CONFIG2 = 0, the VDD test mode is activated.

If STATCON_REG, bit CONFIG1 = 0, the upper VDD test threshold is lowered (overvoltage threshold is reduced to V_{TEST_THH}).

As a result, STATCON_REG, bit STATUS0 = 0 and DIA_REG1, bit NABE_DIS = 0.

Overvoltage is reported and pin NABE is pulled low.

Once the test routine is ended (CONFIG2 = 1) or the upper VDD test threshold is reset to its standard value, STATUS0=1 (no overvoltage anymore) and NABE_DIS =1. Pin NABE is pulled high.

The same test routine can be performed with STATCON_REG, bit CONFIG0 = 1 (latching of overvoltage condition). In that case, ending the test routine will not automatically reset bit NABE_DIS and pin NABE.

Testing of lower thresholds:

By writing STATCON_REG, bit CONFIG2 = 0, the VDD test mode is activated.

If STATCON_REG, bit CONFIG1 = 1, the lower VDD test threshold is lifted (undervoltage threshold is increased to V_{TEST_THL}).

As a result, STATCON_REG, bit STATUS1 = 0 and DIA_REG1, bit NABE_DIS = 0.

Undervoltage is reported and pin NABE is pulled low.

Once the test routine is ended (CONFIG2 = 1) or the lower VDD test threshold is reset to its standard value, STATUS1=1 (no undervoltage anymore) and NABE_DIS =1. Pin NABE is pulled high.

Figure 9. Circuit diagram of VDD monitoring

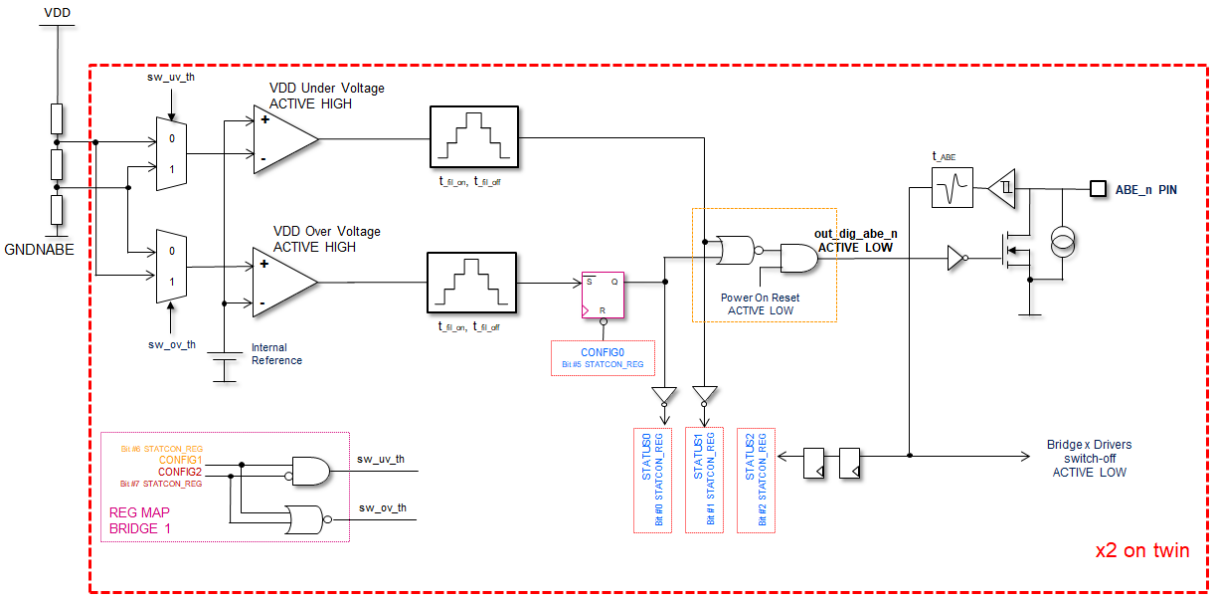


Table 11. VDD Monitoring parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	VDD voltage range at which monitoring circuit shows defined behavior on pin NABE	-	V_{DD_POR}	-	18	V
V_{DD_THL}	VDD Undervoltage threshold	-	4.2	-	4.4	V
V_{DD_THH}	VDD Overvoltage threshold	-	5.25	-	5.5	V
t_{FIL_OFF}	Filtering time before switching off, when VDD voltage goes out of thresholds	-	60	-	135	µs
t_{FIL_ON}	Filtering time before switching on, when VDD comes back inside thresholds	-	60	-	135	µs
V_{TEST_THL}	VDD Undervoltage threshold during VDD Monitoring test	-	5.25	-	5.5	V
V_{TEST_THH}	VDD Overvoltage threshold during VDD Monitoring test	-	4.2	-	4.4	V
V_{DD_slew}	Maximum slew rate on VDD without any change of parameters of VDD monitoring	-	500	-	-	mV/ µs
ΔV_{DD_THx}	Change of VDD_THH or VDD_THL, in case of inverse current on V_S	-	-0.1	-	0.1	V
V_{ABE_INL}	NABE input low level	-	-0.3	-	1.65	V
V_{ABE_INH}	NABE input high level	-	3.15	-	18	V
V_{ABE_INHYS}	NABE input hysteresis	-	0.15	-	1.0	V
I_{ABE_IN}	NABE input current	VABE = 18 V	20	-	70	µA
I_{ABE_IN}	NABE input current	VABE = 5 V	20	40	60	µA
I_{ABE_IN}	NABE input current	0 V < VABE < 1,5 V	0	-	60	µA
V_{ABE_OUTL}	NABE output voltage when VDD below THL	0 V < VDD < VDD_THL IABE_OUTL < 2.5 mA	0.0	-	1.0	V
V_{ABE_OUTL}	NABE output voltage when VDD above THH	VDD_THH < VDD < 18 V IABE_OUTL < 7.5 mA	0.0	-	1.2	V
V_{ABE_OUTL}	Passive output low voltage	Pull down current source to GND, no load Measure voltage at NABE (if NABE is high impedance).	0.0	-	1.0	V
t_{ABE}	NABE pulse width (minimum width required for setting/resetting SPI bits or diagnostic information	-	0.5	1	1.5	µs
ΔI_{ABE}	Change of input current of NABE output pin in case of inverse current on V_S	-	-100	-	100	µA

3 Functional description

3.1 Description of external interfaces

- Voltage supply Vs can be connected directly to the battery voltage via a relay (for example the main relay in an engine control system). Otherwise an additional external inverse voltage protection is necessary.
- The load at the outputs is connected between both outputs (OUT1 and OUT2) in H-bridge mode.
- The ASIC has two inputs controlling the current through the H-bridge: DIR controls the direction of the current (DIR = 0 → Current flows from OUT1 → OUT2; DIR = 1 → Current flows from OUT2 → OUT1) and PWM controls the magnitude of the current (duty cycle 0% → no current … duty cycle 100% → maximum current).

3.2 Functional behavior in detail

All parameters are defined at (unless otherwise specified):

- 4.5 V < VDD < 5.5 V
- VUF < V_S < 28 V (power stages active)
- 0 V < V_S < VUF (power stages inactive)
- -40 °C < T_J < 150 °C
- The HBR can withstand a V_S of 40 V for load dump pulse (see Section 6 Load dump pulse)
- It is recommended to perform the necessary adjustments at high temperature
- All voltages refer to AGND

3.2.1 Power stages

L9969 provides a full H-bridge power stage, consisting of two half bridges, which are intended to be used mainly for the control of DC motors.

The most critical loads are throttle-control actuators with the following electrical characteristics: inductance 0.8 mH to 1.0 mH, resistance 1.2 Ω to 1.8 Ω at room temperature, PWM-frequency f_{min} = 1 Hz and f_{max} = 20 kHz.

5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 12. Power stages parameters

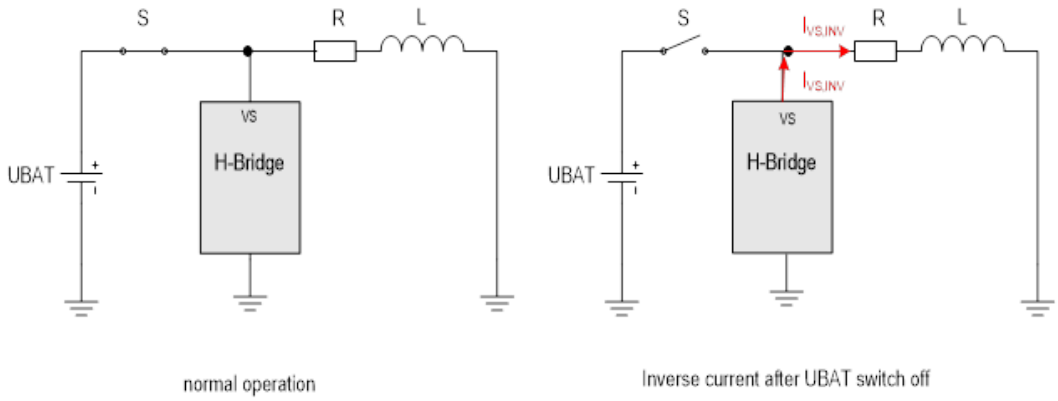
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{OUT-GND}$	Rds_ON resistance low side	I_{OUT} = 3 A 10 V < V_S < 28 V Max. values at T_j= 150 °C	-	-	225	mΩ
R_{OUT-UB}	Rds_ON resistance high side	I_{OUT} = 3 A 10 V < V_S < 28 V Max. values at T_j= 150 °C	-	-	315	mΩ
I_{leak}	OFF State leakage current H-bridge disabled by short circuit detection; this is the current of one stage	V_S = 13 V OUTx = 0 V or V_S	-200	-	200	µA
I_{leak}	OFF State leakage current VDD below VDD_RES	V_S = 13 V OUTx = 0 V or V_S	-200	-	800	µA

3.2.2 Inverse current on V_S

Inverse currents flow out of V_S. An inverse current with maximum 5 A decreasing during a maximum period of 250 ms does not lead to any destruction of the H-bridge ASIC. After exposure to such an inverse current, the full functionality of the device is guaranteed (according to the product target specification).

Information is needed about the behavior of the inputs and outputs during inverse current. Furthermore, information is needed on the reliability of information stored in internal registers during inverse current.

Figure 10. Inverse current



5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 13. Inverse Current

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{VS,INV}$	Inverse Current	250 ms	-	-	5	A
$V_{VS\_slew\_inv}$	Maximum slew rate during inverse current	-	-5	-	-	V/µs

3.2.3 Reverse current

Reverse current is different from inverse Current. It is the current flowing in the load during the passive free-wheeling phase, and passing through the low-side body diode, as soon as the high-side of the same branch is switched OFF.

To reduce internal power losses, the free-wheeling is designed in such a way that, after some period of time, the free-wheel diode is actively short-cut by the transistor channel (beginning the so-called active free-wheeling).

5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 14. Reverse current

Symbol	Parameter	Condition	Min	Typ	Max	Unit
U_D	Free-wheel diode forward voltage	I_{OUT} = 3 A	-	-	2	V
t_{rr}	Free-wheel diode reverse recovery time	-	-	-	100	ns

If the H-bridge is in internal current limitation or in thermal current reduction mode, the above-mentioned short-circuiting of the free-wheeling diode is enabled or disabled according to the status of the free-wheeling bit in the SPI register: CONFIG_REG.FW = 1 (short-cut enabled - active free wheeling) or CONFIG_REG.FW = 0 (short-cut disabled – passive free wheeling).

3.2.4 Power stage switching behavior

Here below (see the Table 15) the possible combinations parallel inputs/driver outputs.

Table 15. Parallel inputs combinations and output states

PWM	DIR	OUT1	OUT2	Remark
L	L	L	L	No active current flow into the load
L	H	L	L	No active current flow into the load
H	L	H	L	A current flows from HS1 toward LS2
H	H	L	H	A current flows from HS2 toward LS1

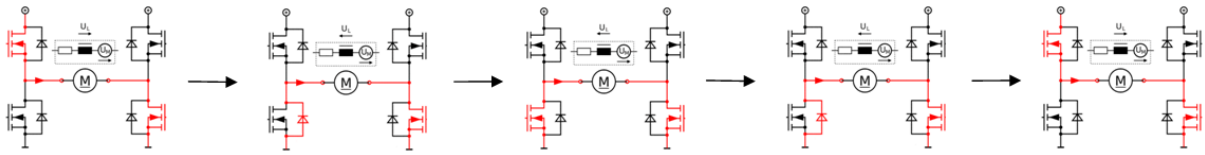
Note: HSx stands for high-side transistor of half-bridge x; LSx stands for low-side transistor of half-bridge x.

3.2.4.1 *Switching sequence during regular operation*

The switching sequence during a regular pulsed width modulation operation is shown in the figure below and is made of 5 steps:

1. The connected load is powered, for example, via HSS1 and LSS2.
2. This is the transition between the powering and the active free-wheeling phase. During this short time where HSS1 is getting non-conductive and LSS1 has not started conducting yet, a passive free-wheeling via the bulk diode of LSS1 takes place.
3. This is the active free-wheeling. In this step LSS1 gets conductive.
4. This is the transition between the active free-wheeling and the powering phase. Similarly to the 2nd step, LSS1 is getting non-conductive and HSS1 has not started conducting yet. A passive free-wheeling via the bulk diode of LSS1 takes place.
5. See 1st step.

Figure 11. Switching sequence during normal operation



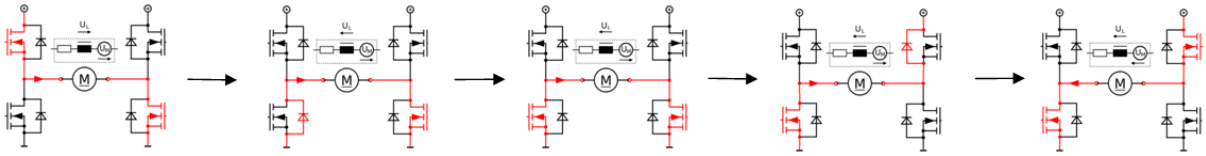
During a regular operation, there is always one half-bridge responsible for the pulsation (in the above example the half-bridge made of HSS1 and LSS1) and one static half-bride (in the above example the half-bridge made of HSS2 and LSS2). As showed in the above example, the LSS of the static half-bridge remains conducting over the complete period whereas the HSS of the static half-bridge is unused.

3.2.4.2 *Switching sequence during change of direction*

The switching sequence during a change of direction is shown in the figure below and is made of 5 steps:

1. The connected load is powered, for example, via HSS1 and LSS2.
2. This is the transition between the powering and the active free-wheeling phase. During this short time where HSS1 is getting non-conductive and LSS1 has not started conducting yet, a passive free-wheeling via the bulk diode of LSS1 takes place.
3. This is the active free-wheeling. In this step LSS1 gets conductive.
4. In this step, the change of direction is starting. Now, LSS2 is getting non-conductive but HSS2 has not started conducting yet. The induced current resulting from the back electromotive force (back-EMF) is still flowing from the left to the right. The current is flowing via the bulk diode of HSS2, the external capacitor and back via LSS1.
5. In this step, HSS2 is getting conductive. The connected load is finally powered in the opposite direction via HSS2 and LSS1.

Figure 12. **Switching sequence during change of direction**



3.2.4.3 *Power stage switching parameters*

Parameters valid at V_S in the range of (8 V…18 V), I_{OUT} = 3 A.

T = -40 °C to 150 °C, unless otherwise specified; C_{OUTxy} = 10 nF connected during all the tests below.

Table 16. **Power stage switching parameters**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{don00_dcm0}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 0	SR = 00	-	-	15	µs
t_{don01_dcm0}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 0	SR = 01	-	-	10	µs
t_{don10_dcm0}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 0	SR = 10	-	-	6	µs
t_{don11_dcm0}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 0	SR = 11	-	-	6	µs
t_{don00_dcm1}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 1	SR = 00	-	-	8	µs
t_{don01_dcm1}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 1	SR = 01	-	-	6	µs
t_{don10_dcm1}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 1	SR = 10	-	-	6	µs
t_{don11_dcm1}	Output HS ON delay PWM or DIR 50% → OUT 20% DCmatching = 1	SR = 11	-	-	6	µs
t_{doff00_dcm0}	Output HS OFF delay PWM or DIR 50% → OUT 80% DCmatching = 0	SR = 00	-	-	25	µs
t_{doff01_dcm0}	Output HS OFF delay PWM or DIR 50% → OUT 80% DCmatching = 0	SR = 01	-	-	20	µs
t_{doff10_dcm0}	Output HS OFF delay PWM or DIR 50% → OUT 80%	SR = 10	-	-	6	µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	DCmatching = 0					
t_{doff11_dcm0}	Output HS OFF delay PWM or DIR 50% → OUT 80% DCmatching = 0	SR = 11	-	-	6	µs
t_{doff00_dcm1}	Output HS OFF delay PWM or DIR 50% → OUT 80% DCmatching = 1	SR = 00	-	-	10.5	µs
t_{doff01_dcm1}	Output HS OFF delay PWM or DIR 50% → OUT 80% DCmatching = 1	SR = 01	-	-	7	µs
t_{doff10_dcm1}	Output HS OFF delay PWM or DIR 50% → OUT 80% DCmatching = 1	SR = 10	-	-	6	µs
t_{doff11_dcm1}	Output HS OFF delay PWM or DIR 50% → OUT 80% DCmatching = 1	SR = 11	-	-	6	µs
$t_{ddelta00\_dcm0}$	Delta HS ON/OFF delay DCmatching = 0	SR = 00	-5	-	18	µs
$t_{ddelta01\_dcm0}$	Delta HS ON/OFF delay DCmatching = 0	SR = 01	-1.5	-	10	µs
$t_{ddelta10\_dcm0}$	Delta HS ON/OFF delay DCmatching = 0	SR = 10	-1.5	-	1.5	µs
$t_{ddelta11\_dcm0}$	Delta HS ON/OFF delay DCmatching = 0	SR = 11	-1.5	-	1.5	µs
$t_{ddelta00\_dcm1}$	Delta HS ON/OFF delay DCmatching = 1	SR = 00	-4	-	4	µs
$t_{ddelta01\_dcm1}$	Delta HS ON/OFF delay DCmatching = 1	SR = 01	-2	-	2	µs
$t_{ddelta10\_dcm1}$	Delta HS ON/OFF delay DCmatching = 1	SR = 10	-1.5	-	1.5	µs
$t_{ddelta11\_dcm1}$	Delta HS ON/OFF delay DCmatching = 1	SR = 11	-1	-	1	µs
t_{don00_spi}	Output HS ON delay (SPI control) SS 50% → OUTx 20% DCmatching = 0	SR = 00	-	-	15	µs
t_{don01_spi}	Output HS ON delay (SPI control) SS 50% → OUTx 20% DCmatching = 0	SR = 01	-	-	10	µs
t_{don10_spi}	Output HS ON delay (SPI control) SS 50% → OUTx 20%	SR = 10	-	-	6	µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	DCmatching = 0					
t_{don11_spi}	Output HS ON delay (SPI control) SS 50% → OUTx 20% DCmatching = 0	SR = 11	-	-	6	µs
$t_{don00\_spi\_dcm1}$	Output HS ON delay (SPI control) SS 50% → OUTx 20% DCmatching = 1	SR = 00	-	-	8	µs
$t_{don01\_spi\_dcm1}$	Output HS ON delay (SPI control) SS 50% → OUTx 20% DCmatching = 1	SR = 01	-	-	6	µs
$t_{don10\_spi\_dcm1}$	Output HS ON delay (SPI control) SS 50% → OUTx 20% DCmatching = 1	SR = 10	-	-	6	µs
$t_{don11\_spi\_dcm1}$	Output HS ON delay (SPI control) SS 50% → OUTx 20% DCmatching = 1	SR = 11	-	-	6	µs
$t_{doff00\_spi\_dcm0}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80% DCmatching = 0	SR = 00	-	-	25	µs
$t_{doff01\_spi\_dcm0}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80% DCmatching = 0	SR = 01	-	-	20	µs
$t_{doff10\_spi\_dcm0}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80% DCmatching = 0	SR = 10	-	-	6	µs
$t_{doff11\_spi\_dcm0}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80% DCmatching = 0	SR = 11	-	-	6	µs
$t_{doff00\_spi\_dcm1}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80% DCmatching = 1	SR = 00	-	-	10.5	µs
$t_{doff01\_spi\_dcm1}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80%	SR = 01	-	-	7	µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	DCmatching = 1					
$t_{doff10\_spi\_dcm1}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80% DCmatching = 1	SR = 10	-	-	6	µs
$t_{doff11\_spi\_dcm1}$	Output HS OFF delay (SPI control) SS 50% → OUTx 80% DCmatching = 1	SR = 11	-	-	6	µs
$t_{r\_HS00\_dcm0}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 00	0.975	-	2.4	V/µs
$t_{r\_HS01\_dcm0}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 01	3.0	-	5.5	V/µs
$t_{r\_HS10\_dcm0}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 10	12.0	-	30.0	V/µs
$t_{r\_HS11\_dcm0}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 11	15.0	-	35.0	V/µs
$t_{r\_HS00\_dcm1}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 00	0.975	-	2.4	V/µs
$t_{r\_HS01\_dcm1}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 01	3	-	5.5	V/µs
$t_{r\_HS10\_dcm1}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 10	12	-	30	V/µs
$t_{r\_HS11\_dcm1}$	Rise Time HS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 11	15.0	-	35.0	V/µs
$t_{f\_HS00\_dcm0}$	Fall Time HS OUTx 80% → OUTx 20%	SR = 00	-2.4	-	-0.975	V/µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	V_S = 14 V; Rload = 14 Ω DCmatching = 0					
$t_{f\_HS01\_dcm0}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 01	-5.5	-	-3.0	V/µs
$t_{f\_HS10\_dcm0}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 10	-30.0	-	-12.0	V/µs
$t_{f\_HS11\_dcm0}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 11	-35.0	-	-15.0	V/µs
$t_{f\_HS00\_dcm1}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 00	-2.4	-	-0.975	V/µs
$t_{f\_HS01\_dcm1}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 01	-5.5	-	-3	V/µs
$t_{f\_HS10\_dcm1}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 10	-30	-	-12	V/µs
$t_{f\_HS11\_dcm1}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 11	-35.0	-	-15.0	V/µs
$t_{r\_LS00\_dcm0}$	Rise Time LS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω only valid for DIR change DCmatching = 0	SR = 00	0.975	-	2.4	V/µs
$t_{r\_LS01\_dcm0}$	Rise Time LS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω only valid for DIR change DCmatching = 0	SR = 01	3.0	-	5.5	V/µs
$t_{r\_LS10\_dcm0}$	Rise Time LS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω	SR = 10	12.0	-	30.0	V/µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	only valid for DIR change DCmatching = 0					
$t_{r\_LS11\_dcm0}$	Rise Time LS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω only valid for DIR change DCmatching = 0	SR = 11	15.0	-	35.0	V/µs
$t_{r\_LS00\_dcm1}$	Rise Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω only valid for DIR change DCmatching = 1	SR = 00	0.975	-	2.4	V/µs
$t_{r\_LS01\_dcm1}$	Rise Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω only valid for DIR change DCmatching = 1	SR = 01	3	-	5.5	V/µs
$t_{r\_LS10\_dcm1}$	Rise Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω only valid for DIR change DCmatching = 1	SR = 10	12	-	3	V/µs
$t_{r\_LS11\_dcm1}$	Rise Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω only valid for DIR change DCmatching = 1	SR = 11	15	-	35	V/µs
$t_{f\_LS00\_dcm0}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 00	-35.0	-	-15.0	V/µs
$t_{f\_LS01\_dcm0}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 01	-35.0	-	-15.0	V/µs
$t_{f\_LS10\_dcm0}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 10	-35.0	-	-15.0	V/µs
$t_{f\_LS11\_dcm0}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 0	SR = 11	-35.0	-	-15.0	V/µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{f\_LS00\_dcm1}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 00	-35.0	-	-15.0	V/µs
$t_{f\_LS01\_dcm1}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 01	-35.0	-	-15.0	V/µs
$t_{f\_LS10\_dcm1}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 10	-35.0	-	-15.0	V/µs
$t_{f\_LS11\_dcm1}$	Fall Time LS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω DCmatching = 1	SR = 11	-35.0	-	-15.0	V/µs
f_{PWM}	Output switching frequency	-	-	-	20	kHz
t_{ddis}	Disable delay time DIS NABE 50% → OUTx 20% Resistive load	-	-	-	12.5	µs
t_{dpwon}	Power On delay time from power down	VS = VUF_ON → output stages active	-	-	1	ms
t_{den}	Enable delay time from disable status DIS NABE 50% → OUTx 80% Resistive load	-	-	-	50	µs
$t_{r\_DIS\_NABE}$	Rise Time LS OUTx 20% → OUTx 80% V_S = 14 V; Rload = 14 Ω	-	60.0	-	-	V/µs
$t_{f\_DIS\_NABE}$	Fall Time HS OUTx 80% → OUTx 20% V_S = 14 V; Rload = 14 Ω	-	-	-	-60.0	V/µs

The Output ON delay and the Output OFF delay are designed symmetrically, having, as a result, a deviation of max. 2% of the PWM value between Input Signal (PWM) and Output signal (OUTx) by 20 kHz.

In case of output control via SPI interface, the parameters are measured from the positive transition of the SPI NSS signal.

Figure 13. **Power On delay from power down**

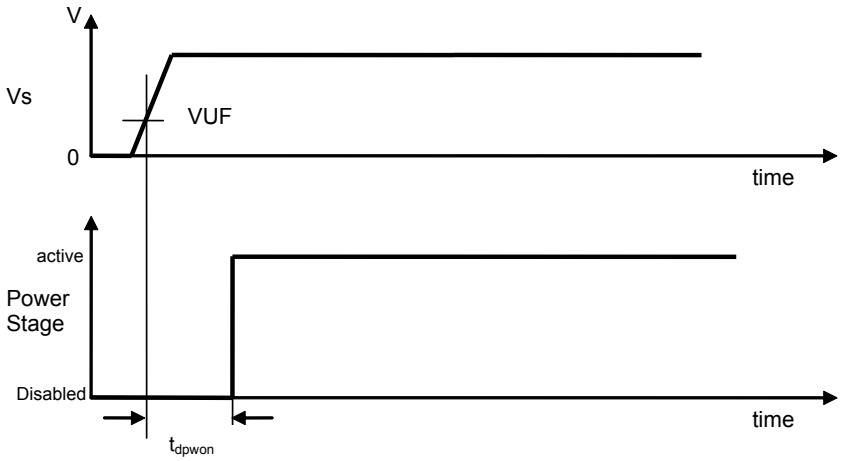


Figure 14. **Output delay time - depicted for LSx**

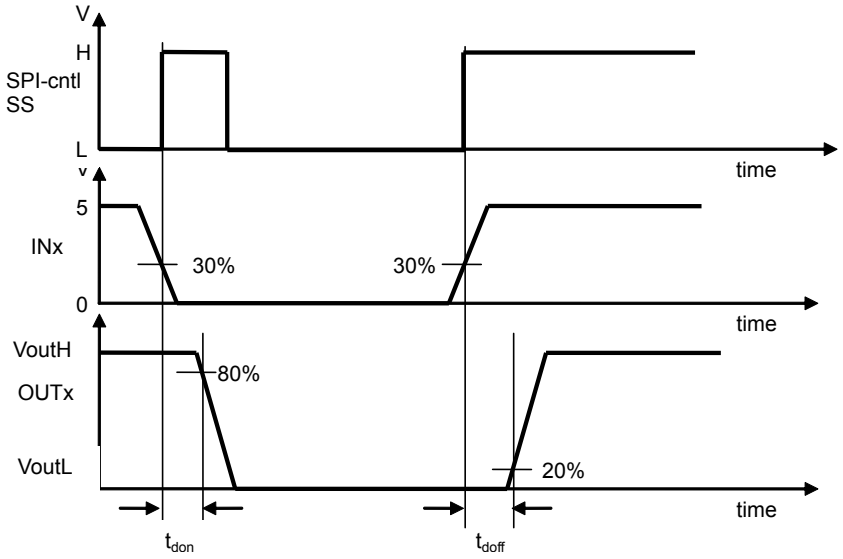


Figure 15. **Output rise and fall times**

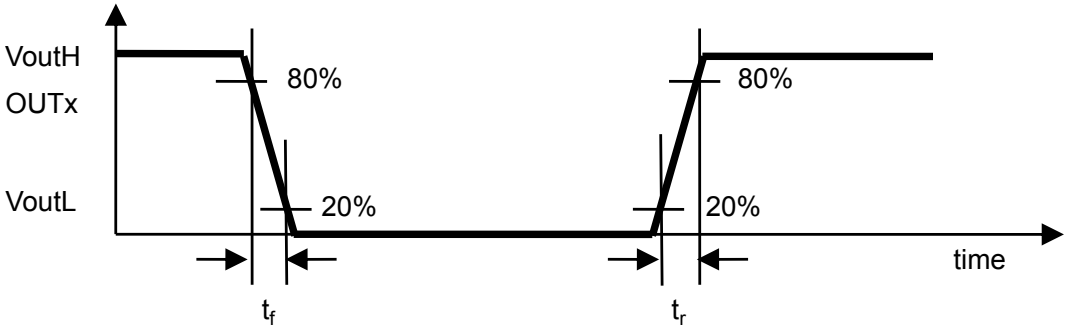


Figure 16. **Output disable and enable time - depicted for NABE input**

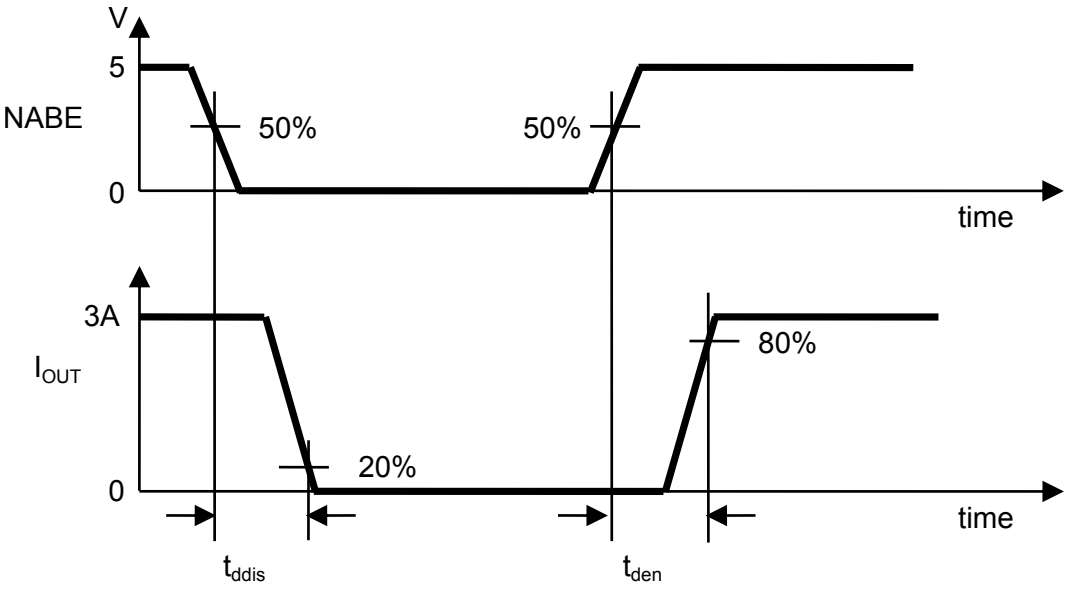
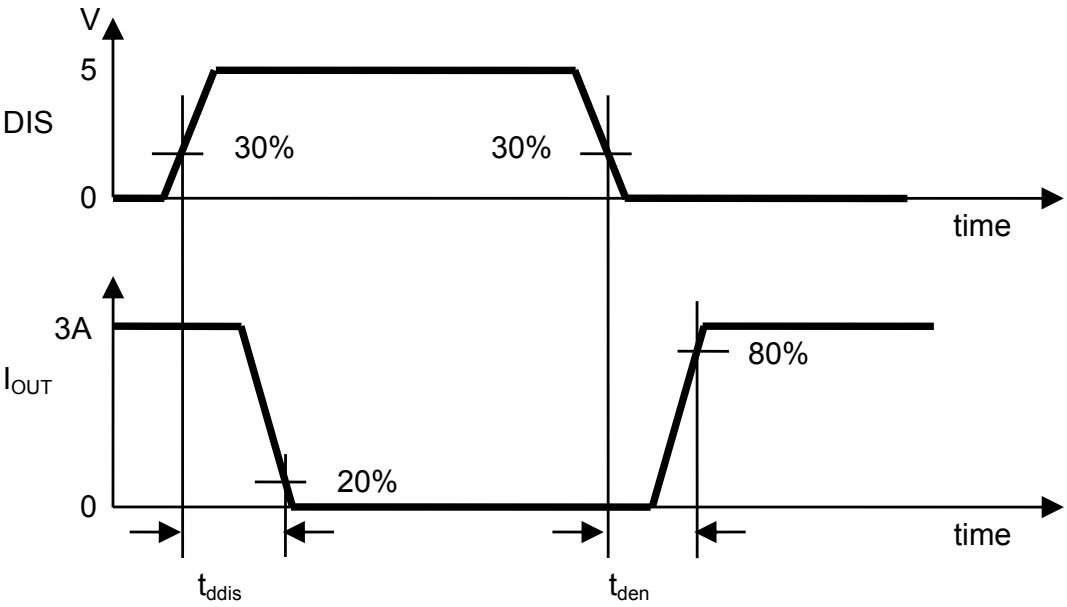


Figure 17. **Output disable and enable time - depicted for DIS input**



3.2.5 Output control

The output stages can be controlled either by two input signals ‘PWM’ and ‘DIR’ (parallel control), or via SPI. Parallel control is the default state.

In order to operate the power stages via SPI bus, the CONFIG_REG.MUX must be set to 0. In this case, the bridges follow the bit values of SDIR and SPWM, in the register CONFIG_REG. Both releasing signals DIS and NABE keep their effectiveness in this (SPI-controlled) mode of operation. However, when SPI-control mode is selected, signals on PWM and DIR are ignored.

The bit CONFIG_REG.FW is used to switch between the active free wheeling (CONFIG_REG.FW = 1), where the body diode is short cut by its transistor, or the passive free wheeling (CONFIG_REG.FW = 0), where the free wheeling is driven only through the body diode. The active free wheeling (CONFIG_REG.FW = 1) is the default state; the free wheeling strategy (active versus passive) applies not only to the regular operation of the power stage but also to the current limitation.

3.2.6 Protection and monitoring

Both output stages feature the following diagnostic functions:

- Short to Battery voltage (SCB). Detection is performed when low side-switches are turned on. The result is reported in the register DIA_REG1.
- Short to Ground (SCG). Detection is performed when high side-switches are turned on. The result is reported in the register DIA_REG1.
- Short across Load (SCL). Detection is performed by an appropriate procedure (combination SCB, SCG). The result is reported in the register DIA_REG1.
- Open Load (OL), available in both active and inactive mode. The result is reported in the register DIA_REG1. Per default only the OL detection in passive is running. If enabled (CONFIG_REG.OLDA → 1), the OL detection in active mode (OLDA) is run automatically.
- Over Temperature (OT), available in active and inactive mode. Once OT is detected, the power stage is switched off. The result is reported in the register DIA_REG1.

Each short-circuits error has to be confirmed before it is stored in the DIA_REG1. In practice, if any error occurs the first time, the HBR has to react correctly. For instance, at SCG at OUT1, the HBR is switched off. After the time t_{retest} the HBR is switched on again. If now the SCG at OUT1 appears again, it is confirmed. If it is not confirmed, the first entry is to be skipped. Only confirmed errors are stored in the DIA_REG1. Open-load in active (OLDA) errors has to be retested as well (refer to Section 3.2.6.9 Open Load diagnosis in active mode). After each confirmed short-circuits error, the HBR is switched off and is not automatically switched on again, even if the error has disappeared in between.

3.2.6.1 *Current feedback*

An analog output signal CF proportional to the load current is provided. The signal CF is valid for 6.5 V < V_S < 28 V.

5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 17. Current feedback parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$CF_{\_0\%}$	CF output voltage with current at OUTx = 0% * I_L (CLx)	I_{CF} > -1.2mA	0.008 * VDD	0.014 * VDD	0.036 * VDD	V
$CF_{\_5\%}$	CF output voltage with current at OUTx = 5% * I_L (CLx); percentage vs. VDD	I_{CF} > -1.2mA	5.27	5.73	6.19	%
$CF_{\_40\%}$	CF output voltage with current at OUTx = 40% * I_L (CLx); percentage vs. VDD	I_{CF} > -1.2mA	33.7	36	38.3	%
$CF_{\_100\%}$	CF output voltage with current at OUTx = 100% * I_L (CLx); percentage vs. VDD	I_{CF} > -1.2mA	76	88	100	%

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CF	CF maximum output voltage	-	-100 mV	-	VDD + 200 mV	V

This current feedback signal could be used for certain applications. To get the direction of the current, the signal DIR (HBR control by parallel inputs) or alternatively the information from CONFIG_REG.DIR is used (HBR control by SPI).

Only positive current (from Outx to GND) at the low side power stage is indicated at the CF output. Negative current and current over the bulk diode are not visible.

3.2.6.2 *Current limitation*

The output stage current limitation levels are adjustable in 3 different ranges, as described in Table 18. The limits are guaranteed over the complete temperature range.

Figure 18. Parameters during current limitation

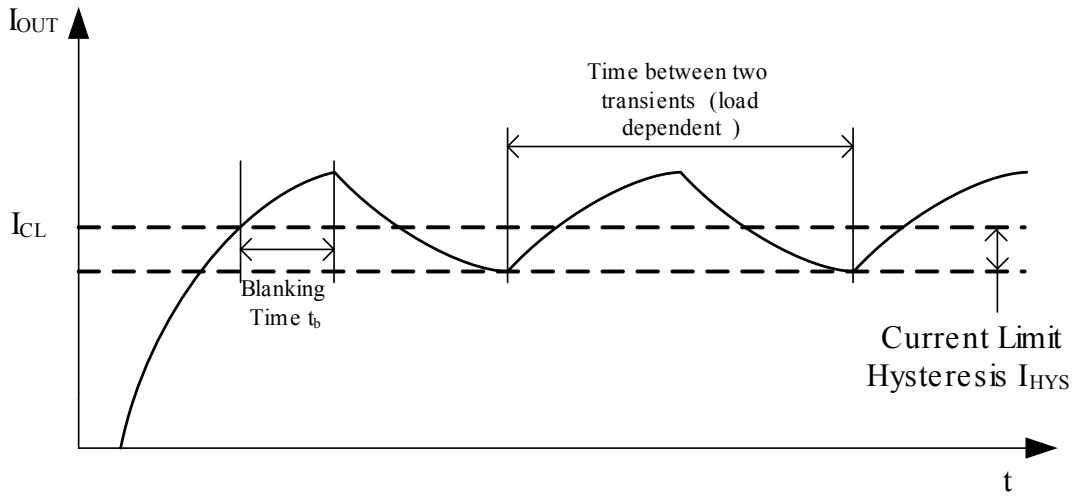


Table 18. Current limitation ranges

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CL2}	Current limit, selection 2	-	4.25	5.0	5.75	A
I_{CL3}	Current limit, selection 3 (default)	-	5.6	6.5	7.6	A
I_{CL4}	Current limit, selection 4	-	7.3	8.5	9.9	A
I_{CL_HYST}	Current limit, hysteresis	-	-10	-	-5	%
t_b	Current limit, blanking time	-	8	11	15	µs

Because the current levels are programmed by SPI, the default value is always ‘switch off current level’ = 3.

A change in one or both input pins terminates the current limitation and the outputs follow the inputs respectively. If the current limitation is running and a load with a high inductive component is connected, the free wheeling may take much time. If the signal on the inputs stays unchanged, the free wheeling will last as long as the lower limit (I_L - I_{hys}) is reached. After that, the path gets active again, the current rises until I_L is reached, then an additional increase follows for t_b and then free wheeling is restarted again, in case PWM is still active.

The time between two transients is mainly related to the time constant of the load, and hence not specified. This time however, cannot drop below the limit t_{trans_lim} defined in Table 19.

The information that the function “Current limitation” is active is stored in the DIA_REG2.

5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

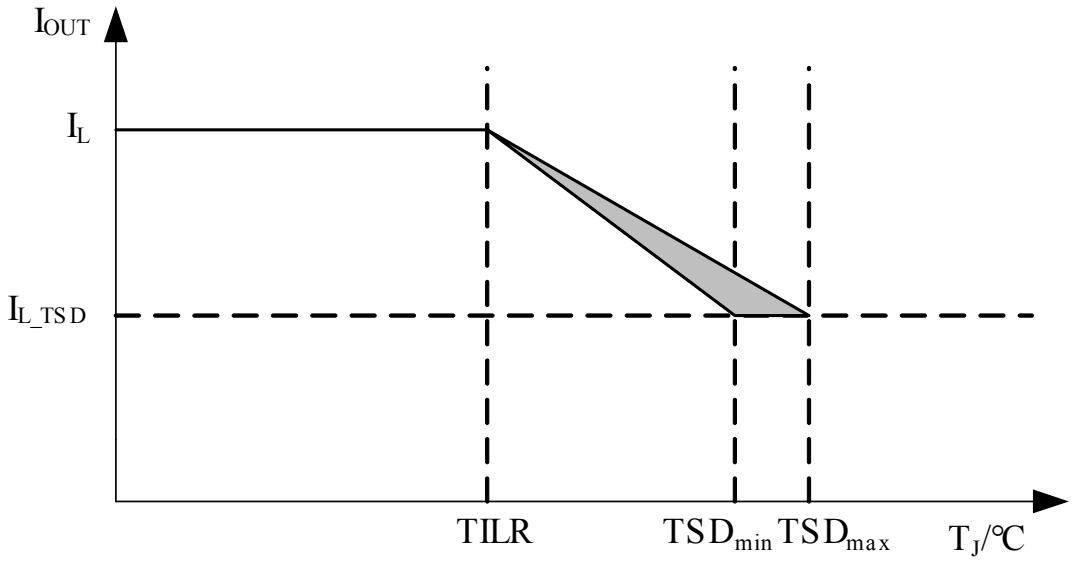
Table 19. Time between transients

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{trans_lim}	Time between two transients	-	90	-	130	µs

3.2.6.3 *Temperature-Dependent Current Reduction (TDCR)*

For $T_{ILR} < T_J < T_{SD}$ the current limit level I_L decreases from its nominal value (for example typ. 6.6 A for current level 3) down to 2.5 A ± 1.1 A as shown in Figure 19.

Figure 19. Temperature-Dependent Current Reduction (TDCR)



5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 20. TDCR parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_L	Current limit at TSD	-	1.4	2.5	3.6	A
T_{ILR}	Start of temperature dependent current reduction	-	150	165	-	°C
T_{SD}	thermal shut-down	-	175	190	-	°C
T_{SD} - T_{ILR}	Range of temperature dependent current reduction	-	20	25	30	°C

3.2.6.4 *Behavior on faults in general*

These are the kind of faults that L9969 is able to detect:

- Faults detected in active or in inactive mode: Open Load (OL), Over Temperature (OT), Undervoltage at Vs (VUF).
- Faults detected in active mode only: Short to GND at OUT1 (SCGOUT1), Short to GND at OUT2 (SCGOUT2), Short to BAT at OUT1 (SCBOUT1), Short to BAT at OUT2 (SCBOUT2), Short across Load (SCL).
- Errors detected in inactive mode: Short to GND at (any) disabled OUTx, Short to BAT at (any) disabled OUTx.

Consequently, errors detected in active mode can only be detected, if the H-bridge is enabled.

Note:

- *The feature VDD monitoring and the corresponding NABE behavior is not considered here as a power stage error. This is described in Section 2.6.2 NABE and VDD monitoring and in the explanation of VDDMON_REG.*
- *There is a difference between errors and information. Information is: CURRLIM (current limitation, reported in DIA_REG2) and TDCR (temperature dependent current reduction, reported in DIA_REG2).*

During the retest procedure for confirming an error, the H-bridge will not react on any signal (and on any signal transition) on PWM or DIR.

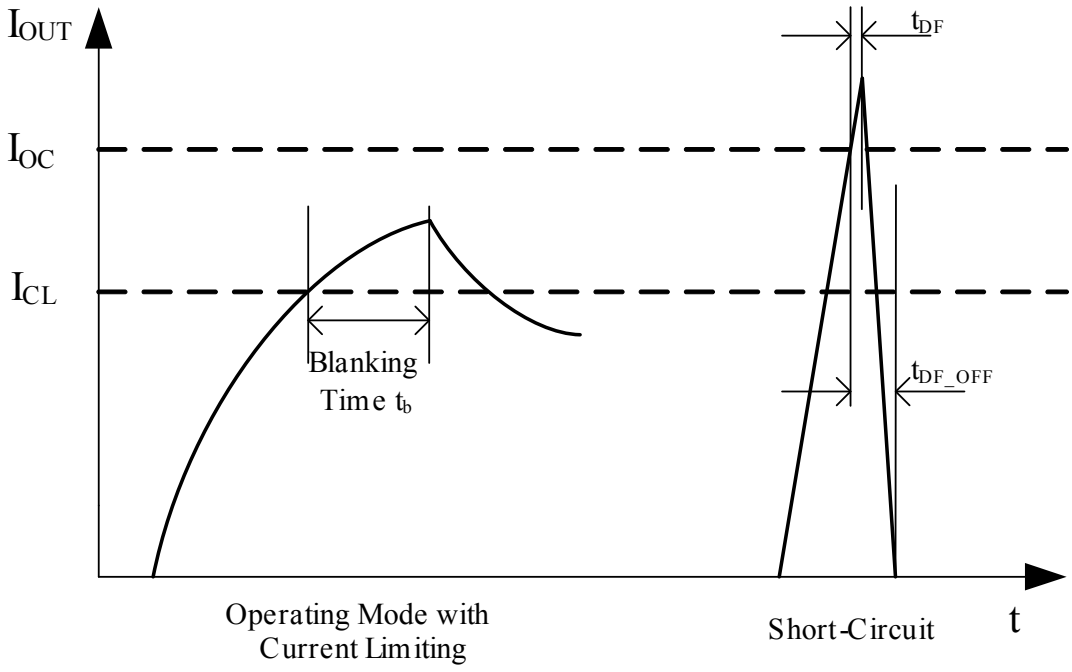
Also, after every confirmed error the H-bridge is switched off and is not automatically switched-on again, even if the error has disappeared in between.

3.2.6.5 *Short circuit detection*

Both high side power stages are supervised continuously to detect any short circuit to ground or short circuit across load on OUT1 or OUT2. If the current rises during the blanking time t_b beyond the limit I_{ouk}, a short circuit to ground is detected. The H-bridge is switched off. After that, the error has to be confirmed in a first step, and it has to be checked whether there is only a simple short cut present or a SCL in a second step. This is to distinguish by an appropriate internal test procedure, refer to Section 3.2.6.6 Short circuit across load.

Both low side power stages are supervised to detect any short circuit to battery or short circuit across load on OUT1 or OUT2. If the current rises during the blanking time t_b beyond the limit Iouk, a short circuit to battery or short circuit across load is detected. The HBR is switched off. Then the error has to be confirmed, the HBR is switched on again. If the short circuit to battery is detected again, the error will be reported to the DIA_REG1. This is to distinguish by an appropriate internal test procedure, refer to Section 3.2.6.6 Short circuit across load.

Figure 20. Short circuit detection principle



In fault case at any output pin, all output stages are switched off. Each half-bridge output stage is equipped with a short circuit protection up to battery voltages of 40 V.

Parameters for overcurrent detection are specified in the range of 8 V to 18 V. The specified limits may vary in the range below 8 V (down to 5.5 V of min VSx) or above 18 V, however the function itself is guaranteed up to 40 V at V_S.

A short circuit condition at level 3 shall be detected, if the circuit, attached to the output, has an impedance ≤ 0.5 Ω and ≤ 25 µH at battery voltage of 13 V and 25 °C junction temperature.

In order to get a good robustness against wrongly detected short circuits, especially with high battery voltages, L9969 is designed in order to keep a certain gap between short-circuit limit and current limitation threshold under all circumstances.

5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 21. Short circuit detection parameters

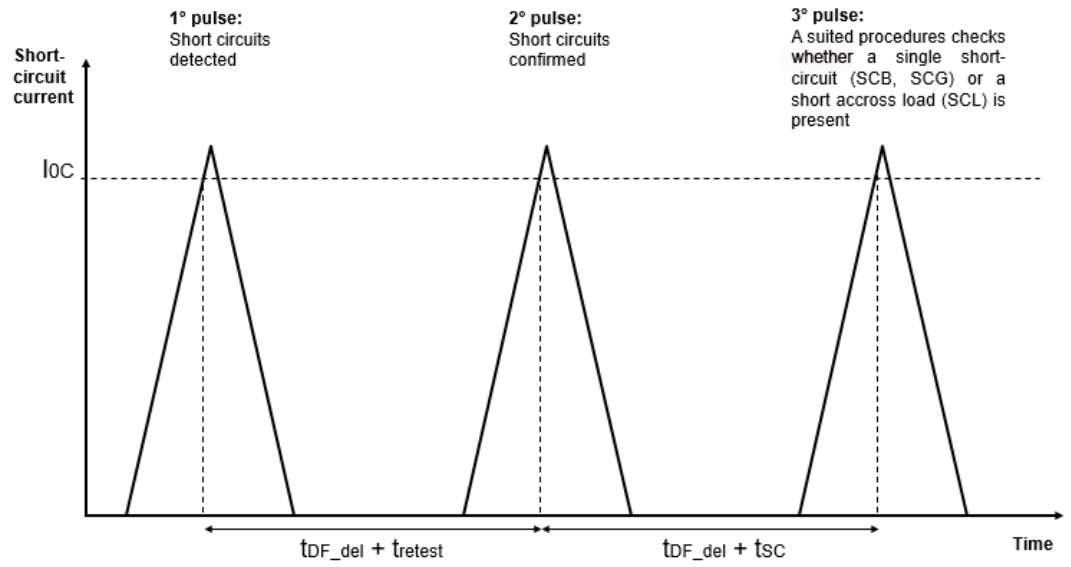
Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_ouk_2	Overcurrent detection at CL = 2	Short Circuit to Ground or Battery or Across Load	4.9	-	8.2	A
I_ouk_3	Overcurrent detection at CL = 3 (default)	Short Circuit to Ground or Battery or Across Load	6.7	-	11.1	A
I_ouk_4	Overcurrent detection at CL = 4	Short Circuit to Ground or Battery or Across Load	8.4	-	14	A
$\Delta\|I_{OUK}\|$	Short circuit current tracking |IOUK| - |Current Limit IL|	-	0.3	-	-	A
t_{DF_H}	Delay time for fault detection	0.5 Ω at 25 µH	1	2	-	µs
t_{DF_off}	Time from detected fault to high impedance of outputs	0.5 Ω at 25 µH	-	-	6	µs
t_{DF_del}	Free-wheeling time. Time for the delayed switch off between the switch off of both outputs after a detected short circuit at one output	-	20	-	200	µs
t_{SC}	Timeout during reconfirmation sequence	-	290	350	413	µs
t_{retest}	Duration of the switch on/switch off sequence of OUTx after a detected short circuit at one output	-	290	350	413	µs

Each error has to be confirmed before being stored in the DIA_REG1.

3.2.6.6 *Short circuit across load*

In case of a short circuit across load, it is possible that two failures are detected at the same time (but not necessarily): a short to ground on one side and a short to battery on the other side. The HBR has to run a sequence internally, if there is only a single short circuit to ground on the high-side switch or a single short circuit to V_S on the low side switch or if there is really a short circuit across the load. This sequence is executed every time a single short cut is detected, to prevent a false error reporting. The SCL algorithm should look as follows (see Figure 21).

Figure 21. Principle of the short circuit across load detection



When an error was detected at any output pin the output stages are turned off immediately.
Below, some examples of how the SCL detection procedure works.

Figure 22. Principle of the short circuit across load detection (OVC on LS1 when PWM = 1)

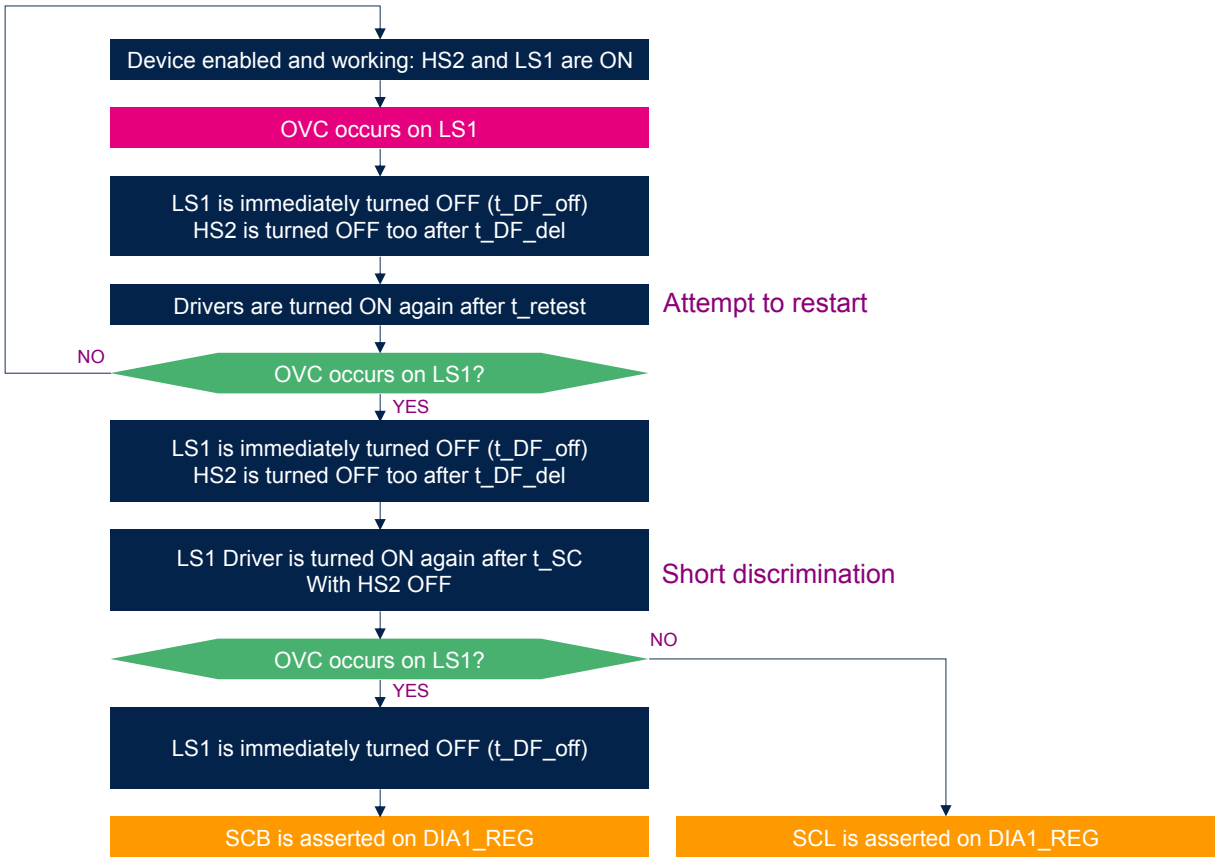


Figure 23. Principle of the short circuit across load detection (OVC on HS2 when PWM = 1)

3.2.6.7 *Short Circuit detection and behavior afterwards*

- After a detected short circuit (SCG, SCB or SCL) both outputs are switched to tri-state.
- If only one output has diagnosed a short circuit, the second output is switched off after a delay time t_{DF_del} . This delay time allows the free-wheeling of the inductive energy stored in the load.
- If a short circuit is detected on both outputs, they are both switched off immediately. If the second short circuit is detected during t_{DF_del}, the second output is switched off immediately too.

Anytime a SCB or a SCG is detected, L9969 allows to distinguish if there is only a single SC or a SCL. Therefore a sequence starts running internally after the detected fault SCB or SCG. This sequence of confirmation is short enough to prevent any mechanical reaction in the connected load.

This is checked internally by switching the second half-bridge to GND and the first half-bridge to GND too, by releasing the power-stage for a short period t_{retest}. If now the SCB on OUT1 disappears, one has a SCL, otherwise the SCB on OUT1 is detected correctly. This testing is different from the normal operation, where only one diagonal path is switched.

Theoretically, there could be the following failure scenario: as DIRx=0 and PWMx=0, a short to battery on OUTx1 occurs, consequently a short to battery detection on OUTx1 LS eventually leads to both OUTx1 LS and OUTx2 LS drivers turn-OFF after filter-time; t_RETEST timer starts. During t_RETEST counting, the short condition changes from short to battery on OUTx1 to short to ground on OUTx1; as t_RETEST counting expires, both OUTx1 LS and OUTx2 LS drivers are re-enabled and the previous fault detection is not confirmed and bridge actuation control returns to the PWMx pin. As PWMx pin status changes back from 0 to 1, OUTx1 HS driver is enabled as requested; by the way, short to ground on OUTx1 is present, thus both OUTx1 HS and OUTx2 LS drivers are turned-OFF after filter-time: as no further scenario change occurs, the short confirmation procedure is completed, confirming the short to ground on OUTx1.

3.2.6.8 *Undervoltage shutdown*

In case of undervoltage on V_S, L9969 reacts by shutting down. The diagnosis of V_S undervoltage is also available on SPI registers; in fact undervoltage on V_S does not reset the SPI interface. The involved parameters in undervoltage shutdown are reported in Table 22.

5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 22. Undervoltage shutdown parameters

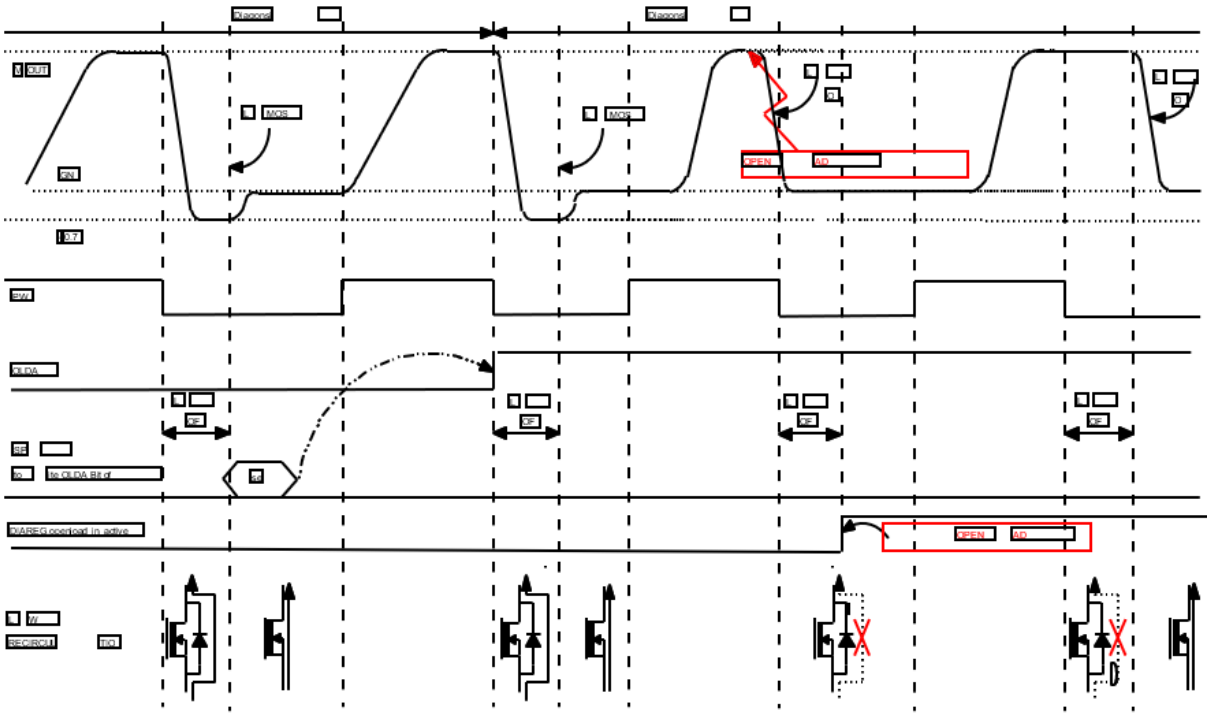
Symbol	Parameter	Condition	Min	Typ	Max	Unit
VUF_OFF	Undervoltage at V_S, switch off threshold	-	3.1	3.8	4.5	V
VUF_ON	Undervoltage at V_S, switch on threshold	-	3.3	4.0	4.7	V
VUF_HYS	Undervoltage at V_S, hysteresis	-	100	-	1000	mV
tUF	Filter time detection undervoltage V_S	-	-	-	1,5	µs

3.2.6.9 *Open Load diagnosis in active mode*

Open Load diagnosis is possible when outputs are switched off by DIS or NABE but also during active operation, in case the feature is enabled via CONFIG_REG.OLDA = 1. However, default value for the open load diagnosis during active operation is: disabled (CONFIG_REG.OLDA = 0).

Figure 24 shows how this could be achieved.

Figure 24. Open Load diagnosis in active mode



In active mode, by default the Open Load diagnostic is deactivated. If one has sent the command CONFIG_REG.OLDA mode = 1, the Open Load diagnostic in active mode (OLDA) is activated. In Figure 24, at the beginning, the OLDA is deactivated. The load is assumed to have an inductive component. The current in the load is toggled by the signal PWM. If the PWM signal is low, one has the free-wheeling of the inductive component of the load via the low-side transistors. At the beginning of the free-wheeling phase, the inductivity must free-wheel. Therefore it is generating a negative voltage on the OUTx. This voltage is detected internally the HBR. As long as there is a negative voltage at the beginning of the free-wheeling phase, no open load fault has occurred. If there is no negative voltage at the beginning of the free-wheeling phase, there is an open load (or a simple resistor connected as load, where this principle does not work).

This principle only works at load currents above a certain threshold. If the load current is below that limit, the free wheeling phase is too short to be detected correctly. This threshold is not specified here but it must be considered in any case in order not to lead to a wrong diagnosis.

Once an OLDA was detected, the error has to be confirmed before being reported in DIA_REG1. The way how the confirmation algorithm works, can be set in SPECIAL_REG, Bit4 (OLDAFILTER). Two alternatives are possible: either the error has to be confirmed during the next possible retry, or the error has to be confirmed during a retry after 40 ms.

5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 23. Under ground thresholds parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
V_{UGND_OUTxy}	Under ground threshold voltage at OUTxy	/	-0.25	-0.15	-0.05	V	OUTxy

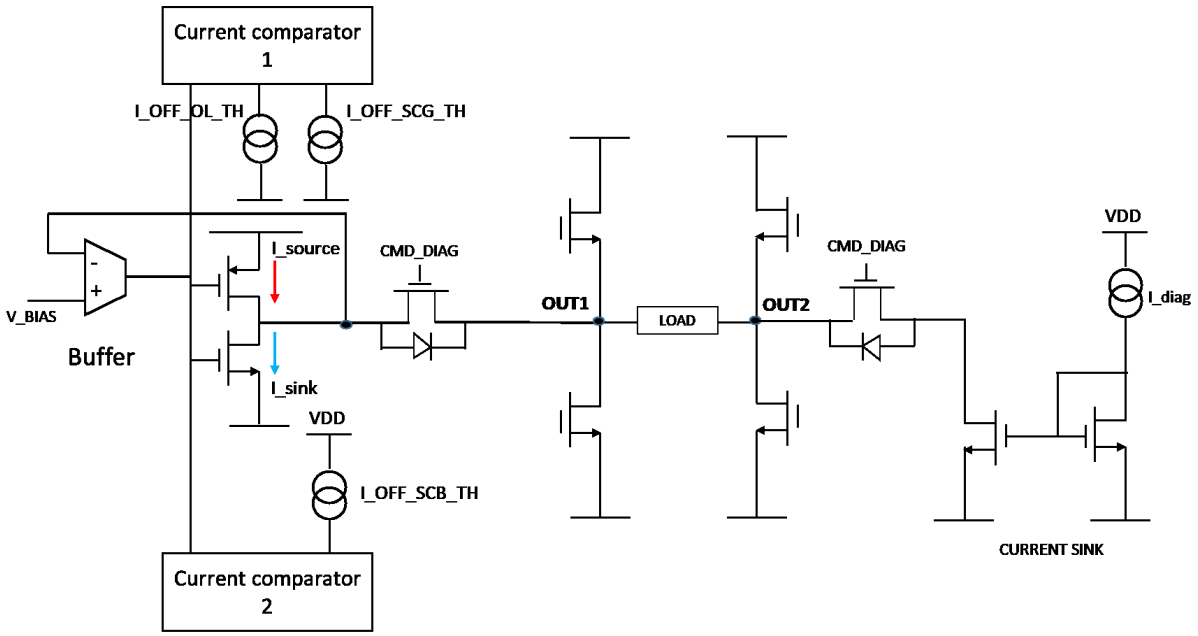
3.2.6.10 *Diagnosis in inactive mode*

In inactive mode, i.e the HBR is disabled via the signals NABE or DIS, both the outputs OUT1 and OUT2 are in the tristate condition (all four power transistors are switched off). In order to avoid any wrong diagnostic by generated effects of the connected load, a filtering time t_{diag_OL} must have expired before the diagnosis is run.

In inactive mode, the following diagnostics are available: Open Load, Short to Ground and Short to Battery. At power-up if load is not connected and OUTx1 is shorted to battery voltage or GND, the diagnosis detects SCG or SCB and no OL.

Figure 25 shows how the OFF diagnosis is working, when the power-stage is disabled.

Figure 25. Principle of diagnosis in inactive mode



When the OFF state diagnosis is enabled, an internal buffer regulates a typical voltage of 1.8 V (V_{OFF_OUT1}) on OUTx1 pin, with a certain I_{SOURCE} and I_{SINK} capability, whose limits are equal to $I_{OFF\_LIM\_SRC\_OUT1}$ and $I_{OFF\_LIM\_SRC\_OUT1}$ respectively; on OUTx2 is present pull-down current ($I_{OFF\_PD\_OUT2}$), whose typical value is 120 µA.

If the load is connected and its resistance is below R_{OL}, the buffer shall source a current equal to $-I_{OFF\_PD\_OUT2}$, so the diagnostic result is “no fault”.

If I_{SOURCE} becomes higher than $I_{OFF\_OL\_TH}$ (lower in absolute value), it means that load is disconnected, or its resistance has become more than R_{OL}, so the diagnostic result is Open Load.

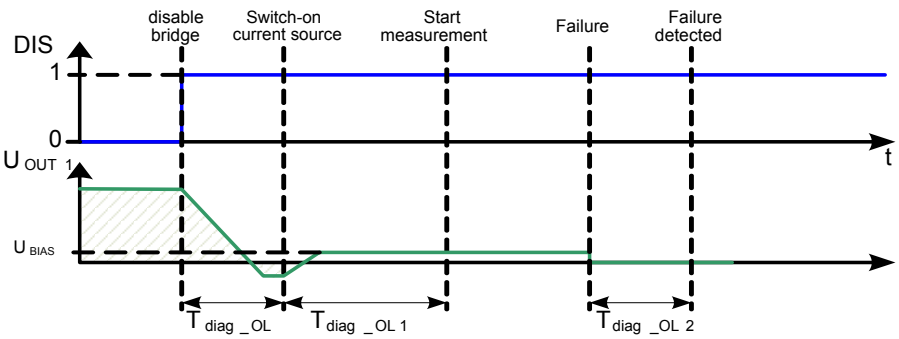
If I_{SOURCE} becomes lower than $I_{OFF\_SCG\_TH}$ (higher in absolute value), it means that there is a short to ground.

If I_{SINK} becomes higher than $I_{OFF\_SCB\_TH}$, it means that there is a short to battery.
5 V < VBATT < 18 V, 4.5 V < VDD < 5.5 V, T_J= -40 °C to 150 °C, unless otherwise specified.

Table 24. OFF state diagnostic detection parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
V_{OFF_OUT1}	OUT1 regulated output voltage, used for OFF diagnostics	-2.4 mA < I_{OUT1} < 2.9 mA	1.2	1.8	2.4	V	OUTx1
$I_{OFF\_PD\_OUT2}$	OUT2 pulldown current, used for OFF diagnostics	V_{OUT2} = 1.6 V	90	120	150	µA	OUTx2
$I_{OFF\_OL\_TH}$	Open-load threshold used for OFF diagnostics, measured at OUT1	-	-80	-60	-30	µA	OUTx1
$I_{OFF\_SCB\_TH}$	Short to battery threshold used for OFF diagnostics, measured at OUT1	-	250	380	500	µA	OUTx1
$I_{OFF\_SCG\_TH}$	Short to ground threshold used for OFF diagnostics, measured at OUT1	-	-2.3	-2	-1.3	mA	OUTx1
$I_{OFF\_LIM\_SRC\_OUT1}$	OFF diagnostic regulator sourcing current limit, measured at OUT1	V_{OUT1} = 0 V	-5.7	-4.1	-2.4	mA	OUTx1
$I_{OFF\_LIM\_SNK\_OUT1}$	OFF diagnostic regulator sinking current limit, measured at OUT1	2.5 V < V_{OUT1} < 18 V	2.9	4.1	5.4	mA	OUTx1
R_{OL}	Load detection threshold	-	2.5	-	50	kΩ	-
t_{diag_OL}	Delay before enabling Open Load diagnostic structure	-	100	-	150	ms	-
$t_{diag\_OL\_1}$	Delay before starting measurement	-	2.4	-	3.6	ms	-
$t_{diag\_OL\_2}$	Open Load diagnostic filtering time	-	200	-	300	µs	-

Figure 26. Timings related to Open Load diagnostics



This means, the open load diagnosis starts automatically after $t_{\_diag\_OL}$ + $t_{\_diag\_OL\_1}$. If now there is no open load condition, the diagnosis phase keeps on running. If the open load condition is detected, this condition must be valid for a time $t_{\_diag\_OL\_2}$. If this is the case, OL is reported to the DIA_REG1. The OL structure keeps on working, so that if the OL disappears and reappears after a certain time, it is detected again, automatically and without any external trigger.

3.2.7 SPI Interface

3.2.7.1 *SPI general description*

The SPI interface establishes a communication between the H-bridge and the systems microcontroller. The H-bridge is always operated in the slave mode whereas the microcontroller provides the master functions.

By applying an active slave select signal at NSS, the H-bridge is selected by the SPI master. SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input), the SPI clock is provided by the SPI master.

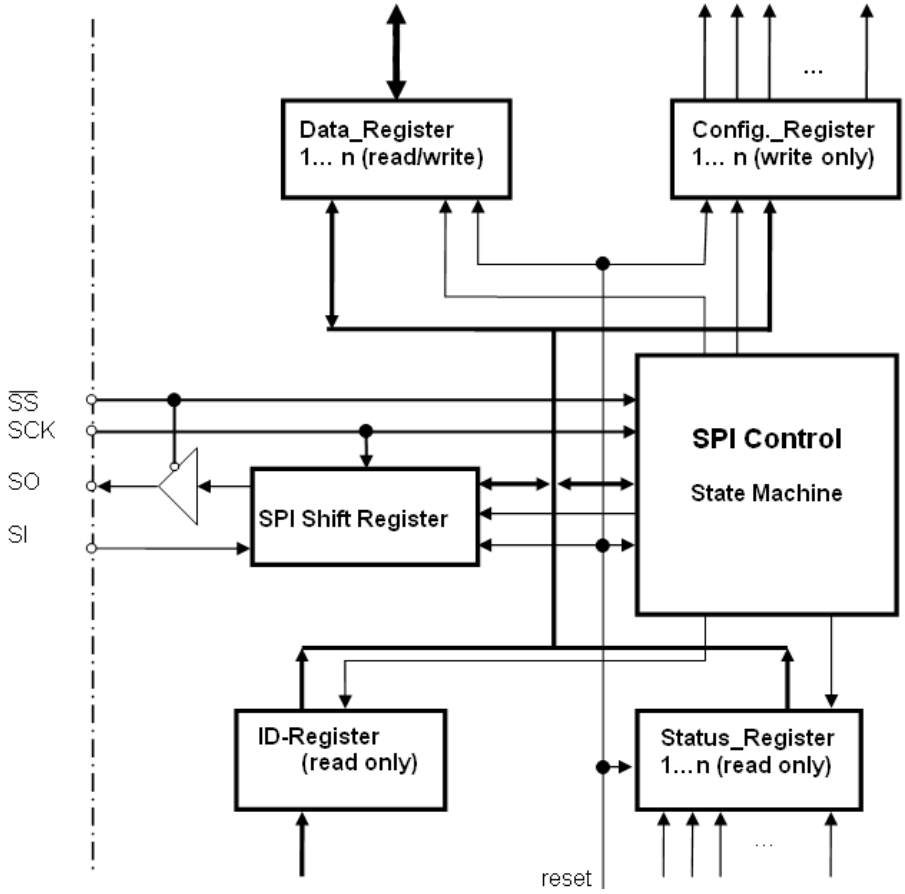
In case of inactive slave select signal (high), the data output SO is in high impedance state (tristate).

Depending on the application, the first two bits of an instruction may be used to establish an extended device-addressing. Doing this, one common NSS channel may be shared by up to 4 Slave-devices.

Thresholds are independent from VDD and defined in a way to be compatible to 3.3 V and 5.0 V ports, if VDD is in its operational range.

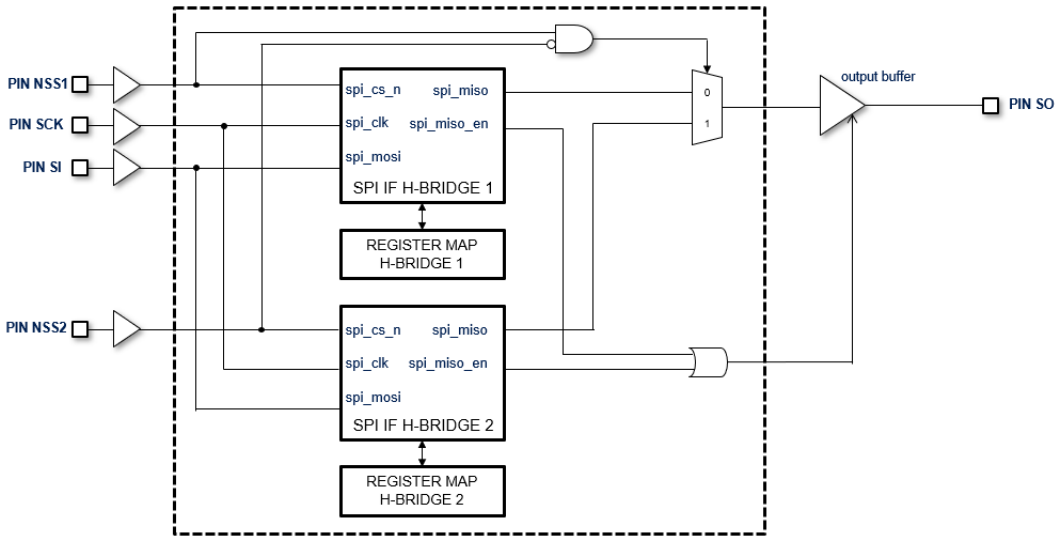
In absence of V_S, the full functionality of the SPI-interface is still given.

Figure 27. SPI block diagram



For twin version, since there are two NSS pins competing for the data lines, they must not be asserted simultaneously. In the event that this occurs, the data lines will be managed as shown in the figure below:

Figure 28. **SPI data line management**



If both the NSS were to be asserted and the communication did not have problems such as those indicated in the following paragraphs, the action will be taken in both bridges. The NSS1 signal has priority over the NSS2, therefore, the value that will be reported on the data output SO will depend on how the two signals are driven.

3.2.7.2 *SPI communication*

A SPI communication always starts with an SPI instruction sent from the controller to the H-bridge.

During a write cycle the controller sends the data after the SPI instruction, beginning with the MSB.

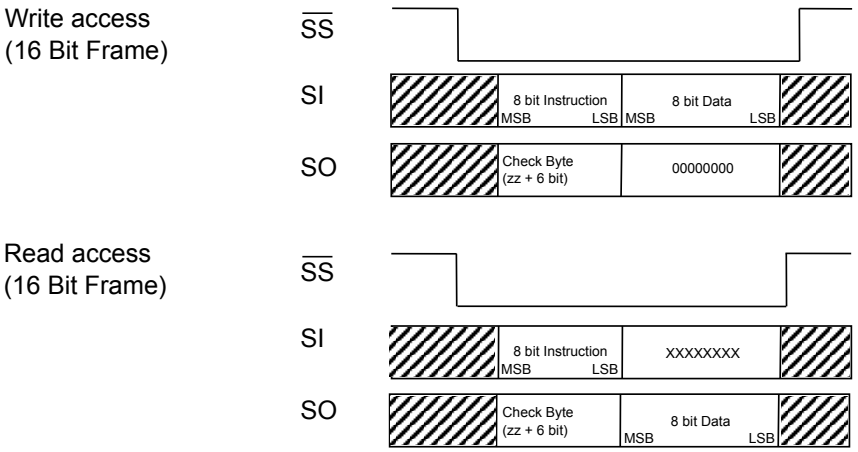
During a reading cycle, after having received the SPI instruction, the H-bridge sends the corresponding data to the controller, also starting with the MSB.

In general, depending on the specific application four different frame types are supported (see the table below). The frames-types are defined by the number of bits being transferred during an active slave-select phase (falling SCK-edges during NSS = low).

Table 25. **Frame Types**

Instruction	Data		
Standard:	16-bit frame	8 bits	8 bits
Extended_2 is not used in H-bridge	-	-	-
Extended_3 is not used in H-bridge	-	-	-
Burst frame types are not used in H-bridge	-	-	-

Figure 29. **Standard SPI frame**



Since the coding of the SPI instructions is done in such a way that at least at bit 5 it is clear, whether a reading or a writing instruction is sent, and moreover, the instructions are not using the LSB of the instruction, there is at least a duration of one bit left in order to provide the requested data for the SO.

3.2.7.3 *Characteristics of the SPI interface*

The characteristics of the SPI interface are the following:

- **During active reset conditions:** the SPI is driven in its default state. When reset becomes inactive, the state machine enters in a wait state for the next instruction. During active reset conditions the output SO is in high impedance state (tristate).
- **If the slave-select signal at NSS is inactive (high):** the state machine is forced to enter the wait state, that is the state machine waits for the following instruction.
- **During active (low) state of the select signal SS:** the falling edge of the serial clock signal SCK will be used to latch the input data at SI. Output data at SO are driven with the rising edge of SCK. Further processing of the data according to the instruction (that corresponds to the modification of the internal registers) will be triggered by the rising edge of the NSS signal.
- **Chip address:** in order to establish the option of extended addressing, the uppermost two bits of the instruction-byte (that is the first two SI-bits of a frame) are reserved to send a chip address.

  For future orientation, a configurable chip-address is requested. This should be achieved by connecting the chip-address register-bits to an electrical low or high potential onto the silicon. The default chip-address (as specified in Section 3.2.7.4 SPI Instruction) should always be 00hex. However, a switch-over, by modifying the bond-wire configuration onto the silicon should be possible later on for a dedicated derivate. As alternative a mask option or fuse can be also used.To avoid a bus conflict the output SO must stay in high impedance state during the addressing phase of a frame (that is until the address bits are recognized as valid chip address). If the chip address does not match, the corresponding access will be ignored and SO remains high impedance for the complete frame regardless of the frame type that is applied. Even in case the lower instruction bits match to a valid instruction, there is no impact on internal registers or any functions (including the Transfer Failure Message).
- **Check byte:** during the receiving of an SPI instruction, the H-bridge transmits a check byte via the output SO to the controller. This byte indicates the correctness of the operation of the SPI. It contains an initial bit pattern and a flag indicating possible invalid instruction of the previous access.
- **Read and write access:** during a read access the data bits at the SPI input SI are rejected/ignored. During a valid write access the SPI will transmit the data byte “00_{hex}” at the output SO after having sent the check byte. When a Bit in the Register is cleared during Read-Access this will be done when the communication is finished successfully (rising edge of SS after 16 bits).

- **Invalid instruction/access**: an instruction is invalid, if one of the following conditions is fulfilled: a) an unused instruction code is detected (see Table 26), b) in case the previous transmission is not completed in terms of internal data processing (violation of the minimum access-time).

  If an invalid instruction is detected, no modifications of the registers of the H-bridge are allowed.

  In case an unused instruction code has occurred, the data byte "FF_{hex}" will be transmitted after having sent the check byte. In order to guarantee the proper operation of the corresponding circuitry the active NSS signal must be stable for at least 50ns. In addition any access is invalid if the number of SPI clock pulses (falling edge) counted during active NSS differs from exactly 16 clock pulses.

  A write access will be internally rejected (that is internal registers will not be affected) in case the number of falling edges applied to the SPI input SCK during the access is not equal to 16.

3.2.7.4 *SPI Instruction*

The uppermost 2 bits of the instruction byte are reserved to feature extended chip addressing.

The individual chip address is an option and has to be defined in accordance to the SPI-Members sharing one NSS line.

Only when the first two bits after the falling edge of NSS are matching, the H-bridge is allowed to transfer data on SO.

Table 26. SPI Instruction byte

MSB							
7	6	5	4	3	2	1	0
CPAD1	CPAD0	INST5	INST4	INST3	INST2	INST1	INST0

Bit	Name	Description
7	CPAD1 (INST7)	Chip Address: Mask-Option Value: 0 (via pad configuration)
6	CPAD0 (INST6)	Chip Address: Mask-Option Value: 0 (via pad configuration)
5…0	INST5	Read/Write: Read: 0 Write: 1
4…0	INST4…0	SPI instruction

3.2.7.5 *Check byte*

Table 27. Check byte

MSB							
7	6	5	4	3	2	1	0
Tristate	Tristate	1	0	1	0	1	TRANS_F

Bit	Name	Description
7	-	Tri state (high impedance)
6	-	Tri state (high impedance)
5	-	Fixed to High
4	-	Fixed to Low
3	-	Fixed to High
2	-	Fixed to Low
1	-	Fixed to High
0	TRANS_F	Transfer-Failure: (reset value '0')

MSB		
		TRANS_F = 0: Previous Transfer was recognized as valid; TRANS_F = 1: Error detected during previous transfer (regarding the actual device, that is: chip address valid)

3.2.7.6 *SPI registers overview*

In Table 28 all the commands to access the SPI registers are summarized.

Table 28. SPI registers overview

Command	INST[7..0]	Description
RD_ID	0000 0100	Read device ID
RD_REV	0000 0110	Read device Revision
RD_DIA1	0001 0000	Read power stage diagnostic information (1)
RD_DIA2	0001 1000	Read power stage diagnostic information (2)
RD_CONFIG	0000 1000	Read power stage configuration
RD_STATCON	0000 1100	Read VDD monitoring status
RD_SPECIAL	0000 1110	Read information from SPECIAL
WR_DIA1	0011 0000	Write special bits in DIA1
WR_DIA2	0011 1000	Write special bits in DIA2
WR_CONFIG	0010 1000	Write power stage configuration
WR_STATCON	0010 1100	Write VDD monitoring status
WR_SPECIAL	0010 1110	Write information to SPECIAL
All other	00xx xxxx	Unused, TRANS_F is set to high, ff hex is sent as data bits

The SFR list describes all the different reset sources. On every SPI register detail, in the next paragraphs, the values of the reset sources after the different resets are also shown.

Table 29. SFR List description

Reset Sources	
POR	Reset after VDD is rising above VDD_POR threshold after the ASIC was disabled during VDD undervoltage.
SPIR	Reset activated by set the bit CONFIG_REG.RESET='0' via SPI
ENDISR	Reset by disable-enable sequence via ABE or DIS Signal (edge triggered)
DISR	Reset by disabling the power stage (DIS or ABE level triggered)
DIACLR1	Reset by setting the bit STATCON_REG.DIACLR1='0'
DIACLR2	Reset by setting the bit STATCON_REG.DIACLR2='0'
RDR	Reset after SPI Read out of the Register
Reset behavior of the Register content	
1	Bit will be changed to '1'
0	Bit will be changed to '0'
x	No change of the bit content

3.2.7.6.1 Device identifier

The H-bridge's identifier is used for production test purposes and features plug and play functionality depending on the systems software release. It is made up of a device-number and a revision number each one read-only accessible via standardized instructions.

The device number is defined once to allow identification of different IC-Types by software.

The revision number may be utilized to distinguish different states of hardware. The content is divided in an upper 4-bit field reserved to define revisions corresponding to specific Software Releases.

The lowest 4-bit field is utilized to identify the actual mask set.

Both (SWR and MSR) will start with 0000b and are increased by 1 every time a corresponding modification of the hardware is introduced.

Table 30. Register ID_REG

Bit	7	6	5	4	3	2	1	0
Bit-Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
POR	1	1	0	1	1	1	1	1
SPIR	1	1	0	1	1	1	1	1
ENDISR	x	x	x	x	x	x	x	x
DISR	x	x	x	x	x	x	x	x
RDR	x	x	x	x	x	x	x	x
Controller access: read only				**(read-access: RD_ID)**				
Bit	Name			Description				
7..0	ID7...ID0			Device number: 0xDF				

Table 31. Register REV_REG

Bit	7	6	5	4	3	2	1	0
Bit-Name	SWR3	SWR2	SWR1	SWR0	MSR3	MSR2	MSR1	MSR0
POR	0	1	0	0	0	0	0	0
SPIR	0	1	0	0	0	0	0	0
ENDISR	x	x	x	x	x	x	x	x
DISR	x	x	x	x	x	x	x	x
RDR	x	x	x	x	x	x	x	x
Controller access: read only				**(read-access: RD_REV)**				
Bit	Name			Description				
7..4	SWR3...SWR0			Revision corresponding to software release default: 4_{hex}				
3..0	MSR3...MSR0			Revision corresponding to mask set default: 0_{hex}; in AA silicon: 0_{hex}				

3.2.7.6.2 Status register (read and write access)

Table 32. Register DIA_REG1

Bit	7	6	5	4	3	2	1	0
Bit-Name	NABE_DIS	OT	Var1	Var0	DIA21	DIA20	DIA11	DIA10
POR	x	1	1	1	1	1	1	1
SPIR	x	1	x	x	1	1	1	1
ENDISR	x	1	x	x	1	1	1	1
RDR	x	x	x	x	x	x	x	x
DIACLR1	x	1	x	x	1	1	1	1
Controller access: read/write				**(write-access: WR_DIA1)** **(read-access: RD_DIA1)**				

Bit	Name	Description	
7	NABE_DIS	0: NABE = Low or/and DIS = High 1: NABE = High and DIS = Low	(not latched) (r)
6	OT	0: Over Temperature 1: no Over Temperature	(latched) (r)
5	VAR1	r/w for special use	(latched) (r/w)
4	VAR0	r/w for special use	(latched) (r/w)
3	DIA21	See Table 33 below	(r)
2	DIA20		
1	DIA11		
0	DIA10		

Table 33. Diagnosis bits (DIA_REG1)

DIA21	DIA20	DIA11	DIA10	Description	Remark
0	0	0	0	Not used	
0	0	0	1	Short Circuit to Ground at OUT1 (SCG1)	latched
0	0	1	0	Short Circuit to Ground on OUT2 (SCG2)	latched
0	0	1	1	Not used	
0	1	0	0		
0	1	0	1	Short Circuit to Battery on OUT1 (SCB1)	latched
0	1	1	0	Short Circuit to Battery on OUT2 (SCB2)	latched
0	1	1	1	Short Circuit across load (SCL)	latched
1	0	0	0	Short Circuit to Battery at disabled output	latched
1	0	0	1	Short Circuit to Ground at disabled output	latched
1	0	1	0	Open Load (at disabled output or in active)	latched
1	0	1	1	Not used	
1	1	0	0		
1	1	0	1	Undervoltage at pin V_S	Not latched
1	1	1	0	Not used	

DIA21	DIA20	DIA11	DIA10	Description	Remark
1	1	1	1	No failure	-

In DIA_REG1 the errors are stored. A read process does not reset DIA_REG1.

Reported errors are: Open Load (OL), Over Temperature (OT), Short Circuit (SCG1, SCG2, SCB1, SCB2, SCL).

General description, how the DIA_REG1 and the DIA_REG2 are related together:

- Any time, an error is detected, the HBR is switched off (exception: Open Load diagnosis)
- The detected error is to be confirmed or in the case of short circuit to clarify, if single SC or SCL
- The confirmed error is set in DIA_REG1
- The HBR can only get active again after Power on reset, this is the reset source POR or after disabling - enabling sequence, this is the reset source ENDISR
- The HBR is disabled by the operating software in the control unit, this is the usual procedure
- Some other action from the operating software in the control unit may happen, f.i. resetting DIA_REG1
- So in the DIA_REG1 there is still the error code or the DIA_REG is reset
- Finally the HBR will be enabled again (ENDISR) by the operating software

If a fault is detected, the H-bridge is switched off and the error is entered in the DIAREG1 (short circuit error after confirmation).

After EN/DIS sequence or setting DIACLR1 the diagnostic related to the error in DIAREG1 is transferred to DIAREG2 and DIAREG1 is cleared.

If now another error happens, the H-bridge is switched off and the new error is entered in the DIAREG1.

Remarks:

The errors can be reset selectively. By writing STATCON_REG.DIACLR2 = 0, this resets all errors in DIA_REG2, that is the previous errors. By writing STATCON_REG.DIACLR1 = 0, this transfers all latched errors from DIA_REG1 to DIA_REG2 and resets DIA_REG1 afterwards, if there is no under voltage condition existing.

To completely delete the whole error log, the following sequence has to be transmitted via SPI:

- STATCON_REG.DIACLR1 = 0
- STATCON_REG.DIACLR2 = 0

Undervoltage at V_S (there is no error but condition):

If there is any error stored and additional the condition ‘undervoltage’ occurs, the condition ‘undervoltage’ is reported as long as the undervoltage condition is present. If the undervoltage condition disappears, the previously reported error is present again until it is reset.

NABE_DIS always shows directly the status of the power stages. NABE_DIS is set to ‘0’, if the power stages are disabled by NABE or DIS or (NABE and DIS).

Table 34. Register DIA_REG2

Bit	7	6	5	4	3	2	1	0
Bit-Name	CurrRed	CurrLim	OT	Var2	DIA21	DIA20	DIA11	DIA10
POR	1	1	1	0	1	1	1	1
SPIR	1	1	1	x	1	1	1	1
ENDISR	1	1	x	x	x	x	x	x
RDR	1	1	x	x	x	x	x	x
DIACLR2	1	1	1	x	1	1	1	1
Controller access: read/write					**(write-access: WR_DIA2)) (read-access: RD_DIA2**			
Bit	Name	Description						
7	CurrRed	Temperature depend current reduction (TDCR) [no error]						

Bit	7	6	5	4	3	2	1	0
7	CurrRed		0: TDCR is active 1: TDCR is not active			(latched) (r)		
6	CurrLim		Current Limitation (CL) [no error] 0: CL is active 1: CL is not active			(latched) (r)		
5	OT		It is the previously OT error from DIA_REG1			(latched) (r)		
4	VAR3		r/w for special use			(latched) (r/w)		
3	DIA21		See Table 35 below			(r)		
2	DIA20							
1	DIA11							
0	DIA10							

Table 35. Diagnosis bits (DIA_REG2)

DIA21	DIA20	DIA11	DIA10	Description	Remark
0	0	0	0	Not used	
0	0	0	1	Short Circuit to Ground at OUT1 (SCG1)	latched
0	0	1	0	Short Circuit to Ground on OUT2 (SCG2)	latched
0	0	1	1	Not used	
0	1	0	0		
0	1	0	1	Short Circuit to Battery on OUT1 (SCB1)	latched
0	1	1	0	Short Circuit to battery on OUT2 (SCB2)	latched
0	1	1	1	Short Circuit across load (SCL)	latched
1	0	0	0	Short Circuit to Battery at disabled output	latched
1	0	0	1	Short Circuit to Ground at disabled output	latched
1	0	1	0	Open Load (at disabled output or in active)	latched
1	0	1	1	Not used	
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1	No failure	-

Any read process of the error information (OL, OT, SCG1, SCG2, SCB1, SCB2, SCL) does not reset this information or register.

The errors can be reset selectively. By writing STATCON_REG.DIACLR2 = 0, this resets all errors in DIA_REG2, that is the previous errors. By writing STATCON_REG.DIACLR1 = 0, this transfers all latched errors from DIA_REG1 to DIA_REG2 and resets DIA_REG1 afterwards, if no undervoltage condition is present.

To fully reset the error logs, the following sequence has to be transmitted via SPI:

- STATCON_REG.DIACLR1 = 0
- STATCON_REG.DIACLR2 = 0

OT is the previously error from DIA_REG1.

CurrRed and CurrLim represent the latched information. Each read process of DIA_REG2 resets this error information. This error information is updated in case the error conditions reappear or are still present.

3.2.7.6.3 Data register (read and write access)

Table 36. Register CONFIG_REG

Bit	7	6	5	4	3	2	1	0
Bit-Name	FW	MUX	SDIR	SPWM	CL1	CL2	RESET	OLDA
POR	1	1	1	1	1	0	1	0
SPIR	1	1	1	1	1	0	1	0
ENDISR	x	x	x	x	x	x	1	x
DISR	x	x	x	x	x	x	x	x
RDR	x	x	x	x	x	x	1	x

Controller access: read/write	(write-access: WR_CONFIG) (read-access: RD_CONFIG)	
Bit	Name	Description
7	FW	‘1’: free wheeling with active short cut of body diode (latched) ‘0’: free wheeling only via body diode (r/w)
6	MUX	‘1’: control by parallel inputs PWM and DIR (latched) ‘0’: control by SPI bits SPWM and SDIR (r/w)
5	SDIR	Same effect like the signal DIR, but transmitted via SPI ‘0’: same effect like DIR = Low (latched) ‘1’: same effect like DIR = High (r/w)
4	SPWM	Same effect like the signal PWM, but transmitted via SPI ‘0’: same effect like PWM = Low (latched) ‘1’: same effect like PWM = High (r/w)
3	CL1	See Table 37 below (latched) (r/w)
2	CL2	
1	RESET	‘1’: no change (r/w) ‘0’: reset of device configuration to default
0	OLDA	‘1’: Open Load diagnosis in active operation switched on (latched) ‘0’: Open Load diagnosis in active operation switched off (r/w)

Table 37. Current Level (CONFIG_REG)

CL1	CL2	Description	Remark
0	0	No change	No change
0	1	2	5.0 A
1	0	3 (reset value)	6.6 A
1	1	4	8.6 A

Table 38. Register STATCON_REG

Bit	7	6	5	4	3	2	1	0
Bit-Name	CONFIG2	CONFIG1	CONFIG0	DIACLR2	DIACLR1	STATUS2	STATUS1	STATUS0
POR	1	1	0	1	1	x	x	x

Bit	7	6	5	4	3	2	1	0
SPIR	1	1	0	1	1	x	x	x
ENDISR	x	x	x	1	1	x	x	x
DISR	x	x	x	x	x	x	x	x
RDR	x	x	x	1	1	x	x	x

Controller access: read/write **(write-access: WR_STATCON)** **(read-access: RD_STATCON)**

Bit	Name	Description	
7	CONFIG2	'1': test of VDD threshold is switched off '0': test of VDD threshold is switched on	(latched) (r/w)
6	CONFIG1	'1': lower threshold of VDD-monitoring is lifted (If CONFIG2 = 0 - test of switch-off path) '0': upper threshold of VDD-monitoring is reduced (If CONFIG2 = 0 - test of switch-off path)	(latched) (r/w)
5	CONFIG0	'1': latch function for overvoltage at VDD is switched on '0': latch function for overvoltage at VDD is switched off	(latched) (r/w)
4	DIACLR2	if set = 0: all previous errors of DIA_REG2 are reset if set = 1: no action if read then always = 1	(not latched) (r/w)
3	DIACLR1	if set = 0 then all latched errors of DIA_REG1 are to be transferred to the register DIA_REG2 and DIA_REG1 is reset. Exception is: if an undervoltage at pin V_S is present, DIACLR1 will not have any effect. if set = 1: no action if read then always = 1	 (not latched) (r)
2	STATUS2	Logic level at NABE	(r)
1	STATUS1	'1': no undervoltage at VDD '0': undervoltage at VDD	(not latched) (r)
0	STATUS0	'1': no overvoltage at VDD '0': overvoltage at VDD resp. state of overvoltage still stored (reset by CONFIG0 = '0') Comment: overvoltage information (bit STATUS0 = 0) will not be reset by undervoltage at V_S. Overvoltage will even be detected and stored (CONFIG0 = 1) during undervoltage at V_S. The information will be reset if an internal (undervoltage at VDD) reset occurs or when CONFIG0 is set to 0 or via SPI reset (CONFIG_REG.RESET = 0).	(r)

Remarks:

Write-access is only possible for CONFIGx and DIACLRx. The bits STATUSx are not affected by a write-access to STATCON_REG, except indirectly by a change of CONFIGx.

Any write access to STATCON_REG will take effect immediately. No re-enabling via switching (DIS to HIGH and then to LOW again) or (NABE via switching to Low and then to High again) is necessary.

Table 39. Register SPECIAL_REG

Bit	7	6	5	4	3	2	1	0
Bit-Name	Not specified	Not specified	DCmatching	OLDAFILTER	Not specified	SR0	SR1	Reserved
POR	0	0	0	1	0	0	0	1
SPIR	0	0	0	1	0	0	0	1
ENDISR	x	x	x	x	x	x	x	x
DISR	x	x	x	x	x	x	x	x
RDR	x	x	x	x	x	x	x	x
Controller access: read/write				**(write-access: WR_SPECIAL) (read-access: RD_SPECIAL)**				

Bit	Name	Description	
7	Not specified		
6	Not specified		
5	DCmatching	‘0’: EMC optimized switching behavior ‘1’: exact duty cycle matching	(latched) (r/w)
4	OLDAFILTER	‘1’: Open Load in on state detected after one retry ‘0’: Open Load in on detected after 40 ms	(latched) (r/w)
3	Not specified		
2	SR0	See Table 40 below	(latched) (r/w)
1	SR1		
0	Reserved	r/w for special use	(latched) (r/w)

Table 40. Slew Rate bits (SPECIAL_REG)

SR1	SR0	Description	Remark
0	0	Slow slew rate	Default slew rate(1)
0	1	Fast slew rate	Fast slew rate(1)
1	0	Very fast slew rate 1	Very fast slew rate(1)
1	1	Very fast slew rate 2	

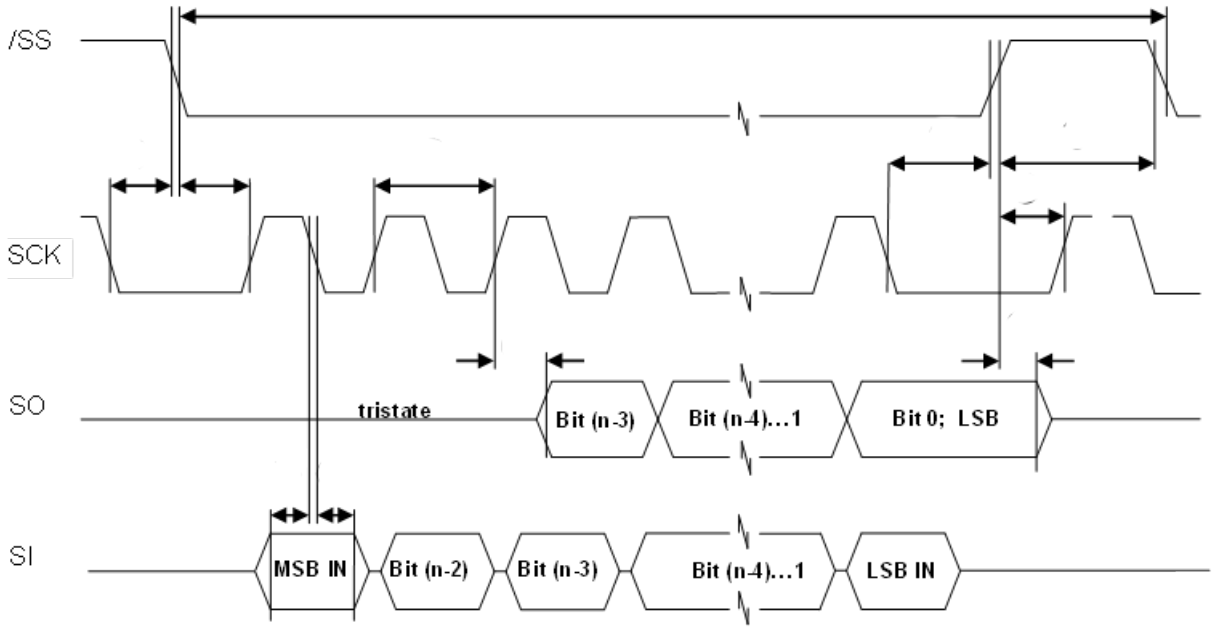
1. See Section 3.2.4.3 Power stage switching parameters

3.2.7.7 *Electrical characteristics*

The timing of the H-bridge is defined as follows:

- The change at output (SO) is forced by the rising edge of the SCK signal.
- The input signal (SI) is latched on the falling edge of the SCK signal.
- The data received during a write access are written into the internal registers at the rising edge of the NSS signal, if exactly 16 SPI clock pulses have been counted during NSS = active.
- The data transmitted during a read access is reflecting the status of the chip just before the SPI read instruction.
- There is only a SPI communication with a clock; without clock, the H-bridge should not react on SO.

Figure 30. **SPI Timing diagrams**



All parameters at VDD: 4.4 V to 5.6 V.
Battery supply V_S is as specified in Section 2.6 Power Supply.
Test condition: 2 V bias, 1 MHz, 20 mV (peak to peak) magnitude.

Table 41. **SPI parameters**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Pin SI, SCK						
VSI_L	input low level	-	-0.3	-	0.8	V
VSI_H	input high level	-	2.0	-	VDD + 0.3	V
VSI_HYS	input hysteresis	-	0.15	-	1.0	V
I_{puSI}	Pullup current	V_{SI} = 0 V	20	40	60	µA
C_{SI}	Input capacity	-	-	-	10	pF
Chip addressing bonding pad						
VCA_L	input low level	-	-0.3	-	0.8	V
VCA_H	input high level	-	2.0	-	VDD + 0.3	V
I_{puSCK}	Pullup current	V_{SCK} = 0 V	20	40	60	µA
C_{SCK}	Input capacity	-	-	-	10	pF
Pin NSS						
VSS_L	input low level	-	-0.3	-	0.8	V
VSS_H	input high level	-	2.0	-	VDD + 0.3	V
VSS_HYS	input hysteresis	-	0.15	-	1.0	V
I_{puSS}	Pullup current	V_{NSSx}=0V	20	40	60	µA

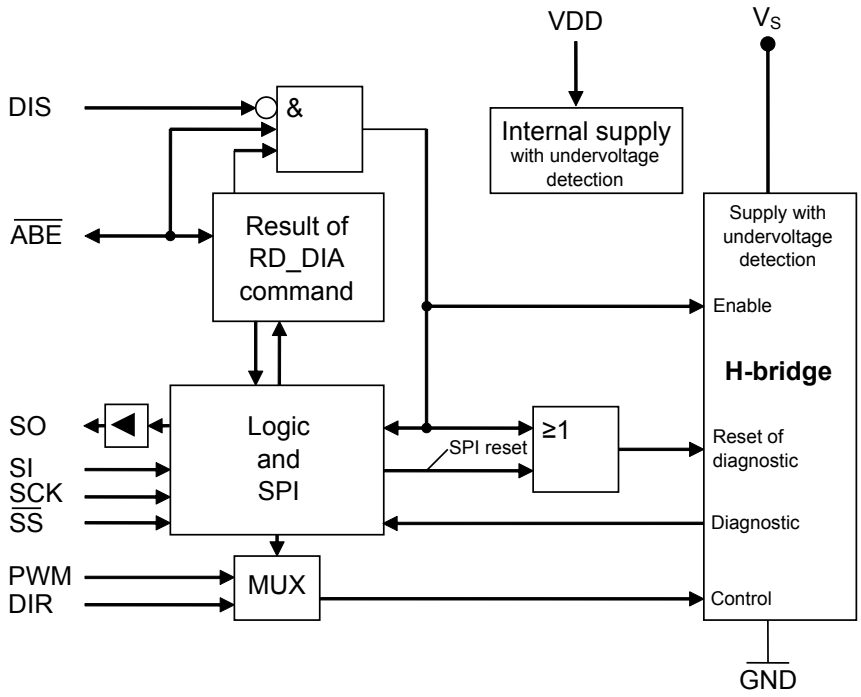
Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{SS}	Input capacity	-	-	-	15	pF
Pin SO						
-	Tristate output of the H-bridge. On active reset (VDD < VDD_POR) output SO is in tristate) In case of small current, resistive behavior can be assumed	-	-	-	-	-
VSO_L	output low level	I_SO = 2 mA	0.0	-	0.4	V
VSO_H	output high level	I_SO = -2 mA	VDD -0.5	-	VDD	V
t_{rf}	Rise/fall times (10% to 90%)	C_L = 25 pF C_L = 100 pF C_L = 200 pF	8 20 38	-	22 50 82	ns
I_{SO}	Leakage current	0 < VSO < VDD	-10	-	10	µA
I_{SO}	Leakage current	VDD < VSO < 18 V SO in tri-state mode	600	800	1000	µA
C_{SO}	Capacity of SO in tristate	-	-	-	10	pF
Disturbance of SPI interface						
ΔVx_L ΔVx_H	Change of input low or high level of SPI input pins in case of inverse current on V_S	-	-0.1	-	0.1	V
ΔI_{Sx}	Change of input current of SPI input pins in case of inverse current on V_S	-	-100	-	100	µA
ΔI_{SO}	Change of leakage current of SPI output pin in case of inverse current on V_S	-	-100	-	100	µA

Table 42. SPI timing parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_s	Baud Rate	-	-	-	2	Mbit/s
t_{cyc}	1 - Cycle Time (referred to master)	-	490	-	-	ns
t_{lead}	2 - Enable Lead Time (referred to master)	-	50	-	-	ns
t_{lag}	3 - Enable Lag Time (referred to master)	-	150	-	-	ns
t_v	4 - Data Valid (referred to master)	C_L = 25 pF C_L = 100 pF C_L = 200 pF	-	-	90 110 150	ns
t_{su}	5 - Data Setup Time (referred to master)	-	40	-	-	ns
t_h	6 - Data Hold Time (referred to master)	-	40	-	-	ns
t_{dis}	7 - Disable Time (referred to the H-bridge)	-	-	-	100	ns
t_{dt}	8 - Transfer Delay (referred to master)	-	250	-	-	ns
t_{dld}	9 - Disable Lead Time (referred to master)	-	250	-	-	ns
t_{dlg}	10 - Disable Lag Time (referred to master)	-	250	-	-	ns
t_{acc}	11 - Access Time (referred to master)	-	8.35	-	-	µs

3.2.7.8 *Logic inputs and outputs*

Figure 31. Inputs/outputs of the H-bridge



Note:
- *Both NABE and DIS release the power stages.*
- *VDD monitoring sets NABE → low, in case VDD is out of the operational range.*

3.2.7.8.1 Logic I/O electrical characteristics

Table 43. Logic I/O electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Pin DIR, PWM						
VINx_L	input low level	-	-0.3	-	0.8	V
VINx_H	input high level	-	2.0	-	VDD + 0.3	V
VINx_HYS	input hysteresis	-	0.15	-	1.0	V
I_{pulNx}	Pullup current	V_{INx} = 0 V	20	40	60	µA
I_{INx}	input current VINx > 3.0 V (without Pull Up)	-	-5	-	+5	µA
C_{INx}	Input capacity	-	-	-	20	pF
Pin DIS						
VDIS_L	input low level	-	-0.3	-	0.8	V
VDIS_H	input high level	-	2.0	-	VDD + 0.3	V
VDIS_HYS	input hysteresis	-	0.15	-	1.0	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{PUDIS}	Pullup current	0 V < V_{DISx} < 2.1 V	50	100	150	µA
I_{DISx}	input current VDIS > 3.0 V (without Pull Up)	-	-5	-	5	µA
C_{DIS}	Input capacity	-	-	-	20	pF
t_{DIS}	DIS pulse width pin DIS requires min. low level pulse width for setting/resetting SPI bits or diagnostic information	-	0.5	1	1.5	µs
Disturbance of input pin						
ΔVx_L ΔVx_H	Change of input low or high level of input pins in case of inverse current on V_S	-	-0.1	-	0.1	V
ΔIx	Change of input low or high level of input pins in case of inverse current on V_S	-	-100	-	100	µA

3.2.7.9 *TEST pin*

TEST pin is a high-voltage-driven input, exclusively used to provide one of the mandatory conditions in order to enter IC factory test-mode; externally providing a minimum required voltage value to TEST pin is not enough to successfully enter IC test-mode, as many other software conditions have to be met as well.

TEST pin input circuitry is provided with an internal resistive pull-down path to AGNDx ground, ensuring that input buffer does not provide wrong/uncertain information to the logic section in case TEST pin is left floating; thus, in ECU normal operation scenario, TEST pin can be either left open or connected to AGNDx ground (suggested implementation).

Table 44. TEST pin electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
VTEST_NOTM_MAX	TEST pin maximum allowed voltage in order to avoid IC test-mode activation	-	9	-	-	V	TEST

4 Functional safety

The device is used for the control of actuators from the safety-relevant path, the classification implemented is ISO 26262 ASIL- B(D).

This is done in order to allow the system to guarantee that the vehicle can be led in a safe state in case of any type of failure.

The IC development process has been carried out according to ISO 26262-5 ASIL B(D).

Figure 32. Block diagram of the H-bridge module

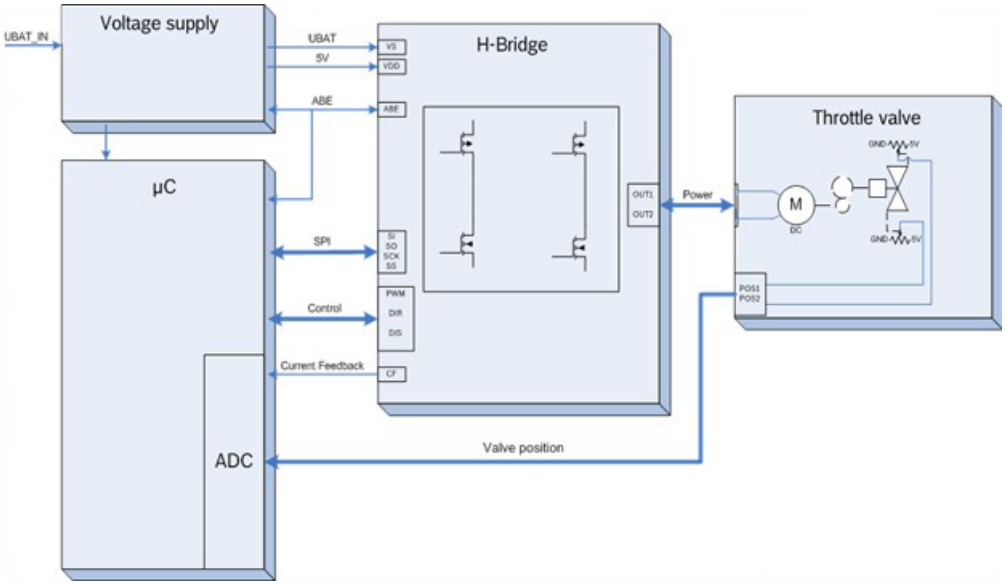
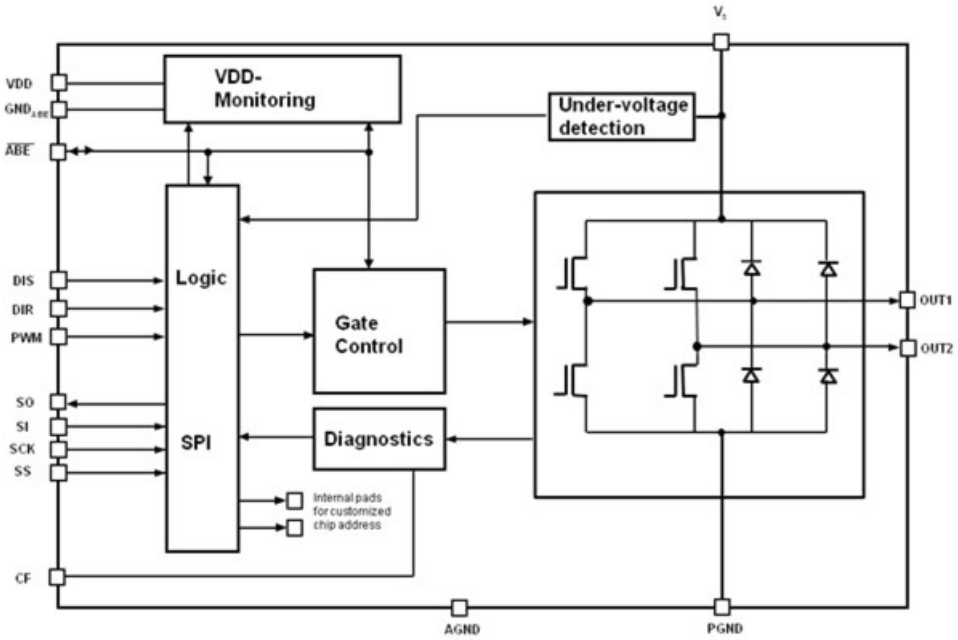
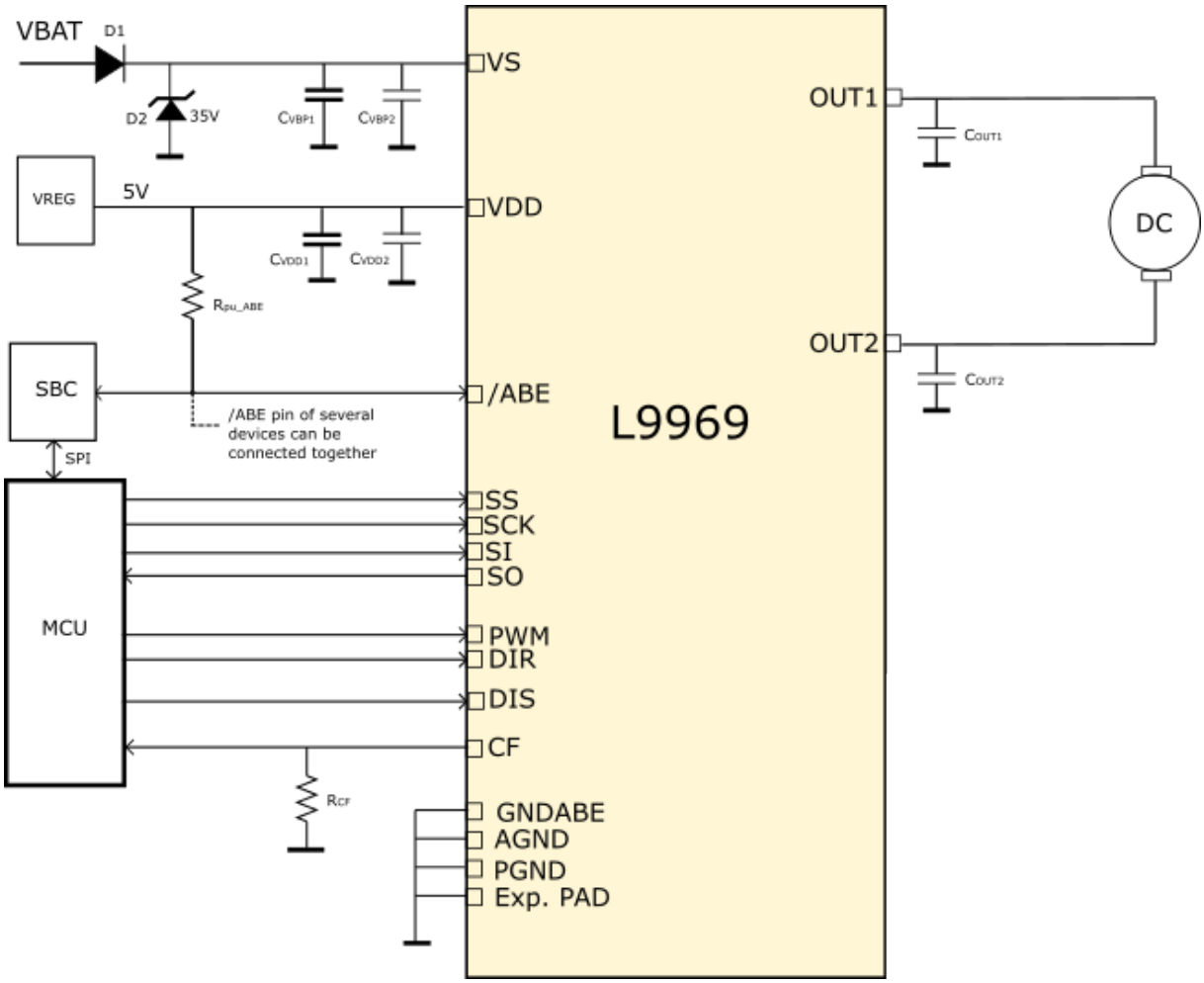


Figure 33. Block diagram of the H-bridge FS marking



5 Application circuit

Figure 34. **Application circuit**



5.1 Bill Of Materials

Table 45. Bill Of Materials

Component	Min	Typ	Max	Unit	Requirement	Comment
C_{VBP1}	-	100	-	µF	-	50 V
C_{VBP2}	-	1	-	µF	To be mounted close to pin	-
C_{VDD1}	-	10	-	µF	-	50 V
C_{VDD2}	-	100	-	nF	To be mounted close to pin	-
C_{OUT1}	10	-	33	nF	To be mounted close to pin	Values as big as possible (max 33 nF) are recommended if Open Load in OFF detection is disturbed
C_{OUT2}	10	-	33	nF	To be mounted close to pin	Values as big as possible (max 33 nF) are recommended if Open Load in OFF detection is disturbed
R_{CF}	-	5.1	-	kΩ	-	-
R_{pu_ABE}	-	1	30	kΩ	-	-
D1	-	-	-	-	STPS5L60S	-
D2	-	-	-	-	SMA6T33AY	Clamp max: 35 V

6 Load dump pulse

Figure 35. **Load dump pulse clamped**

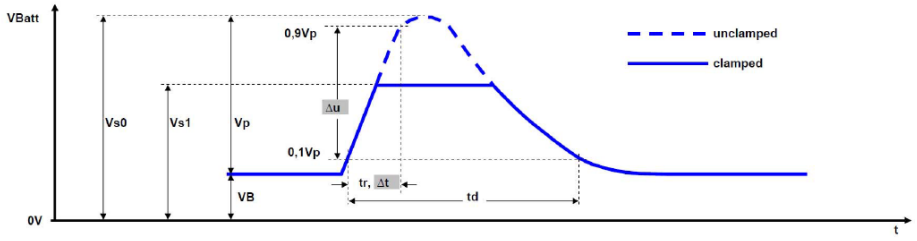


Table 46. **Load dump pulse parameters**

Parameter	Value	Tolerance	Test condition	Remark
VB	14.0 V	-	Tamb: RT and 85 °C ±3 °C	UBAT, nominal
Vsp0	101 V	-		Unclamped
Vp	87.0 V	-		Pulse-peak
Vs1	40.0 V	-		Clamped
Ri≤	0.5 Ω	-		-
Δu/Δt	7.0 V/ms	-		Vp/tr
Tr	10 ms	-5 ms		-
Td	400 ms	-		Pulse duration
To	60 s	-		Pulse periode
N	15	-		Number of pulses

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO24 (exposed pad opt. A) package information

Figure 36. PowerSSO24 (exposed pad opt. A) package outline

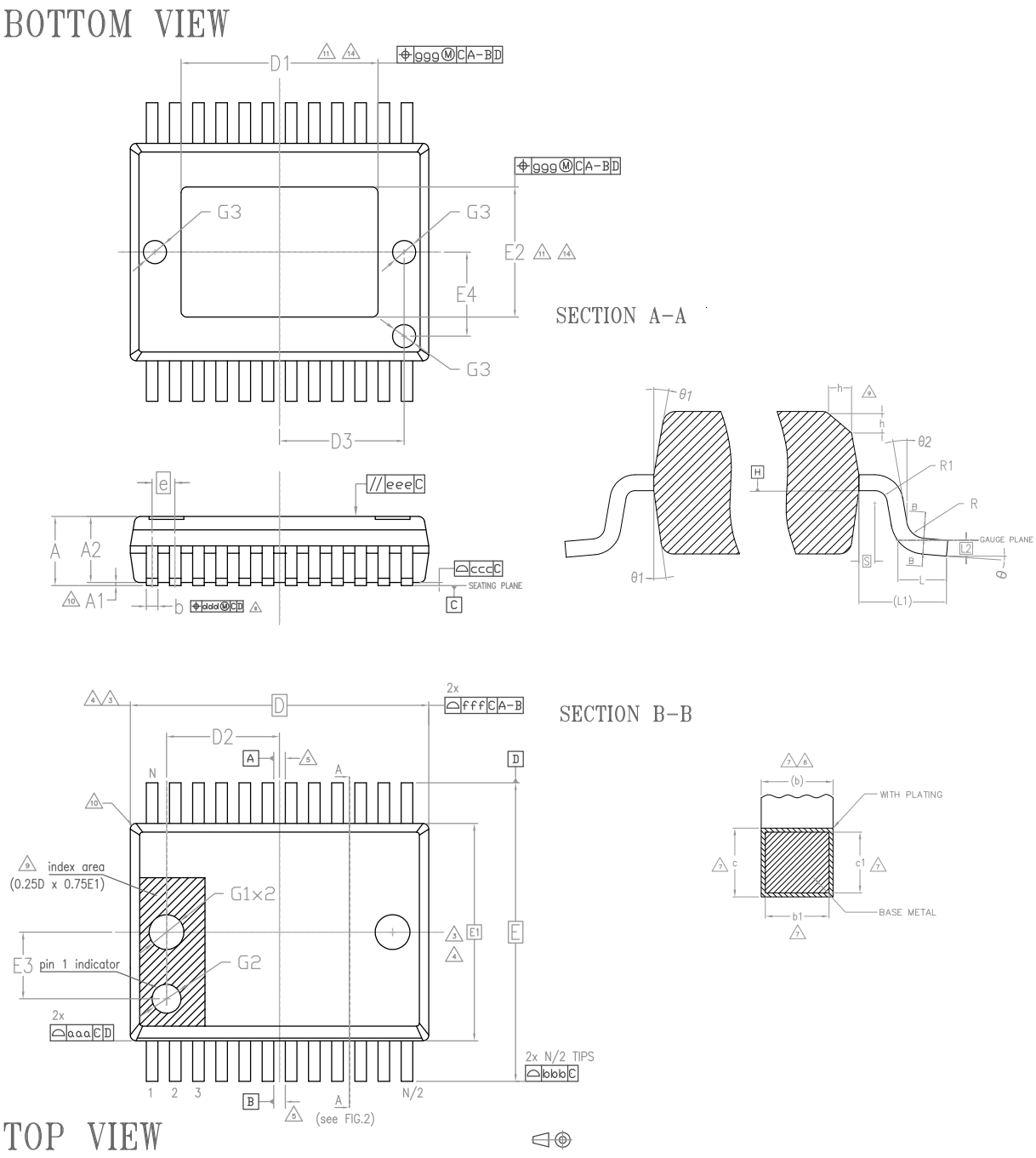


Table 47. PowerSSO24 (exposed pad opt. A) package mechanical data

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
Θ	0°	-	8°
Θ1	5°	-	10°
Θ2	0°	-	-
A	-	-	2.45
A1	0.0	-	0.1
A2	2.15	-	2.35
b	0.33	-	0.51
b1	0.28	0.40	0.48
c	0.23	-	0.32
c1	0.20	0.20	0.30
D(1)	10.30 BSC		
D1	VARIATION		
D2	-	3.65	-
D3	-	4.30	-
e	0.80 BSC		
E	10.30 BSC		
E1(1)	7.50 BSC		
E2	VARIATION		
E3	-	2.30	-
E4	-	2.90	-
G1	-	1.20	-
G2	-	1.0	-
G3	-	0.80	-
h	0.30	-	0.40
L	0.55	0.70	0.85
L1	1.40 REF		
L2	0.25 BSC		
N	24 (# lead)		
R	0.30	-	-
R1	0.20	-	-
S	0.25	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
eee	0.10		
ffff	0.20		
ggg	0.15		

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
Option A			
D1	6.5	-	7.1
E2	4.1	-	4.7

1. *Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is '0.25 mm' per side D and '0.15 mm' per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.*

7.2 PowerSSO36 (exposed pad opt. A) package information

Figure 37. PowerSSO36 (exposed pad opt. A) package outline

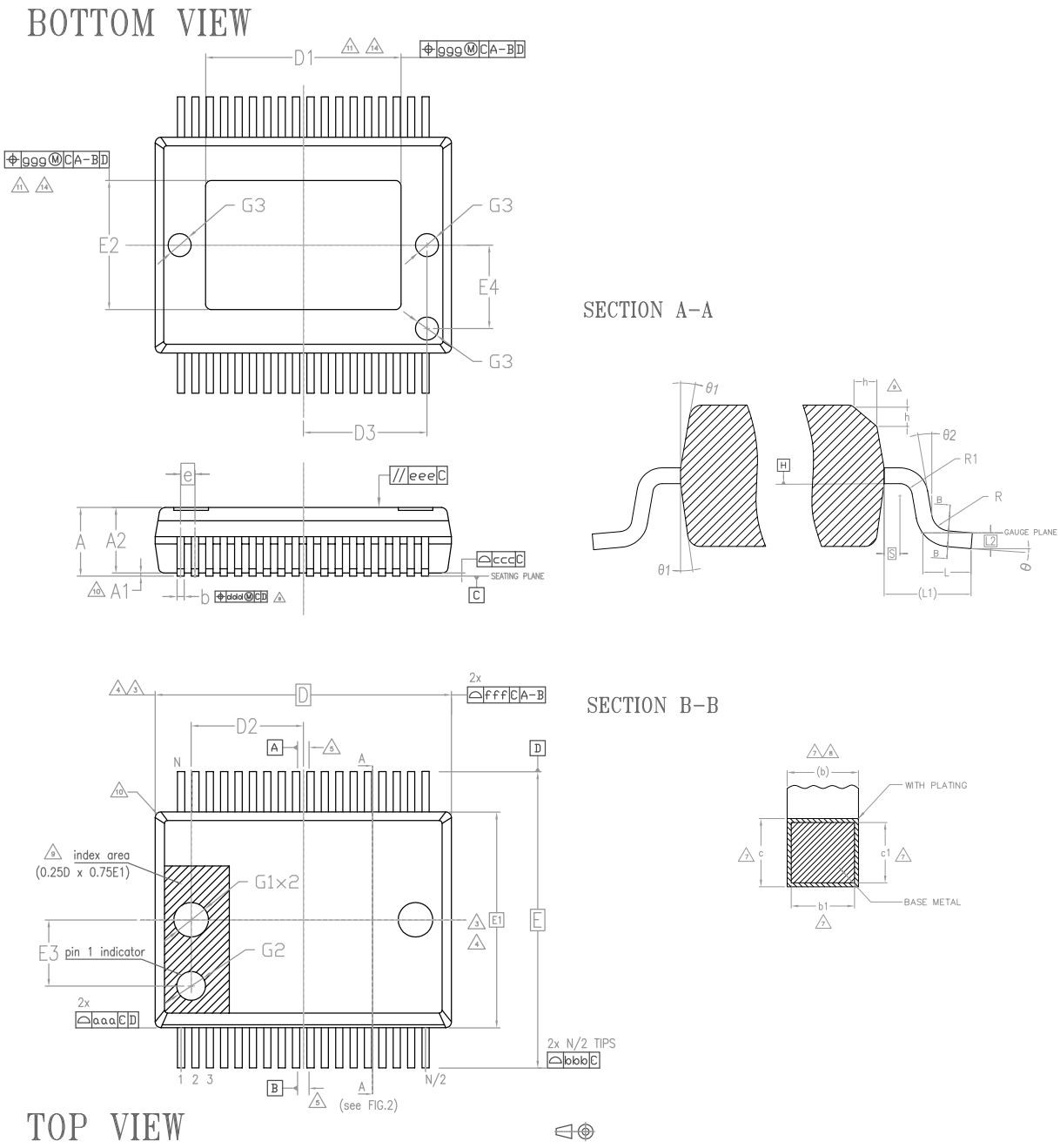


Table 48. PowerSSO36 (exposed pad opt. A) package mechanical data

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
Θ	0°	-	8°
Θ1	5°	-	10°
Θ2	0°	-	-
A	2.15	-	2.45
A1	0.0	-	0.1
A2	2.15	-	2.35
b	0.18	-	0.32
b1	0.13	0.25	0.3
c	0.23	-	0.32
c1	0.2	0.2	0.3
D(1)	10.30 BSC		
D1	VARIATION		
D2	-	3.65	-
D3	-	4.3	-
e	0.50 BSC		
E	10.30 BSC		
E1(1)	7.50 BSC		
E2	VARIATION		
E3	-	2.3	-
E4	-	2.9	-
G1	-	1.2	-
G2	-	1	-
G3	-	0.8	-
h	0.3	-	0.4
L	0.55	0.7	0.85
L1	1.40 REF		
L2	0.25 BSC		
N	36		
R	0.3	-	-
R1	0.2	-	-
S	0.25	-	-
Tolerance of form and position			
aaa	0.2		
bbb	0.2		
ccc	0.1		
ddd	0.2		
eee	0.1		
ffff	0.2		
ggg	0.15		

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
Option A			
D1	6.5	-	7.1
E2	4.1	-	4.7

1. *Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is '0.25 mm' per side D and '0.15 mm' per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.*

Revision history

Table 49. **Document revision history**

Date	Version	Changes
13-Oct-2022	1	Initial release.
10-Nov-2022	2	To improve readability Figure 1. L9969S/L9969U single bridge IC block diagram and Figure 2. L9969T twin bridge IC block diagram have been updated. Added product status links on cover page.
16-Nov-2022	3	Updated: • Figure 1. L9969S/L9969U single bridge IC block diagram; • Figure 2. L9969T twin bridge IC block diagram.

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