

## Automotive-grade N-channel 40 V, 7 mΩ typ., 54 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

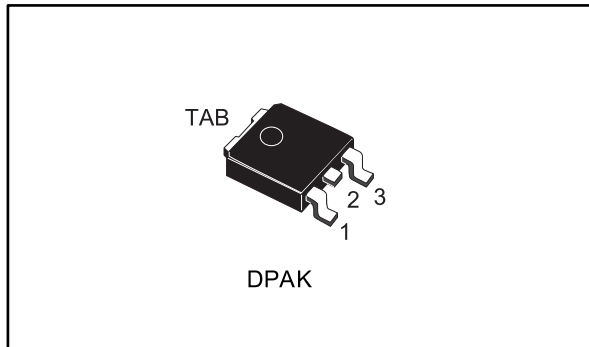
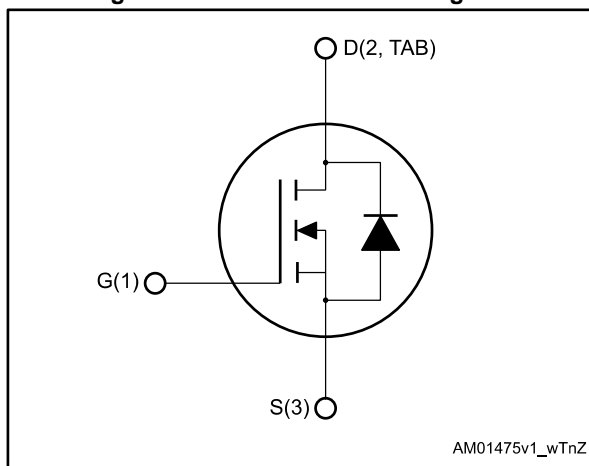


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD64N4F6AG	40 V	8.2 mΩ	54 A	60 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STD64N4F6AG	64N4F6	DPAK	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ °C}$ <sup>(1)</sup>	54	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	46	
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	216	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ °C}$	60	W
$T_{stg}$	Storage temperature	-55 to 175	°C
$T_j$	Operating junction temperature		

**Notes:**

<sup>(1)</sup> Current is limited by package.

<sup>(2)</sup> Pulse width is limited by safe operating area.

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj-pcb}$ <sup>(1)</sup>	Thermal resistance junction-pcb	35	

**Notes:**

<sup>(1)</sup> When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$ <sup>(1)</sup>	Avalanche current, repetitive or not repetitive	54	A
$E_{AS}$ <sup>(2)</sup>	Single pulse avalanche energy	180	mJ

**Notes:**

<sup>(1)</sup> Pulse width limited by  $T_{jmax}$ .

<sup>(2)</sup> starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AS}$ ,  $V_{DD} = 25\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			10	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 27\text{ A}$		7	8.2	m $\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	2415	-	$\mu\text{F}$
$C_{oss}$	Output capacitance		-	232	-	
$C_{rss}$	Reverse transfer capacitance		-	170	-	
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 54\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> : "Gate charge test circuit")	-	44	-	nC
$Q_{gs}$	Gate-source charge		-	15	-	
$Q_{gd}$	Gate-drain charge		-	12	-	

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 27\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> : "Switching times test circuit for resistive load" and <a href="#">Figure 18</a> : "Switching time waveform")	-	21.2	-	ns
$t_r$	Rise time		-	113	-	
$t_{d(off)}$	Turn-off delay time		-	40.4	-	
$t_f$	Fall time		-	25.2	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		54	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		216	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 27\text{ A}$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 54\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 32\text{ V}$ (see <a href="#">Figure 15</a> : "Test circuit for inductive load switching and diode recovery times")	-	29.4		ns
$Q_{rr}$	Reverse recovery charge		-	31.3		nC
$I_{RRM}$	Reverse recovery current		-	2.1		A

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

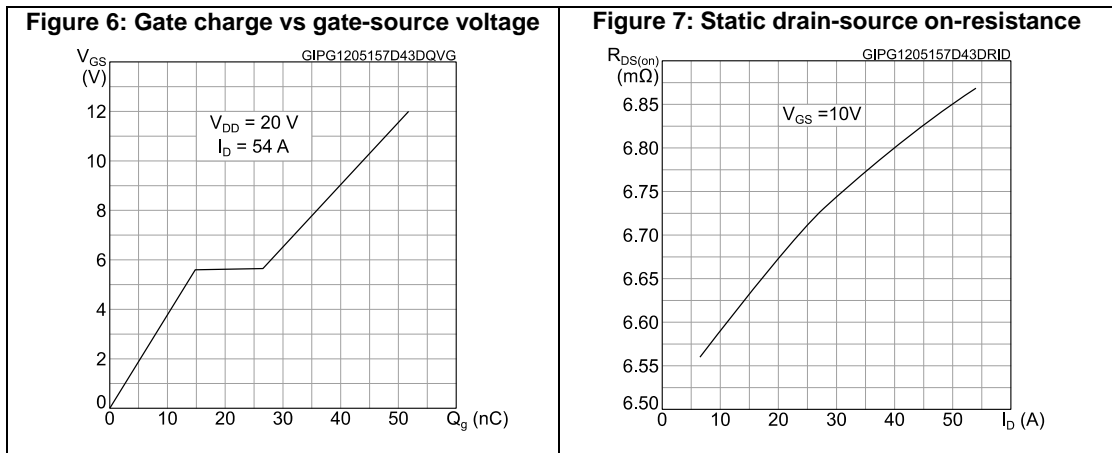
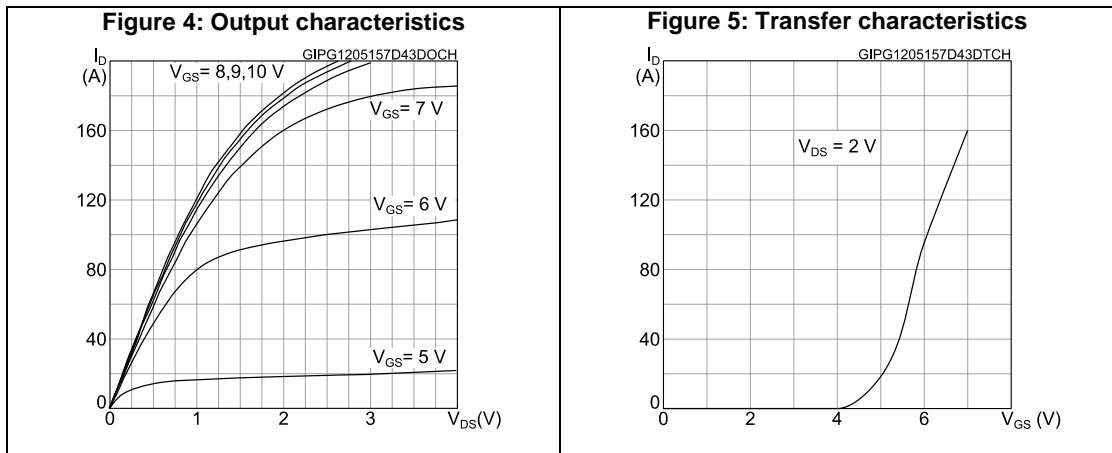
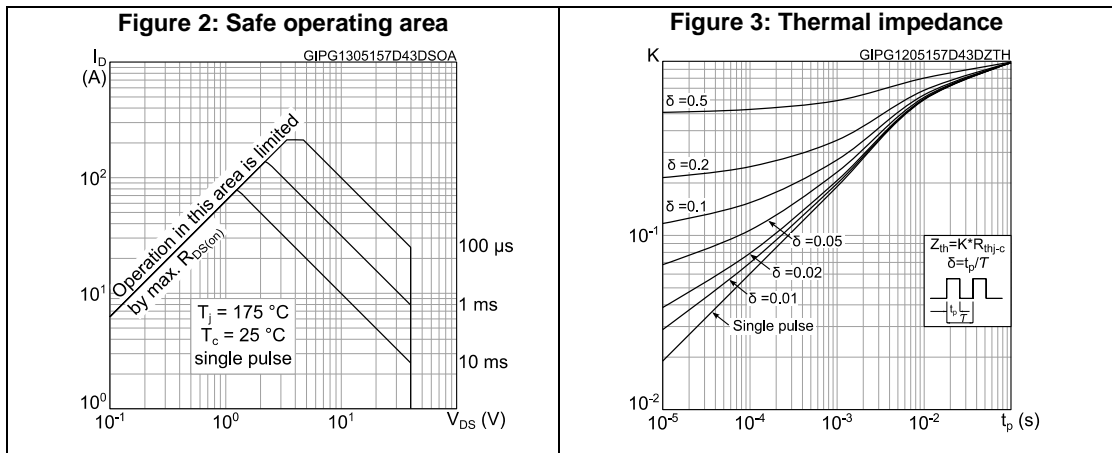


Figure 8: Capacitance variations

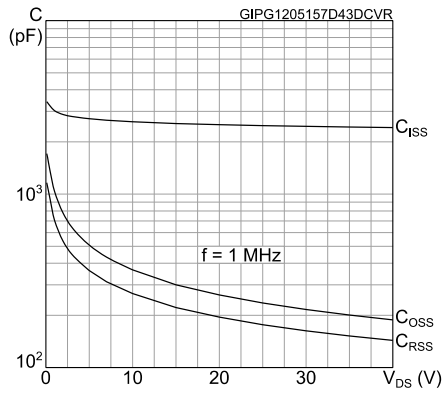


Figure 9: Normalized gate threshold voltage vs temperature

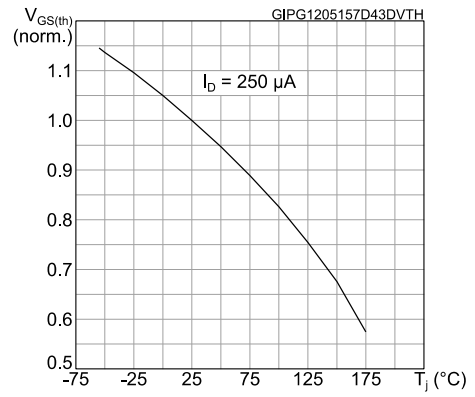


Figure 10: Normalized on-resistance vs temperature

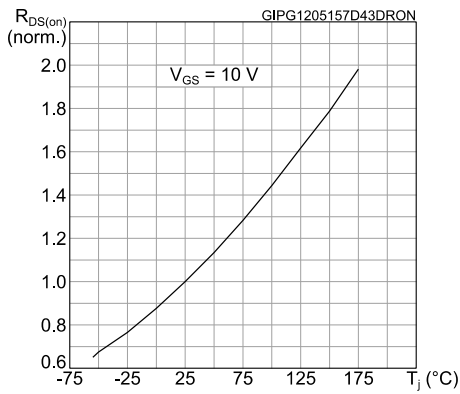


Figure 11: Normalized V(BR)DSS vs temperature

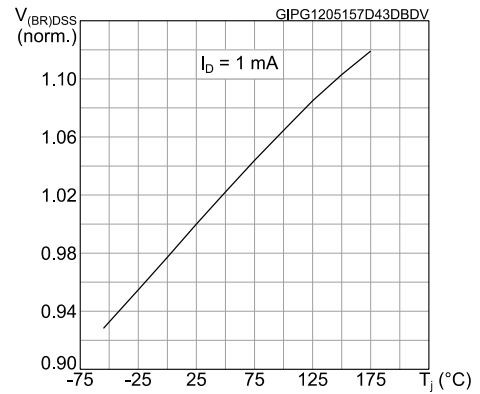
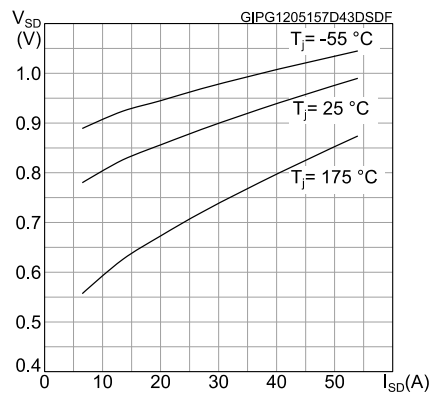
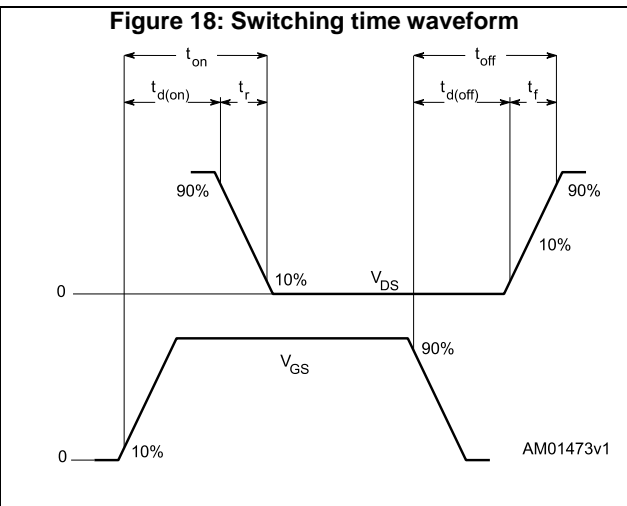
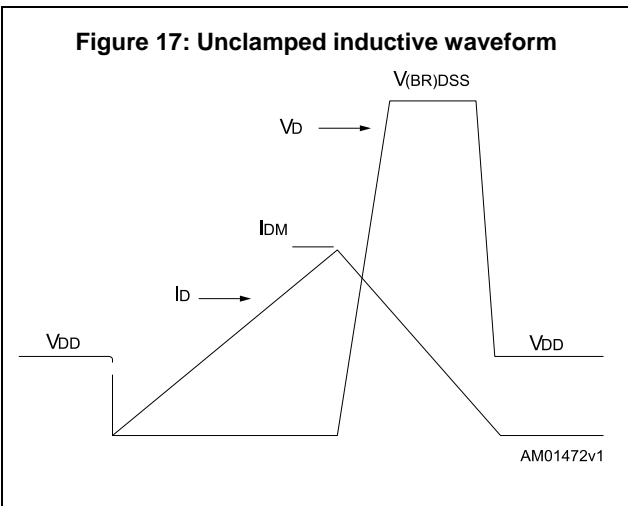
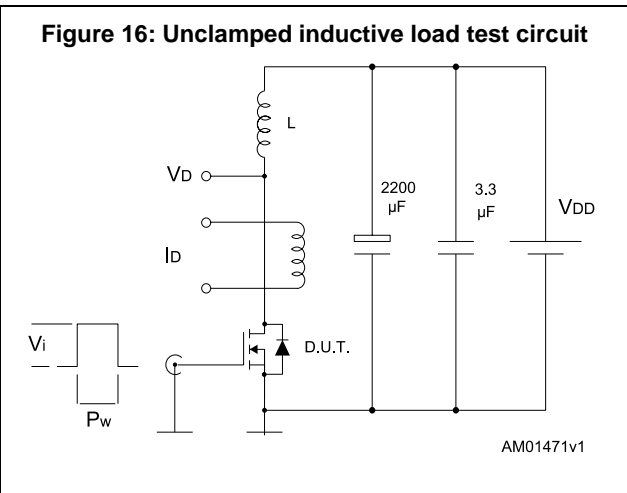
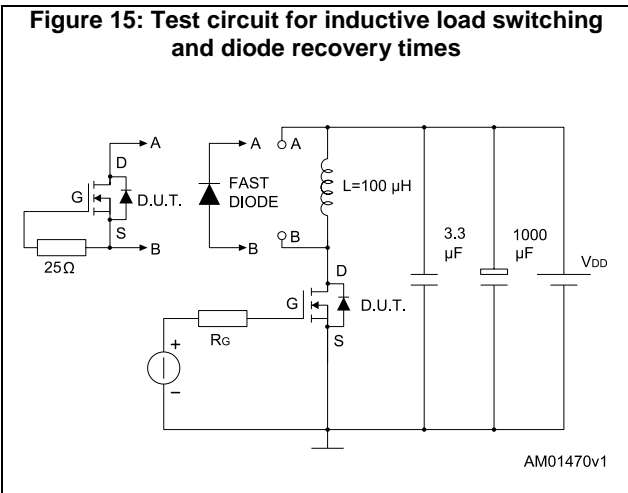
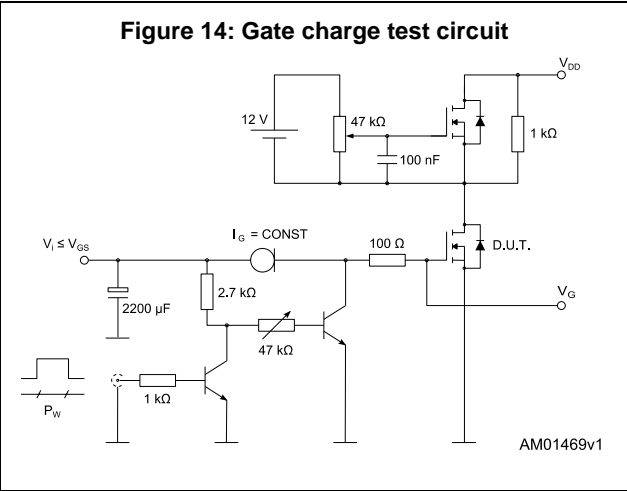
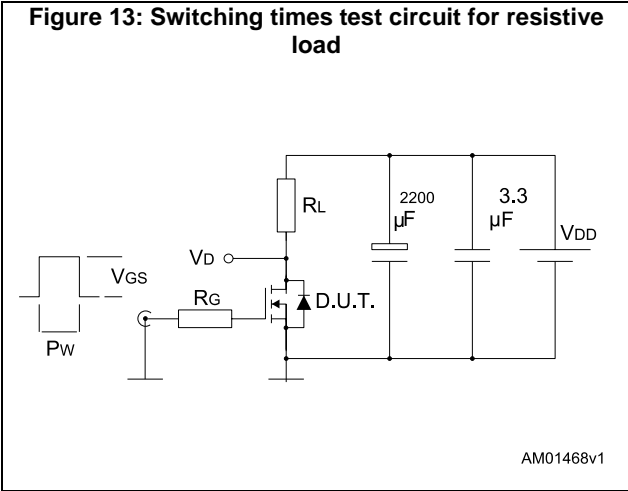


Figure 12: Source-drain diode forward characteristics



### 3 Test circuits





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 DPAK (TO-252) type A package information

Figure 19: DPAK (TO-252) type A package outline

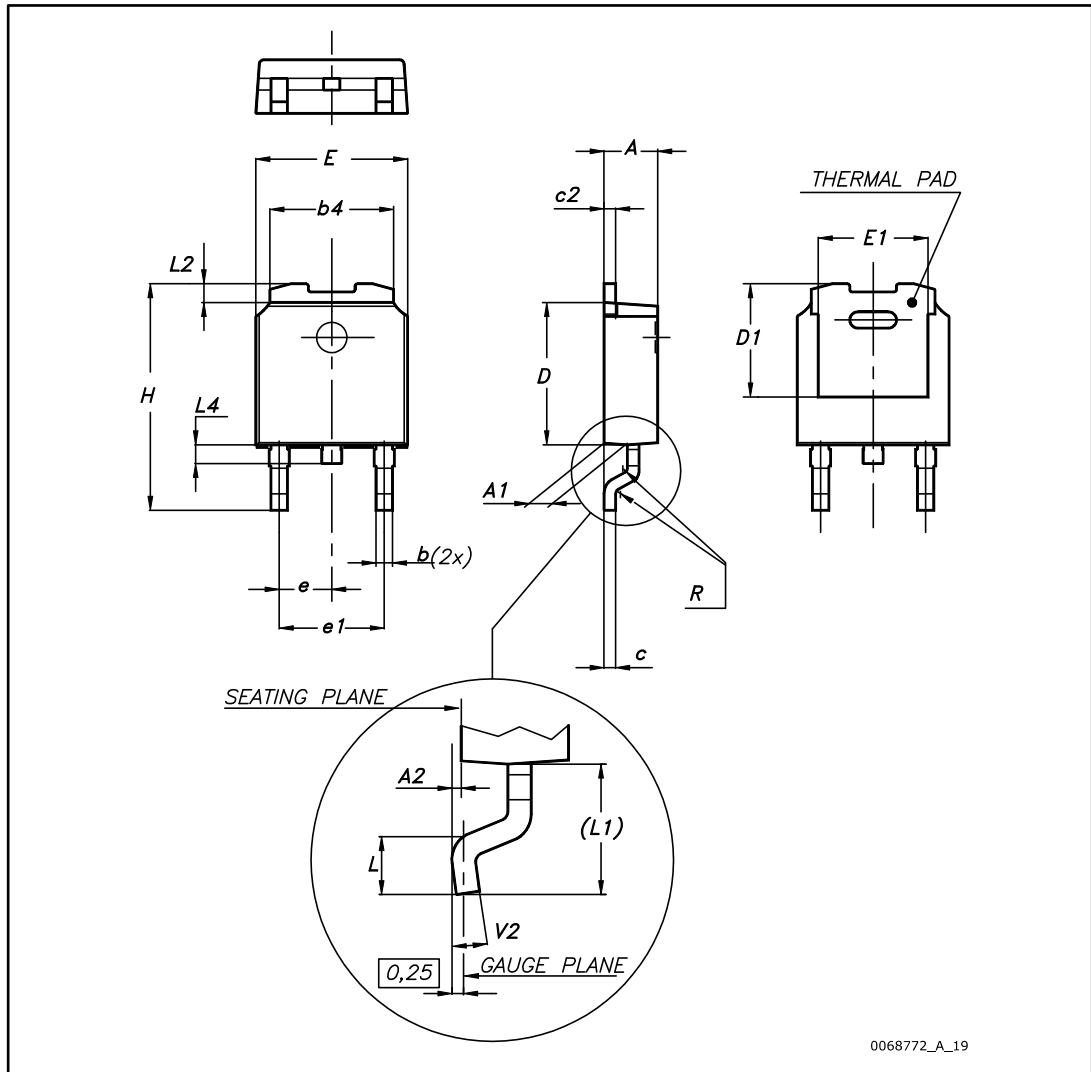
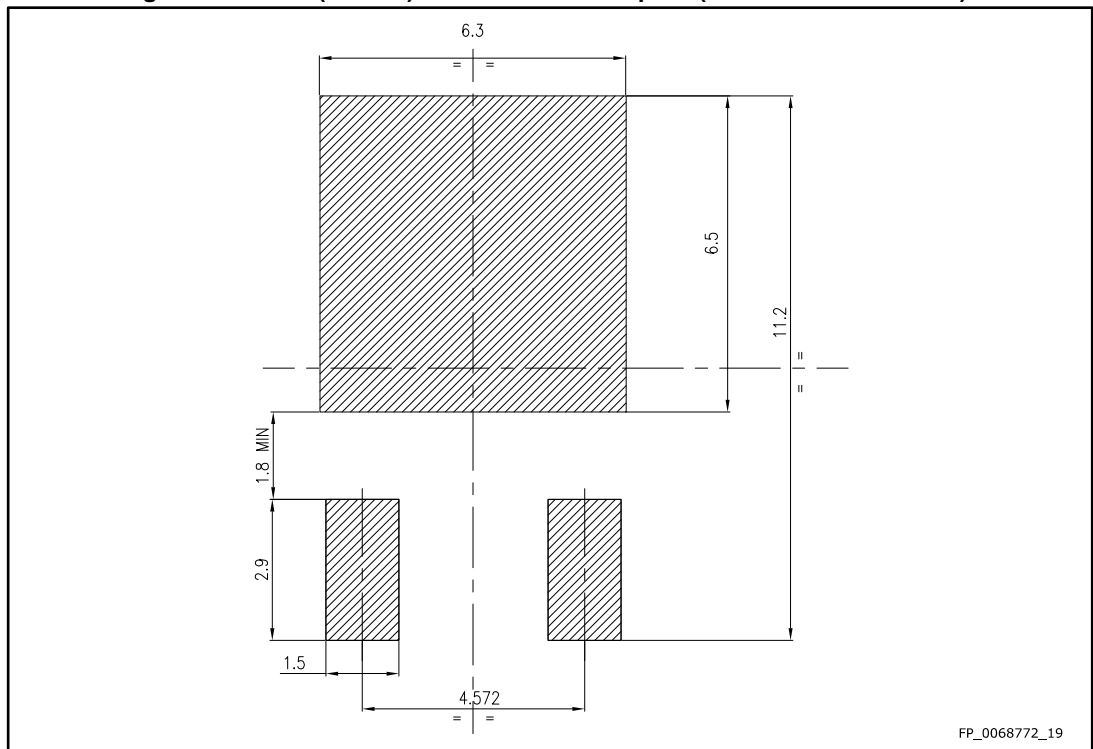


Table 9: DPAK (TO-252) type A mechanical data

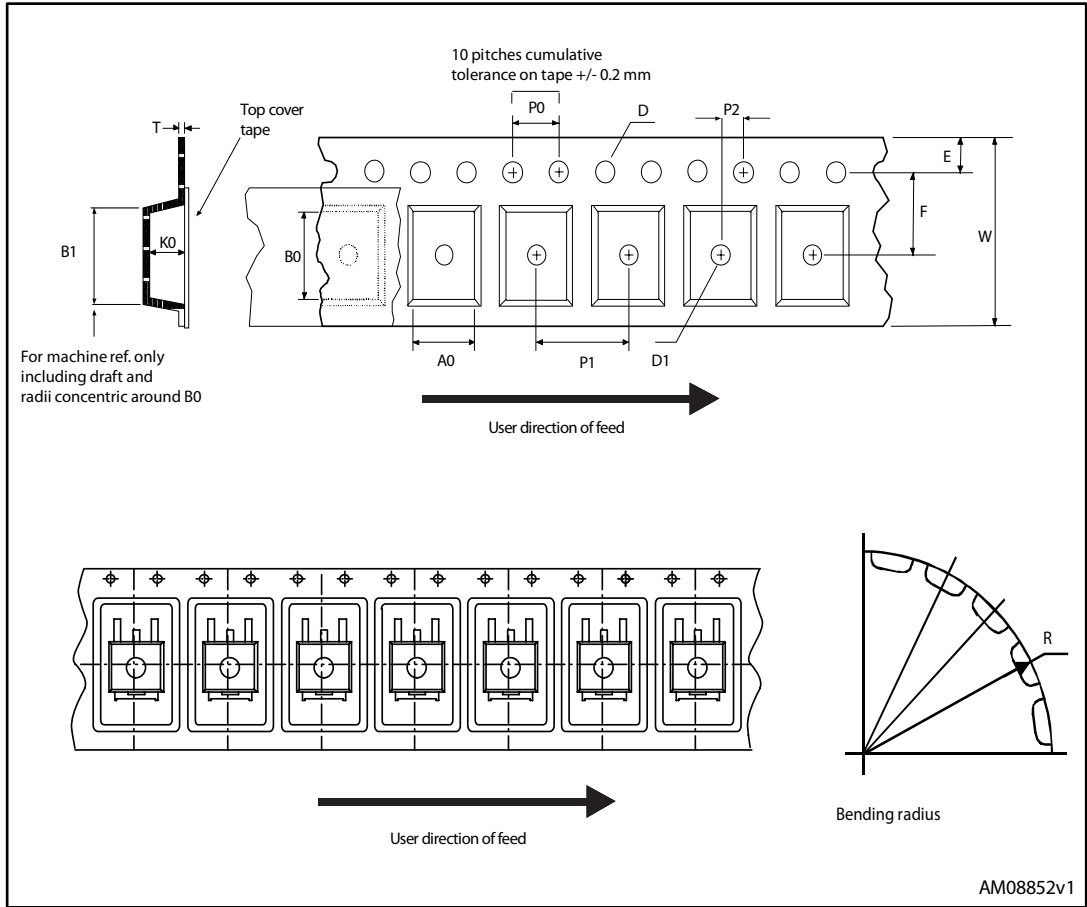
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) recommended footprint (dimensions are in mm)



### 4.2 DPAK (TO-252) packing information

Figure 21: DPAK (TO-252) tape outline





## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
10-Jun-2015	1	First release.

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