Document Title

2Mx16 bit Synchronous Burst Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft - Design target	September 02, 2004	Preliminary
0.1	Revised - Corrected the name of 9th row of balls on the pakage to 'J' from 'I' on page.2 and page.42	November 01, 2004	Preliminary
1.0	Finalize	April 06, 2005	Final

2M x 16 bit Synchronous Burst Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 2M x16 bit
- Power Supply Voltage: 1.7~2.0V
- Three State Outputs
- Supports MRS (Mode Register Set)
- MRS control - Software Control
- Supports Driver Strength Optimization for system environment
- Supports Async. 4-Page Read / Async. Write Mode
- Supports Sync. Burst Read / Async. Write Mode
  (Address Latch Type and Low ADV Type)
- Supports Sync. Burst Read / Sync. Burst Write Mode
  - Supports 4 word / 8 word / 16 word burst Length
  - Supports Linear(Wrap) Burst type
  - Latency support : Latency 5 @ 66MHz(tCD 10ns)
    Latency 4 @ 54MHz(tCD 10ns)
  - Supports Burst Read Suspend
  - Supports Burst Write Data Masking by /UB & /LB control
  - Supports WAIT function to indicate data availability.
- Max. Burst Clock Frequency : 66MHz
- Package Type : 54 FBGA 6.00 x 8.00

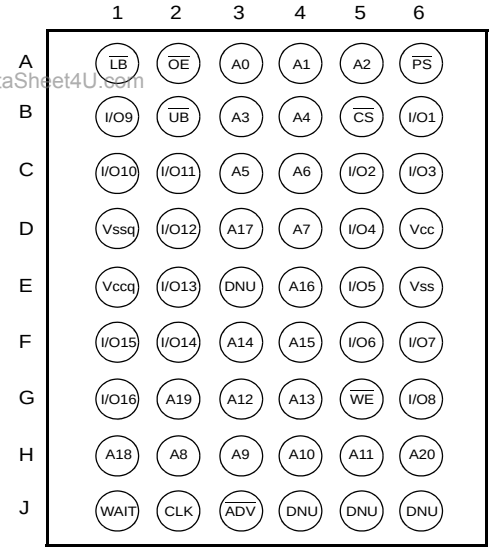
GENERAL DESCRIPTION

The world is moving into the mobile multi-media era and therefore the mobile handsets need much bigger memory capacity to handle the multi-media data. SAMSUNG's UtRAM products are designed to meet all the request from the various customers who want to cope with the fast growing mobile market. UtRAM is the perfect solution for the mobile market with its low cost, high density and high performance feature. K1B3216BDD is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports the traditional SRAM like asynchronous bus operation (asynchronous page read and asynchronous write), the NOR flash like synchronous bus operation (synchronous burst read and asynchronous write) and the fully synchronous bus operation (synchronous burst read and synchronous burst write). These three bus operation modes are defined through the mode register setting. The optimization of output driver strength is possible through the mode register setting to adjust for the different data loadings. Through this driver strength optimization, the device can minimize the noise generated on the data bus during read operation.

Table 1. PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Clock Freq. (Max)	Async. Speed (tAA)	Power Dissipation		PKG Type
					Standby (I_{SB1}, Max.)	Operating (I_{CC2}, Max.)	
K1B3216BDD-I	Industrial(-40~85°C)	1.7~2.0V	66MHz	70ns	100uA	35mA	54 FBGA 6.00 x 8.00

Fig.1 PIN DESCRIPTION



54-FBGA - 6.00 x 8.00 Top View (Ball Down)

Table 2. PIN DESCRIPTION

Name	Function	Name	Function
CLK	Clock Input	V_{CC}	Power Supply
$\overline{ADV}$	Address Input Valid	V_{CCQ}	I/O Power Supply
$\overline{PS}$*	Power Save	V_{SS}	Ground
$\overline{CS}$	Chip Select	V_{SSQ}	I/O Ground
$\overline{OE}$	Output Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
$\overline{WE}$	Write Enable Input	$\overline{LB}$	Lower Byte($I/O_{1\sim8}$)
A_0~A_{20}	Address Inputs	$\overline{WAIT}$	Data Availability
I/O_1~I/O_{16}	Data Inputs/Outputs	DNU	Do Not Use

* $\overline{PS}$ must be tied to V_{CC}.

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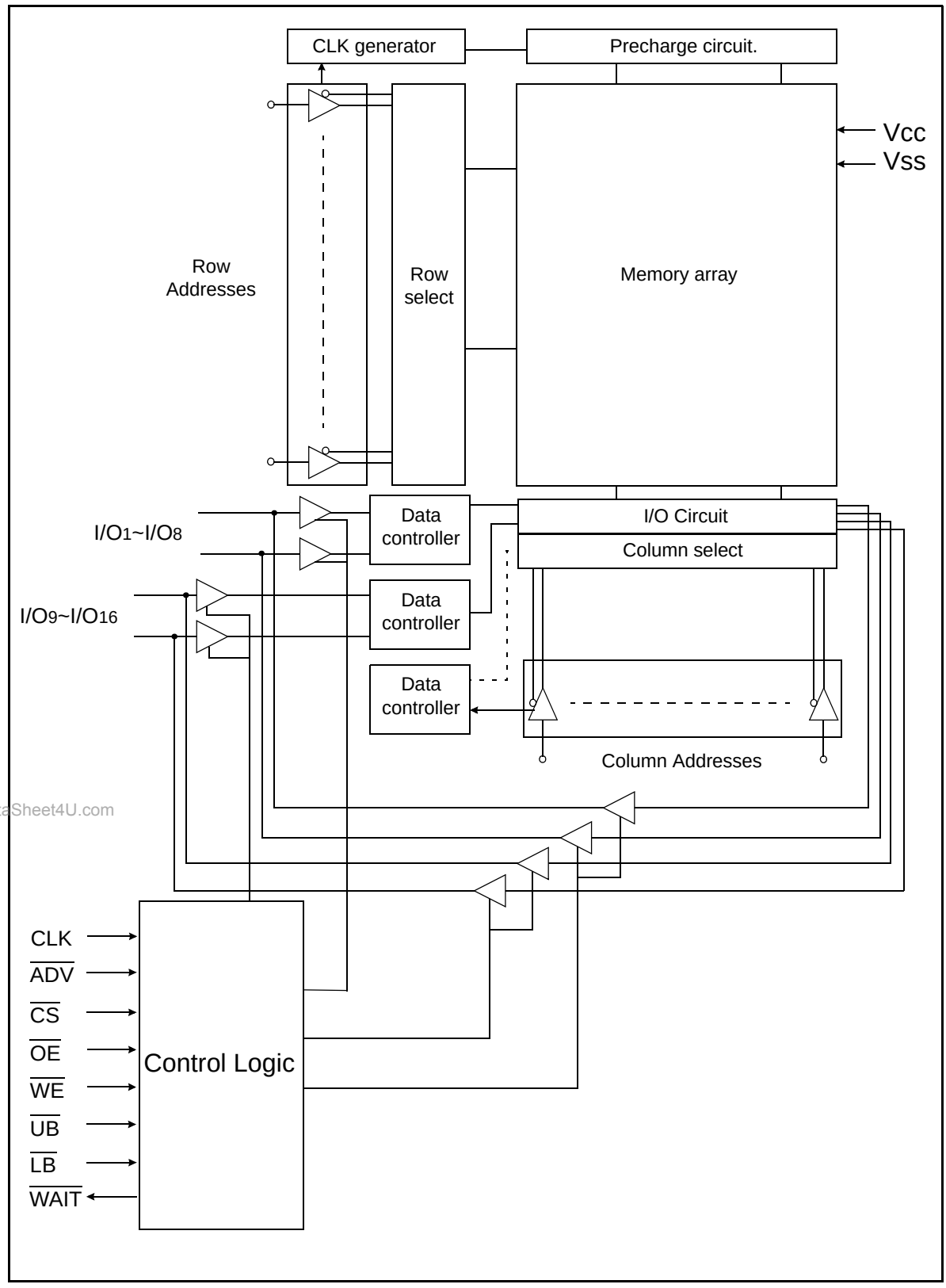
Fig.2 FUNCTIONAL BLOCK DIAGRAM



POWER UP SEQUENCE

After applying V_{CC} upto minimum operating voltage(1.7V), drive $\overline{CS}$ High. Then the device gets into the Power Up mode. Wait for minimum 200μs to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.

1. Apply power.
2. Maintain stable power(Vcc min.=1.7V) for a minimum 200μs with $\overline{CS}$ high.

Fig.3 POWER UP TIMING

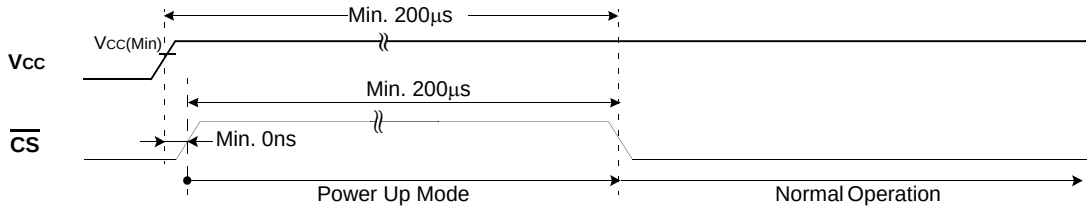
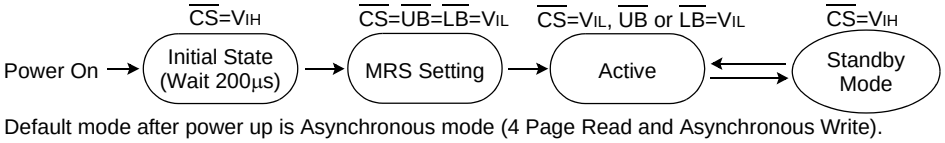


Fig.4 STANDBY MODE STATE MACHINES



Default mode after power up is Asynchronous mode (4 Page Read and Asynchronous Write).
But this default mode is not 100% guaranteed so MRS setting sequence is highly recommended after power up.

FUNCTIONAL DESCRIPTION

Table 3. ASYNCHRONOUS 4 PAGE READ & ASYNCHRONOUS WRITE MODE (A15/A14=0/0)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
L	H	H	X[1)]	X[1)]	High-Z	High-Z	Output Disabled	Active
L	X[1)]	X[1)]	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	H	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	L	L	L	Din	Din	Word Write	Active

1. X must be VIL or VIH.
2. In asynchronous mode, Clock and $\overline{ADV}$ are ignored.
3. /WAIT pin is High-Z in Asynchronous mode.

Table 4. SYNCHRONOUS BURST READ & ASYNCHRONOUS WRITE MODE(A15/A14=0/1)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	CLK	$\overline{ADV}$	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[1)]	X[1)]	Deselected	Standby
L	H	H	X[1)]	X[1)]	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	X[1)]	X[1)]	H	H	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	X[1)]	H	X[1)]	X[1)]	High-Z	High-Z	⌐	⌐¬⌐	Read Command	Active
L	L	H	L	H	Dout	High-Z	⌐	H	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	⌐	H	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	⌐	H	Word Read	Active
L	H	L	L	H	Din	High-Z	X[1)]	⌐ or ⌐¬	Lower Byte Write	Active
L	H	L	H	L	High-Z	Din	X[1)]	⌐ or ⌐¬	Upper Byte Write	Active
L	H	L	L	L	Din	Din	X[1)]	⌐ or ⌐¬	Word Write	Active

1. X must be VIL or VIH.
2. /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.

Table 5. SYNCHRONOUS BURST READ & SYNCHRONOUS WRITE MODE(A15/A14=1/0)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	CLK	$\overline{ADV}$	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	X[1]	X[1]	Deselected	Standby
L	H	H	X[1]	X[1]	High-Z	High-Z	X[1]	H	Output Disabled	Active
L	X[1]	X[1]	H	H	High-Z	High-Z	X[1]	H	Output Disabled	Active
L	X[1]	H	X[1]	X[1]	High-Z	High-Z	⌐¬	¬_¬	Read Command	Active
L	L	H	L	H	Dout	High-Z	⌐¬	H	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	⌐¬	H	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	⌐¬	H	Word Read	Active
L	X[1]	L or ⌐¬	X[1]	X[1]	High-Z	High-Z	⌐¬	¬_¬	Write Command	Active
L	H	X[1]	L	H	Din	High-Z	⌐¬	H	Lower Byte Write	Active
L	H	X[1]	H	L	High-Z	Din	⌐¬	H	Upper Byte Write	Active
L	H	X[1]	L	L	Din	Din	⌐¬	H	Word Write	Active

1. X must be VIL or VIH.
3. /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.
4. The last data written in the previous Asynchronous write mode is not valid. To make the lastly written data valid, then implement at least one dummy write cycle before change mode into synchronous burst read and synchronous burst write mode.
5. The data written in Synchronous burst write operation can be corrupted by the next Asynchronous write operation. So the transition from Synchronous burst write operation to Asynchronous write operation is prohibited.

MODE REGISTER SETTING OPERATION

The device has several modes : Asynchronous Page Read mode, Asynchronous Write mode, Synchronous Burst Read mode, Synchronous Burst Write mode, Standby mode. Mode Register Set(MRS) option also defines Burst Length, Burst Type, Wait Polarity and Latency Count at Synchronous Burst Read/Write mode.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operation modes of UtRAM. It programs Burst Length, Burst Type, Latency Count and various vendor specific options to make UtRAM useful for a variety of different applications. The default values of mode register are defined, therefore when the reserved address is input, the device runs at default modes. The mode register is written by driving $\overline{CS}$, $\overline{ADV}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$ to V_{IL} and $\overline{OE}$ to V_{IH} during valid address. The mode register is divided into various fields depending on the fields of functions. Burst Length field uses A5~A7, Burst Type uses A8, Latency Count uses A9~A11, Wait Polarity uses A13, Operation Mode uses A14~A15 and Driver Strength uses A16~A17.
Refer to the Table below for detailed Mode Register Setting. A18~A22 addresses are "Don't care" in Mode Register Setting.

Table 6. Mode Register Setting according to field of function

Address	A17~A16	A15~A14	A13	A12	A11~A9	A8	A7~A5	A4~A0
Function	DS	MS	WP	RFU	Latency	BT	BL	RFU

NOTE : DS(Driver Strength), MS(Mode Select), WP(Wait Polarity), Latency(Latency Count), BT(Burst Type), BL(Burst Length), RFU(Reserved for Future Use)

Table 7. Mode Register Set

Driver Strength			Mode Select		
A17	A16	DS	A15	A14	MS
0	0	Full Drive	0	0	Async. 4 Page Read / Async. Write
0	1	1/2 Drive	0	1	Sync. Burst Read / Async. Write
1	0	1/4 Drive	1	0	Sync. Burst Read / Sync. Burst Write

$\overline{WAIT}$ Polarity		RFU		Latency Count				Burst Type		Burst Length			
A13	WP	A12	RFU	A11	A10	A9	Latency	A8	BT	A7	A6	A5	BL
0	Low Enable	0	**Must**	0	0	0	3	0	Linear	0	1	0	4 word
1	High Enable	1	DNU*	0	0	1	4	1	DNU*	0	1	1	8 word
				0	1	0	5			1	0	0	16 word
				0	1	1	6			1	1	1	DNU*

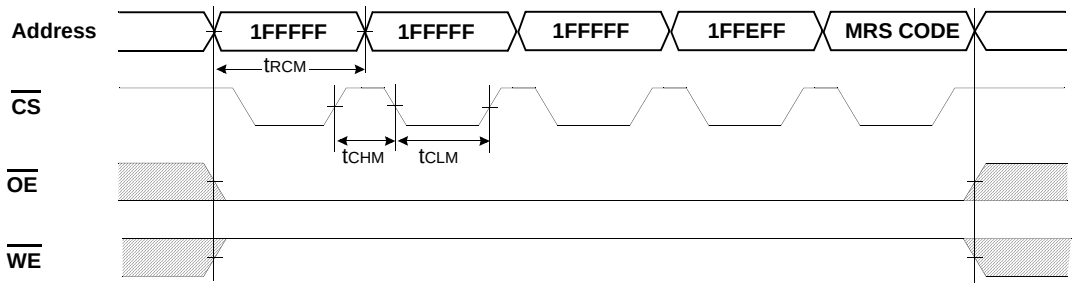
* DNU: Do Not Use.

NOTE :
* The address bits other than those listed in the table above are reserved.
  For example, Burst Length address bits(A7:A6:A5) have 4 sets of reserved bits like 0:0:0, 0:0:1, 1:0:1 and 1:1:0.
  If the reserved address bits are input, then the mode will be set into the default mode. Each field has its own default mode and these default modes are written in blue-bold in the table above.
* **A12 is a reserved bit for future use. A12 must be set as "0".**
* **Not all the mode settings are tested**. Per the mode settings to be tested.
* The last data written in the previous Asynchronous write mode is not valid. To make the lastly written data valid, then implement at least one dummy write cycle before change mode into synchronous burst read and synchronous burst write mode.
* The data written in Synchronous burst write operation can be corrupted by the next Asynchronous write operation. So the transition from Synchronous burst write operation to Asynchronous write operation is prohibited.

MODE REGISTER SETTING TIMING

This device supports software access control type mode register setting timing. This timing consists of 5 cycles of Read operation. Each cycle of Read Operation is normal asynchronous read operation. Clock and $\overline{ADV}$ are don't care and $\overline{WAIT}$ signal is High-Z. $\overline{CS}$ should be toggling between cycles. The address for 1st, 2nd and 3rd cycle should be 1FFFFF(h) and the address for 4th cycle should be 1FFEFF. The address for 5th cycle should be MRS code(Register setting values).

MRS TIMING WAVEFORM(Clock, $\overline{ADV}$, $\overline{UB}$, $\overline{LB}$ are Don't care, $\overline{WAIT}$=High-Z)



AC CHARACTERISTICS

Parameter	Sym-	Min	Max	Unit	Parameter	Sym-	Mi	Ma	Unit
Read Cycle time	tRCM	70	-	ns	$\overline{CS}$ Low pulse width	tCLM	60	-	ns
$\overline{CS}$ High pulse width	tCHM	10	-	ns					

ASYNCHRONOUS OPERATION

Asynchronous 4 Page Read Operation

Asynchronous normal read operation starts when $\overline{CS}$, $\overline{OE}$ and $\overline{UB}$ or $\overline{LB}$ are driven to V_{IL} under the valid address without toggling page addresses(A0, A1). If the page addresses(A0, A1) are toggled under the other valid address, the first data will be out with the normal read cycle time(tRC) and the second, the third and the fourth data will be out with the page cycle time(tPC). ($\overline{WE}$ should be driven to V_{IH} during the asynchronous (page) read operation)
Clock, $\overline{ADV}$, $\overline{WAIT}$ signals are ignored during the asynchronous (page) read operation.

Asynchronous Write Operation

Asynchronous write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are driven to V_{IL} under the valid address.($\overline{OE}$ should be driven to V_{IH} during the asynchronous write operation.) Clock, $\overline{ADV}$, $\overline{WAIT}$ signals are ignored during the asynchronous (page) read operation.

Asynchronous Write Operation in Synchronous Mode

A write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are driven to V_{IL} under the valid address. Clock input does not have any affect to the write operation($\overline{OE}$ should be driven to V_{IH} during write operation. $\overline{ADV}$ can be either toggling for address latch or held in V_{IL}). Clock, $\overline{ADV}$, $\overline{WAIT}$ signals are ignored during the asynchronous (page) read operation.

Fig.6 ASYNCHRONOUS 4-PAGE READ

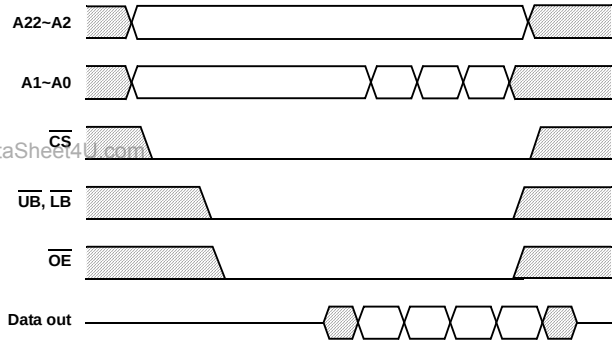
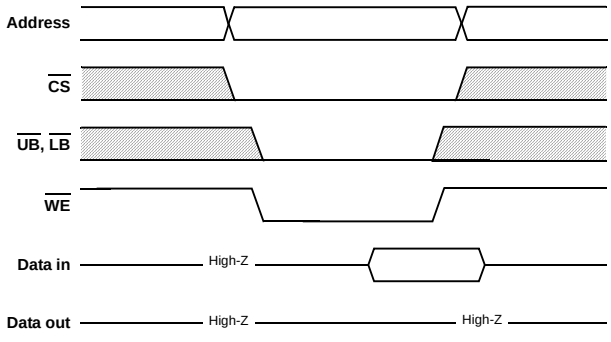


Fig.7 ASYNCHRONOUS WRITE



SYNCHRONOUS BURST OPERATION

Burst mode operations enable the system to get high performance read and write operation. The address to be accessed is latched on the rising edge of clock or $\overline{ADV}$(whichever occurs first). $\overline{CS}$ should be setup before the address latch. During this first clock rising edge, $\overline{WE}$ indicates whether the operation is going to be a Read($\overline{WE}$ High) or a Write($\overline{WE}$ Low).
For the optimized Burst Mode to each system, the system should determine how many clock cycles are required for the first data of each burst access(Latency Count), how many words the device outputs at an access(Burst Length) and which type of burst operation(Burst Type : Linear) is needed. The Wait Polarity should also be determined.(See Table "Mode Register Set")

Synchronous Burst Read Operation

The Synchronous Burst Read command is implemented when the clock rising is detected during the $\overline{ADV}$ low pulse. $\overline{ADV}$ and $\overline{CS}$ should be set up before the clock rising. During Read command, $\overline{WE}$ should be held in V_{IH}. The multiple clock risings(during low $\overline{ADV}$ period) are allowed but the burst operation starts from the first clock rising. The first data will be out with Latency count and tCD.

Synchronous Burst Write Operation

The Synchronous Burst Write command is implemented when the clock rising is detected during the $\overline{ADV}$ and $\overline{WE}$ low pulse. $\overline{ADV}$, $\overline{WE}$ and $\overline{CS}$ should be set up before the clock rising. The multiple clock risings(during low $\overline{ADV}$ period) are allowed but the burst operation starts from the first clock rising. The first data will be written in the Latency clock with tDS.

Fig.8 SYNCHRONOUS BURST READ(Latency 5, BL 4, WP : Low Enable)

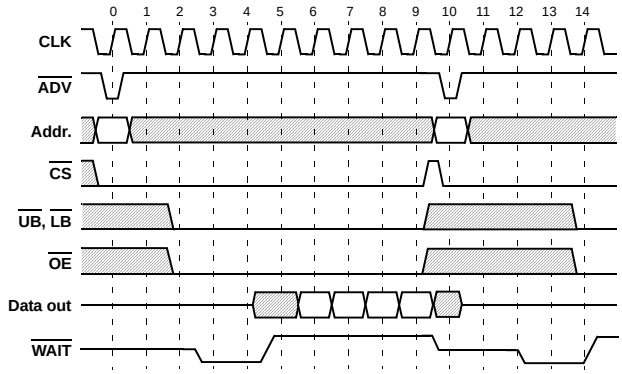
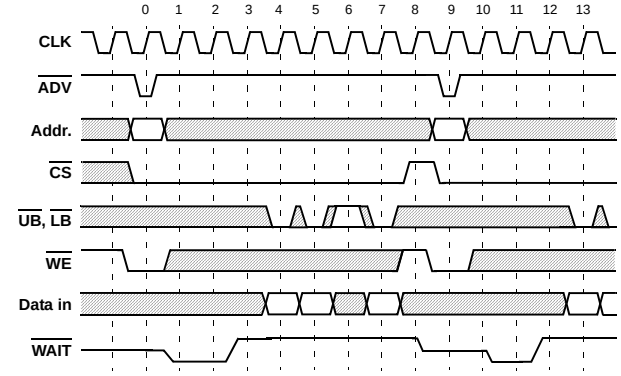


Fig.9 SYNCHRONOUS BURST WRITE(Latency 5, BL 4, WP : Low Enable)



SYNCHRONOUS BURST OPERATION TERMINOLOGY

Clock(CLK)

The clock input is used as the reference for synchronous burst read and write operation of UtRAM. The synchronous burst read and write operation is synchronized to the rising edge of the clock. The clock transitions must swing between V_{IL} and V_{IH}.

Latency Count

The Latency Count configuration tells the device how many clocks must elapse from the burst command before the first data should be available on its data pins. This value depends on the input clock frequency.
The supported Latency Count is as follows.

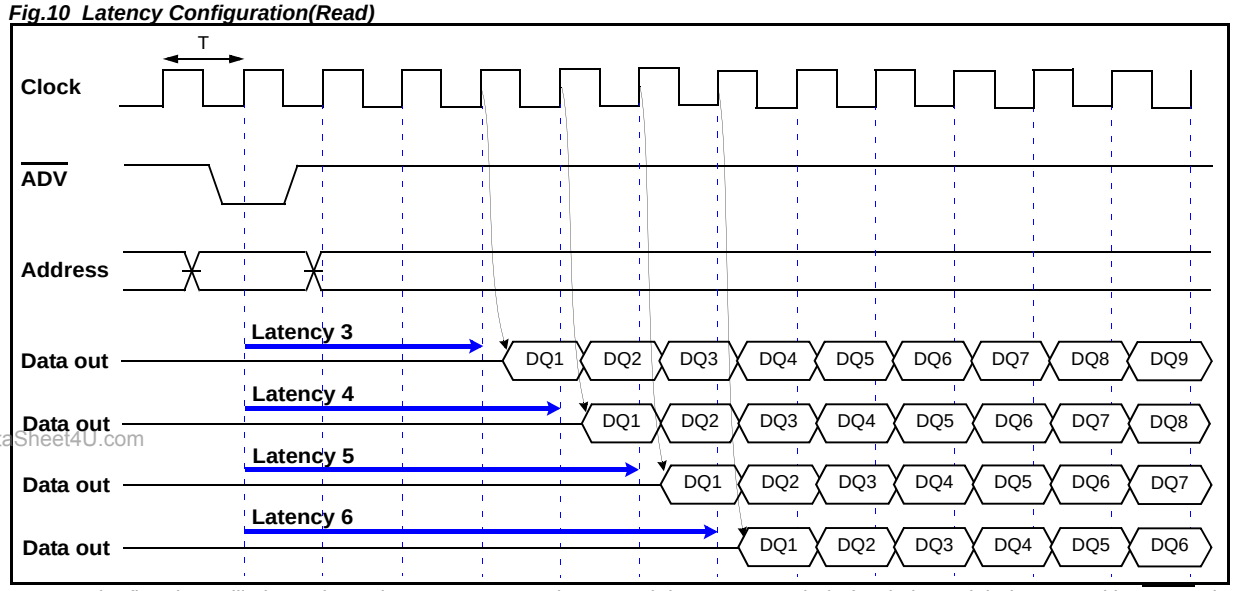
Table 8. Latency Count support : 3, 4, 5

Clock Frequency	Upto 66MHz	Upto 54MHz	Upto 40MHz
Latency Count	5	4	3

Table 9. Number of Clocks for 1st Data

Set Latency	Latency 3	Latency 4	Latency 5
# of Clocks for 1st data(Read)	4	5	6
# of Clocks for 1st data(Write)	2	3	4

Fig.10 Latency Configuration(Read)



NOTE : The first data will always keep the Latency. From the second data, some period of wait time might be caused by $\overline{WAIT}$ pin.

Burst Length

Burst Length identifies how many data the device outputs at an access. The device supports 4 word, 8 word and 16 word burst read or write. The first data will be out with the set Latency + tCD. From the second data, the data will be out with tCD from each clock.

Burst Stop

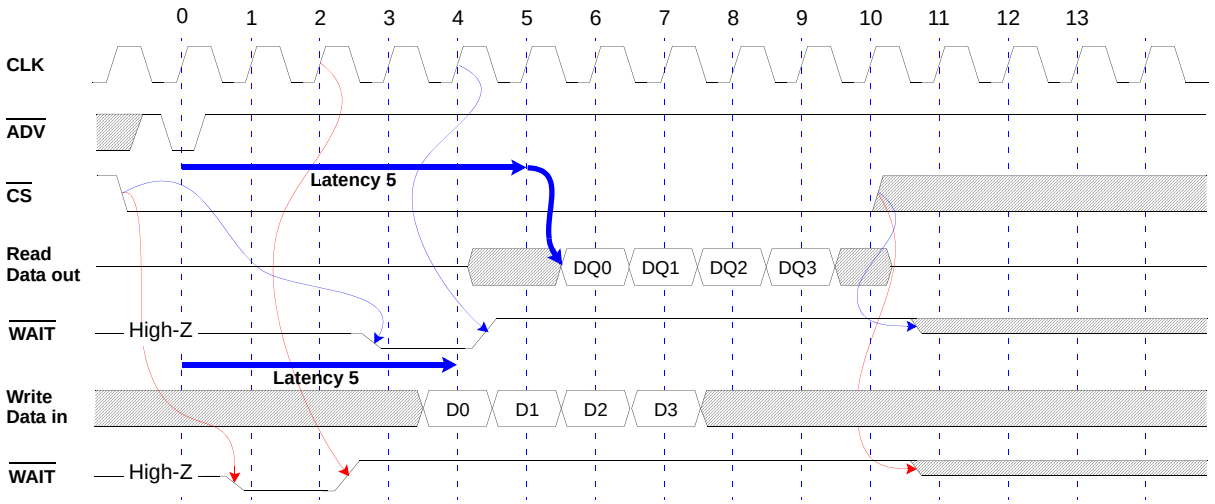
Burst stop is used when the system wants to stop burst operation on special purpose. If driving $\overline{CS}$ to V_{IH} during the burst read operation, then the burst operation will be stopped. During the burst read operation, the new burst operation can not be issued. The new burst operation can be issued only after the previous burst operation is finished.
The burst stop feature is very useful because it enables the user to utilize the un-supported burst length such as 1 burst or 2 burst which accounts for big portion in usage for the mobile handset application environment.

SYNCHRONOUS BURST OPERATION TERMINOLOGY

WAIT Control(WAIT)

The WAIT signal is the device's output signal which indicates to the host system when the device's data-out or data-in is valid.
To be compatible with the Flash interfaces of various microprocessor types, the WAIT polarity(WP) can be configured. The polarity can be programmed to be either low enable or high enable.
For the timing of WAIT signal, the WAIT signal should be set active one clock prior to the data regardless of Read or Write cycle.

Fig.11 WAIT Control and Read/Write Latency Control(LATENCY : 5, Burst Length : 4, WP : Low Enable)



Burst Type

The device supports Linear type burst sequence. Linear type burst sequentially increments the burst address from the starting address. The detailed Linear type burst address sequence is shown in burst sequence table.

Table 10. Burst Sequence

Start	Burst Address Sequence(Decimal)		
Length	4 word Burst	8 word Burst	16 word Burst
0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15
1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0
2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1
3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2
4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3
5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4
6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5
7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6
~			~
14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13
15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14

Table 11. PRODUCT LIST

Industrial Temperature Products (-40~85°C)	
Part Name	**Function**
K1B3216BDD	1.8V, 70ns, 66MHz

Table 12. ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Power supply voltage relative to Vss	V_{CC}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

Table 13. RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	1.7	1.85	2.0	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	0.8 x V_{CC}	-	V_{CC}+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.3	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+1.0V in case of pulse width ≤3ns.
3. Undershoot: -1.0V in case of pulse width ≤3ns.
4. Overshoot and undershoot are sampled, not 100% tested.

Table 14. CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

Table 15. DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}	-1	-	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to V_{CC}	-1	-	1	μA
Average Operating Current	I_{CC2}	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}	-	-	35	mA
Output Low Voltage	V_{OL}	I_{OL}=0.1mA	-	-	0.2	V
Output High Voltage	V_{OH}	I_{OH}=-0.1mA	1.4	-	-	V
Standby Current(CMOS)	I_{SB1}[1)]	$\overline{CS}$≥V_{CC}-0.2V, Other inputs=Vss to V_{CC}	-	-	100	μA

1. Standby mode is supposed to be set up after at least one active operation.
I_{SB1} is measured after 60ms from the time when standby mode is set up.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CC}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CC}
Output load: C_L=30pF

Figure 12. AC Output Load Circuit

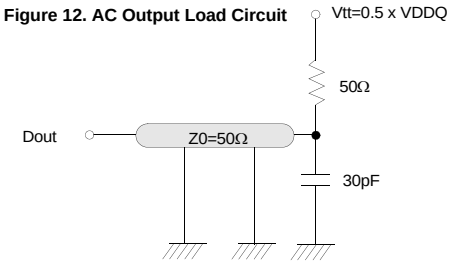


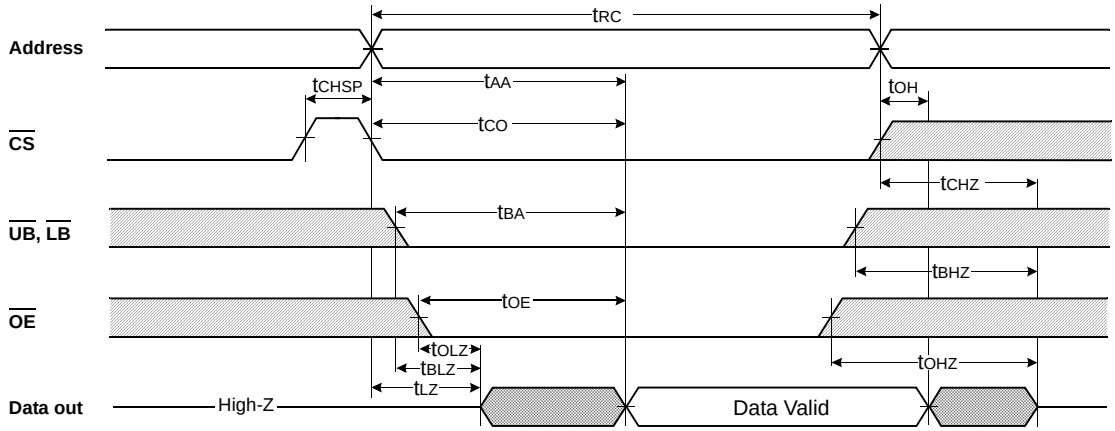
Table 16. ASYNCHRONOUS AC CHARACTERISTICS *(V_{CC}=1.7~2.0V, T_A=-40 to 85℃)*

Parameter List		Symbol	Speed		Units
			Min	Max	
Async. (Page) Read	$\overline{CS}$ High pulse width	t_{CSHP}	10	-	ns
	Read Cycle Time	t_{RC}	70	-	ns
	Page Read Cycle Time	t_{PC}	25	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Page Access Time	t_{PA}	-	20	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	35	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	5	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{CHZ}	0	12	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	12	ns
	Output Disable to High-Z Output	t_{OHZ}	0	12	ns
	Output Hold	t_{OH}	3	-	ns
Async. Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	$\overline{ADV}$ Minimum Low Pulse Width	t_{ADV}	7	-	ns
	Address Set-up Time to Beginning of Write	t_{AS}	0	-	ns
	Address Set-up Time to $\overline{ADV}$ Falling	$t_{AS(A)}$	0	-	ns
	Address Hold Time from $\overline{ADV}$ Rising	$t_{AH(A)}$	7	-	ns
	$\overline{CS}$ Setup Time to $\overline{ADV}$ Rising	$t_{CSS(A)}$	10	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	ns
	$\overline{WE}$ High Pulse Width	t_{WHP}	5 ns	Latency-1 clock	-
	Write Recovery Time	t_{WR}	0	-	ns
	$\overline{WE}$ Low to Read Latency	t_{WLRL}	1	-	clock
	Data to Write Time Overlap	t_{DW}	30	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns

1. tWC(min)=90ns or t_{WP}(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS READ TIMING WAVEFORM

Fig.13 TIMING WAVEFORM OF ASYNCHRONOUS READ CYCLE *($\overline{WE}$=V_{IH}, $\overline{WAIT}$=High-Z)*



(ASYNCHRONOUS READ CYCLE)

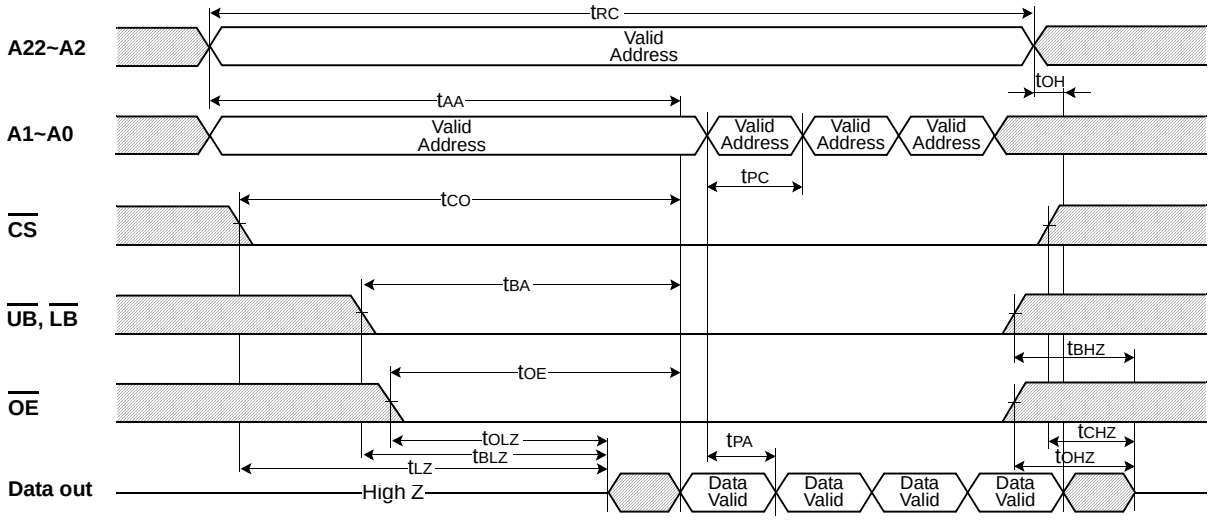
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. In asynchronous read cycle, Clock, $\overline{ADV}$ and $\overline{WAIT}$ signals are ignored.

Table 17. ASYNCHRONOUS READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{RC}	70	-	ns	t_{OLZ}	5	-	ns
t_{AA}	-	70	ns	t_{BLZ}	5	-	ns
t_{CO}	-	70	ns	t_{LZ}	10	-	ns
t_{BA}	-	35	ns	t_{CHZ}	0	12	ns
t_{OE}	-	35	ns	t_{BHZ}	0	12	ns
t_{OH}	3	-	ns	t_{OHZ}	0	12	ns
t_{CSHP}	10	-	ns				

ASYNCHRONOUS READ TIMING WAVEFORM

Fig.14 TIMING WAVEFORM OF PAGE READ CYCLE *($\overline{WE}$=V_{IH}, $\overline{WAIT}$=High-Z)*



(ASYNCHRONOUS 4 PAGE READ CYCLE)

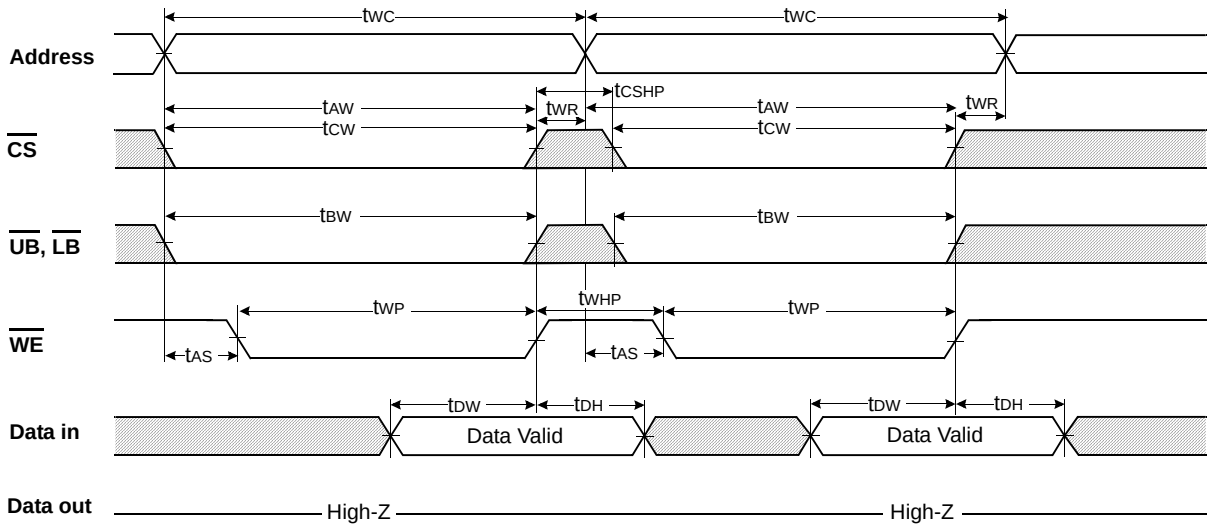
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. In asynchronous 4 page read cycle, Clock, $\overline{ADV}$ and $\overline{WAIT}$ signals are ignored.

Table 18. ASYNCHRONOUS PAGE READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{RC}	70	-	ns	t_{OH}	3	-	ns
t_{AA}	-	70	ns	t_{OLZ}	5	-	ns
t_{PC}	25	-	ns	t_{BLZ}	5	-	ns
t_{PA}	-	20	ns	t_{LZ}	10	-	ns
t_{CO}	-	70	ns	t_{CHZ}	0	12	ns
t_{BA}	-	35	ns	t_{BHZ}	0	12	ns
t_{OE}	-	35	ns	t_{OHZ}	0	12	ns

ASYNCHRONOUS WRITE TIMING WAVEFORM

Fig.15 TIMING WAVEFORM OF WRITE CYCLE(1) *($\overline{OE}$=V_{IH}, $\overline{WAIT}$=High-Z, $\overline{WE}$ Controlled)*



(ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ Controlled)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. In asynchronous write cycle, Clock, $\overline{ADV}$ and $\overline{WAIT}$ signals are ignored.
6. Condition for continuous write operation over 50 times : t_{WP}(min)=70ns

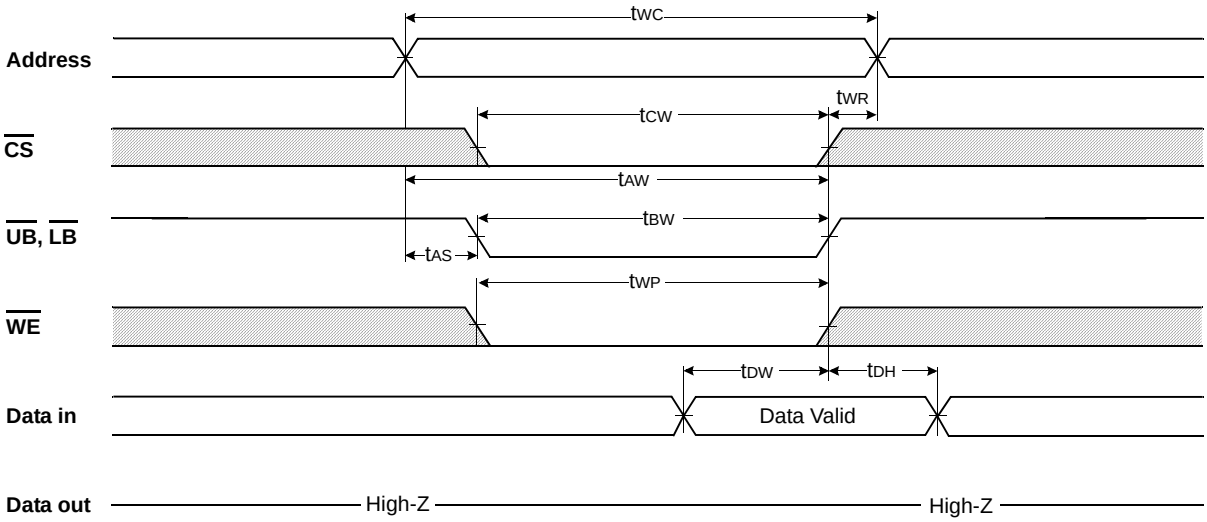
Table 19. ASYNCHRONOUS WRITE AC CHARACTERISTICS *($\overline{WE}$ Controlled)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{WR}	0	-	ns
t_{AW}	60	-	ns	t_{DW}	30	-	ns
t_{BW}	60	-	ns	t_{DH}	0	-	ns
t_{WP}	55[1)]	-	ns	t_{CSHP}	10	-	ns

1. t_{WP}(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM

Fig.16 TIMING WAVEFORM OF WRITE CYCLE(2) *($\overline{OE}$=V_{IH}, $\overline{WAIT}$=High-Z, $\overline{UB}$ & $\overline{LB}$ Controlled)*



(ASYNCHRONOUS WRITE CYCLE - $\overline{UB}$ & $\overline{LB}$ Controlled)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. In asynchronous write cycle, Clock, $\overline{ADV}$ and $\overline{WAIT}$ signals are ignored.

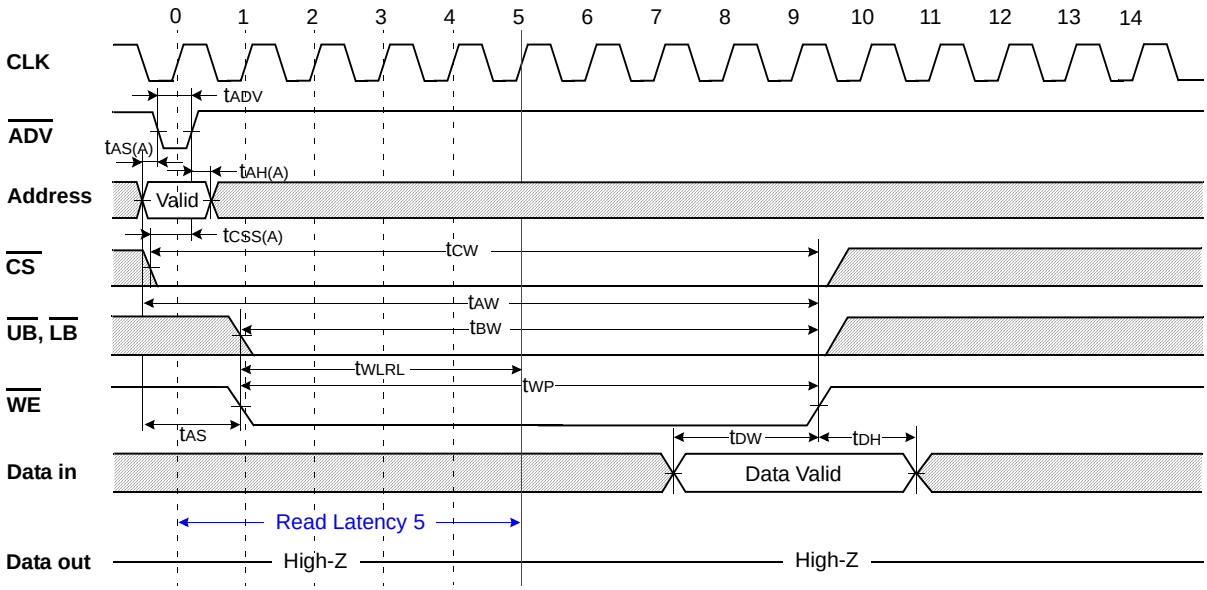
Table 20. ASYNCHRONOUS WRITE AC CHARACTERISTICS *($\overline{UB}$ & $\overline{LB}$ Controlled)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{WR}	0	-	ns
t_{AW}	60	-	ns	t_{DW}	30	-	ns
t_{BW}	60	-	ns	t_{DH}	0	-	ns
t_{WP}	55[1)]	-	ns				

1. tWC(min)=90ns or tWP(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.17 TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type) *($\overline{OE}$=V_{IH}, $\overline{WAIT}$=High-Z, $\overline{WE}$ Controlled)*



(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ Controlled)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for word operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the address valid to the end of write. In this address latch type write timing, t_{WC} is same as t_{AW}.
3. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
4. t_{BW} is measured from the $\overline{UB}$ and $\overline{LB}$ going low to the end of write.
5. Clock input does not have any affect to the write operation if the parameter tWLRL is met.

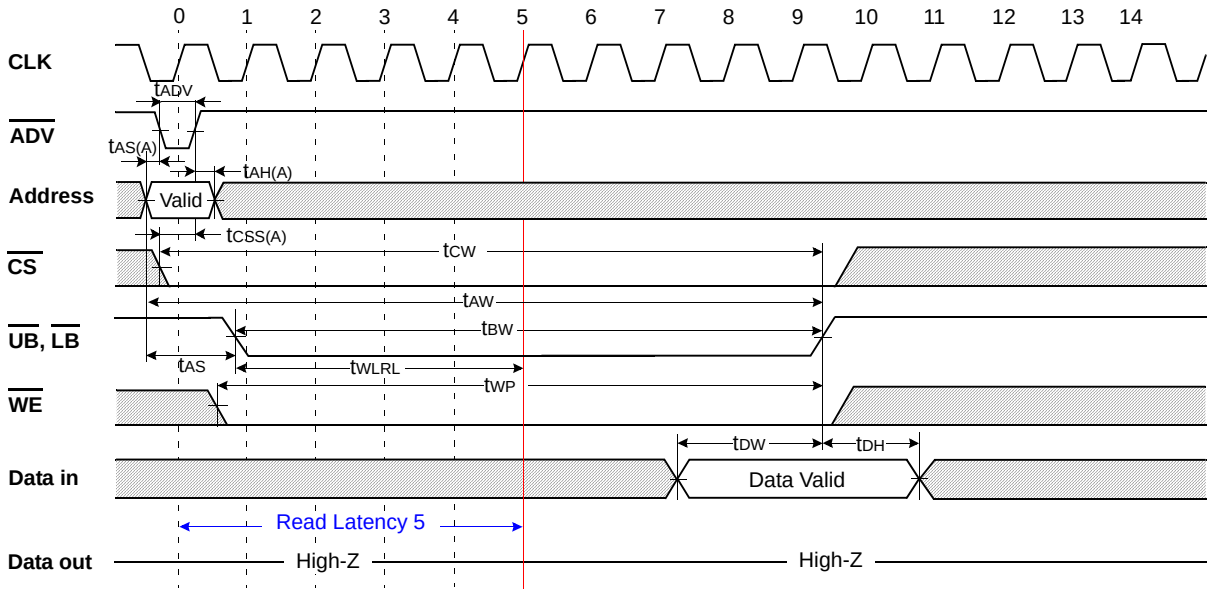
Table 21. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS *(Address Latch Type, $\overline{WE}$ Controlled)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{ADV}	7	-	ns	t_{BW}	60	-	ns
$t_{AS(A)}$	0	-	ns	t_{WP}	55[1)]	-	ns
$t_{AH(A)}$	7	-	ns	t_{WLRL}	1	-	clock
$t_{CSS(A)}$	10	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{DW}	30	-	ns
t_{AW}	60	-	ns	t_{DH}	0	-	ns

1. tWC(min)=90ns or t_{WP}(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.18 TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type) *($\overline{OE}$=V_{IH}, $\overline{WAIT}$=High-Z, $\overline{UB}$ & $\overline{LB}$ Controlled)*



(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{UB}$ & $\overline{LB}$ Controlled)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for word operation. A write ends at the earliest transition when $\overline{CS}$ goes or and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the address valid to the end of write. In this address latch type write timing, t_{WC} is same as t_{AW}.
3. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
4. t_{BW} is measured from the $\overline{UB}$ and $\overline{LB}$ going low to the end of write.
5. Clock input does not have any affect to the write operation if the parameter tWLRL is met.

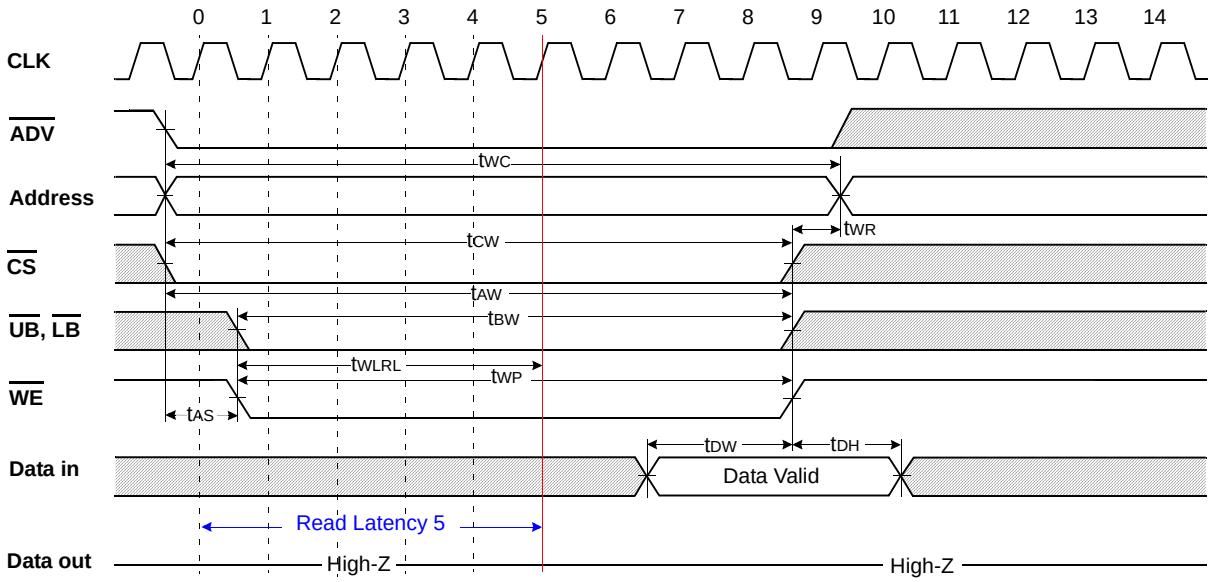
Table 22. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS *(Address Latch Type, $\overline{UB}$ & $\overline{LB}$ Controlled)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{ADV}	7	-	ns	t_{BW}	60	-	ns
$t_{AS(A)}$	0	-	ns	t_{WP}	55[1)]	-	ns
$t_{AH(A)}$	7	-	ns	t_{WLRL}	1	-	clock
$t_{CSS(A)}$	10	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{DW}	30	-	ns
t_{AW}	60	-	ns	t_{DH}	0	-	ns

1. tWC(min)=90ns or t_{WP}(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.19 TIMING WAVEFORM OF WRITE CYCLE(Low ADV Type) *(OE=VIH, WAIT=High-Z, WE Controlled)*



(LOW ADV TYPE WRITE CYCLE - WE Controlled)

1. A write occurs during the overlap(tWP) of low CS and low WE. A write begins when CS goes low and WE goes low with asserting UB or LB for single byte operation or simultaneously asserting UB and LB for double byte operation. A write ends at the earliest transition when CS goes high or WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS going low to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends with CS or WE going high.
5. Clock input does not have any affect to the write operation if the parameter tWLRL is met.

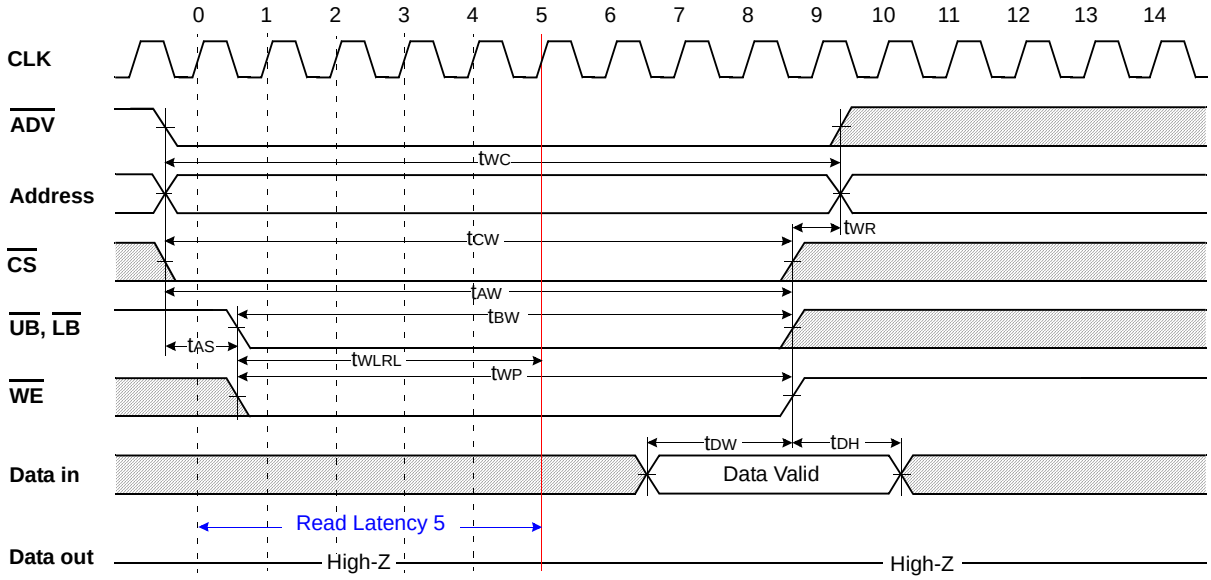
Table 23. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS *(Low ADV Type, WE Controlled)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tWC	70	-	ns	tWLRL	1	-	clock
tCW	60	-	ns	tAS	0	-	ns
tAW	60	-	ns	tWR	0	-	ns
tBW	60	-	ns	tDW	30	-	ns
tWP	55[1)]	-	ns	tDH	0	-	ns

1. tWC(min)=90ns or tWP(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.20 TIMING WAVEFORM OF WRITE CYCLE(Low ADV Type) *(OE=VIH, WAIT=High-Z, UB & LB Controlled)*



(LOW ADV TYPE WRITE CYCLE - UB & LB Controlled)

1. A write occurs during the overlap(tWP) of low CS and low WE. A write begins when CS goes low and WE goes low with asserting UB or LB for single byte operation or simultaneously asserting UB and LB for double byte operation. A write ends at the earliest transition when CS goes high or WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS going low to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends with CS or WE going high.
5. Clock input does not have any affect to the write operation if the parameter tWLRL is met.

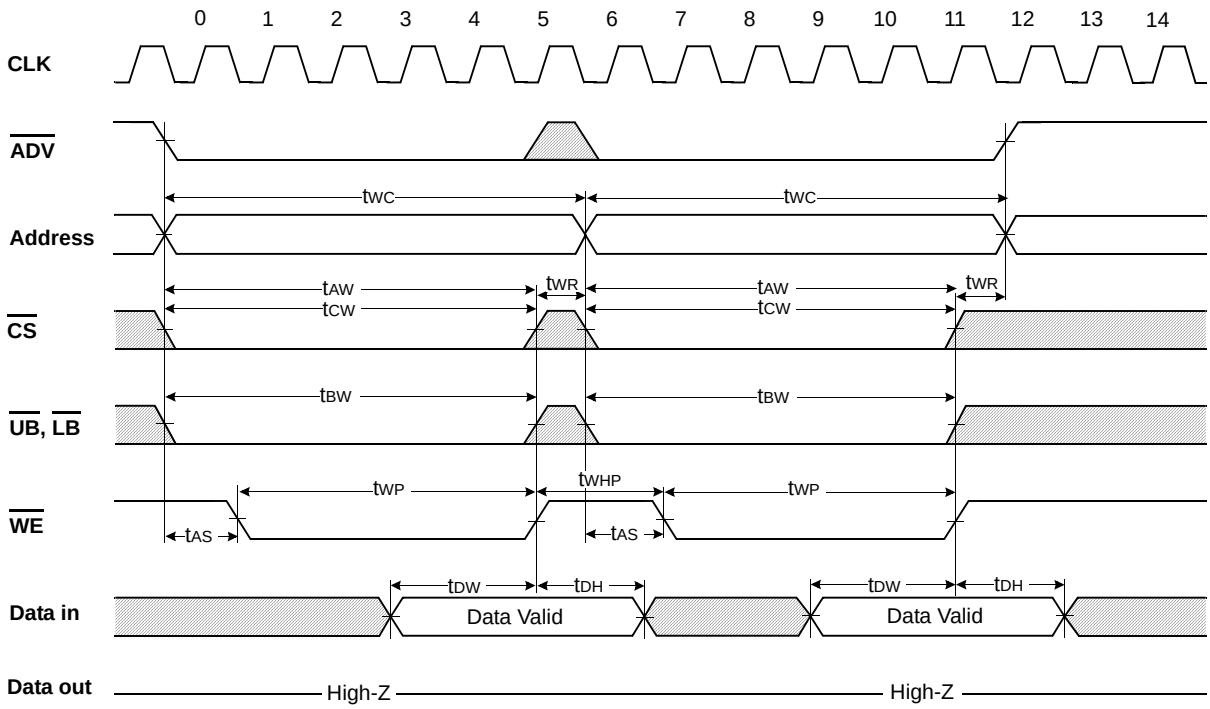
Table 24. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS *(Low ADV Type, UB & LB Controlled)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tWC	70	-	ns	tWLRL	1	-	clock
tCW	60	-	ns	tAS	0	-	ns
tAW	60	-	ns	tWR	0	-	ns
tBW	60	-	ns	tDW	30	-	ns
tWP	55[1)]	-	ns	tDH	0	-	ns

1. tWC(min)=90ns or tWP(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.21 TIMING WAVEFORM OF MULTIPLE WRITE CYCLE(Low $\overline{ADV}$ Type) *($\overline{OE}$=V_{IH}, $\overline{WAIT}$=High-Z, $\overline{WE}$ Controlled)*



(LOW $\overline{ADV}$ TYPE MULTIPLE WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. Clock input does not have any affect to the asynchronous multiple write operation if t_{WHP} is shorter than (Read Latency - 1) clock duration.
6. t_{WP}(min)=70ns for continuous write operation over 50 times.

Table 25. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS *(Low $\overline{ADV}$ Type Multiple Write, $\overline{WE}$ Controlled)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{WHP}	5ns	Latency-1 clock	-
t_{CW}	60	-	ns	t_{AS}	0	-	ns
t_{AW}	60	-	ns	t_{WR}	0	-	ns
t_{BW}	60	-	ns	t_{DW}	30	-	ns
t_{WP}	55[1)]	-	ns	t_{DH}	0	-	ns

1. tWC(min)=90ns or t_{WP}(min)=70ns for continuous write operation over 50 times.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CC}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CC}
Output load: C_L=30pF

Figure 22. AC Output Load Circuit

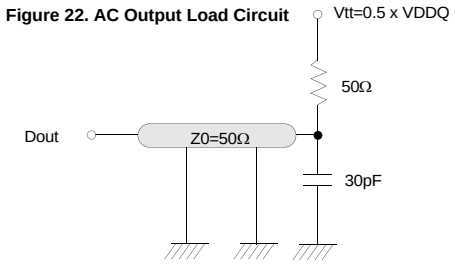


Table 26. SYNCHRONOUS AC CHARACTERISTICS *(V_{CC}=1.7~2.0V, T_A=-40 to 85℃, Maximum Main Clock Frequency=66MHz)*

Parameter List		Symbol	Speed		Units
			Min	Max	
Burst Operation (Common)	Clock Cycle Time	T	15	200	ns
	Burst Cycle Time	t_{BC}	-	2500	ns
	Address Set-up Time to $\overline{ADV}$ Falling(Burst)	$t_{AS(B)}$	0	-	ns
	Address Hold Time from $\overline{ADV}$ Rising(Burst)	$t_{AH(B)}$	7	-	ns
	$\overline{ADV}$ Setup Time	t_{ADVS}	5	-	ns
	$\overline{ADV}$ Hold Time	t_{ADVH}	7	-	ns
	$\overline{CS}$ Setup Time to Clock Rising(Burst)	$t_{CSS(B)}$	5	-	ns
	Burst End to New $\overline{ADV}$ Falling	t_{BEADV}	7	-	ns
	Burst Stop to New $\overline{ADV}$ Falling	t_{BSADV}	12	-	ns
	$\overline{CS}$ Low Hold Time from Clock	t_{CSLH}	7	-	ns
	$\overline{CS}$ High Pulse Width	t_{CSHP}	5	-	ns
	$\overline{ADV}$ High Pulse Width	t_{ADHP}	5	-	ns
	Chip Select to $\overline{WAIT}$ Low	t_{WL}	-	10	ns
	$\overline{ADV}$ Falling to $\overline{WAIT}$ Low	t_{AWL}	-	10	ns
	Clock to $\overline{WAIT}$ High	t_{WH}	-	12	ns
	Chip De-select to $\overline{WAIT}$ High-Z	t_{WZ}	-	12	ns
Burst Read Operation	$\overline{UB}$, $\overline{LB}$ Enable to End of Latency Clock	t_{BEL}	1	-	Clock
	Output Enable to End of Latency Clock	t_{OEL}	1	-	Clock
	$\overline{UB}$, $\overline{LB}$ Valid to Low-Z Output	t_{BLZ}	5	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Latency Clock Rising Edge to Data Output	t_{CD}	-	10	ns
	Output Hold	t_{OH}	3	-	ns
	Burst End Clock to Output High-Z	t_{HZ}	-	12	ns
	Chip De-select to Output High-Z	t_{CHZ}	-	12	ns
	Output Disable to Output High-Z	t_{OHZ}	-	12	ns
	$\overline{UB}$, $\overline{LB}$ Disable to Output High-Z	t_{BHZ}	-	12	ns
Burst Write Operation	$\overline{WE}$ Set-up Time to Command Clock	t_{WES}	5	-	ns
	$\overline{WE}$ Hold Time from Command Clock	t_{WEH}	5	-	ns
	$\overline{WE}$ High Pulse Width	t_{WHP}	5	-	ns
	$\overline{UB}$, $\overline{LB}$ Set-up Time to Clock	t_{BS}	5	-	ns
	$\overline{UB}$, $\overline{LB}$ Hold Time from Clock	t_{BH}	5	-	ns
	Byte Masking Set-up Time to Clock	t_{BMS}	7	-	ns
	Byte Masking Hold Time from Clock	t_{BMH}	7	-	ns
	Data Set-up Time to Clock	t_{DS}	5	-	ns
	Data Hold Time from Clock	t_{DHC}	3	-	ns

SYNCHRONOUS BURST OPERATION TIMING WAVEFORM

Fig.23 TIMING WAVEFORM OF BASIC BURST OPERATION [Latency=5,Burst Length=4]

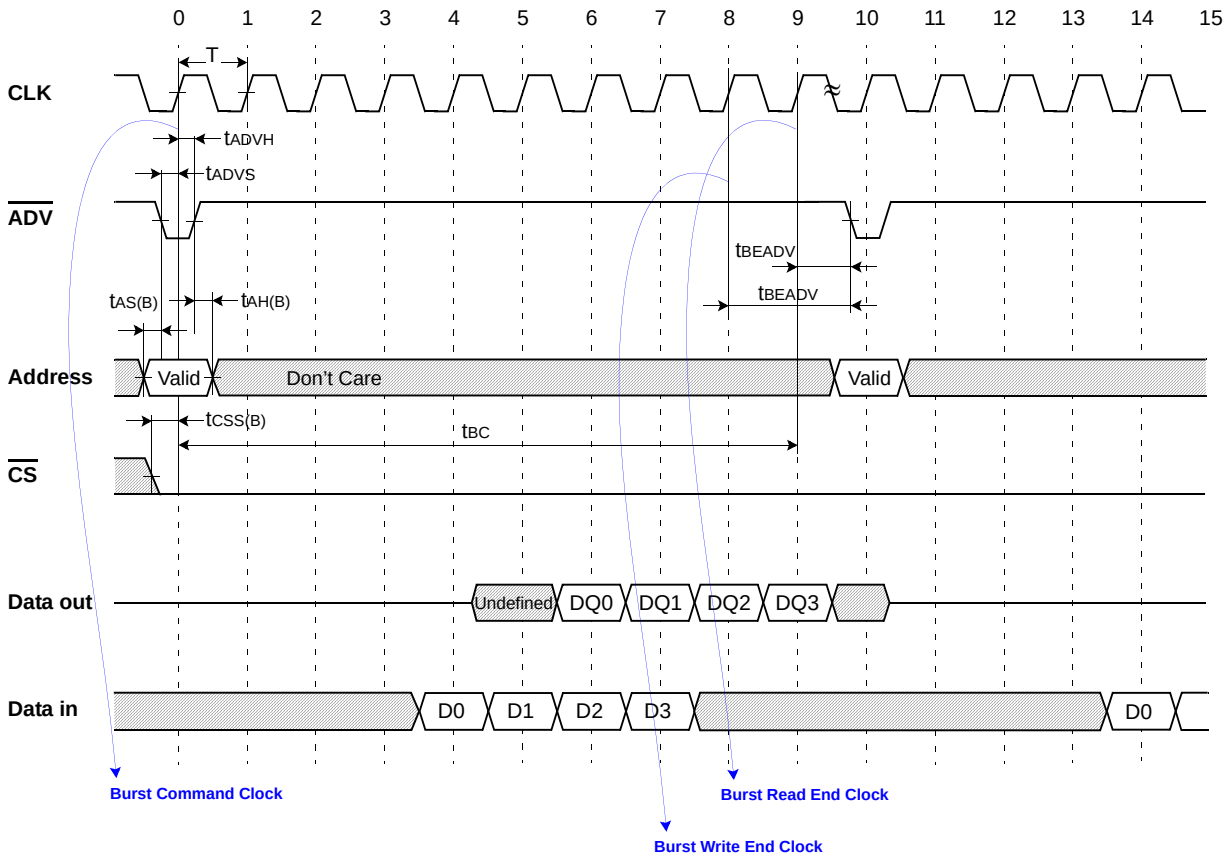
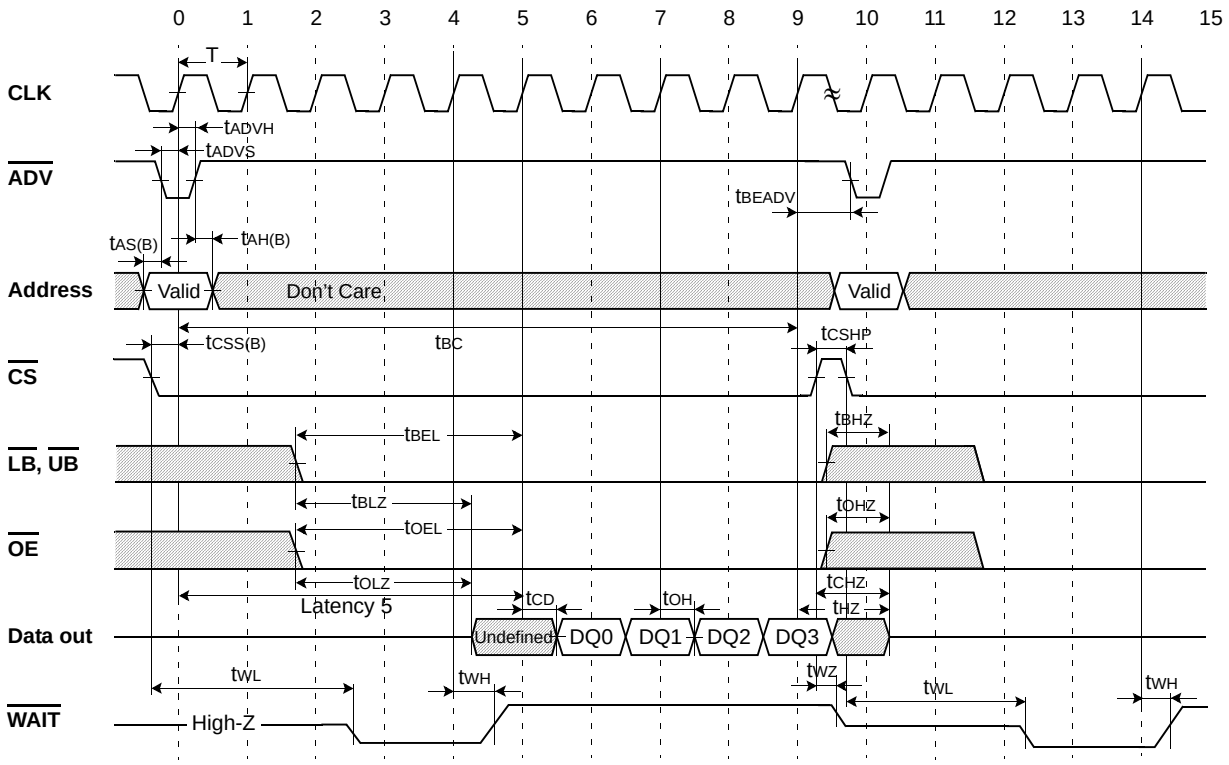


Table 27. BURST OPERATION AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
T	15	200	ns	$t_{AS(B)}$	0	-	ns
t_{BC}	-	2500	ns	$t_{AH(B)}$	7	-	ns
t_{ADVS}	5	-	ns	$t_{CSS(B)}$	5	-	ns
t_{ADVH}	7	-	ns	t_{BEADV}	7	-	ns

SYNCHRONOUS BURST READ TIMING WAVEFORM

Fig.24 TIMING WAVEFORM OF BURST READ CYCLE(1) ***[Latency=5,Burst Length=4,WP=Low enable](WE=VIH)***
- CS Toggling Consecutive Burst Read



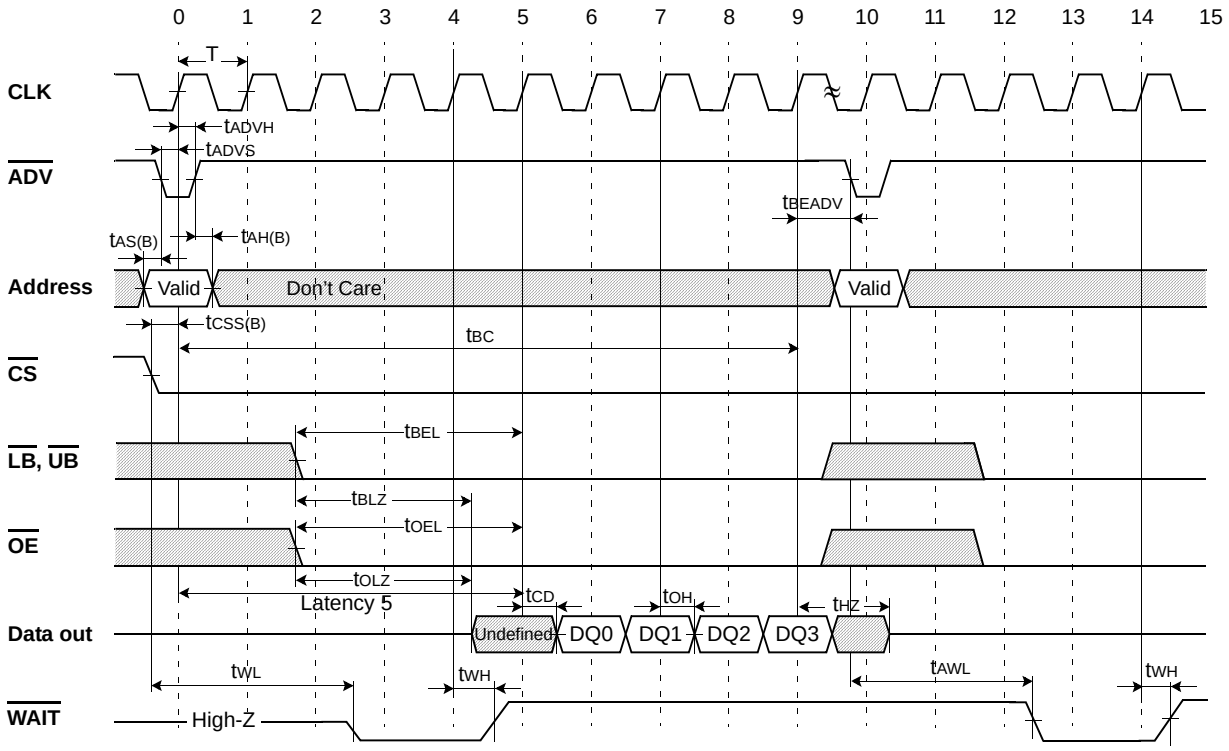
(SYNCHRONOUS BURST READ CYCLE - $\overline{CS}$ Toggling Consecutive Burst Read)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 28. BURST READ AC CHARACTERISTICS *($\overline{CS}$ Toggling Consecutive Burst)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tCSHP	5	-	ns	tOHZ	-	12	ns
tBEL	1	-	clock	tBHZ	-	12	ns
tOEL	1	-	clock	tCD	-	10	ns
tBLZ	5	-	ns	tOH	3	-	ns
tOLZ	5	-	ns	tWL	-	10	ns
tHZ	-	12	ns	tWH	-	12	ns
tCHZ	-	12	ns	tWZ	-	12	ns

SYNCHRONOUS BURST READ TIMING WAVEFORM

Fig.25 TIMING WAVEFORM OF BURST READ CYCLE(2) *[Latency=5,Burst Length=4,WP=Low enable](WE=VIH)*
- CS Low Holding Consecutive Burst Read



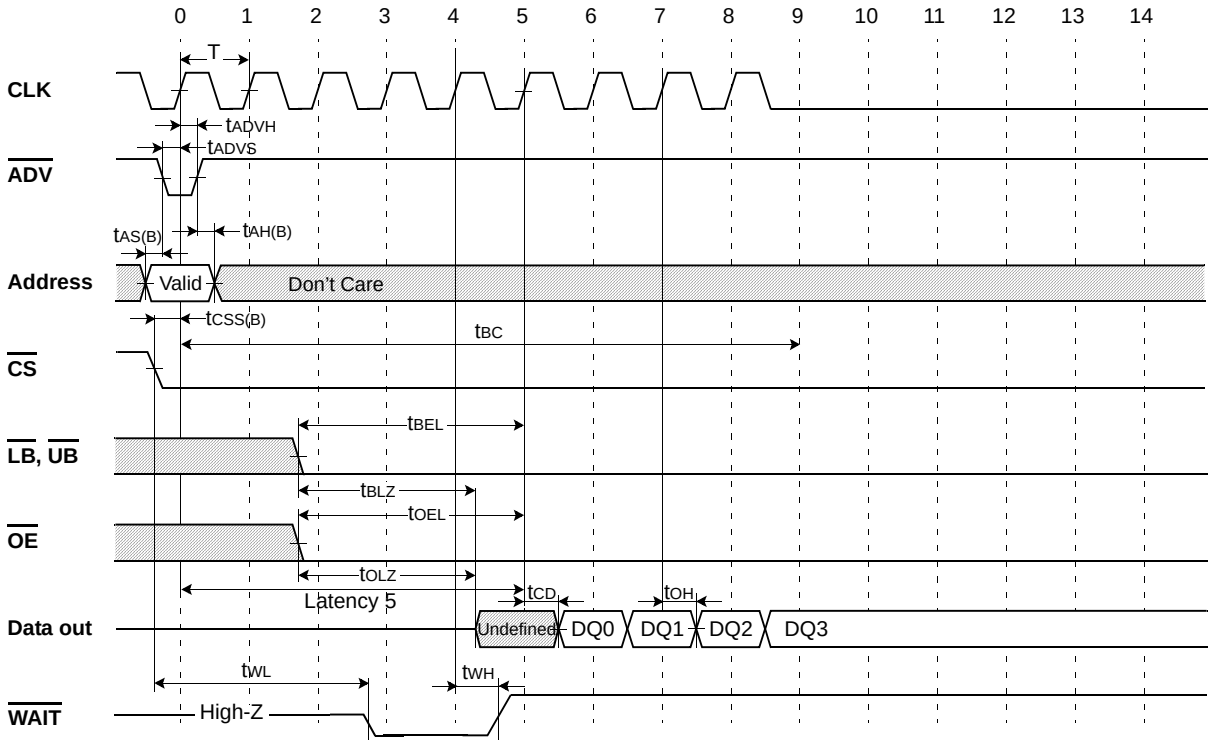
(SYNCHRONOUS BURST READ CYCLE - $\overline{CS}$ Low Holding Consecutive Burst Read)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. The consecutive multiple burst read operation with holding $\overline{CS}$ low is possible through issuing only new $\overline{ADV}$ and address.
5. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 29. BURST READ AC CHARACTERISTICS *($\overline{CS}$ Low Holding Consecutive Burst)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEL	1	-	clock	tCD	-	10	ns
tOEL	1	-	clock	tOH	3	-	ns
tBLZ	5	-	ns	tWL	-	10	ns
tOLZ	5	-	ns	tAWL	-	10	ns
tHZ	-	12	ns	tWH	-	12	ns

SYNCHRONOUS BURST READ TIMING WAVEFORM

Fig.26 TIMING WAVEFORM OF BURST READ CYCLE(3) [Latency=5,Burst Length=4,WP=Low enable](WE=VIH)
- Last Data Sustaining



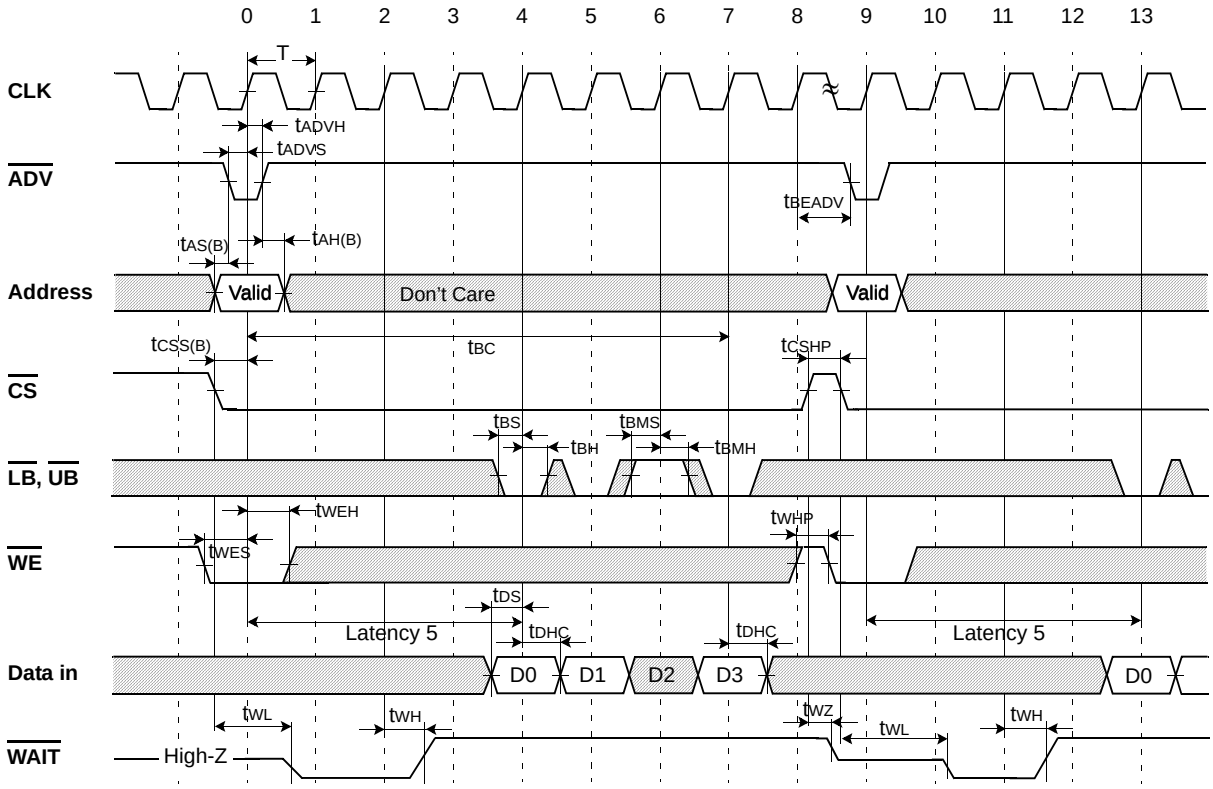
(SYNCHRONOUS BURST READ CYCLE - Last Data Sustaining)
1. /WAIT Low(tWL or tAWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
2. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
3. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 30. BURST READ AC CHARACTERISTICS(Last Data Sustaining)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEL	1	-	clock	tCD	-	10	ns
tOEL	1	-	clock	tOH	3	-	ns
tBLZ	5	-	ns	tWL	-	10	ns
tOLZ	5	-	ns	tWH	-	12	ns

SYNCHRONOUS BURST WRITE TIMING WAVEFORM

Fig.27 TIMING WAVEFORM OF BURST WRITE CYCLE(1) ***[Latency=5,Burst Length=4,WP=Low enable]*** *($\overline{OE}$=V_{IH})*
- CS Toggling Consecutive Burst Write



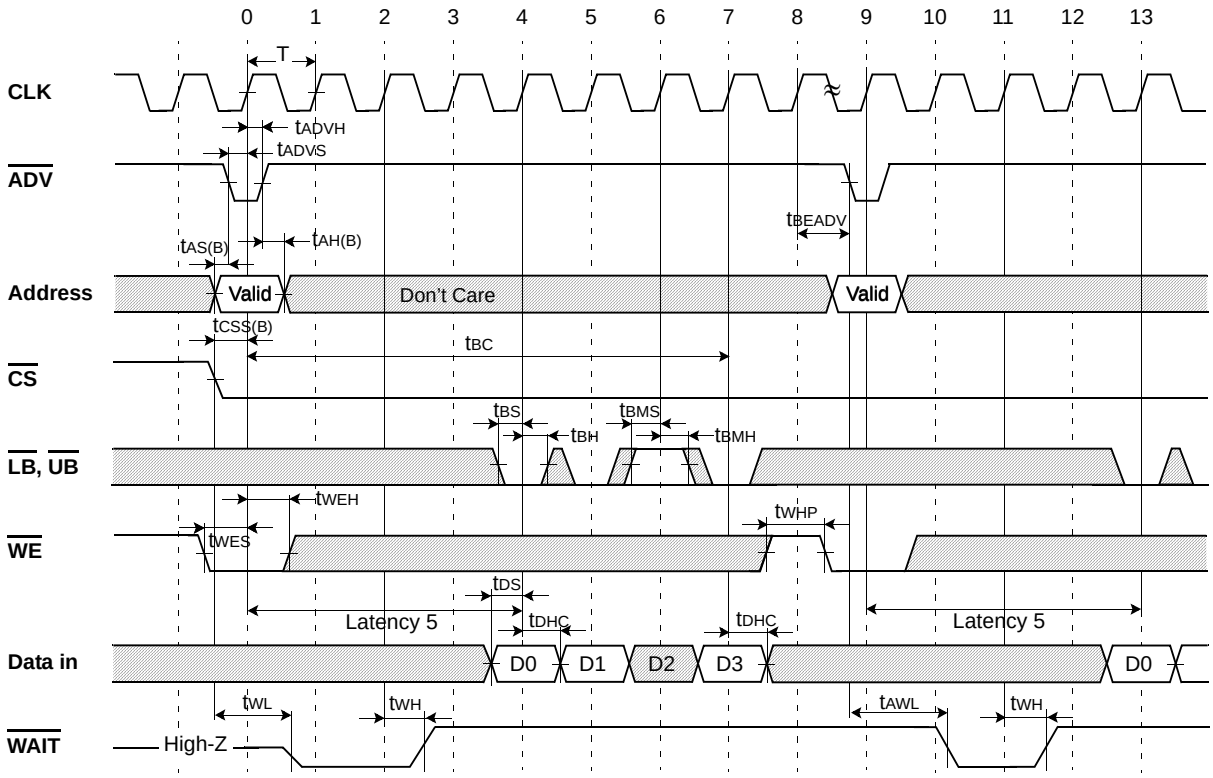
(SYNCHRONOUS BURST WRITE CYCLE - $\overline{CS}$ Toggling Consecutive Burst Write)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
3. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
4. D2 is masked by $\overline{UB}$ and $\overline{LB}$.
5. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 31. BURST WRITE AC CHARACTERISTICS *($\overline{CS}$ Toggling Consecutive Burst)*

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tCSHP	5	-	ns	tWHP	5	-	ns
tBS	5	-	ns	tDS	5	-	ns
tBH	5	-	ns	tDHC	3	-	ns
tBMS	7	-	ns	tWL	-	10	ns
tBMH	7	-	ns	tWH	-	12	ns
tWES	5	-	ns	tWZ	-	12	ns
tWEH	5	-	ns				

SYNCHRONOUS BURST WRITE TIMING WAVEFORM

Fig.28 TIMING WAVEFORM OF BURST WRITE CYCLE(2) [Latency=5,Burst Length=4,WP=Low enable](OE=VIH)
- CS Low Holding Consecutive Burst Write



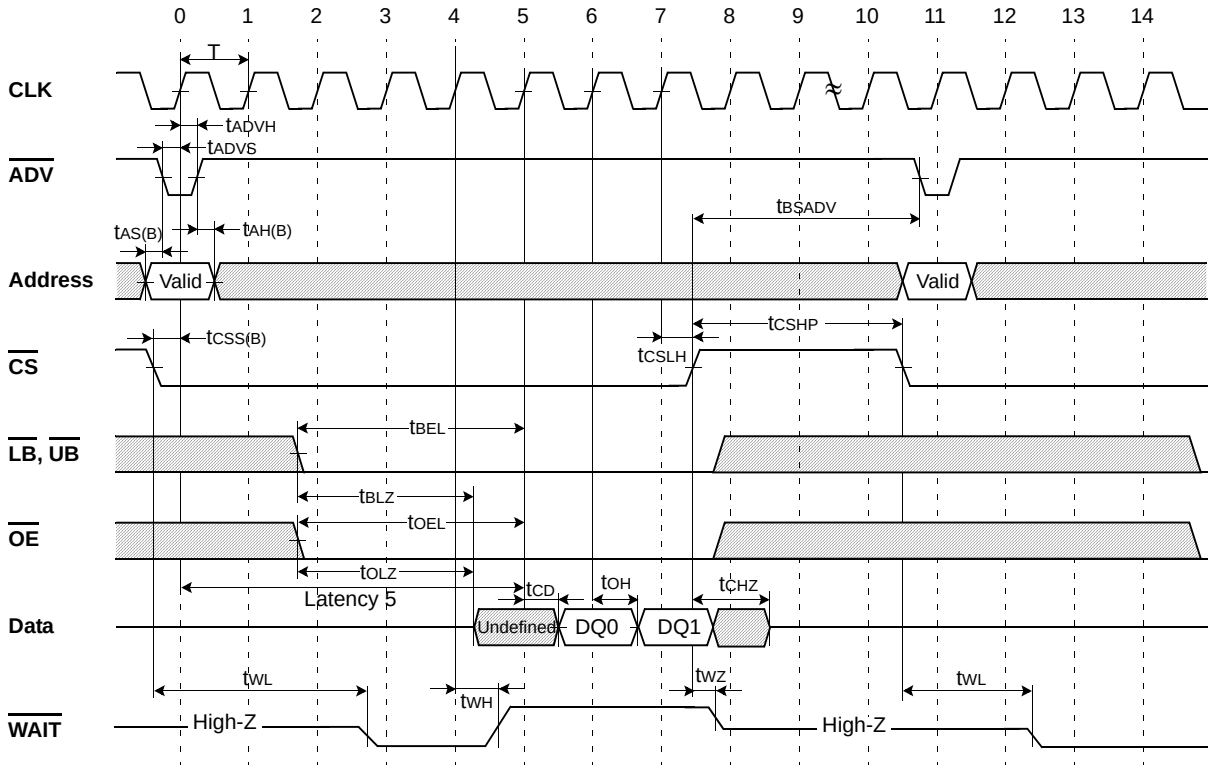
(SYNCHRONOUS BURST WRITE CYCLE - CS Low Holding Consecutive Burst Write)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
3. /WAIT Low(tWL or tAWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
4. D2 is masked by UB and LB.
5. The consecutive multiple burst read operation with holding CS low is possible through issuing only new ADV and address.
6. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 32. BURST WRITE AC CHARACTERISTICS(CS Low Holding Consecutive Burst)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBS	5	-	ns	tWHP	5	-	ns
tBH	5	-	ns	tDS	5	-	ns
tBMS	7	-	ns	tDHC	3	-	ns
tBMH	7	-	ns	tWL	-	10	ns
tWES	5	-	ns	tAWL	-	10	ns
tWEH	5	-	ns	tWH	-	12	ns

SYNCHRONOUS BURST READ STOP TIMING WAVEFORM

Fig.29 TIMING WAVEFORM OF BURST READ STOP by $\overline{CS}$ [Latency=5,Burst Length=4,WP=Low enable]($\overline{WE}$=V_{IH})



(SYNCHRONOUS BURST READ STOP TIMING)

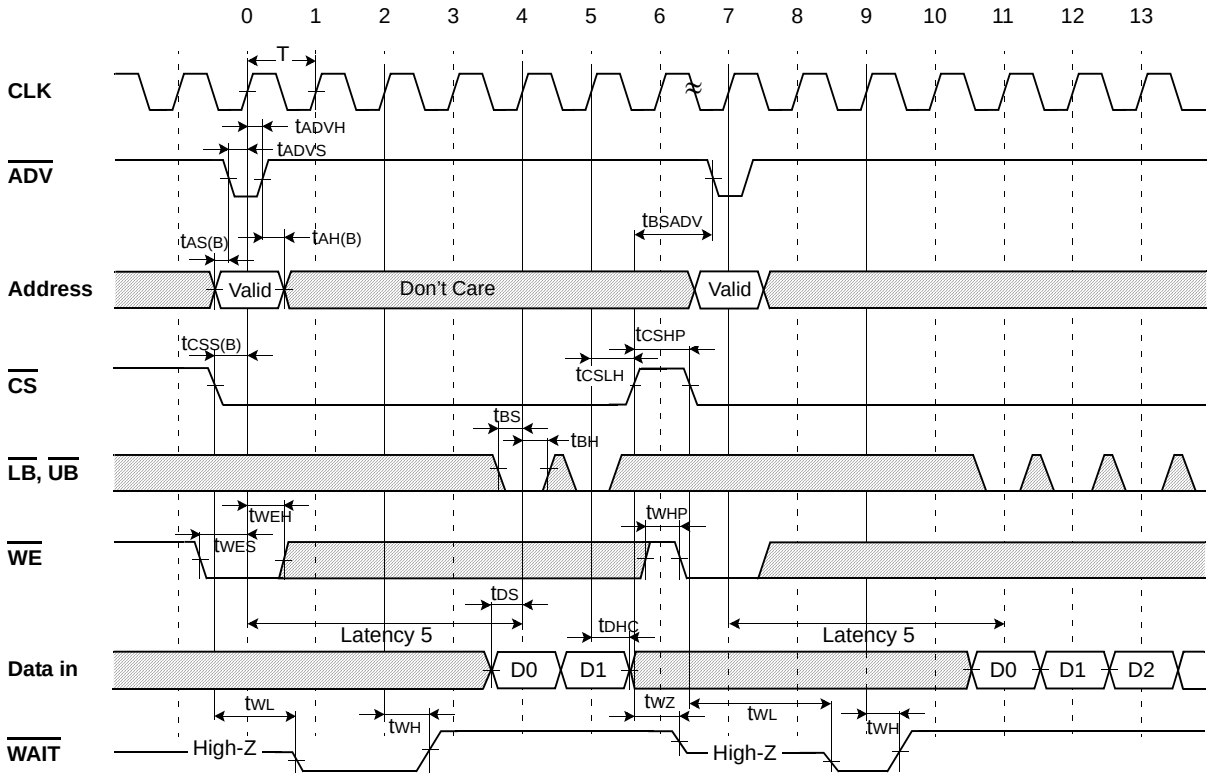
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBSADV should be met
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. The burst stop operation should not be repeated for over 2.5μs.

Table 33. BURST READ STOP AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBSADV	12	-	ns	tCD	-	10	ns
tCSLH	7	-	ns	tOH	3	-	ns
tCSHP	5	-	ns	tCHZ	-	12	ns
tBEL	1	-	clock	tWL	-	10	ns
tOEL	1	-	clock	tWH	-	12	ns
tBLZ	5	-	ns	tWZ	-	12	ns
tOLZ	5	-	ns				

SYNCHRONOUS BURST WRITE STOP TIMING WAVEFORM

Fig.30 TIMING WAVEFORM OF BURST WRITE STOP by $\overline{CS}$ [Latency=5,Burst Length=4,WP=Low enable]($\overline{OE}$=V_{IH})



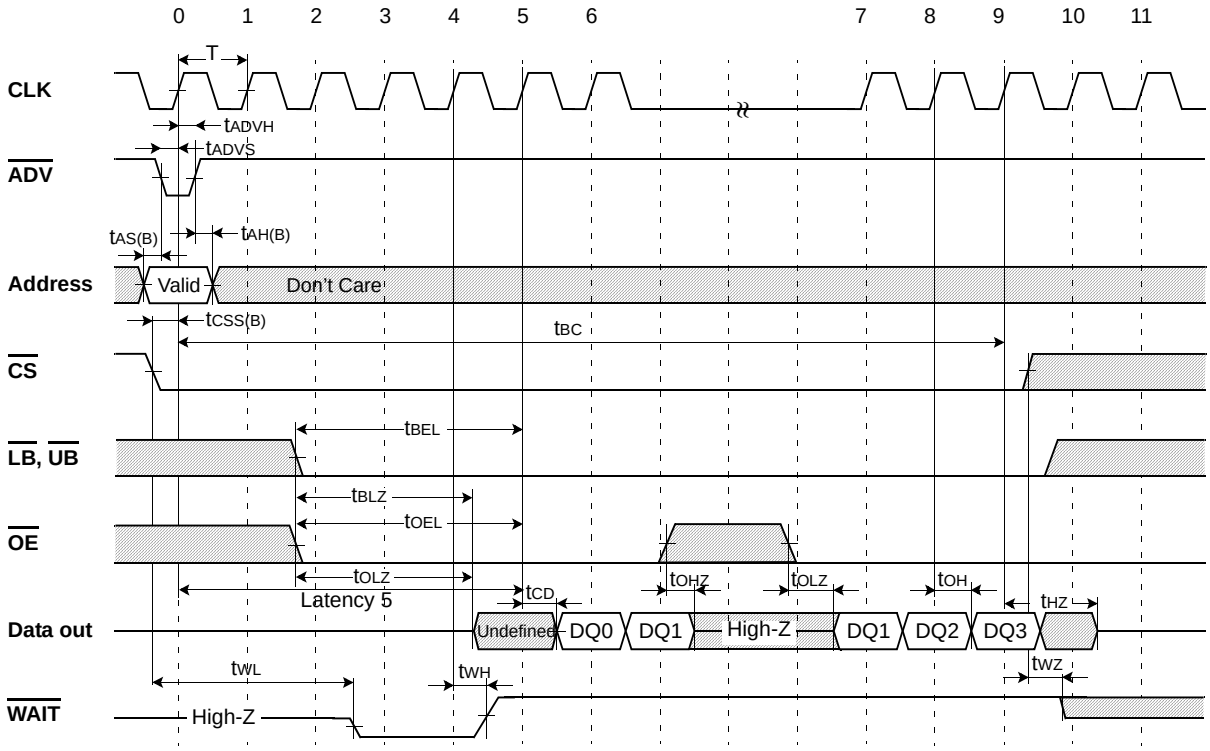
(SYNCHRONOUS BURST WRITE STOP TIMING)
1. The new burst operation can be issued only after the previous burst operation is finished.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. The burst stop operation should not be repeated for over 2.5μs.

Table 34. BURST WRITE STOP AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBSADV	12	-	ns	tWHP	5	-	ns
tCSLH	7	-	ns	tDS	5	-	ns
tCSHP	5	-	ns	tDHC	3	-	ns
tBS	5	-	ns	tWL	-	10	ns
tBH	5	-	ns	tWH	-	12	ns
tWES	5	-	ns	tWZ	-	12	ns
tWEH	5	-	ns				

SYNCHRONOUS BURST READ SUSPEND TIMING WAVEFORM

Fig.31 TIMING WAVEFORM OF BURST READ SUSPEND CYCLE(1) [Latency=5,Burst Length=4,WP=Low enable]($\overline{WE}$=V_{IH})



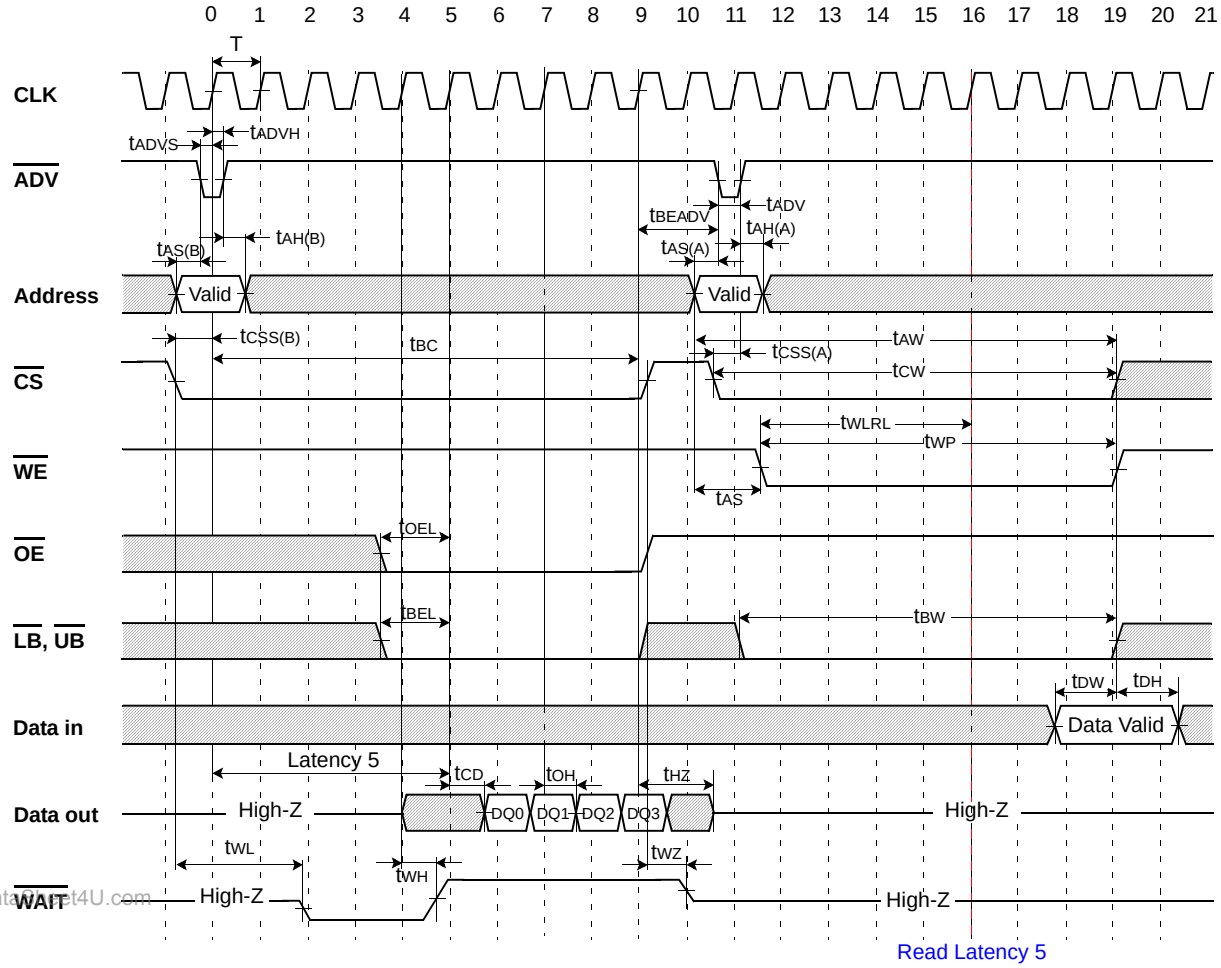
(SYNCHRONOUS BURST READ SUSPEND CYCLE)
1. If clock input is halted during burst read operation, the data out will be suspended. During the burst read suspend period, $\overline{OE}$ high drives data out to high-Z. If clock input is resumed, the suspended data will be out first.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. During suspend period, $\overline{OE}$ high drives DQ to High-Z and $\overline{OE}$ low drives DQ to Low-Z.
   If OE stays low during suspend period, the previous data will be sustained.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 35. BURST READ SUSPEND AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{BEL}	1	-	clock	t_{HZ}	-	12	ns
t_{OEL}	1	-	clock	t_{OHZ}	-	12	ns
t_{BLZ}	5	-	ns	t_{WL}	-	10	ns
t_{OLZ}	5	-	ns	t_{WH}	-	12	ns
t_{CD}	-	10	ns	t_{WZ}	-	12	ns
t_{OH}	3	-	ns				

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.32 SYNCH. BURST READ to ASYNCH. WRITE(Address Latch Type) TIMING WAVEFORM
[Latency=5, Burst Length=4]



(SYNCHRONOUS BURST READ CYCLE)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

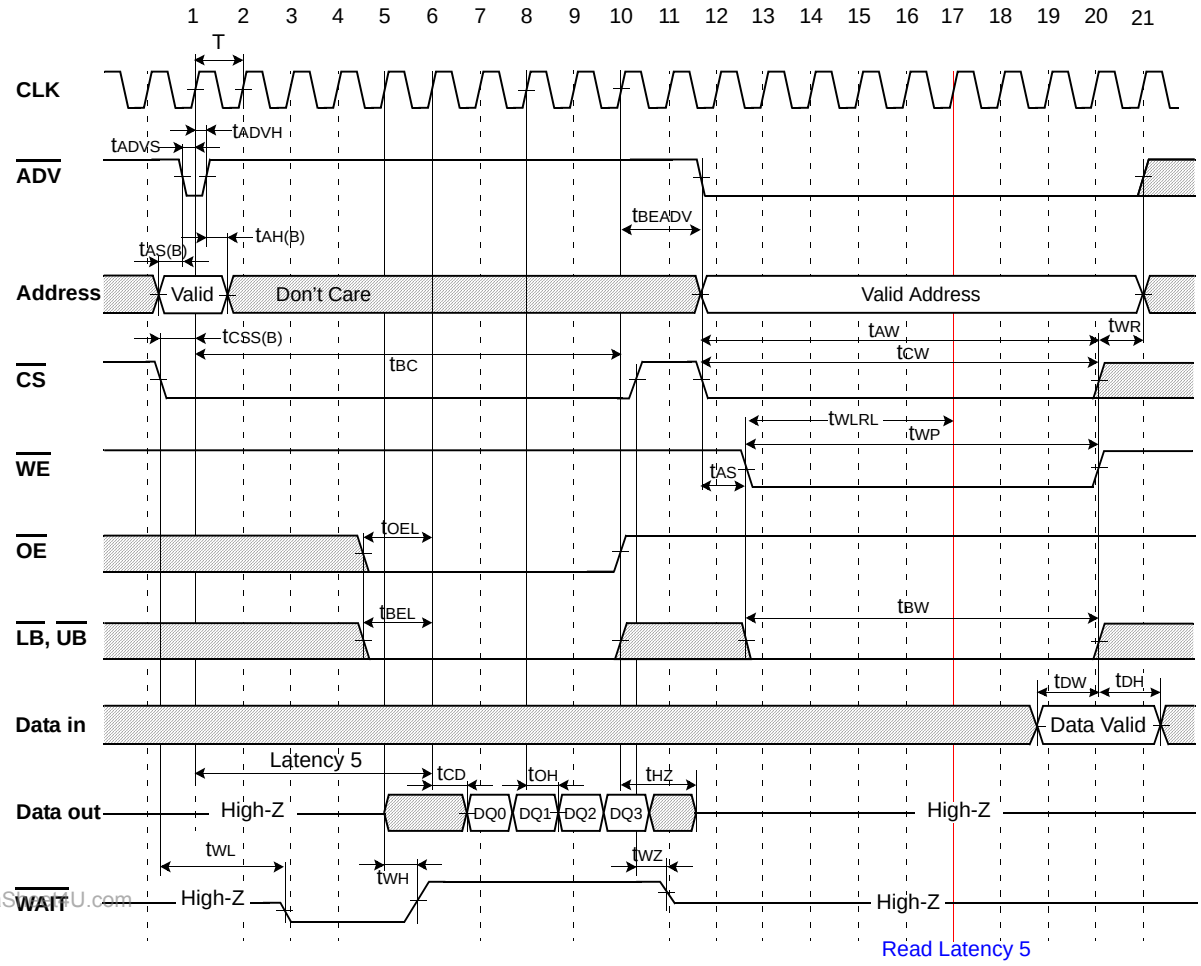
(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

Table 36. BURST READ to ASYNCH. WRITE(Address Latch Type) AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEADV	7	-	ns	tWLRL	1	-	clock

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.33 SYNCH. BURST READ to ASYNCH. WRITE(Low $\overline{ADV}$ Type) TIMING WAVEFORM
[Latency=5, Burst Length=4]



(SYNCHRONOUS BURST READ CYCLE)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

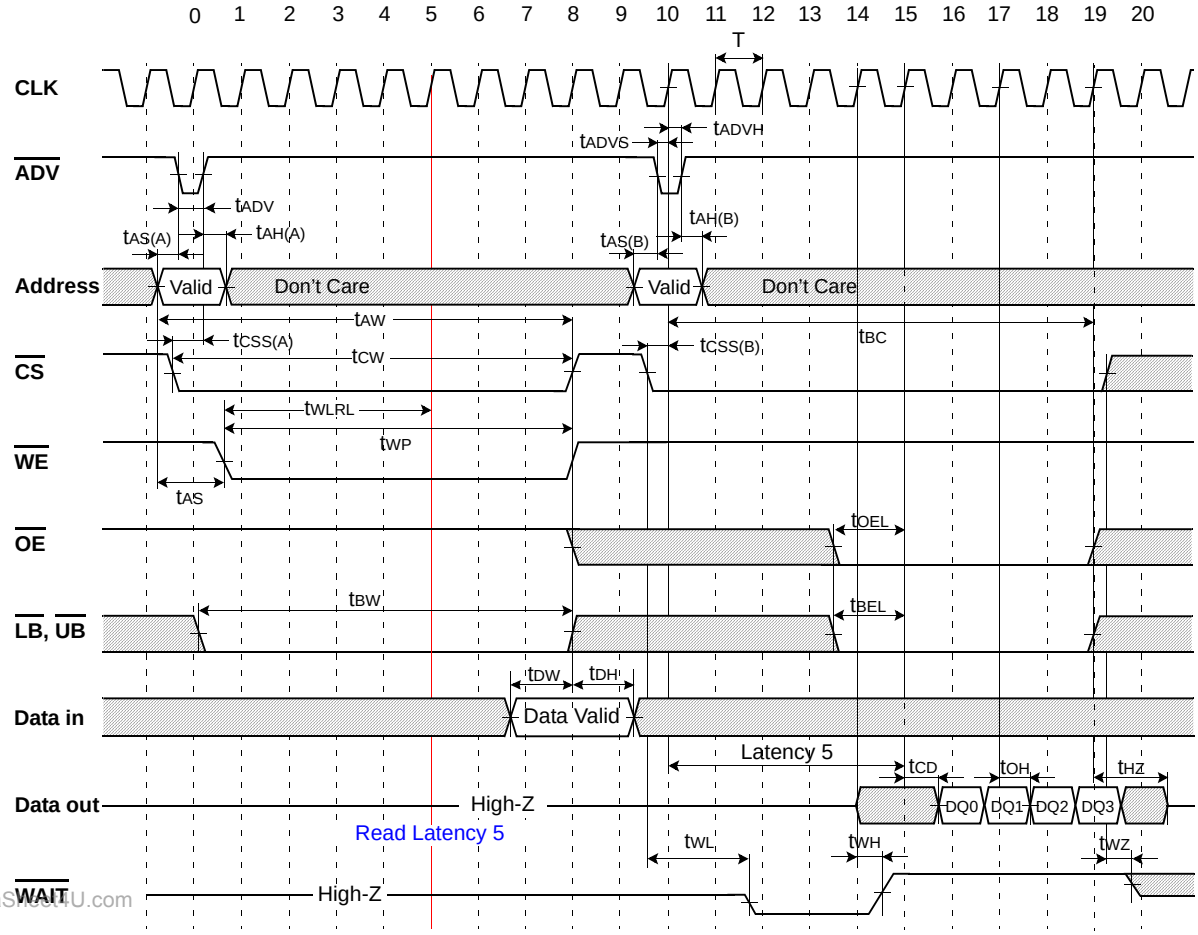
(LOW $\overline{ADV}$ TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

Table 37. BURST READ to ASYNCH. WRITE(Low $\overline{ADV}$ Type) AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEADV	7	-	ns	tWLRL	1	-	clock

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.34 ASYNCH. WRITE(Address Latch Type) to SYNCH. BURST READ TIMING WAVEFORM [Latency=5, Burst Length=4]



(SYNCHRONOUS BURST READ CYCLE)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

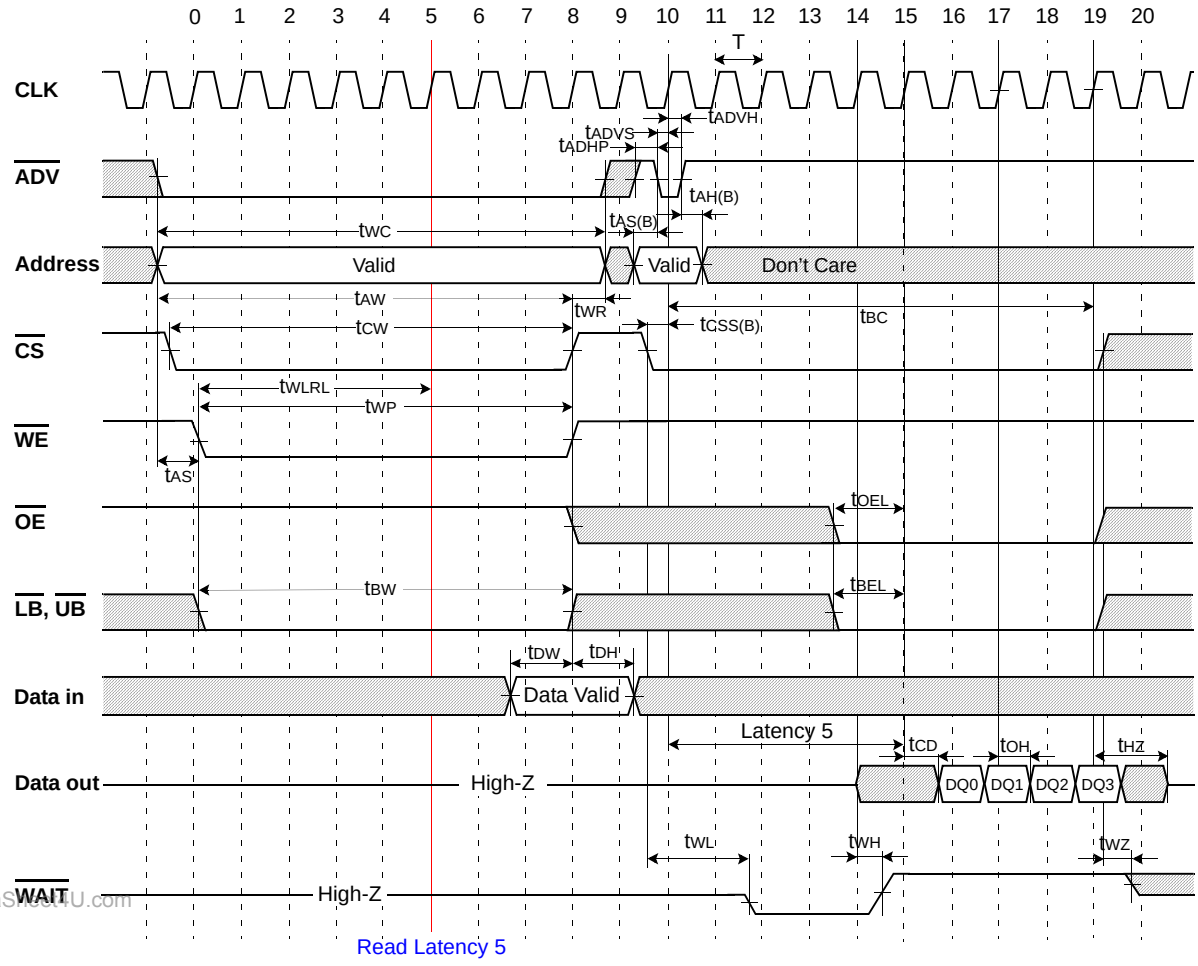
(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

Table 38. ASYNCH. WRITE(Address Latch Type) to BURST READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tWLRL	1	-	clock				

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.35 ASYNCH. WRITE(Low $\overline{ADV}$ Type) to SYNCH. BURST READ TIMING WAVEFORM
[Latency=5, Burst Length=4]



(SYNCHRONOUS BURST READ CYCLE)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low $\overline{ADV}$ period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

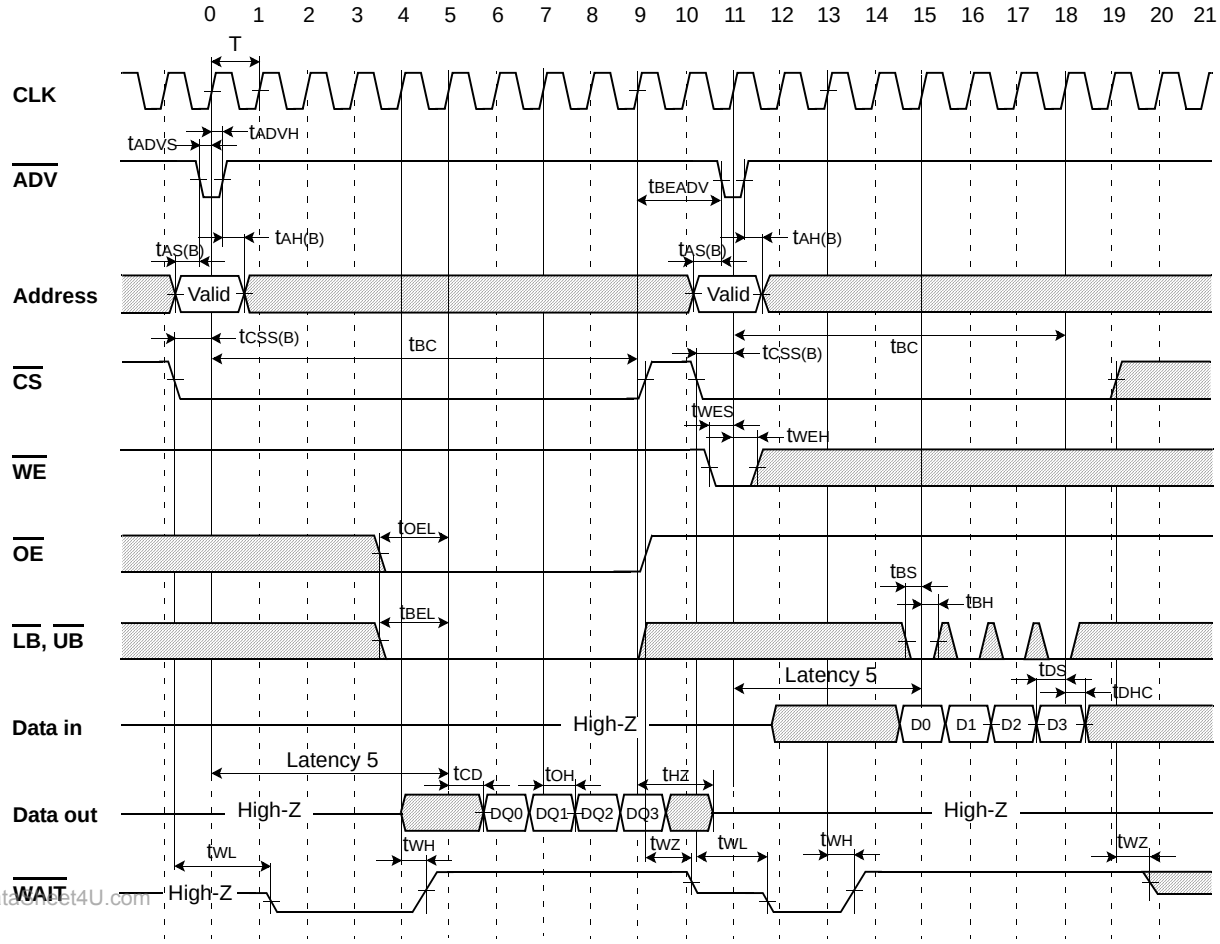
(LOW $\overline{ADV}$ TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

Table 39. ASYNCH. WRITE(Low $\overline{ADV}$ Type) to BURST READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tWLRL	1	-	clock	tADHP	5	-	ns

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.36 SYNCH. BURST READ to SYNCH. BURST WRITE TIMING WAVEFORM
[Latency=5, Burst Length=4]



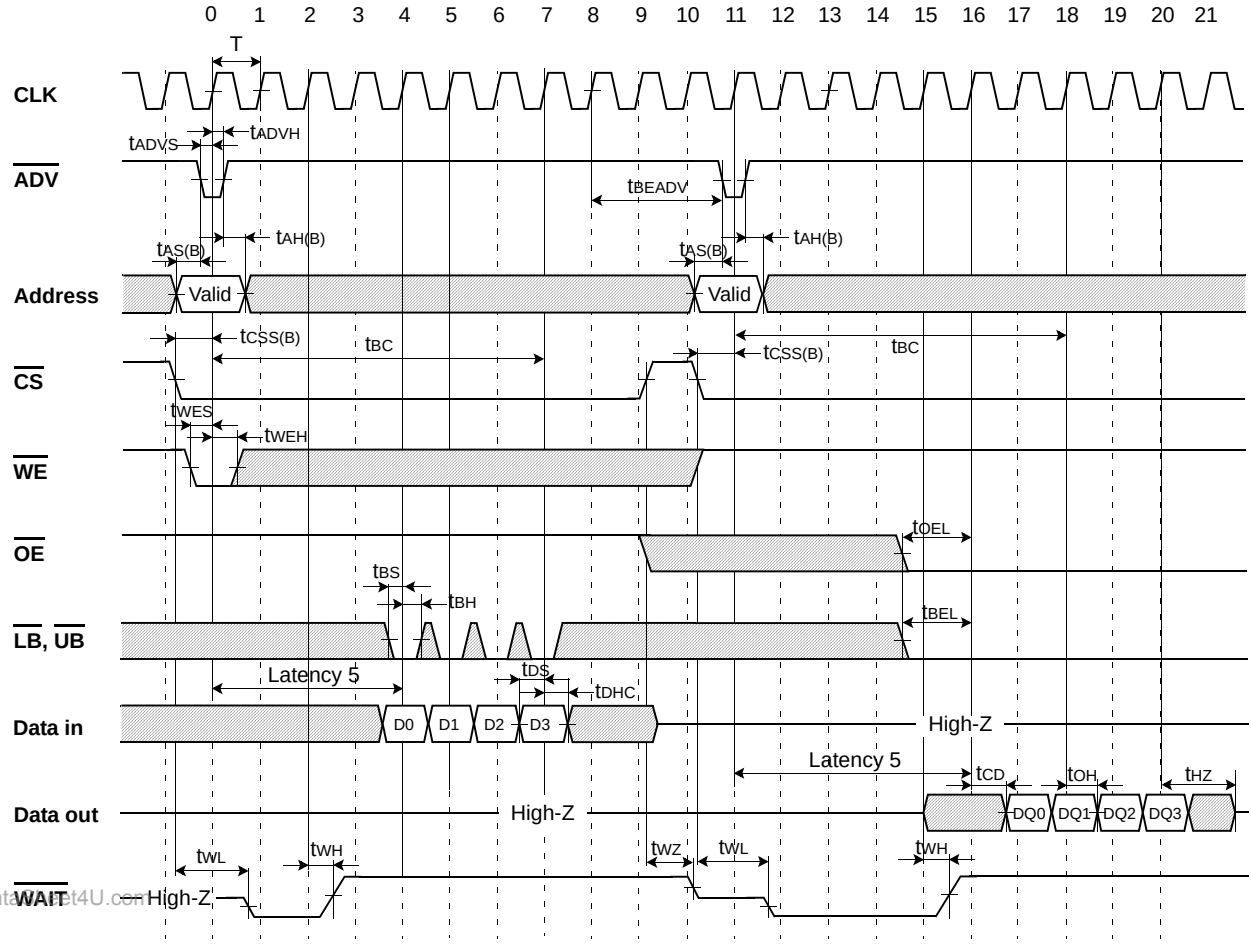
(SYNCHRONOUS BURST READ & WRITE CYCLE)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 40. BURST READ to BURST WRITE AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEADV	7	-	ns				

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.37 SYNCH. BURST WRITE to SYNCH. BURST READ TIMING WAVEFORM
[Latency=5, Burst Length=4]



(SYNCHRONOUS BURST READ & WRITE CYCLE)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 41. BURST WRITE to BURST READ AC CHARACTERISTICS

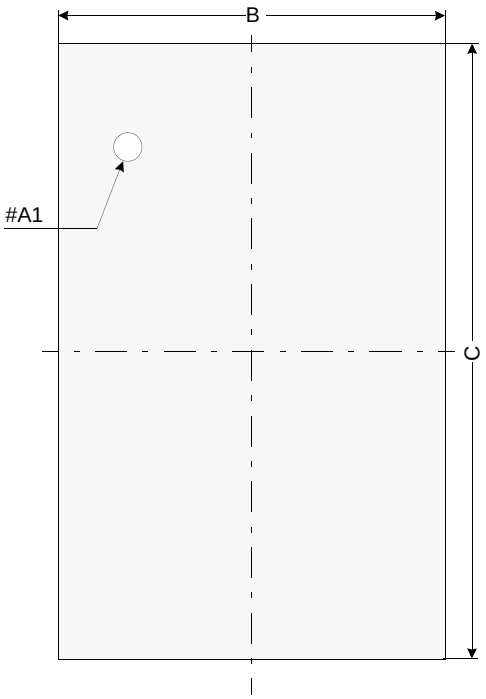
Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEADV	7	-	ns				

PACKAGE DIMENSION

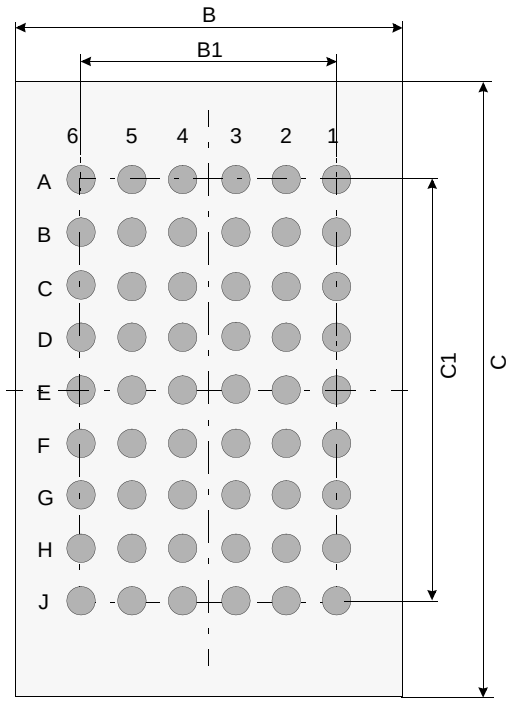
Unit: millimeters

54 BALL FINE PITCH BALL GRID ARRAY(0.75mm ball pitch)

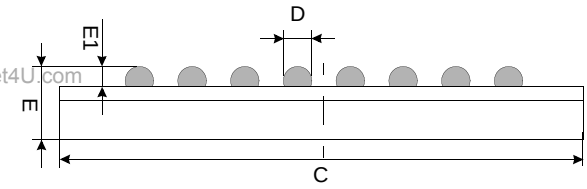
Top View



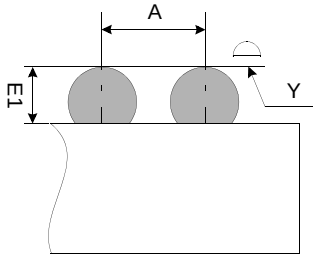
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	6.00	-
D	0.40	0.45	0.50
E	-	-	1.00
E1	0.25	-	-
Y	-	-	0.10

Notes.

1. Ball counts: 54(9 row x 6 column)
2. Ball pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless specified beside figure.
4. Typ: Typical
5. Y is coplanarity