

KM641003C**CMOS SRAM****Document Title****256Kx4 Bit (with OE) High-Speed CMOS Static RAM(5.0V Operating).****Revision History**

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	Initial release with Preliminary.	Aug. 5. 1998	Preliminary
Rev. 1.0	Release to Final Data Sheet. 1.1. Delete Preliminary.	Mar. 3. 1999	Final

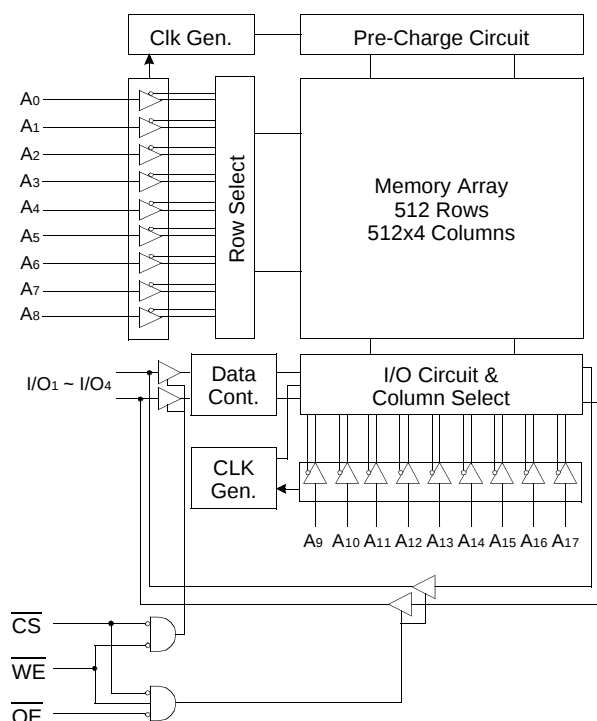
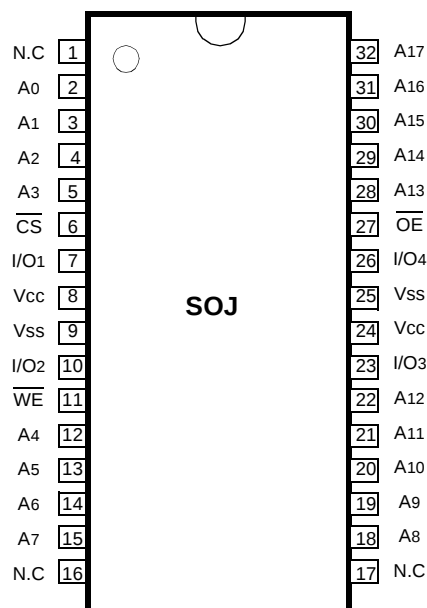
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

KM641003C**CMOS SRAM****256K x 4 Bit (with OE) High-Speed CMOS Static RAM****FEATURES**

- Fast Access Time 12,15,20ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 30mA(Max.)
 - (CMOS) : 5mA(Max.)
 - Operating KM641003C - 12 : 70mA(Max.)
 - KM641003C - 15 : 68mA(Max.)
 - KM641003C - 20 : 65mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration :
 - KM641003CJ : 32-SOJ-400

GENERAL DESCRIPTION

The KM641003C is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641003C uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641003C is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM**PIN CONFIGURATION (Top View)****PIN FUNCTION**

Pin Name	Pin Function
A ₀ - A ₁₇	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O ₁ ~ I/O ₄	Data Inputs/Outputs
V _{cc}	Power(+5.0V)
V _{ss}	Ground
N.C.	No Connection

KM641003C**CMOS SRAM****ABSOLUTE MAXIMUM RATINGS***

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5V	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-0.5 to 7.0	V
Power Dissipation	P _d	1	W
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5**	V
Input Low Voltage	V _{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-2	2	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ =V _{IH} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} V _{OUT} =V _{SS} to V _{CC}		-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty $\overline{CS}$ =V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	12ns	-	70	mA
			15ns	-	68	
			20ns	-	65	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}$ =V _{IH}		-	30	mA
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V		-	5	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA		-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA		2.4	-	V
	V _{OH1} *	I _{OH1} =-0.1mA		-	3.95	V

* V_{CC}=5.0V±5%, Temp.=25°C.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

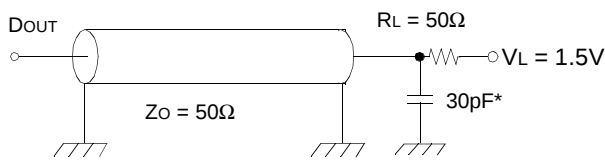
Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

* Capacitance is sampled and not 100% tested.

KM641003C**CMOS SRAM****AC CHARACTERISTICS**($T_A=0$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$, unless otherwise noted.)**TEST CONDITIONS**

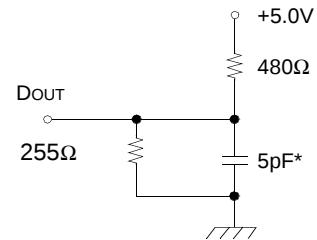
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



* Capacitive Load consists of all components of the test environment.

Output Loads(B)

for t_{HZ} , t_{LZ} , t_{WHZ} , t_{OW} , t_{OLZ} & t_{OHZ} 

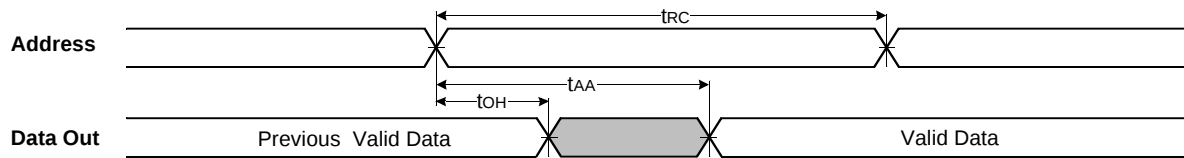
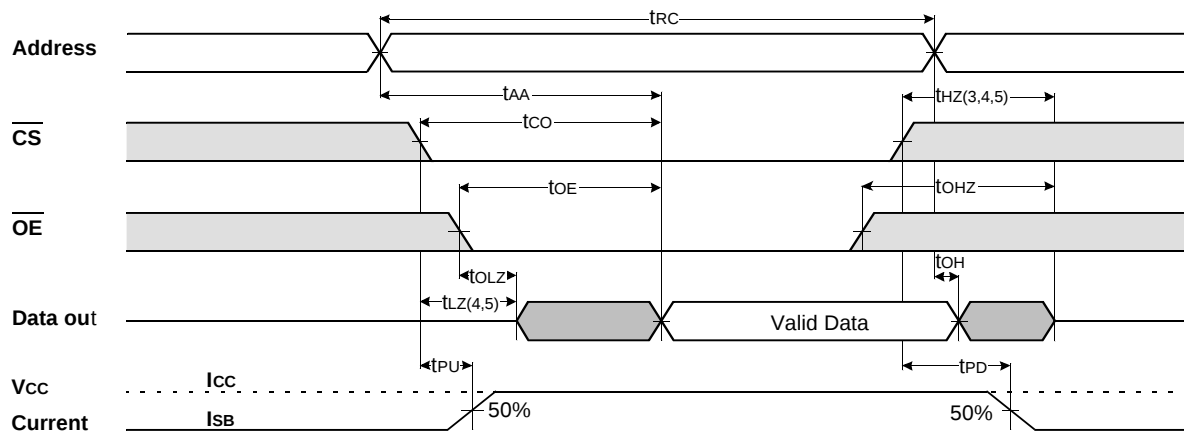
* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641003C-12		KM641003C-15		KM641003C-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select to Output	t_{CO}	-	12	-	15	-	20	ns
Output Enable to Valid Output	t_{OE}	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	-	7	-	9	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	t_{PD}	-	12	-	15	-	20	ns

KM641003C**CMOS SRAM****WRITE CYCLE**

Parameter	Symbol	KM641003C-12		KM641003C-15		KM641003C-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	12	-	15	-	20	-	ns
Chip Select to End of Write	t _{CW}	8	-	9	-	10	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	t _{WP}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	t _{WP1}	12	-	15	-	20	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	6	0	7	0	9	ns
Data to Write Time Overlap	t _{DW}	6	-	7	-	8	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	ns

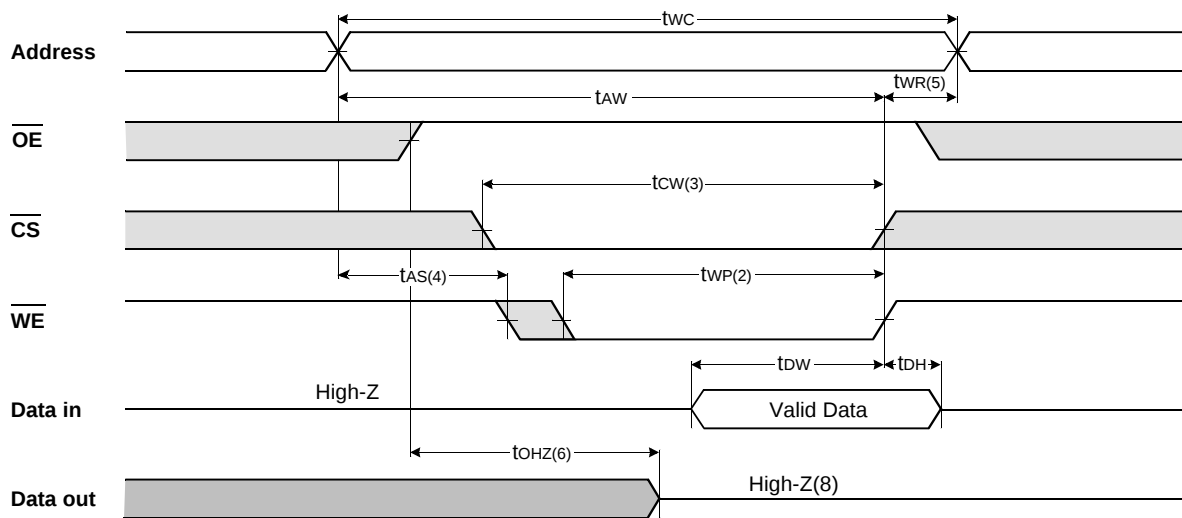
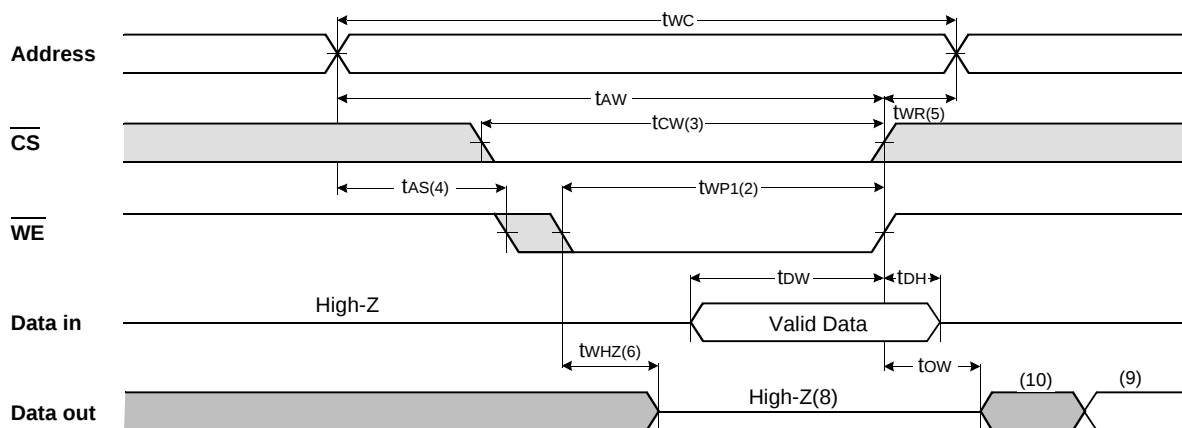
TIMING DIAGRAMS**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{WE}}=V_{\text{IH}}$)**TIMING WAVEFORM OF READ CYCLE(2)** ($\overline{\text{WE}}=V_{\text{IH}}$)

KM641003C

CMOS SRAM

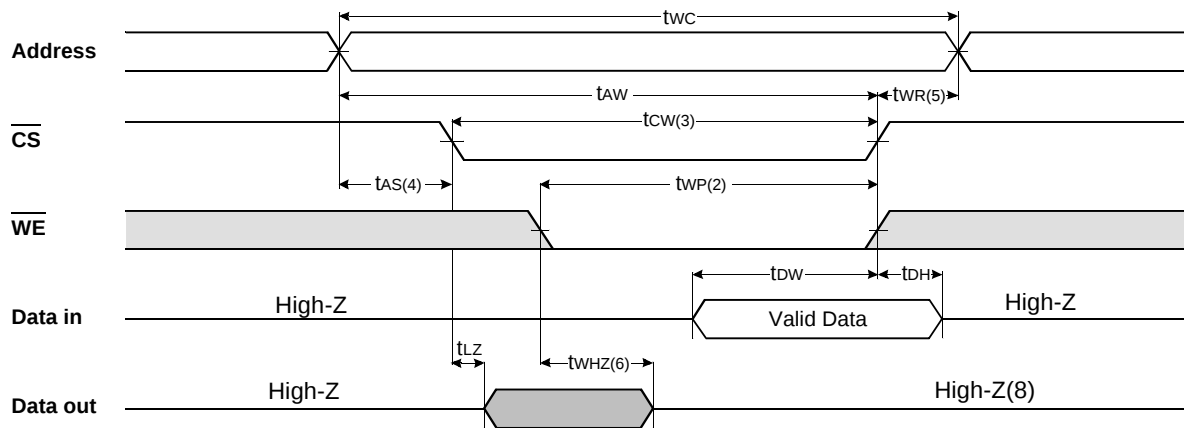
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE} = \text{Clock}$)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE} = \text{Low Fixed}$)

KM641003C

CMOS SRAM

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{CS}}$ =Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low ; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{\text{CS}}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. DOUT is the read data of the new address.
10. When CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	$I_{\text{SB}}, I_{\text{SB1}}$
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

* X means Don't Care.

KM641003C**CMOS SRAM****PACKAGE DIMENSIONS**

Units: millimeters/Inches

32-SOJ-400