

Silicon NPN Power Transistors

2SC1445

DESCRIPTION

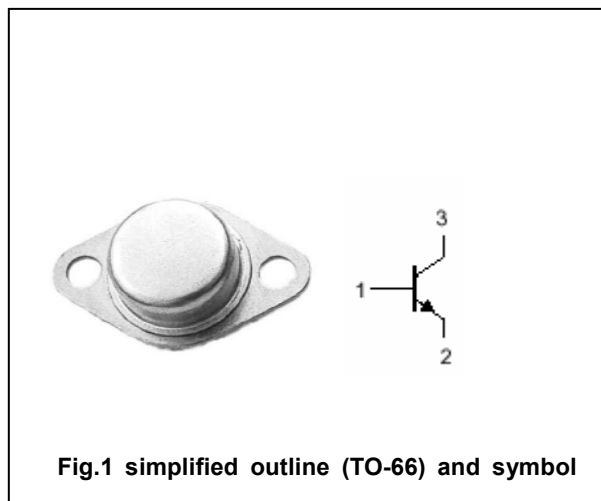
- With TO-66 package
- Excellent safe operating area
- Low collector saturation voltage

APPLICATIONS

- For switching and wide-band amplifier applications.

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	100	V
V_{CEO}	Collector-emitter voltage	Open base	80	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		6	A
I_B	Base current		1	A
P_D	Total power dissipation	$T_C = 25 \square$	40	W
T_j	Junction temperature		150	\square
T_{stg}	Storage temperature		-65~200	\square

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =100mA ; I _B =0	80			V
V _{CEsat-1}	Collector-emitter saturation voltage	I _C =2A ; I _B =0.2A			0.7	V
V _{CEsat-2}	Collector-emitter saturation voltage	I _C =6A ; I _B =0.6A			1.2	V
V _{BE sat-1}	Base-emitter saturation voltage	I _C =2A ; I _B =0.2A			1.2	V
V _{BE sat-2}	Base-emitter saturation voltage	I _C =6A ; I _B =0.6A			2.0	V
I _{CB0}	Collector cut-off current	V _{CB} =100V ; I _E =0			0.1	mA
I _{EB0}	Emitter cut-off current	V _{EB} =6V ; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =4V	30			
f _T	Transition frequency	I _C =0.5A ; V _{CE} =10V		10		MHz

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PACKAGE OUTLINE



Fig.2 outline dimensions