Signetics

N3001
Microprogram Control Unit

Product Specification

Logic Products

FEATURES

- **Schottky TTL process**
- **45ns cycle time (typ.)**
- **Direct addressing of standard bipolar PROM or ROM**
- **512 microinstruction addressability**
- **Advanced organization:**
  - **9-bit microprogram address register and bus organized to address memory by row and column**
  - **4-bit program latch**
  - **2-flag registers**
- **11 address control functions:**
  - **3 jump and test latch functions**
  - **16 way jump and test instructions**
- **8 flag control functions:**
  - **4 flag input functions**
  - **4 flag output functions**

DESCRIPTION

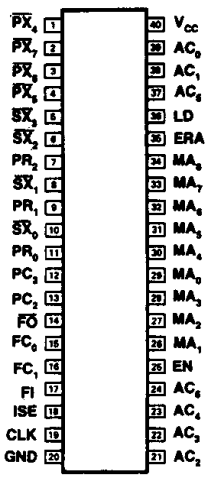
The N3001 MCU is 1 element of a bipolar microcomputer set. When used with the N3002, 74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

The N3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the N3001 include:

- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input buses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

PIN CONFIGURATION

I PACKAGE

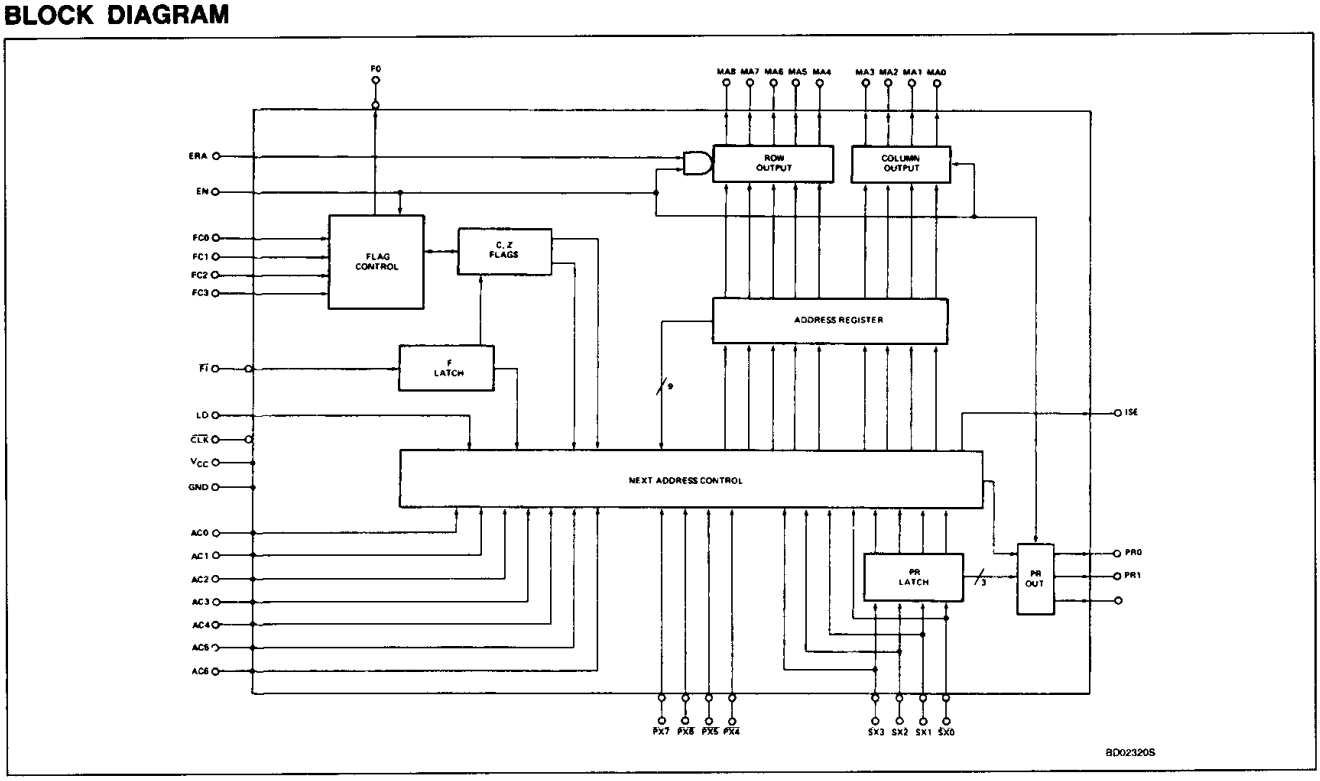


TOP VIEW

ORDERING NUMBER

N3001

BLOCK DIAGRAM



Microprogram Control Unit N3001

PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1 – 4	$\overline{PX_4} - \overline{PX_7}$	**Primary Instruction Bus Inputs:** Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active low
5, 6, 8, 10	$\overline{SX_0} - \overline{SX_3}$	**Secondary Instruction Bus Inputs:** Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active low
7, 9, 11	$PR_0 - PR_2$	**PR-Latch Outputs:** The PR-latch outputs ($SX_0 - SX_2$) are synchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collector
12, 13 15, 16	$FC_0 - FC_3$	**Flag Logic Control Inputs:** The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active high
14	$\overline{FO}$	**Flag Logic Output:** The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	Active low Three-state
17	$\overline{FI}$	**Flag Logic Input:** The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active low
18	ISE	**Interrupt Strobe Enable Output:** The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active high
19	CLK	**Clock Input**	
20	GND	**Ground**	
21 – 24 37 – 39	$AC_0 - AC_6$	**Next Address Control Function Inputs:** All jump functions are selected by these control lines.	Active high
25	EN	**Enable Input:** When in the high state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26 – 29	$MA_0 - MA_3$	**Microprogram Column Address Outputs**	Three-state
30 – 34	$MA_4 - MA_8$	**Microprogram Row Address Outputs**	Three-state
35	ERA	**Enable Row Address Input:** When in the low state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilitate the implementation of priority interrupt systems.	Active high
36	LD	**Microprogram Address Load Input:** When the active high state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction buses into the microprogram address register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active high
40	V_{CC}	**+5 Volt supply**	

THEORY OF OPERATION

The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaneously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

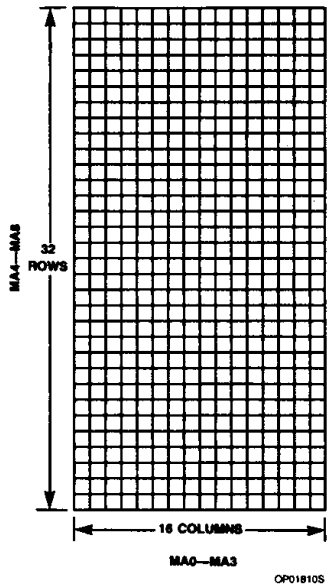
The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each intruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as a 5-bit row and 4-bit column address.

Microprogram Control Unit

N3001

ADDRESSING ORGANIZATION



MA0 – MA3

FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and column addresses.

MNEMONIC	FUNCTION
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

Unconditional Address Control (Jump) Functions

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs (AC0 – AC6) to generate the next microprogram address.

JUMP FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JCC	Jump in current column. $AC_0 - AC_4$ are used to select 1 of 32 row addresses in the current column, specified by $MA_0 - MA_3$, as the next address.
JZR	Jump to zero row. $AC_0 - AC_3$ are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. $AC_0 - AC_3$ are used to select 1 of 16 addresses in the current row, specified by $MA_4 - MA_8$, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. $AC_0 - AC_2$ are used to select 1 of 8 row addresses in the current row group, specified by $MA_7 - MA_8$, as the next row address. The current column is specified by $MA_0 - MA_3$. The PR-latch outputs are asynchronously enabled.

JUMP/TEST FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JFL	Jump/test F-latch. $AC_0 - AC_3$ are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is $col_0 - col_7$, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group $col_8 - col_{15}$, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag, $AC_0 - AC_2$ are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is $col_0 - col_7$, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group $col_8 - col_{15}$, the C-flag is used to select col_{10} or col_{11} as the next column address. JZF
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.
JPR	Jump/test PR-latch. $AC_0 - AC_2$ are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The 4 PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test rightmost PR-latch bits. $AC_0 - AC_2$ are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to select 1 of 4 column addresses in col_4 through col_7 as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high – order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{16} as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by $MA_6 - MA_8$, as the next row address. $PX_4 - PX_7$ are used to select 1 of 16 possible column addresses as the next column address. $SX_0 - SX_3$ data is locked in the PR-latch at the rising edge of the clock.

Flag Conditional Address Control (Jump Test) Functions

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

PX-Bus and PR-Latch Conditional Address Control (Jump/Test) Functions

The PX-bus jump/test function uses the data on the primary instruction bus ($PX_4 - PX_7$), the current microprogram address control function to generate the next microprogram address. The PR-latch jump/test functions use the data in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Flag Control Functions

The flag control functions of the MCU are selected by the 4 input lines designated $FC_0 - FC_3$. Function code formats are given in "Flag Control Function summary".

The following is a detailed description of each of the 8 flag control functions.

Flag Input Control Functions

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line.

Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Flag Output Control Functions

The flag output control functions select the value to which the flag output (FO) line will be forced.

FLAG CONTROL FUNCTION

MNEMONIC	FUNCTION DESCRIPTION
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z-flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTION TABLE

MNEMONIC	FUNCTION DESCRIPTION
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	0
	STC	Set C-flag to f	1	1
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	1	0
	FFZ	Force FO to Z-flag	0	1
	FF1	Force FO to 1	1	1

LOAD FUNCTION	NEXT ROW					NEXT COL			
LD	MA_8	7	6	5	4	MA_3	2	1	0
0	See Address Control Function Summary								
1	0	X_3	X_2	X_1	X_0	X_7	X_6	X_5	X_4

NOTES:
f = Contents of the F-latch
xn = Data on PX – or
SX – bus line n (active low)

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION							NEXT ROW					NEXT COL			
		AC_6	5	4	3	2	1	0	MA_8	7	6	5	4	MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JZR	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F-latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	Z
JPR	Jump/test PR-latch	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_2	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p_1	p_0
JPX	Jump/test PX – bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	X_7	X_6	X_5	X_4

NOTES:
dn = Data on address control line n
mn = Data in microprogram address register bit n
Pn = Data in PR-latch bit n
xn = Data on PX – bus line n (active low)
f, c, z = Contents of F-latch, C-flag, or Z-flag respectively

STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active high at the rising edge of the clock, the data on the primary and secondary instruction buses, $PX_4 - PX_7$ and $SX_0 - SX_3$, is loaded into the microprogram address register. $PX_4 - PX_7$ are loaded into $MA_4 - MA_7$. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

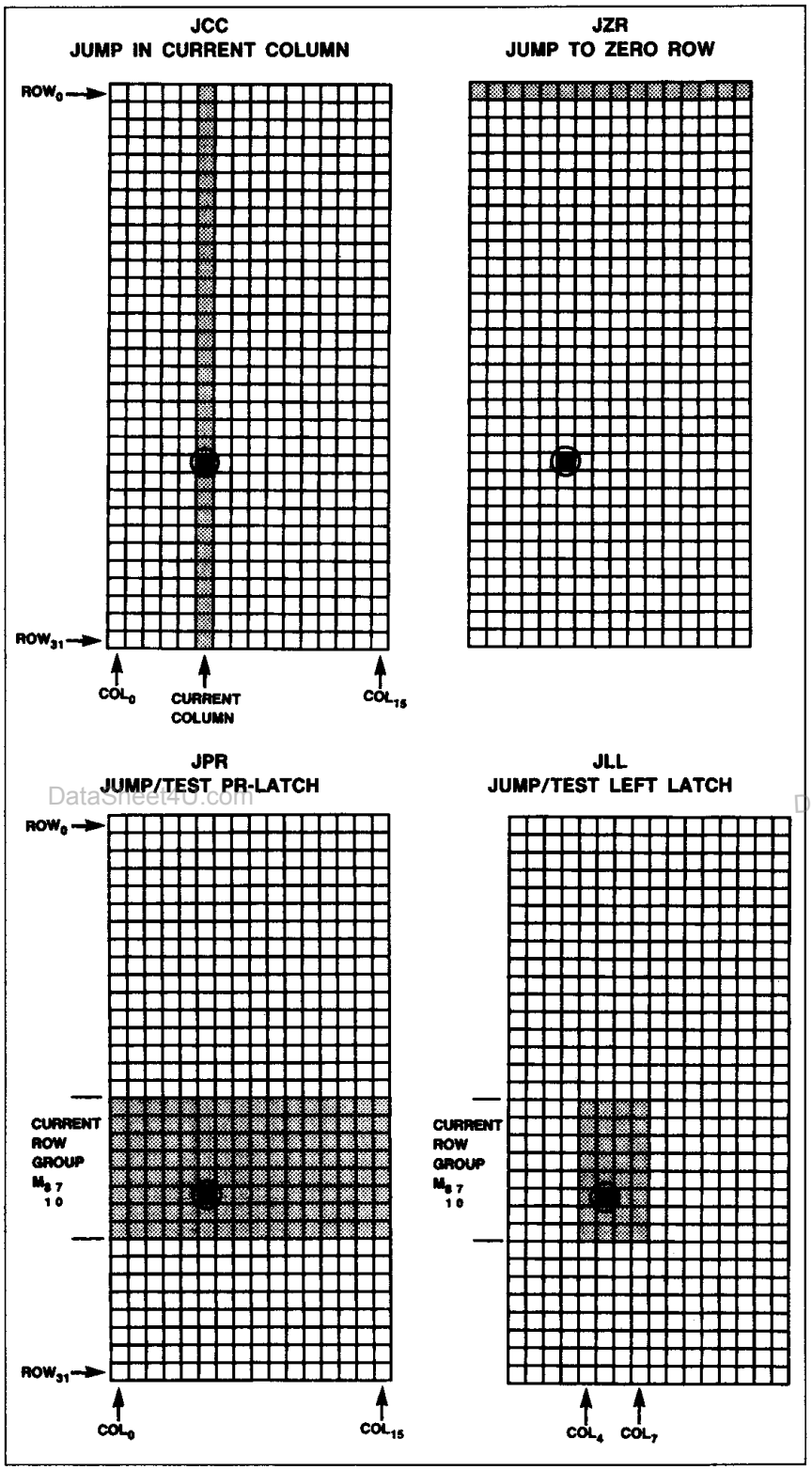
The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in active high state whenever a JZR is col_{15} is selected as the address control function. Generally, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so the interrupt control may be enabled at the beginning of the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on $AC_0 - AC_6$. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

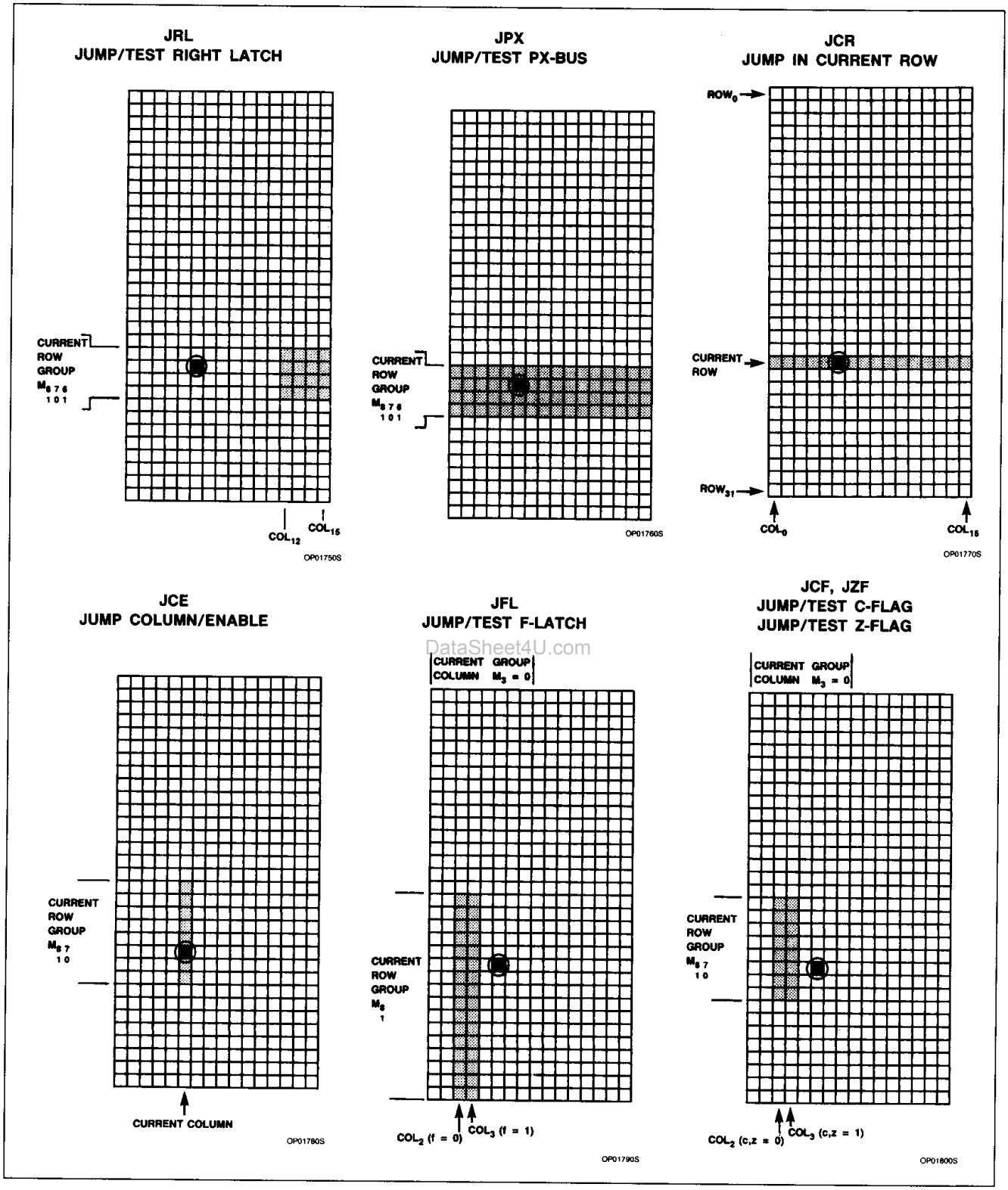
JUMP SET DIAGRAMS

The following 10 diagrams illustrate the jump set for each of the 11 jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents 1 current row (row_{21}) and current column (col_5) address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

JUMP SET DIAGRAMS



JUMP SET DIAGRAMS (Continued)



Microprogram Control Unit N3001

AC ELECTRICAL CHARACTERISTICS N3001 $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V$, ±5% 10%

PARAMETER		N3001			UNIT
		Min	Typ[1]	Max	
t_{CY}	Cycle time	60	45		ns
t_{PW}	Clock pulse width	17	10		ns
t_{SF}	Control and data input set-up times: LD, $AC_0 - AC_6$ (Set to "1"/"0")	20	3/14		ns
t_{SK}	FC_0, FC_1	7	5		ns
t_{SX}	$PX_4 - PX_7$ (Set to "1"/"0")	28	4/13		ns
t_{SI}	FI (Set to "1"/"0")	12	-6/0		ns
t_{SX}	$SX_0 - SX_3$	15	5		ns
t_{HF}	Control and data input hold times: LD, $AC_0 - AC_6$ (Hold to "1"/"0")	4	-3/-14		ns
t_{HK}	FC_0, FC_1	4	-5		ns
t_{HX}	$PX_4 - PX_7$ (Hold to "1"/"0")	0	-4/-13		ns
t_{HI}	FI (Hold to "1"/"0")	16	6.5/0		ns
t_{HX}	$SX_0 - SX_3$	0	-5		ns
t_{CO}	Propagation delay from clock input (CLK) to outputs ($mA_0 - mA_8$, FO) (t_{PHL}/t_{PLH})		17/24	36	ns
t_{KO}	Propagation delay from control inputs FC_2 and FC_3 to flag out (FO)		13	24	ns
t_{FO}	Propagation delay from control inputs $AC_0 - AC_6$ to latch outputs ($PR_0 - PR_2$)		21	32	ns
t_{EO}	Propagation delay from enable inputs EN and ERA to outputs ($mA_0 - mA_8$, FO, $PR_0 - PR_2$)		17	26	ns
t_{FI}	Propagation delay from control inputs $AC_0 - AC_6$ to interrupt strobe enable output (ISE)		20	32	ns

NOTES:
1. Typical values are for TA = 25°C and 5.0 supply voltage

7

VOLTAGE WAVEFORMS